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LightPix: Scalable digital readout for cryogenic SiPM applications

Stephen Greenberg

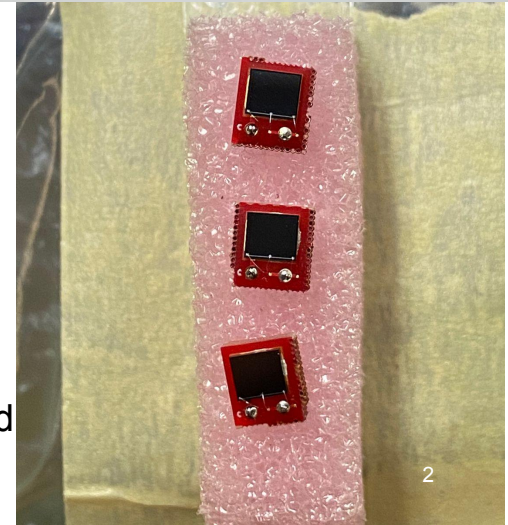
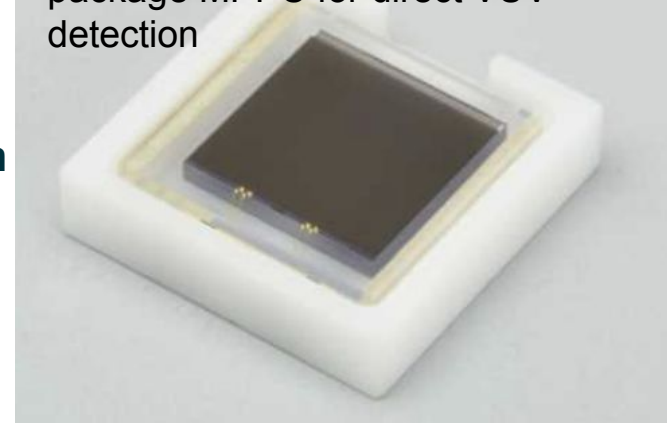
CPAD Workshop 2023, November 10

Silicon Photomultipliers (SiPMs)

Inherently digital light readout

- **Extremely attractive light readout (LRO) technology in noble liquid detectors (and beyond)**
 - LRO of choice for DUNE, nEXO, Darkside-20k, etc...
 - Single photon sensitivity with low ($\sim 30\text{-}60\text{V}$) bias
 - Fast timing, high gain,
 - Compact form factor for **high granularity**
- Continued developments in SiPM technology:
 - Direct-VUV with high PDE down to 128nm for LAr and LXe
 - Radiation hardness for collider environments

HPK S13374 series Ultralow-RI package MPPC for direct VUV detection



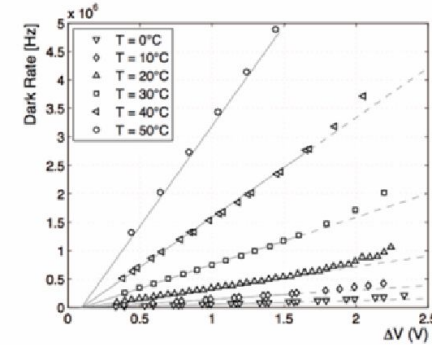
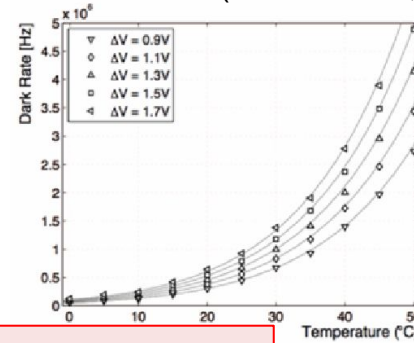
FBK VUV-HD bare dies bonded at LBNL

SiPM Readout Challenges

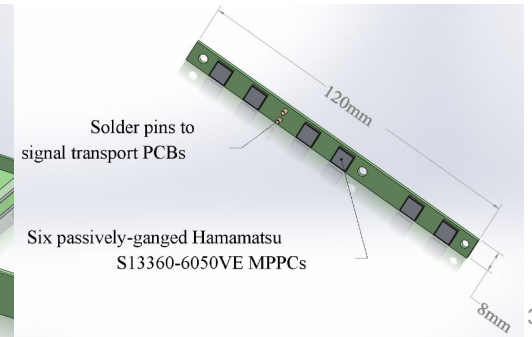
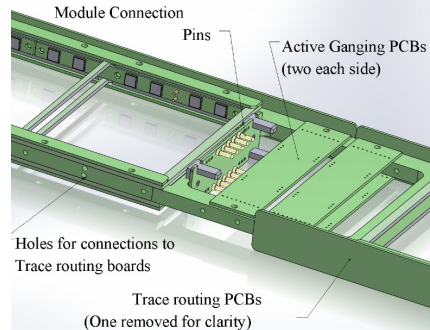
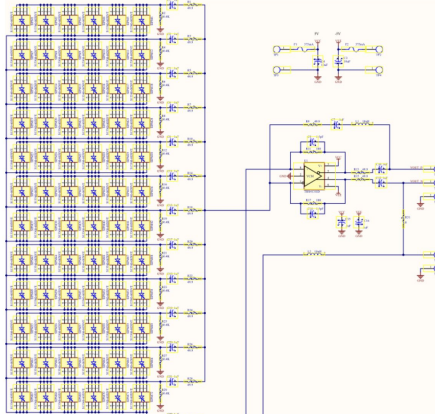
High readout burden → high power, summing electronics

- High granularity → high channel count electronics or SiPM summing/ganging
- High dark count rate:
 - $O(10^6/\text{mm}^2)$ at room temperature
 - For $O(100)$ SiPM detector at room temperature, approaching GHz data rate

High Temperature DCR measured by HPK (1.3x1.3 mm², S10362-11-050C)



Example from DUNE:
6x passive ganging + 8x active ganging
48 SiPM sum per readout

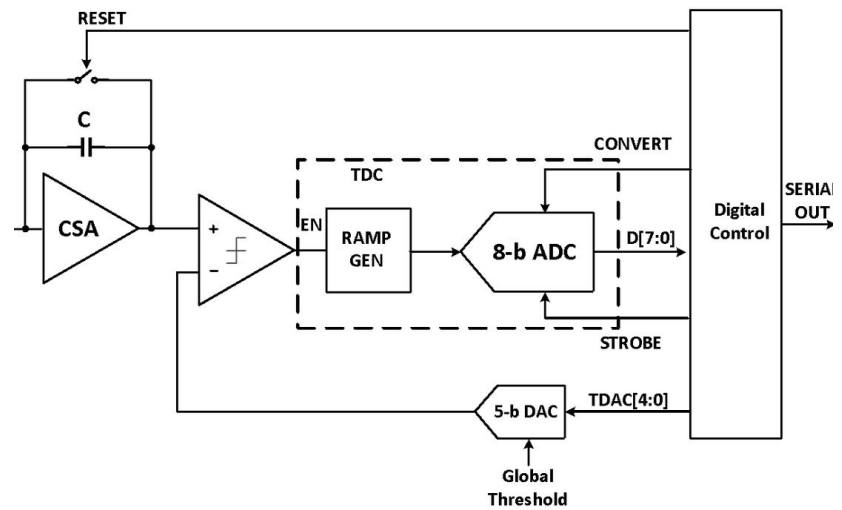


LightPix Concept

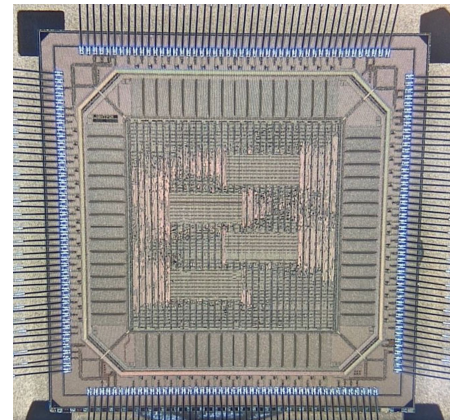
Scalable cryo-SiPM readout

- **Scalable, 'pixelated' SiPM readout ASIC**
 - No summing channels
- **Sister ASIC to LArPix** with same charge-sensitive front-end and digital core
 - **Demonstrated manufacturing:** full-industry, $O(10^6)$ channels produced
 - **Scalable readout** with PACMAN, hydra-I/O
- **Key upgrades from LArPix→LightPix-v1**
 - TDC with sub-ns precision
 - Tuneable hit coincidence requirements (1-64 channels over 100 ns-13 μ s)

See talks from D. Dwyer, K. Wood, C. Grace



LightPix v1b packaged chip on PCB

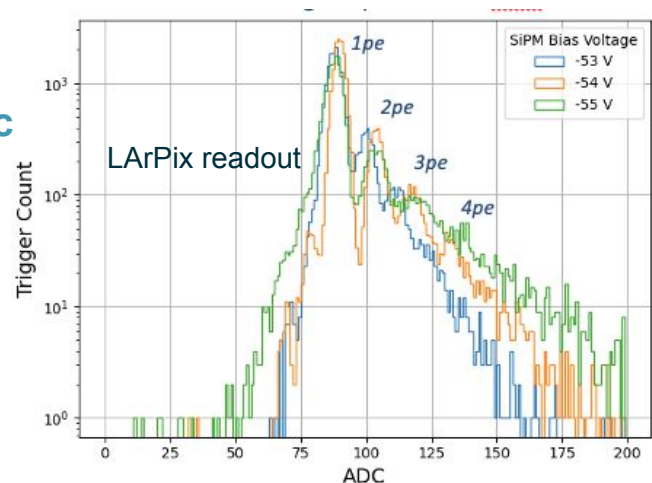


LightPix v1b die in 180nm CMOS ⁴

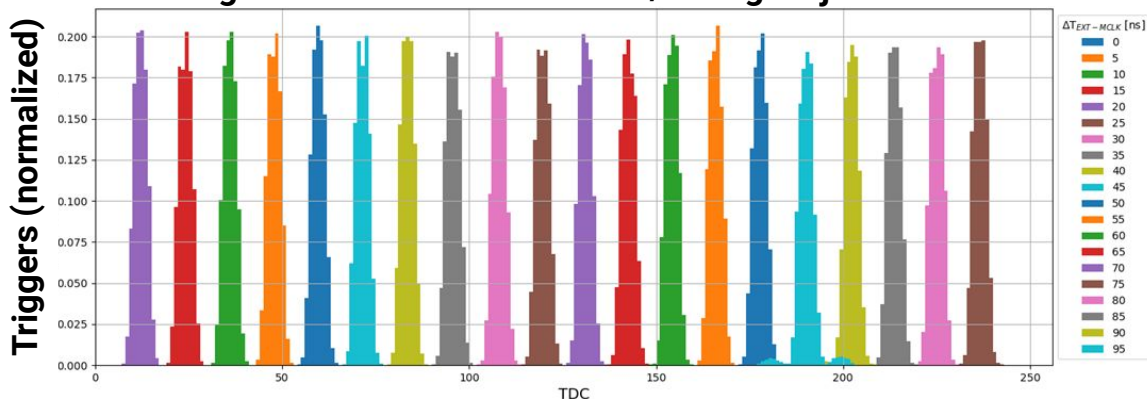
LightPix-v1b ASIC Performance

O(ns) TDC performance and verified hit coincidence logic

- **Verified functionality of digital core:**
 - Inter-ASIC I/O
 - Hit coincidence logic
- TDC evaluation for ~SPE inputs
 - Linear to <1 ns over 100 ns timing range
 - < 1 ns jitter
 - < 2 ns time-walk bias
- Ongoing evaluation with larger (3 x 3 mm²) SiPMs
 - Known design limitation– CSA dealing with higher terminal capacitance



LightPix TDC ~ns Precision w/ Charge Injection

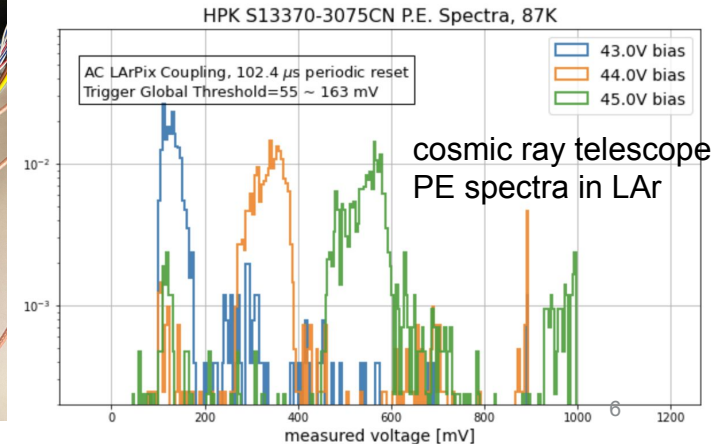
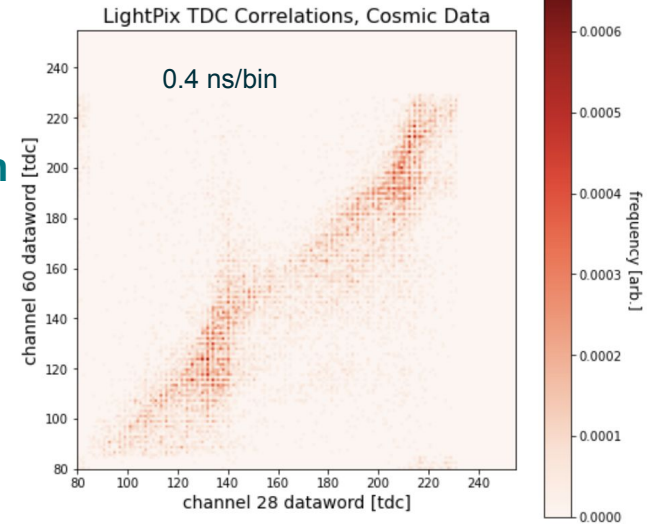
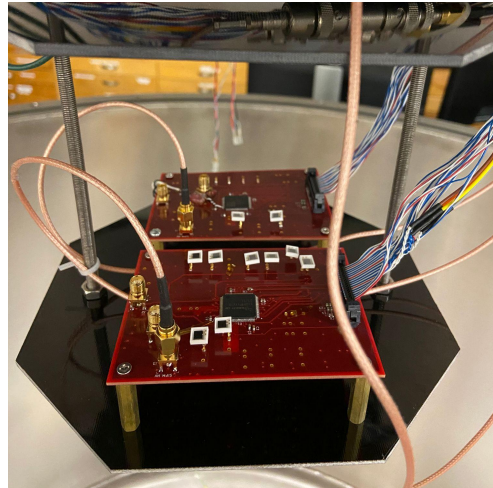


LArTPC Light Readout

Demonstrated direct-VUV detection, ongoing TPC integration

- **Successful LRO prototyping steps:**
 - » Operation of direct VUV cosmic ray telescope (CRT)
 - » Completed LRO board design (loading in progress)
- TPC constructed, HV and charge system checkouts completed
- First data run expected end of November 2023

LightPix CRT
test stand in
LAr

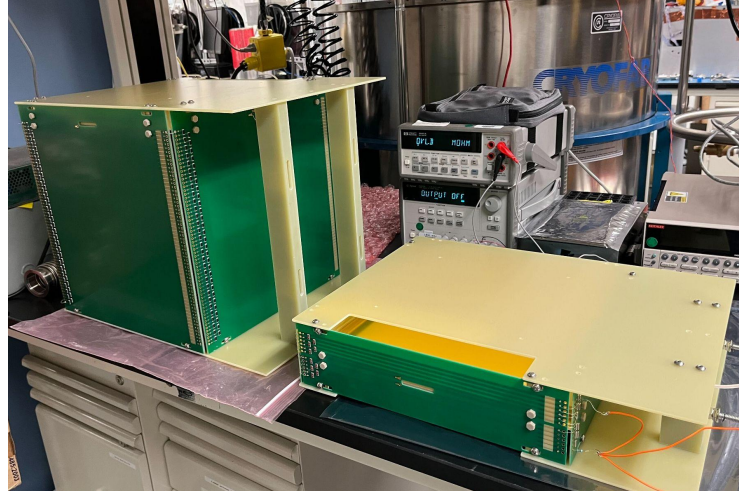


LArTPC Light Readout

Demonstrated direct-VUV detection, ongoing TPC integration

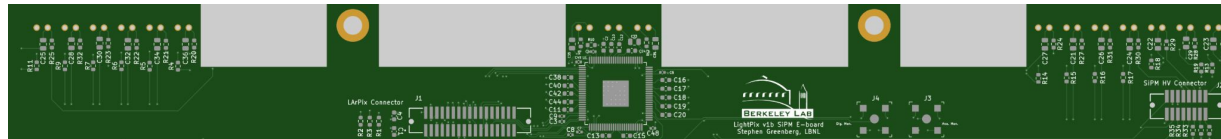


High Purity test stand at LBNL with SingleCube 30cm drift LArPix TPC



Assembled 30cm drift and 5cm drift central cathode TPC

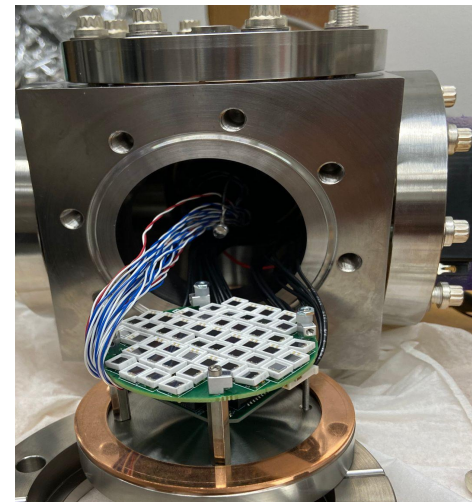
Direct-VUV LRO board design



GHe Neutron Detector

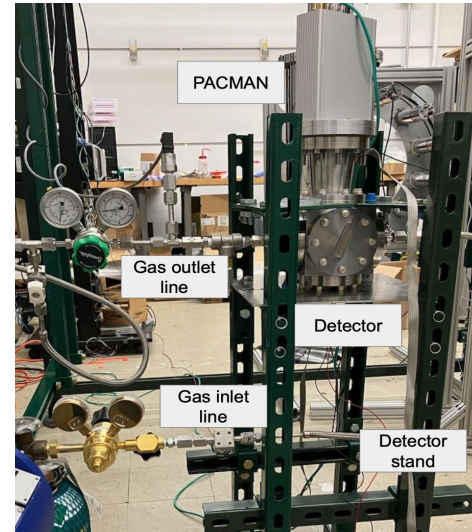
Room temperature detector with GHz DCR suppression

- R&D towards novel **room temp** neutron detector
 - High pressure (10-15 bar) GHe+% level GAR
 - 300 3x3 mm² direct VUV SiPMs → **GHz DCR**
- **1 LightPix ASIC / 50 SiPMs**
 - No summing/ganging → fully pixelated
- First prototype goals: demonstrate neutron sensitivity with DD neutron generator
 - Scientific goals: understanding helium scintillation and excimer formation



50 SiPMs
on single
detector
wall

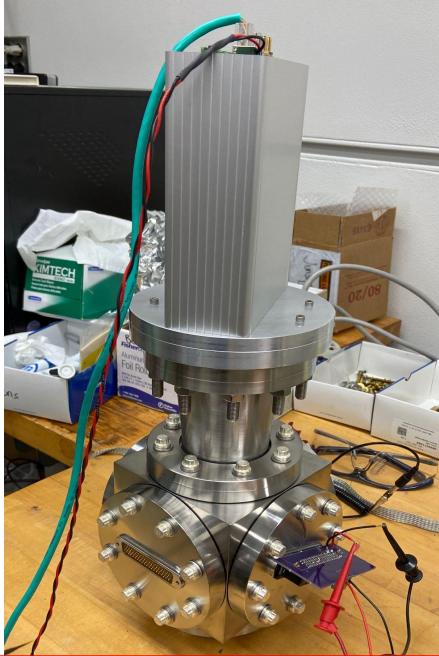
5x5x5 cm³
cube



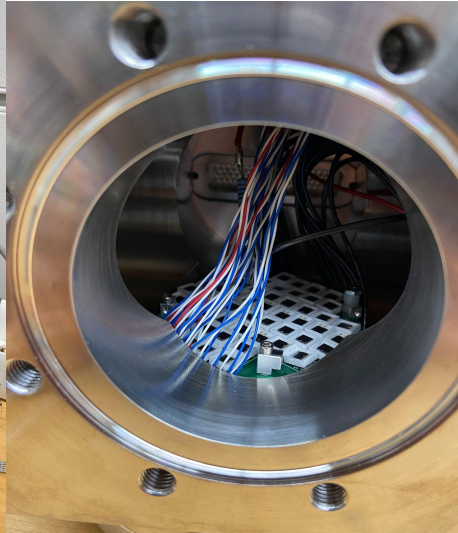
GHe test
stand at
UC
Berkeley

GHe Neutron Detector

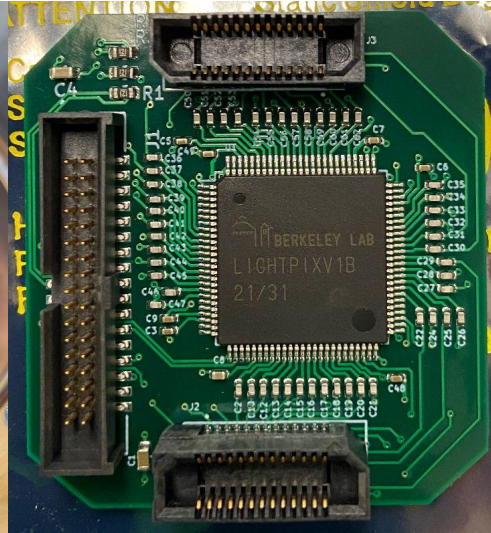
Room temperature detector with GHz DCR suppression



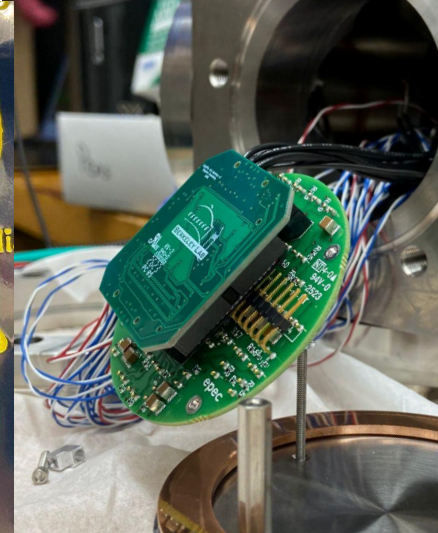
Conflat cube with PACMAN



SiPMs inside detector



LightPix readout PCB



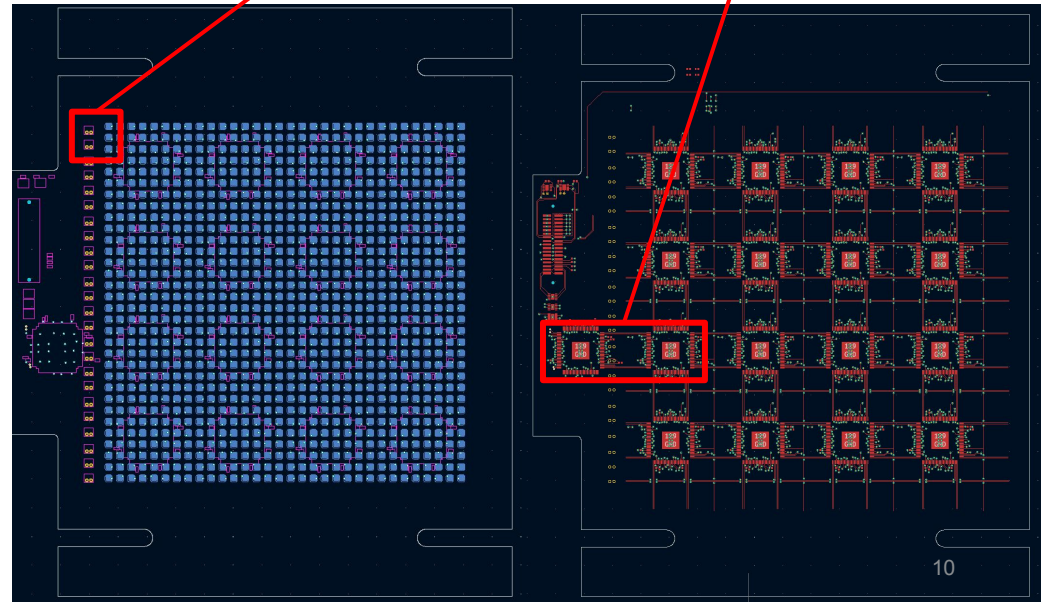
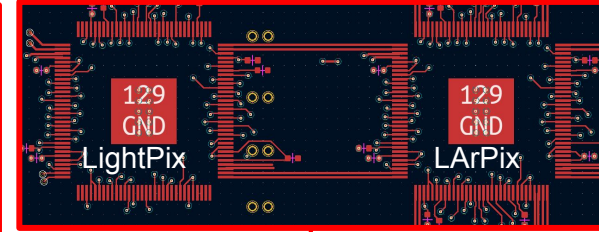
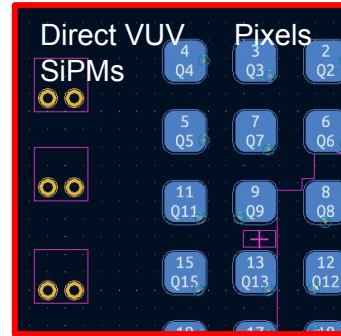
LightPix board mounted to SiPM board

LArPix / LightPix Co-Design

Single-cable charge+light readout in LArTPC

- Strong interest in direct light detection with VUV SiPMs integrated into TPC anode
 - E.g. SoLAr concept
- **Chip-to-chip I/O is ASIC-family independent**
 - LArPix+LightPix: shared power/IO/single cable

LArPix/LightPix dual charge+Light anode prototype design



LightPix-v3 Design

Design ramping up for next generation 'LightPix-v3' ASIC

- **Retain synergy with LArPix**
 - Digital core based on (recently re-designed) LArPix-v3
 - Same cabling, feedthrough, warm electronics as LArPix-v3
- **Major front-end improvements and additional digital features**
 - Higher power budget→higher bandwidth and larger loads
 - Charge sensitive amplifier→transimpedance amplifier
- **Inclusion of per-channel 10b ADC+ sub-ns TDC**

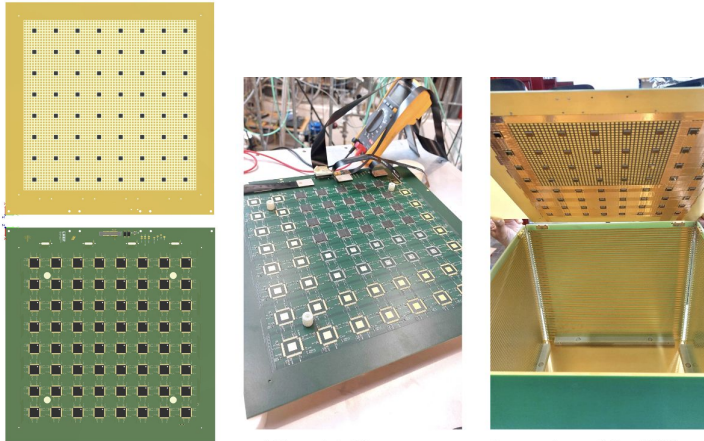
| Version | CMOS Process | Receipt Date | Front End | Readout |
|---------|--------------|--------------|-----------|-----------|
| 1b | 180 nm | Aug. 2021 | CSA | TDC |
| 3 | 130 nm | N/A* | TIA** | TDC+ADC** |

**ongoing design

Next Generation Detectors

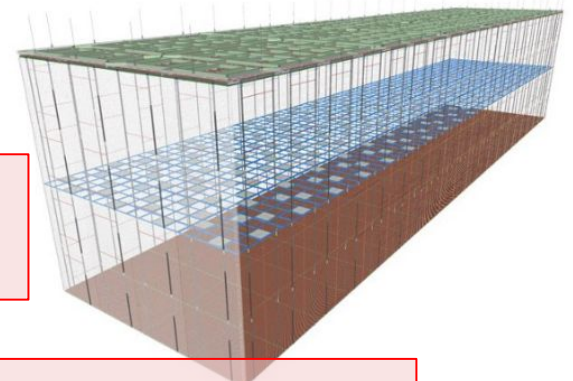
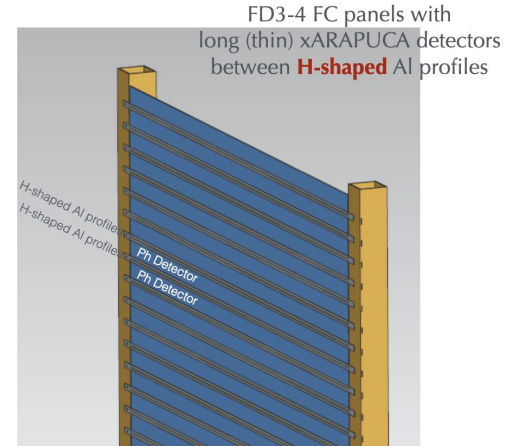
LightPix features aligned with community needs

- Major focus on enhanced PDS and increased SiPM channel count for DUNE FD3/4
- **LightPix suitable to retain granularity, ns timing**



SoLAR: <https://arxiv.org/abs/2203.07501>

SoLAR-v2 design (left) and realized prototype (right) from S. Parsa



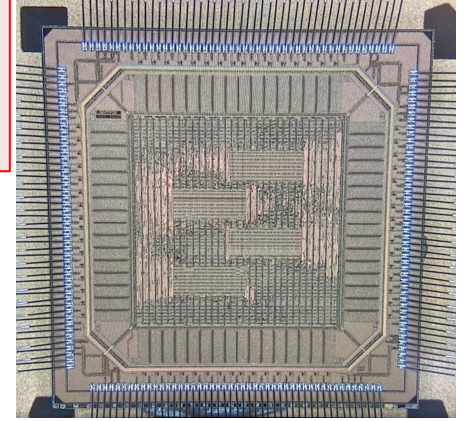
Example: “VD Optimized FD3” w/
enhanced PDS (*F. Cavanna*)
<https://indico.fnal.gov/event/59908/>

Summary

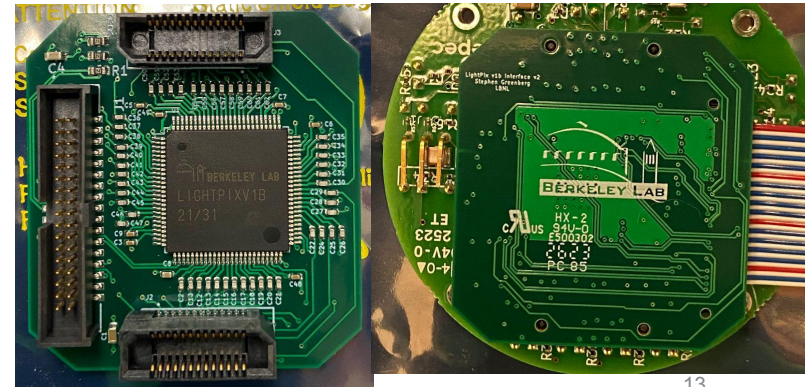
LightPix: scalable cryo-SiPM readout

- **LightPix: maintain LRO granularity**
 - Utilizing technologies demonstrated by LArPix
 - Synergy with LArPix for scalable combined detectors
- ASIC functionality demonstrated, ongoing in-detector demonstrations
 - LArTPC light readout with direct VUV technology
 - Room temperature GHe neutron detector
- **Next generation ASIC design ramping up**
- Prime candidate for large scale experiments
 - O(ns) timing, granular, low occupancy

LightPix-v1b
die in 180nm
CMOS



LightPix single-chip adapter
PCB+SiPM board



Backup

LArPix Concept

Scalable, True 3D Cryo-Readout for Pixels

- 64 channels/ASIC with CSA, self-triggering with tunable threshold, ADC
- Low noise, low power analog front-end
 - <100 uW passive per channel
 - ~800 e- ENC rms
- Self triggering → continuously active pixels with data streaming
 - ~0% dead-time, independent of light system
- Highly multiplexed digital I/O
 - 6400 channels/cable
 - 51,200 channels/warm controller
- Scalable at cost (O(\$0.10) per channel, including cables/controllers/assembly/etc.)

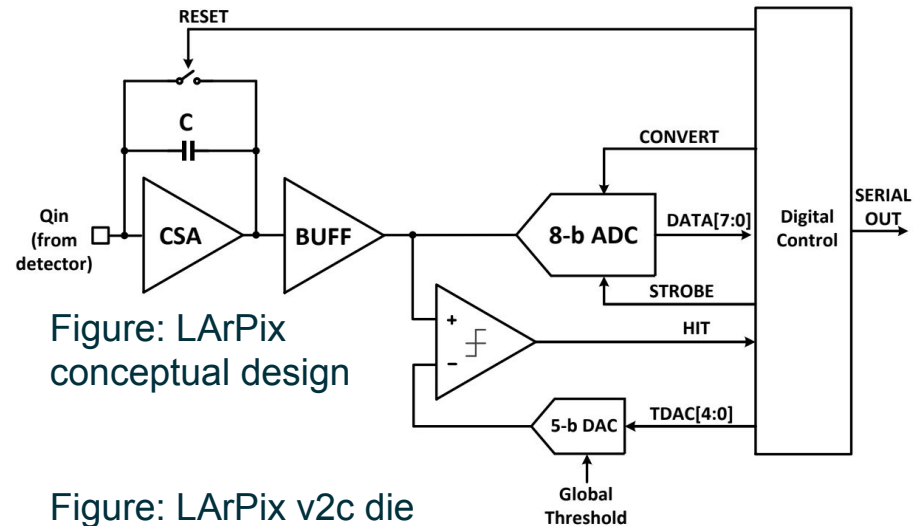
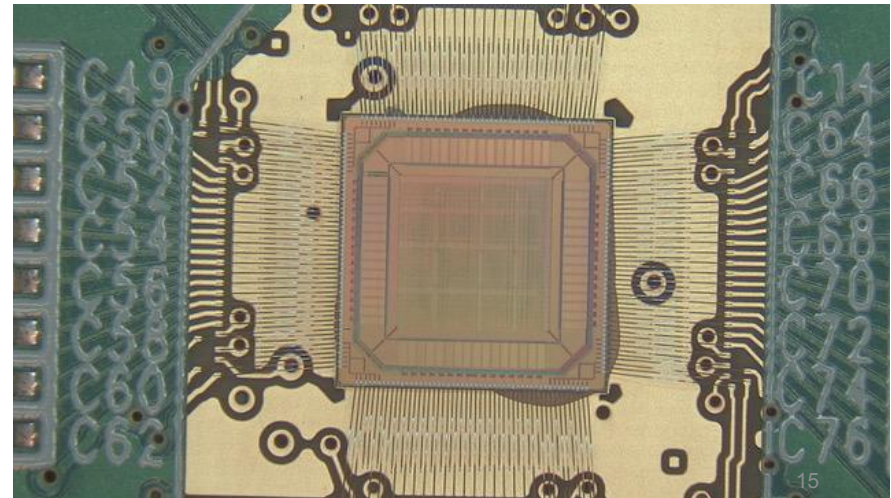


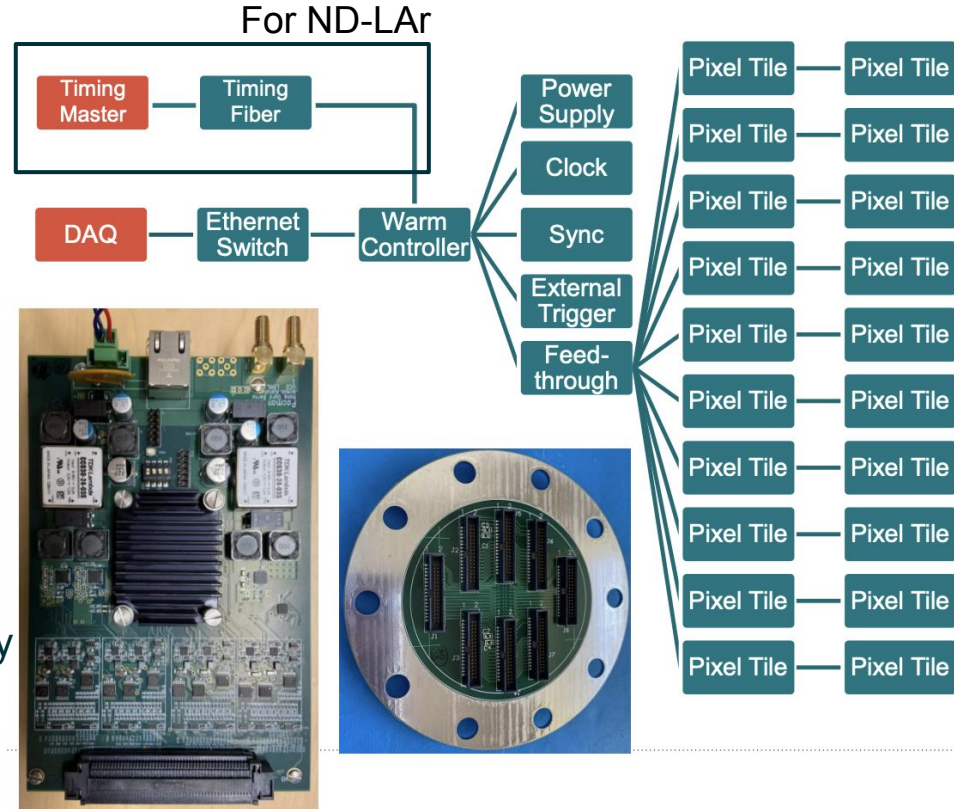
Figure: LArPix conceptual design

Figure: LArPix v2c die



LArPix/LightPix Full Detector System

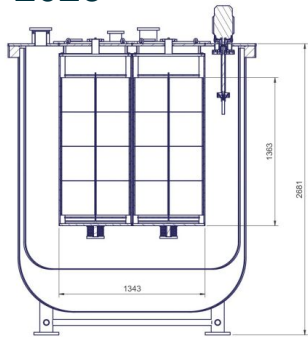
- Single cable per tile carries power/data/configuration commands
- Control and DAQ from PACMAN board at cryostat feedthrough
 - In use: 8 tiles/PACMAN
 - For ND-LAr: 10 tiles/PACMAN
- Data streamed continuously over ethernet to host machine



LArPix Demonstrations

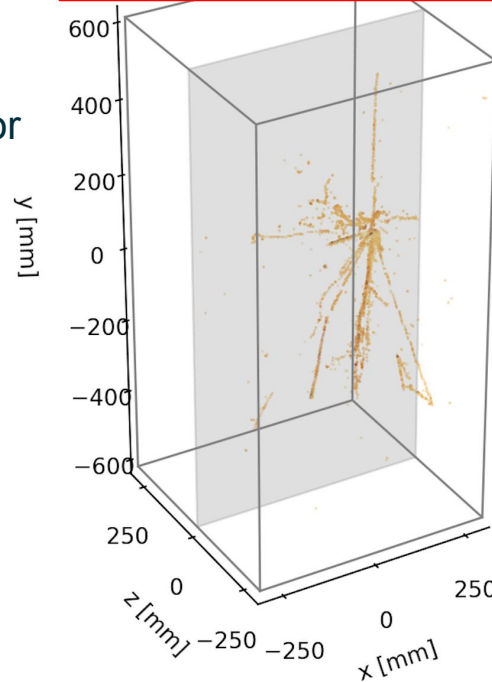
DUNE ND 2x2-Demonstrator Modules at LHEP → NuMI Beam at FNAL

- ~330k LArPix channels operated (78,000-102,000 / Module)
- 4.5 ke⁻ (~200 keV) triggering thresholds achieved in low threshold runs
- Ongoing installation of 2x2 Demonstrator in MINOS hall at Fermilab
- FNAL NuMI Beam data expected late 2023

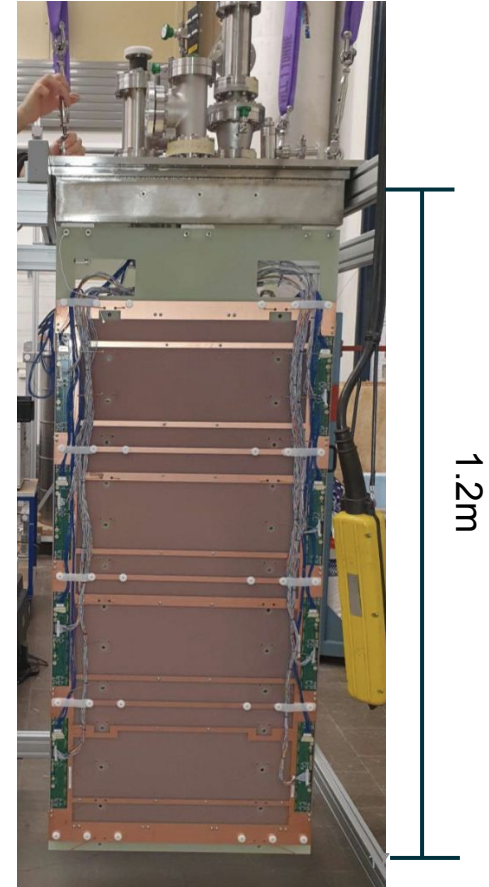


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LArPix raw 3D data
Module 2, Nov.-Dec. 2022

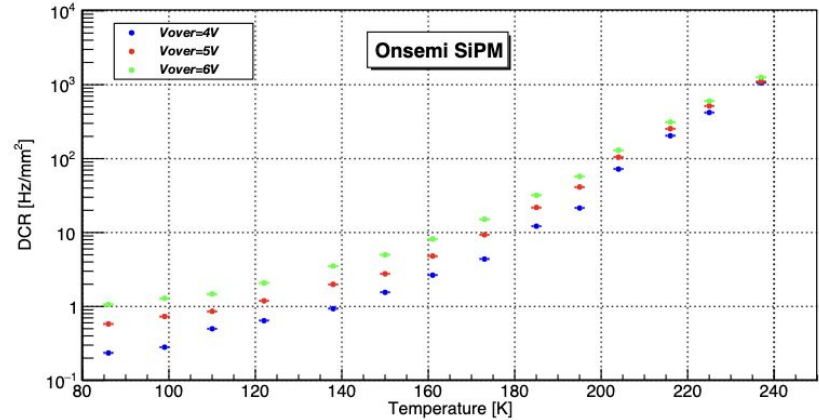
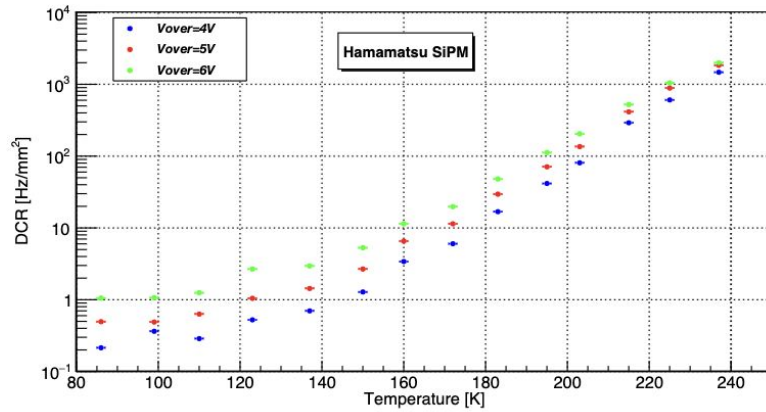


Fully Assembled Module



SiPM Cryogenic DCR

Cryogenic DCR for sample of HPK and Onsemi SiPMs



<https://arxiv.org/pdf/2210.15970.pdf>