Design of a 16 Channel 40 GS/sec 10 mW/Channel Waveform Sampling ASIC in 65 nm CMOS

Jinseo Park[2],

D. Braga[1], F. Fahim[1], N. J. Pastika[1], P. M. Rubinov[1], T. N. Zimmerman[1],

T. England[1], H. J. Frisch[2], M. Heintz[2], E. Oberla[2], C. Poe[2], Y. R. Yeung[2],

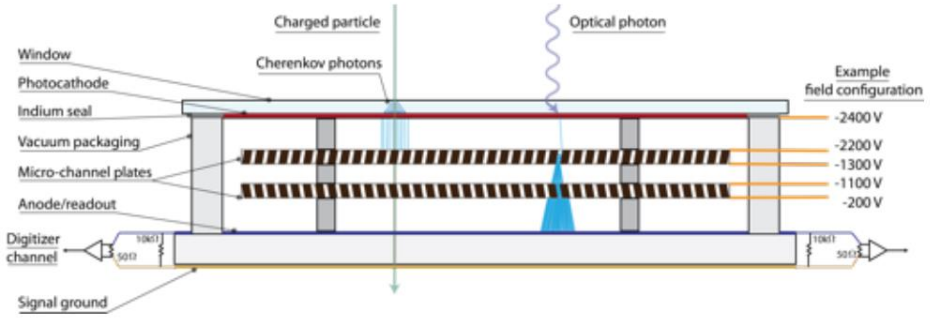
C. Ertley[3], N. Sullivan[4],

E. Angelico[5],

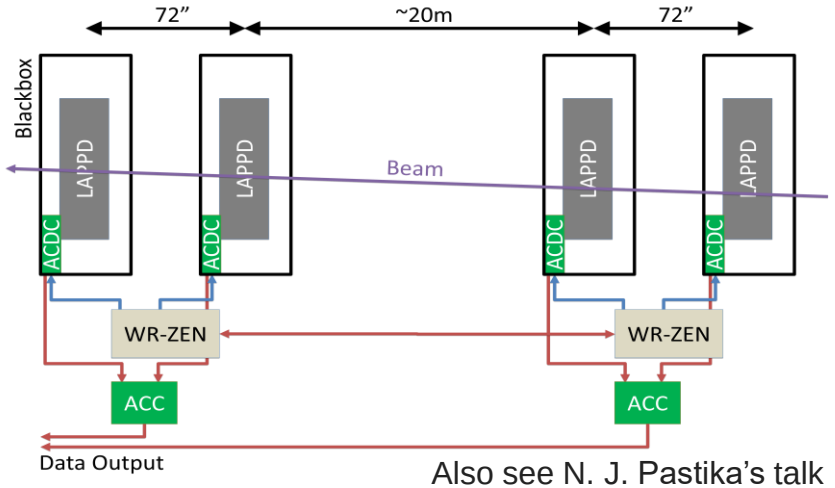
Hector Rico-Aniles[6]

1. Fermi National Accelerator Laboratory 2. University of Chicago 3. Southwest Research Institute 4. Angstrom Research Inc. 5. Stanford University 6. North Central College

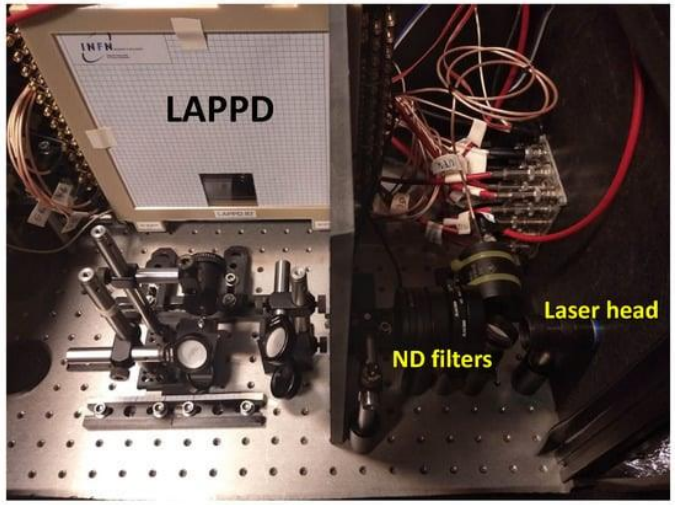
Motivation: Detectors with ps resolution



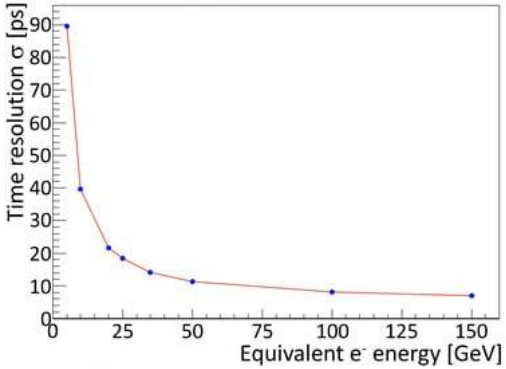
LAPPD^{TM}, psec.uchicago.edu

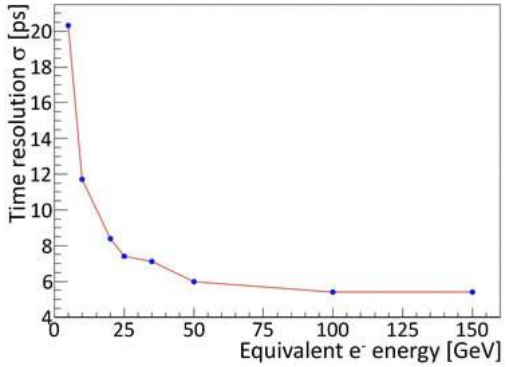


Also see N. J. Pastika's talk



Perazzini S, Ferrari F, Vagnoni VM, on behalf of the LHCb ECAL Upgrade-2 R&D Group. Development of an MCP-Based Timing Layer for the LHCb ECAL Upgrade-2





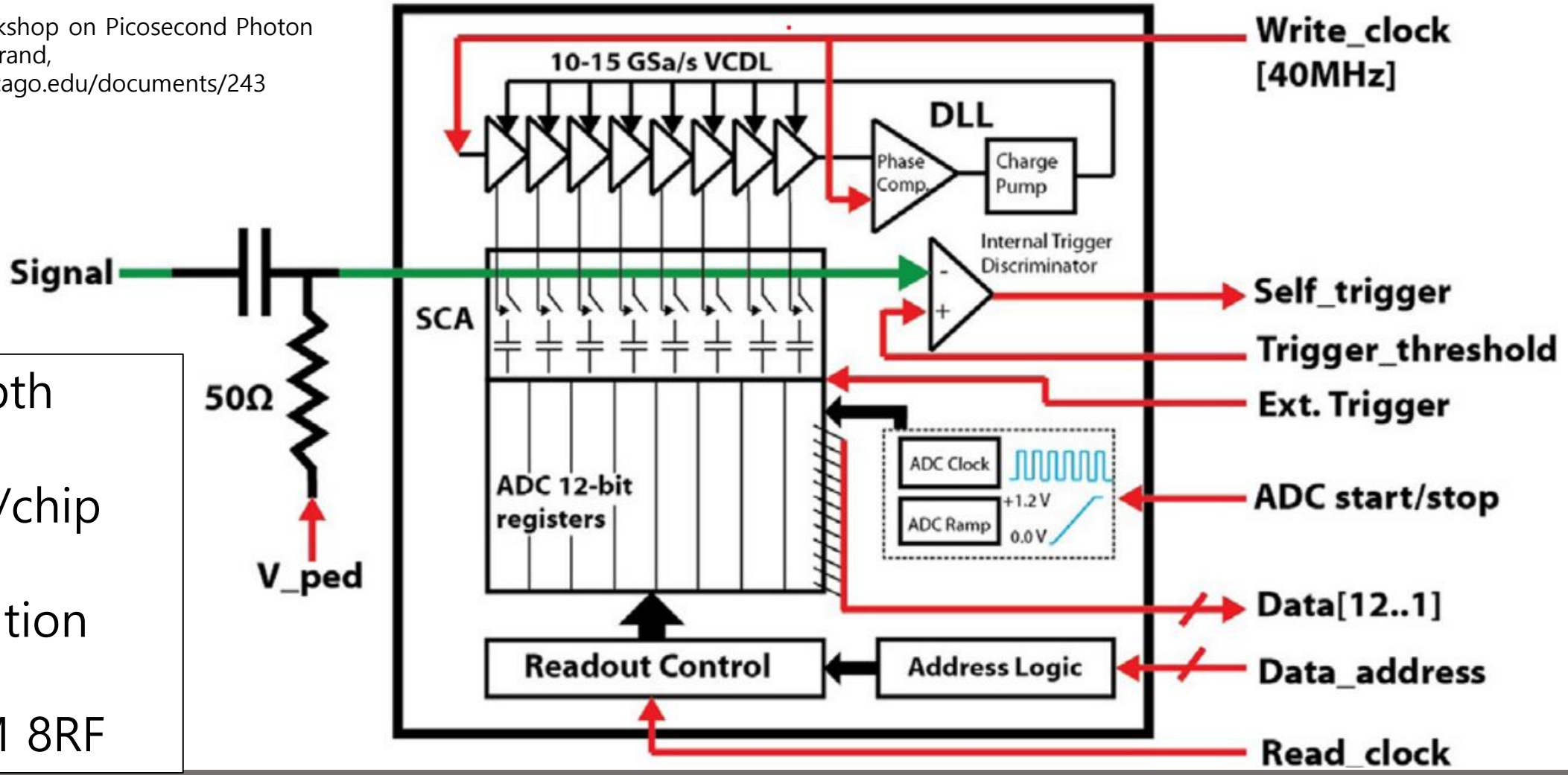
Timing resolution ~5ps

…WE ALSO NEED SUB-PS RESOLUTION FE ELECTRONICS!

PSEC4 ASIC(2014)

E. Oberla , H. Frisch, K. Nishimura, G. Varner, arxiv.org/abs/1309.4397

E. Oberla, Talk at Workshop on Picosecond Photon Sensors, Clermont-Ferrand, http://lappddocs.uchicago.edu/documents/243



- 12-bit depth
- 6 channel/chip
- 5ps resolution
- 130ns IBM 8RF

Performance Measurement

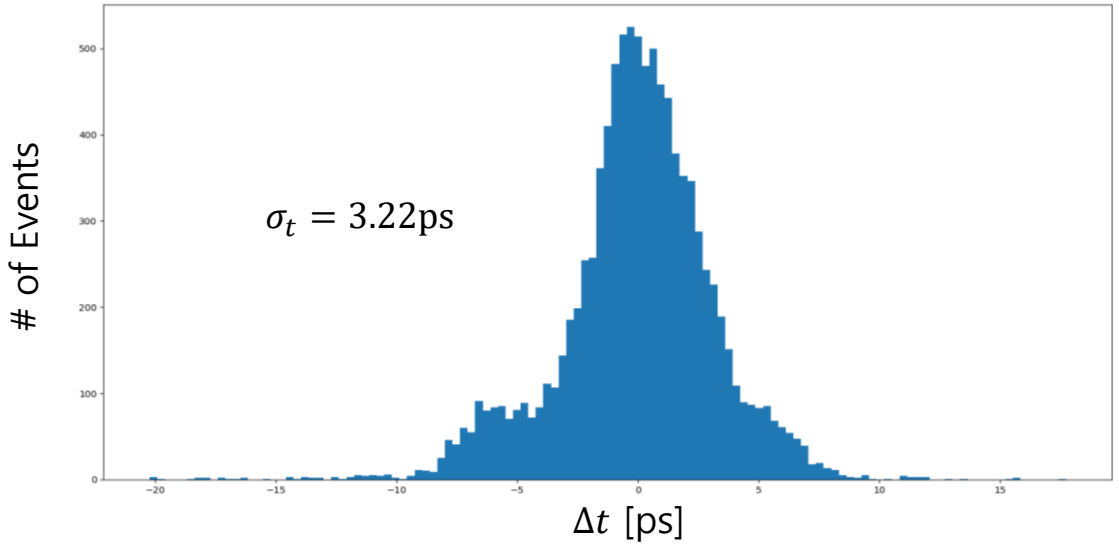
Same signal fed into two different channels of the same readout board.

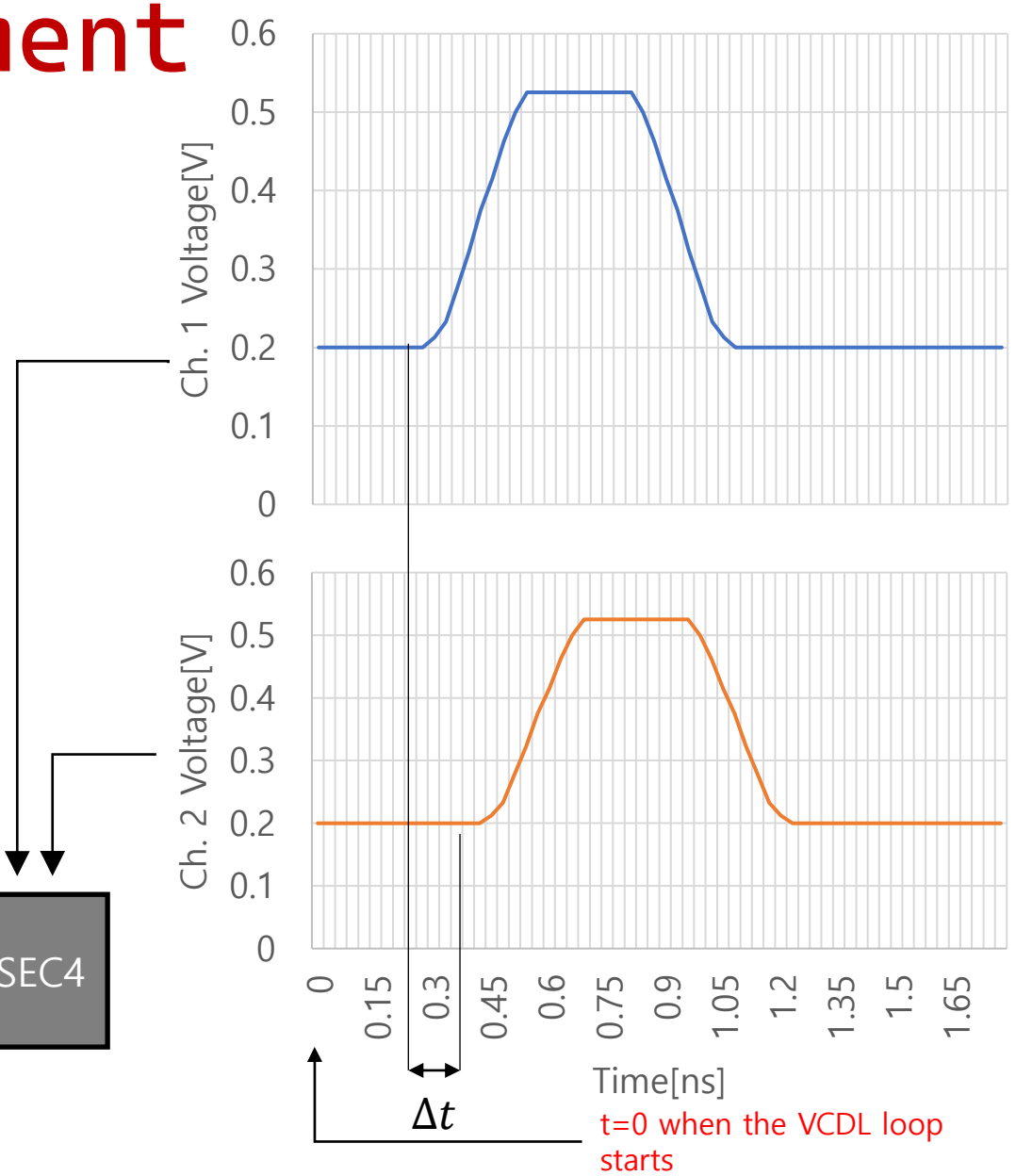
1. Δt measured for many events.
2. Distribution of Δt acquired.

Depends on the source

- Sin
- Pulse/square

Depends on algorithm determining Δt.





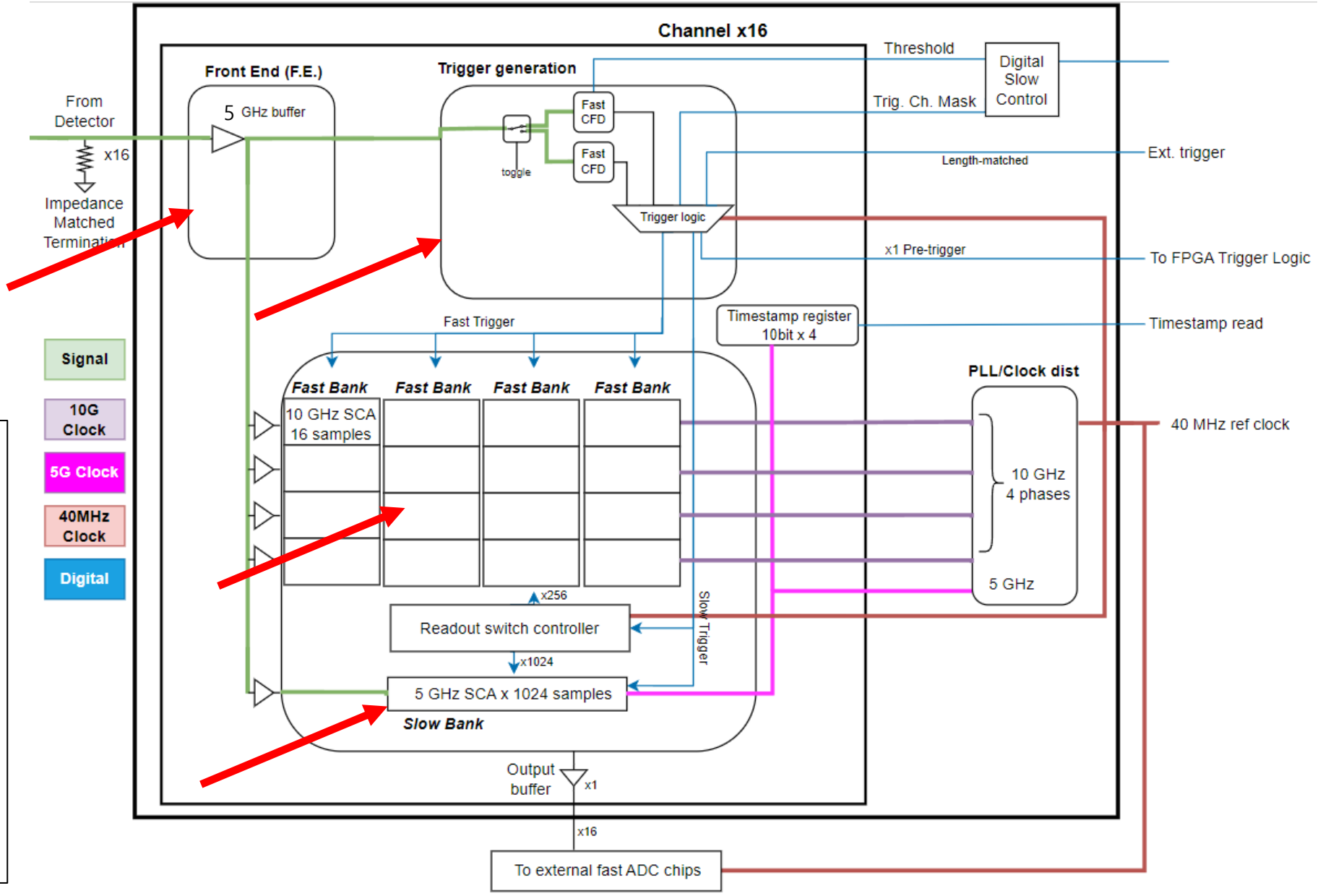
Primary goal

- Achieve **<1ps resolution** in measuring the arrival time of LAPPD pulses.

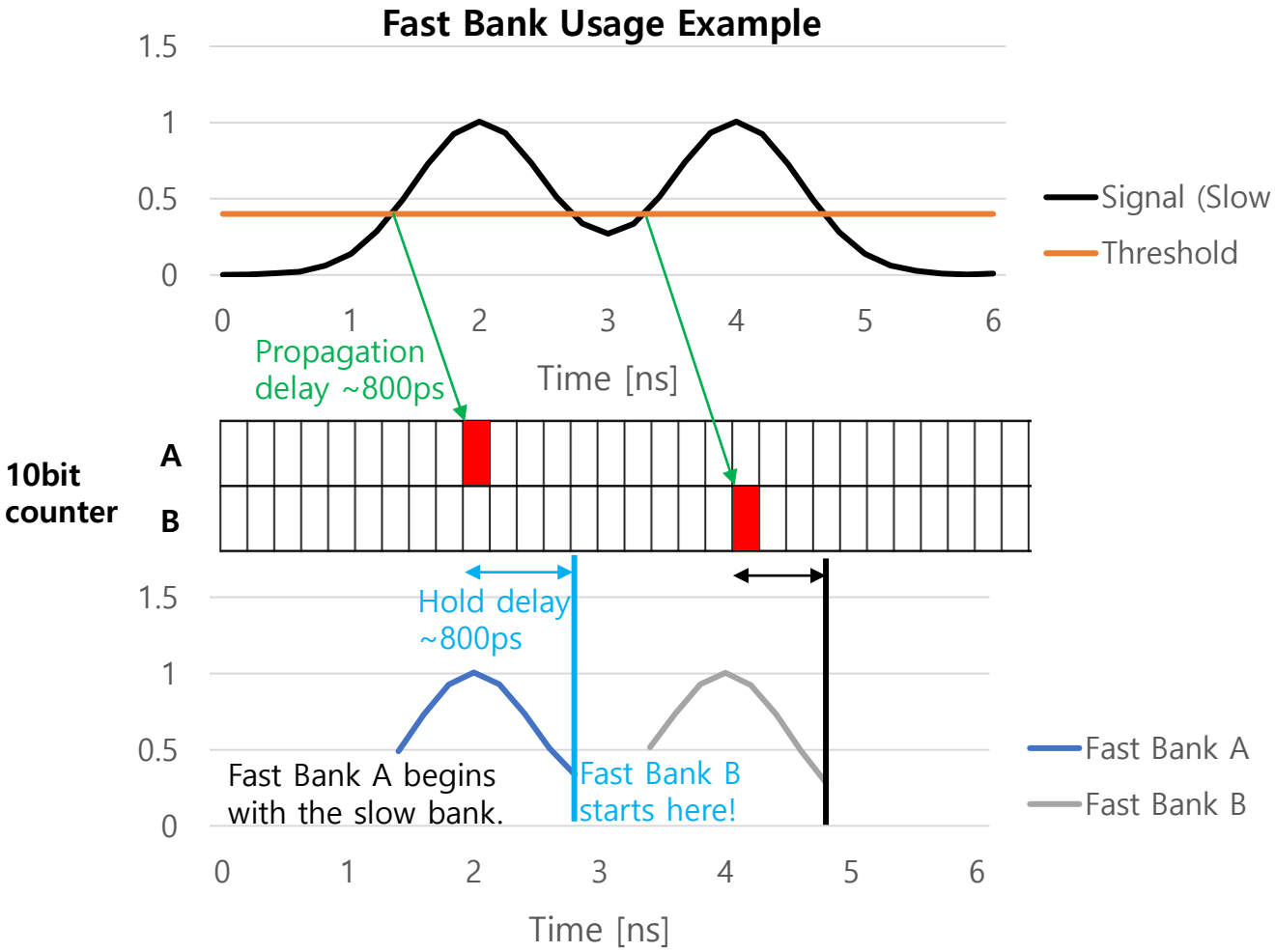
- But we also aim for a versatile chip, so that it is applicable to other fast-timing applications

PSEC5

- 65nm TSMC
- 10-bit depth
- 40GSa/s
- 5GHz Analog BW
- 16 channel/chip
- <10mW/ch
- UChicago & Fermilab

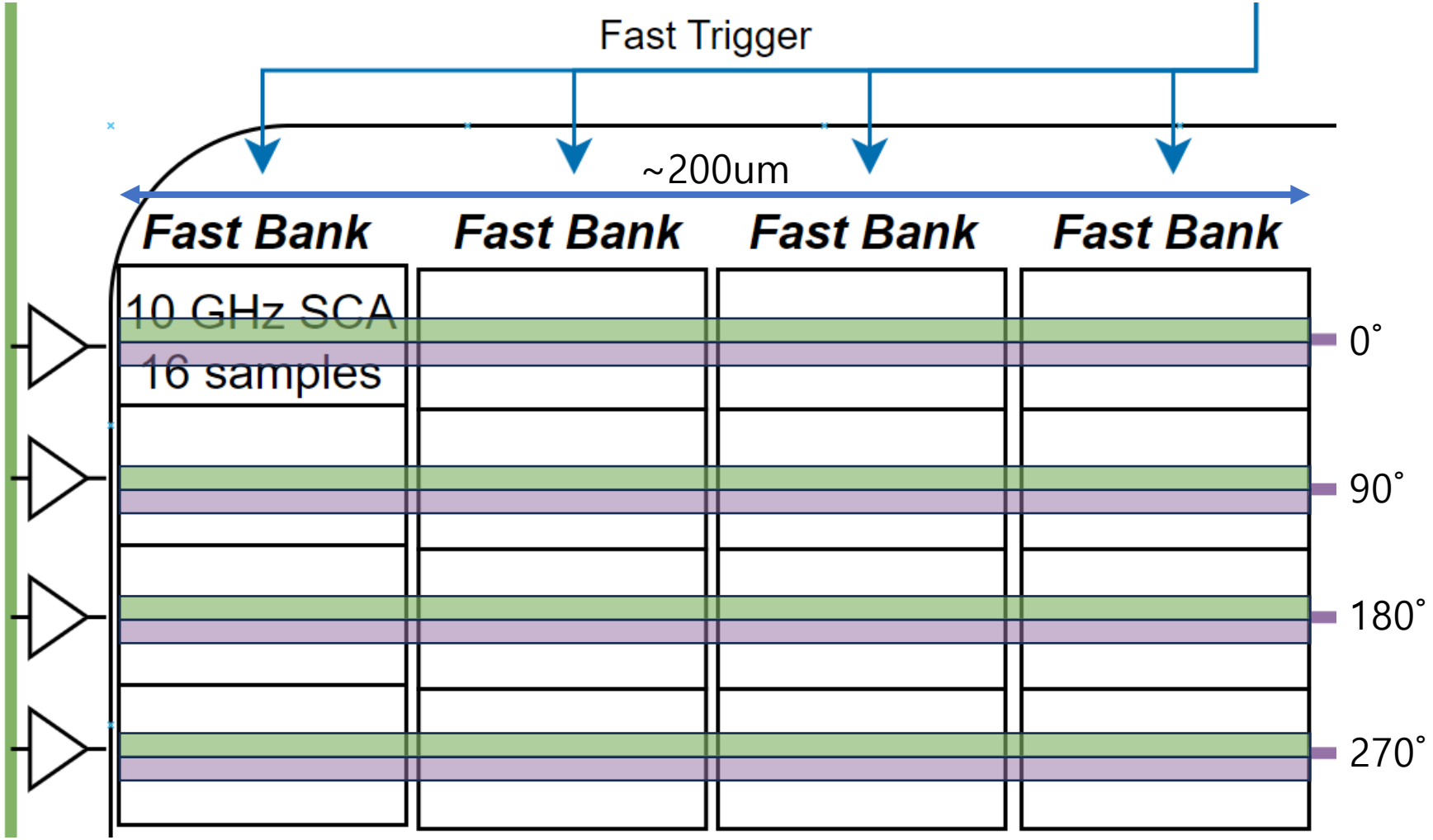


Point 1. Fast & Slow Banks

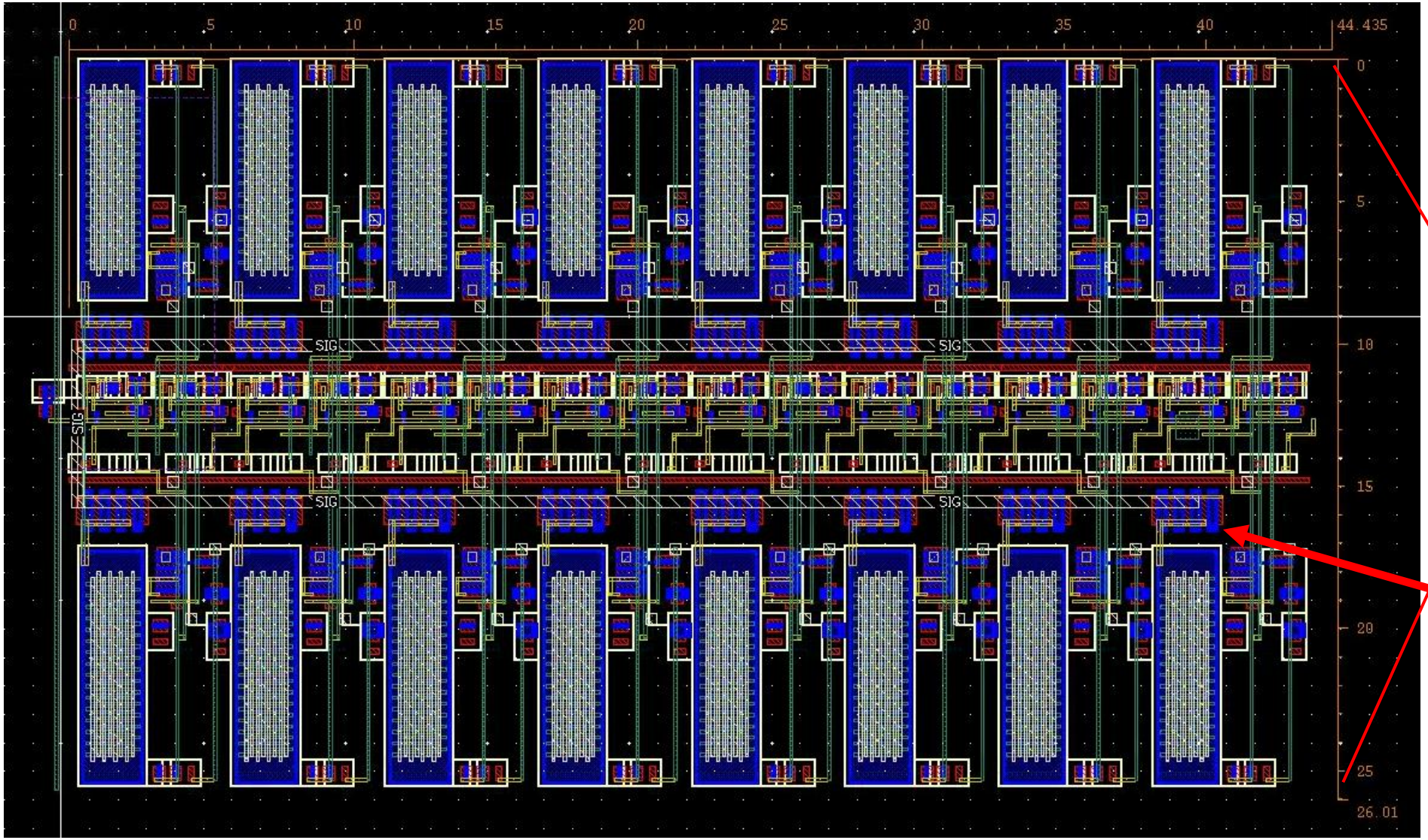


- Fast Bank: 4 of them
  - 64 samples
  - 1.6ns of sampling window
  - High power consumption
  - Run sequentially
- Slow Bank (Timestamp)
  - 1024 samples
  - 204.8ns of sampling window
  - Low power consumption
  - Fast banks are triggered within the sampling window

Fast sampling – interleaved



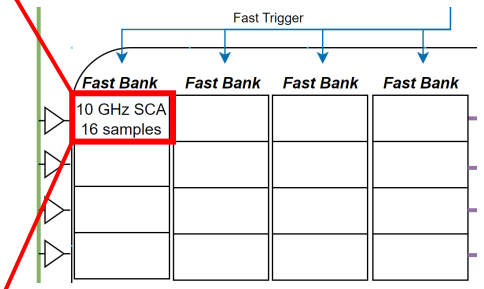
Layout of a single column (16 cells)



Size: $45\mu m \times 25\mu m$

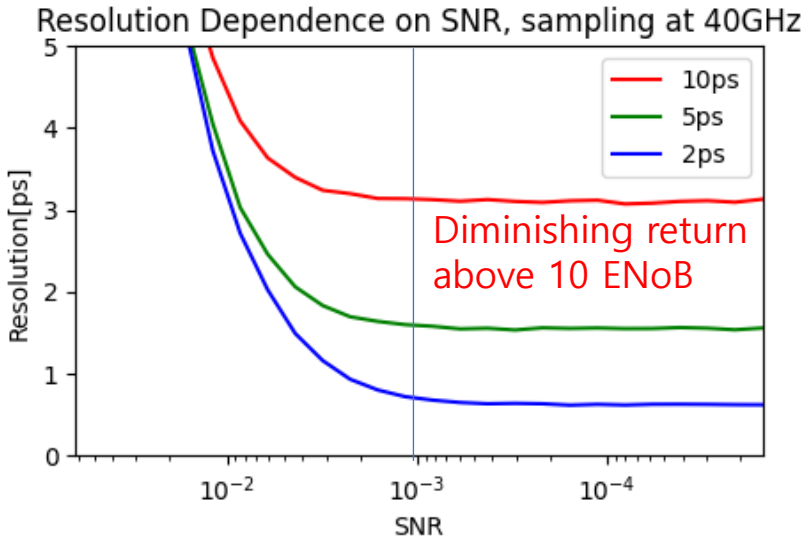
Capacitor: 35fF

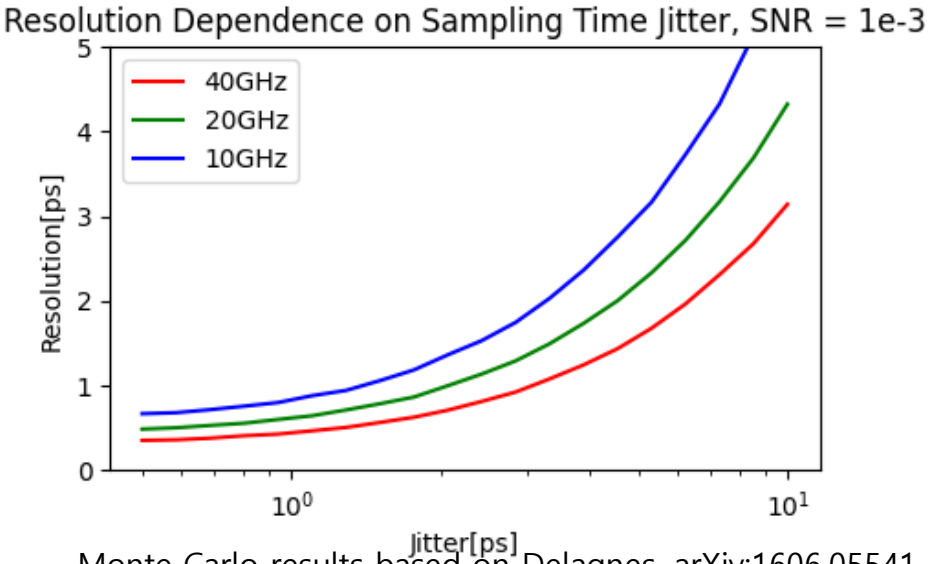
Power: 2mW



Sampling Switch
2.5V NMOS
Size: $4\mu m \times 280nm$

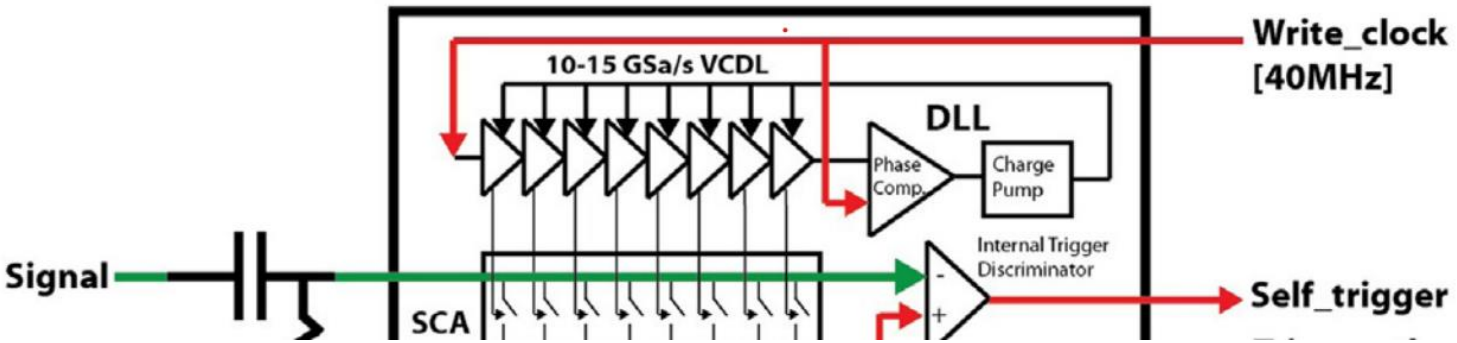
Point 2. Sampling Jitter



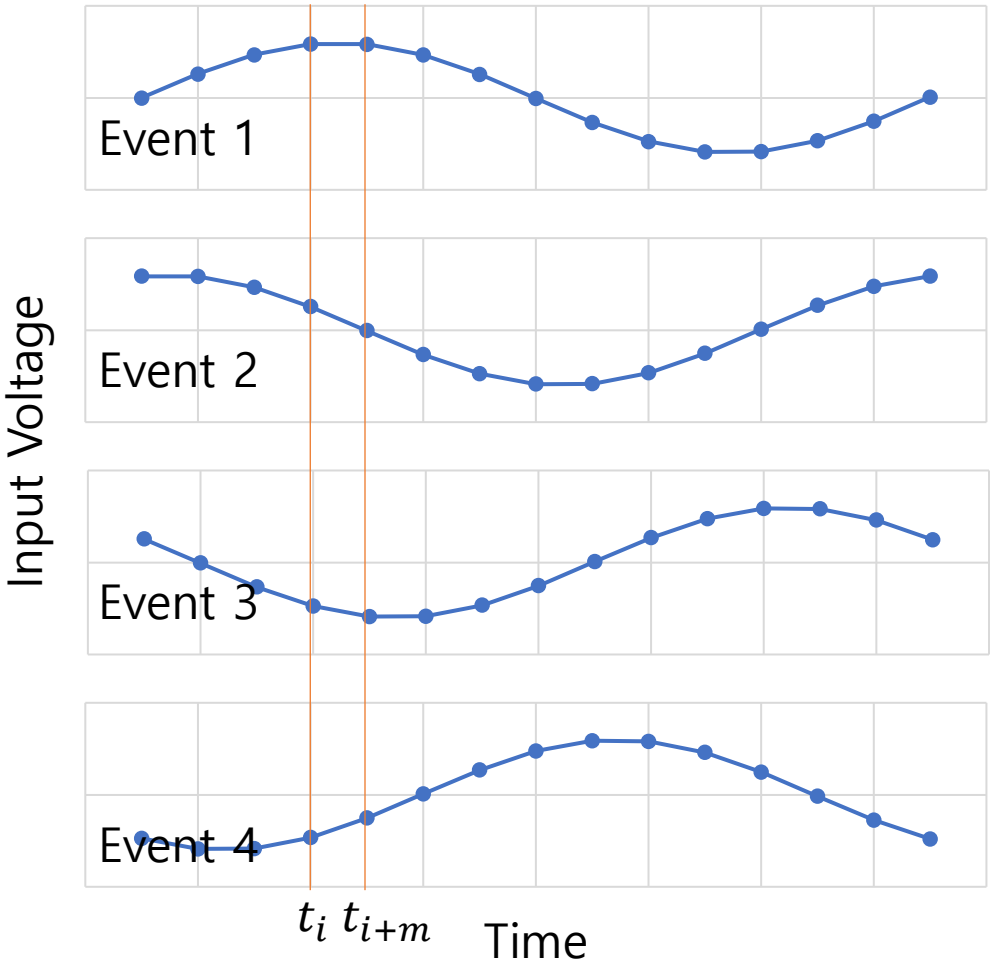


Monte Carlo results based on Delagnes, arXiv:1606.05541

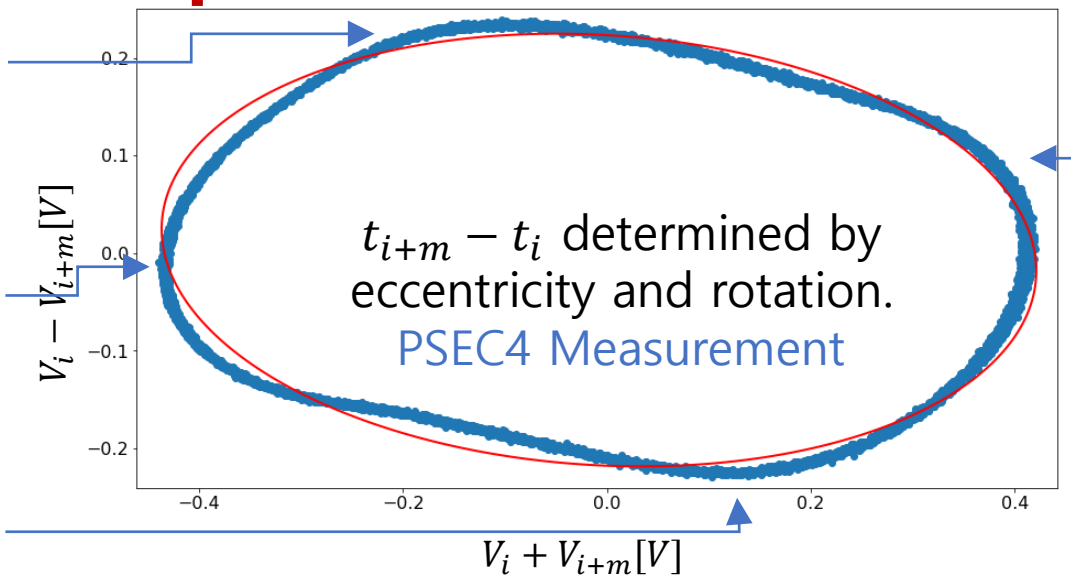
- At <1ps timing resolution region, sampling jitter is a **dominant component** of the overall uncertainty.
- PSEC4 employs Delay Loop Lines (DLL) to control sampling switches.



1. Measure many events of a sine wave.
2. Sum vs. Difference of two adjacent samples, over all events, form an ellipse.
3. Time offset can be determined from the coefficients.

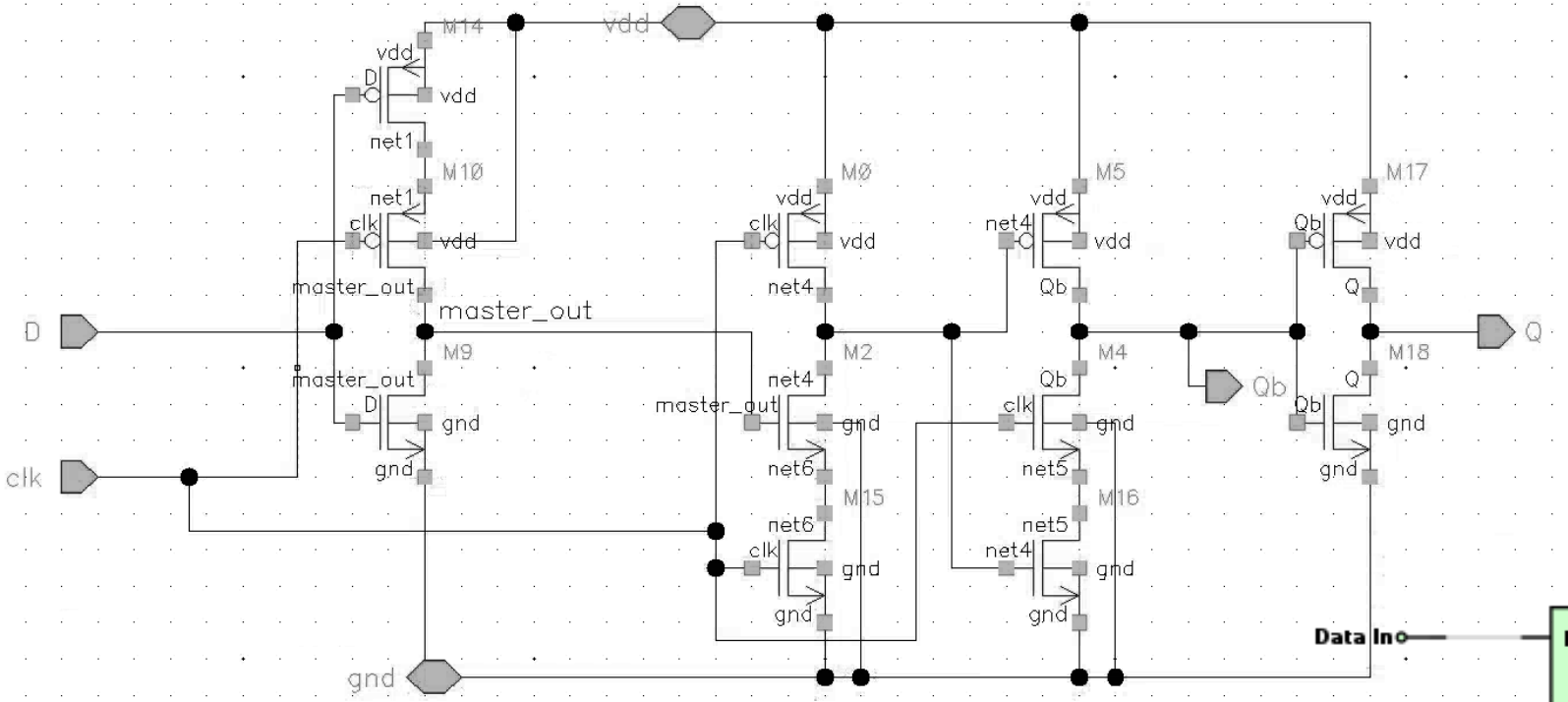


Bandwidth affects sample time uncertainty!

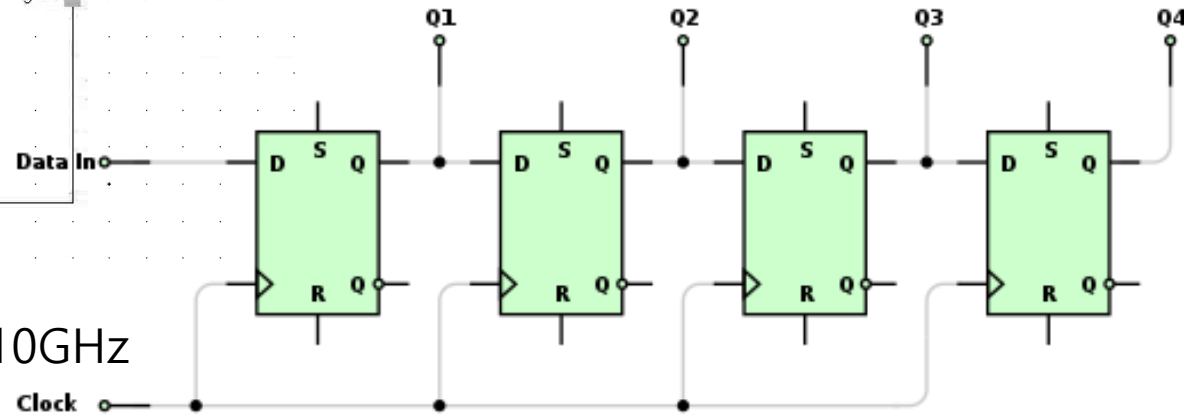


Low SNR → fainter, more spread curve.
Nonlinearity → distorted curve

10GHz True Single Phase Clock D Flip Flop

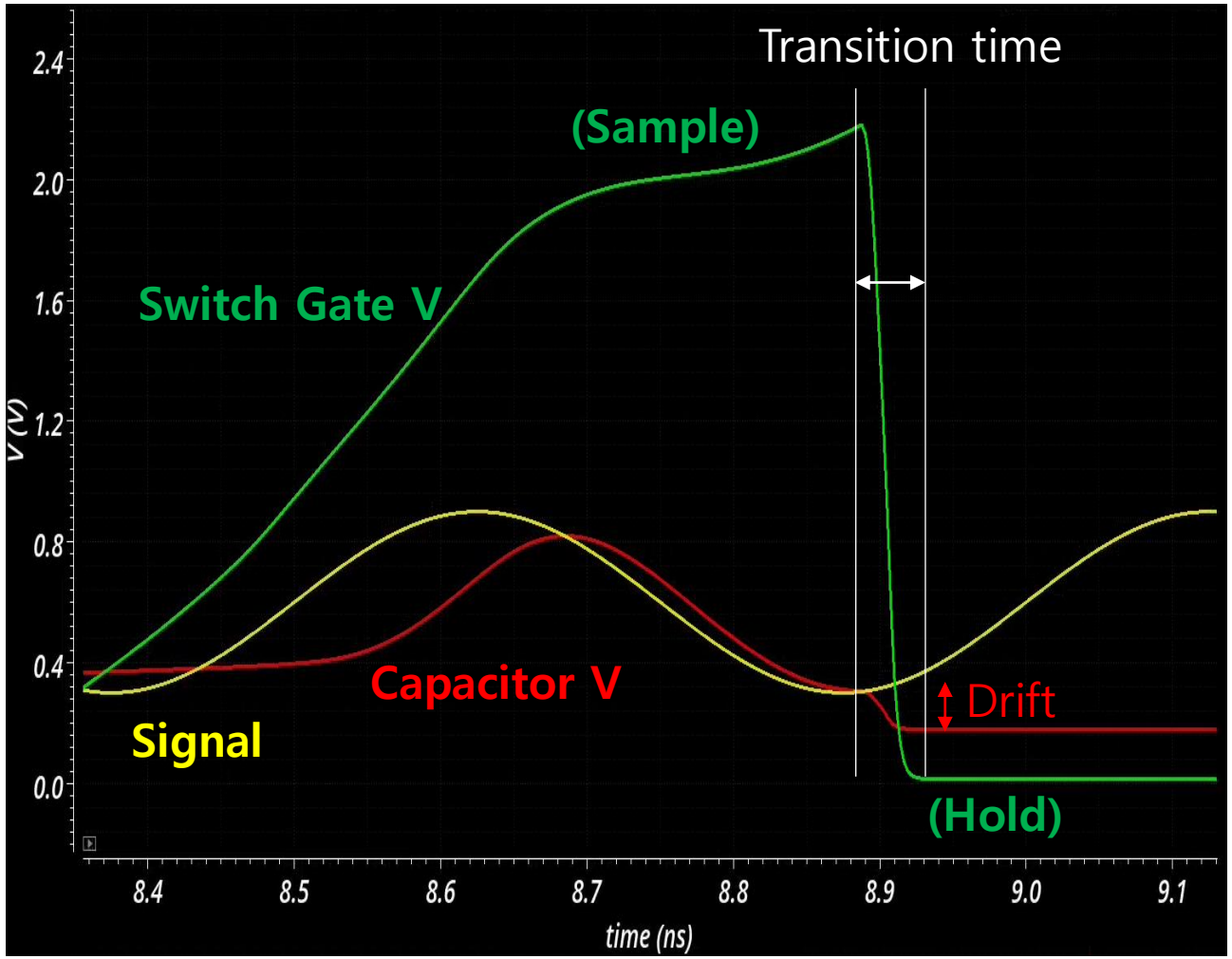


To each sampling switches



- Still, we expect to use similar calibration technique as PSEC4

Switching Drift



- The value of a capacitor **drifts while it switches off** from the signal line.
- Drift consists of **switch gate charge injection**, which is a fixed value and is calibratable, and **resistive drift**, which is dependent on signal V.
- It is essential to keep the

[Sample → Hold] transition time low.

→NMOS instead of CMOS for the sampling switch!

Summary

- MCP-based detectors can reach excellent timing resolution, and for a working ToF system with it, we want **<1ps timing resolution** of the front-end electronics.
- We think a **waveform sampling** ASIC is the most reliable, reusable, and cost-efficient solution.
  - Lower power consumption and dead time
  - Avails various methods of external calibration
  - **High channel count** per chip
- The **fast-slow architecture** of the chip makes it relatively versatile
  - Long time window per event
  - While also achieving high timing resolution on regions of interest
  - Using **D Flip Flops** instead of Delay Line improves sampling time jitter
  - **Discriminator/Trigger logic with low propagation delay** is the key
- 65nm is an adequate technology for this
  - **Faster sampling speed**, due to dynamic flip flops, compared to coarser technologies
  - High voltage transistors available compared to smaller technologies, can achieve a high V **dynamic range**