Lightweight embedding and interconnection of flexible ultra-thin silicon detectors

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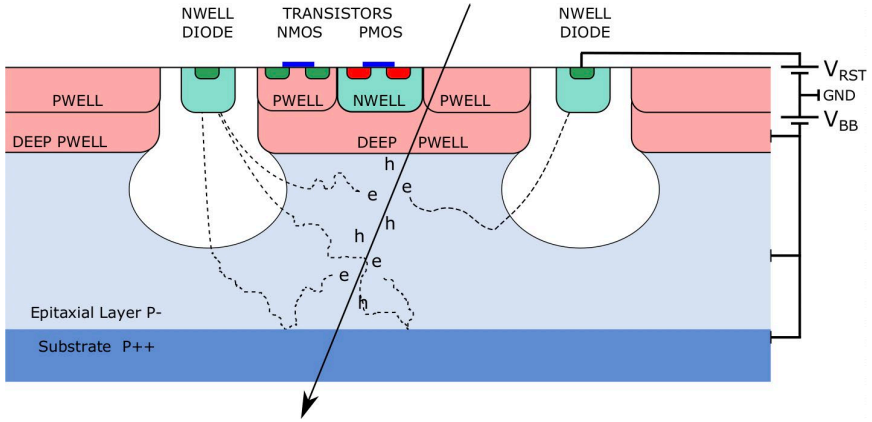
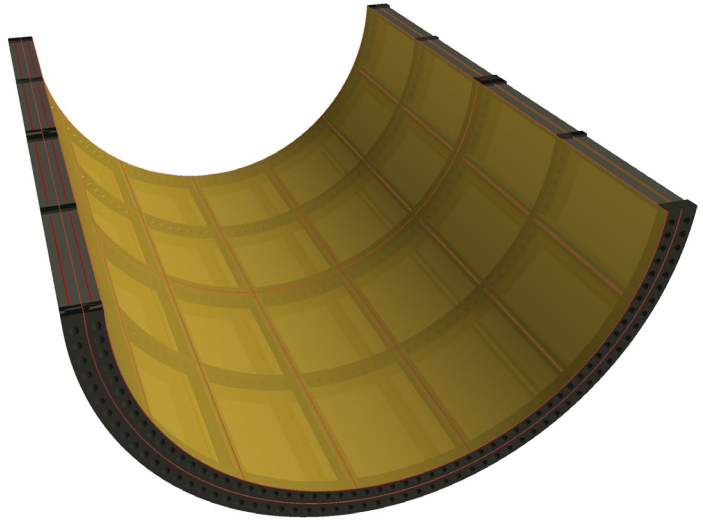
ORNL is managed by UT-Battelle LLC for the US Department of Energy

Introduction

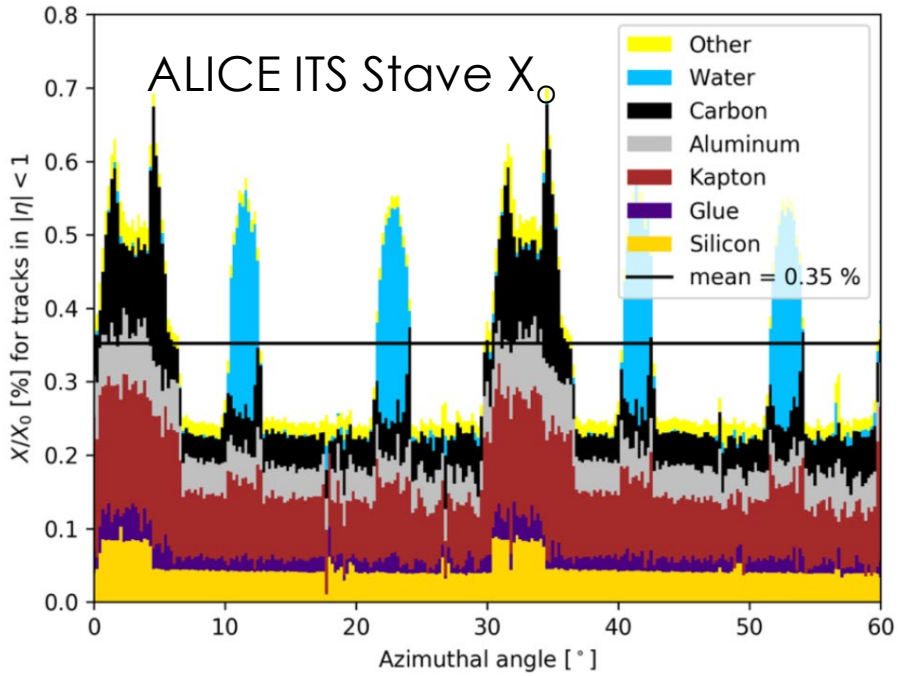
EIC ePIC Silicon Vertex detector (SVT) plans to make use of ALICE ITS3 Monolithic Active Pixel Sensors (MAPS)

- Large area, full wafer scale sensors using stitching techniques
- Thin substrate possible due to technology (<50 µm), entering a mechanical regime where silicon is flexible
- The ePIC SVT plan to use these sensors in a self substaining mechanical configuration to achieve close to optimal X_0

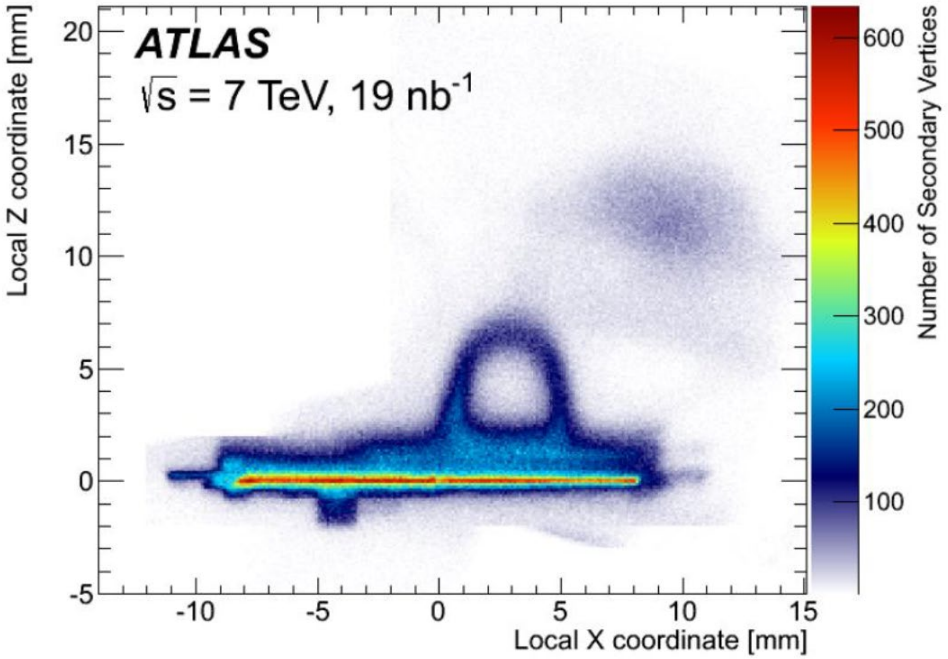




Motivation

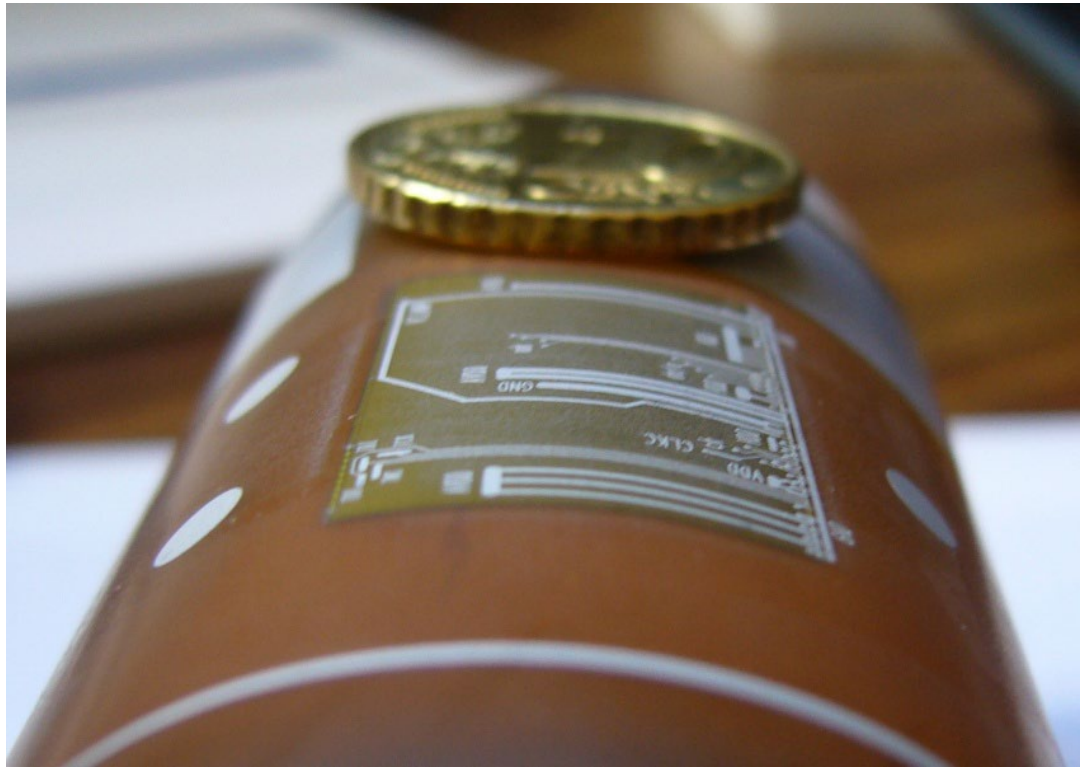


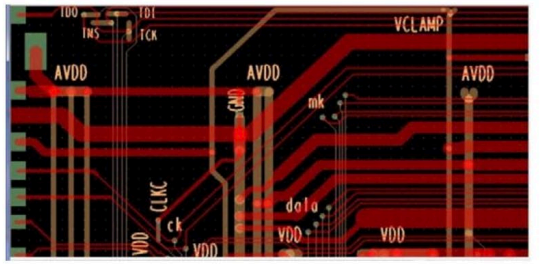
Secondary vertices in an ATLAS Stave



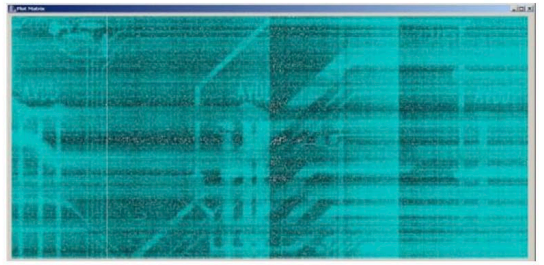
- Modern tracking detector's material budget are dominated by cooling, supports and signal and power routing.
- Next generation of experiment will achieve larger-than-ever instrumented area and will require large scale production
  - Increase durability of sensor modules ensure better yield
  - Kapton embedding makes modules more resistant to vibration, handling damage, harsh environements

Flex embedded sensors, an old new concept

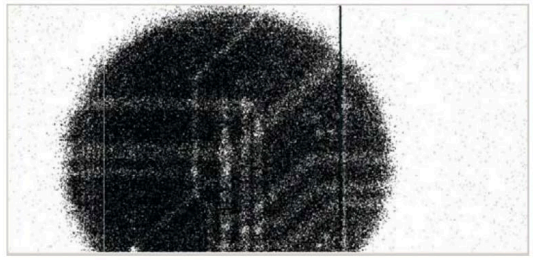




Lithography details of interconnecting metal (two layers of ~10 µm thick Al) deposited on top of the pixel sensor



"Shadow" of metal measured by pixel sensor in visible light



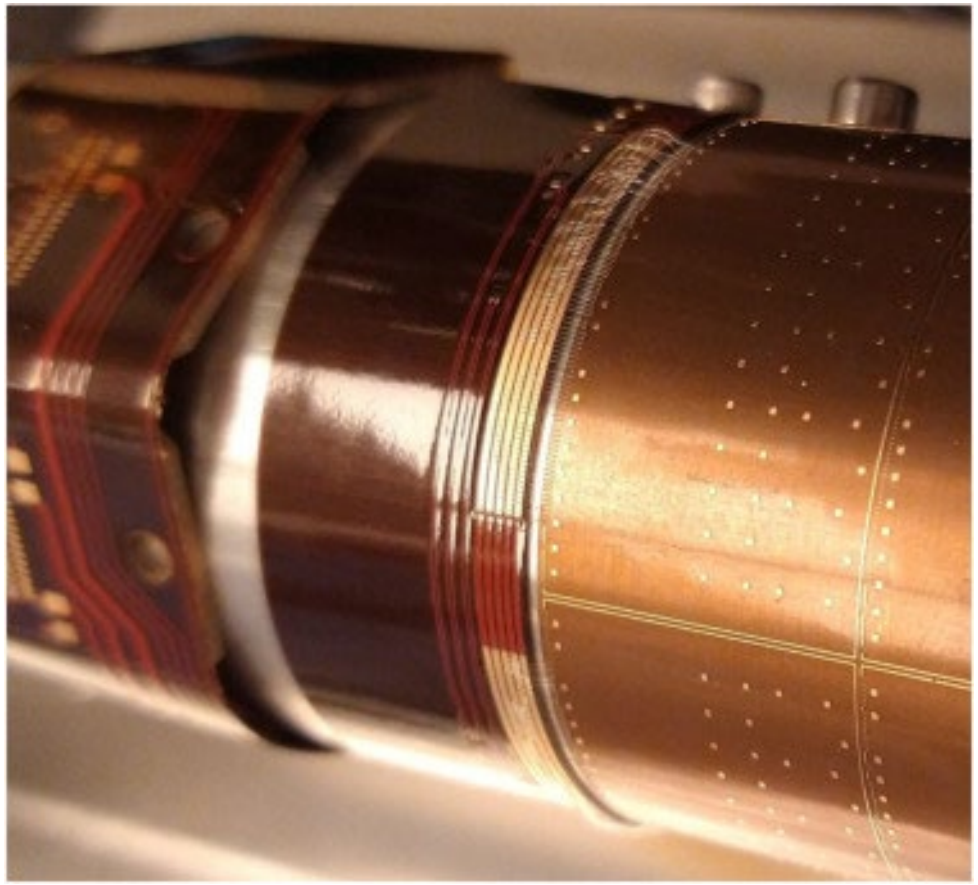
Auto-radiography of metal measured by pixel sensor using 5.9 keV Xrays (^{55}Fe)

Already more than a decade ago, PLUME, SERVIETTE and PLUMETTE collaboration investigated and succeeded at embedding thin MAPS sensors in Kapton flex

New fabrication and packaging technologies for CMOS pixel sensors: closing gap between hybrid and monolithic, W. Dulinski

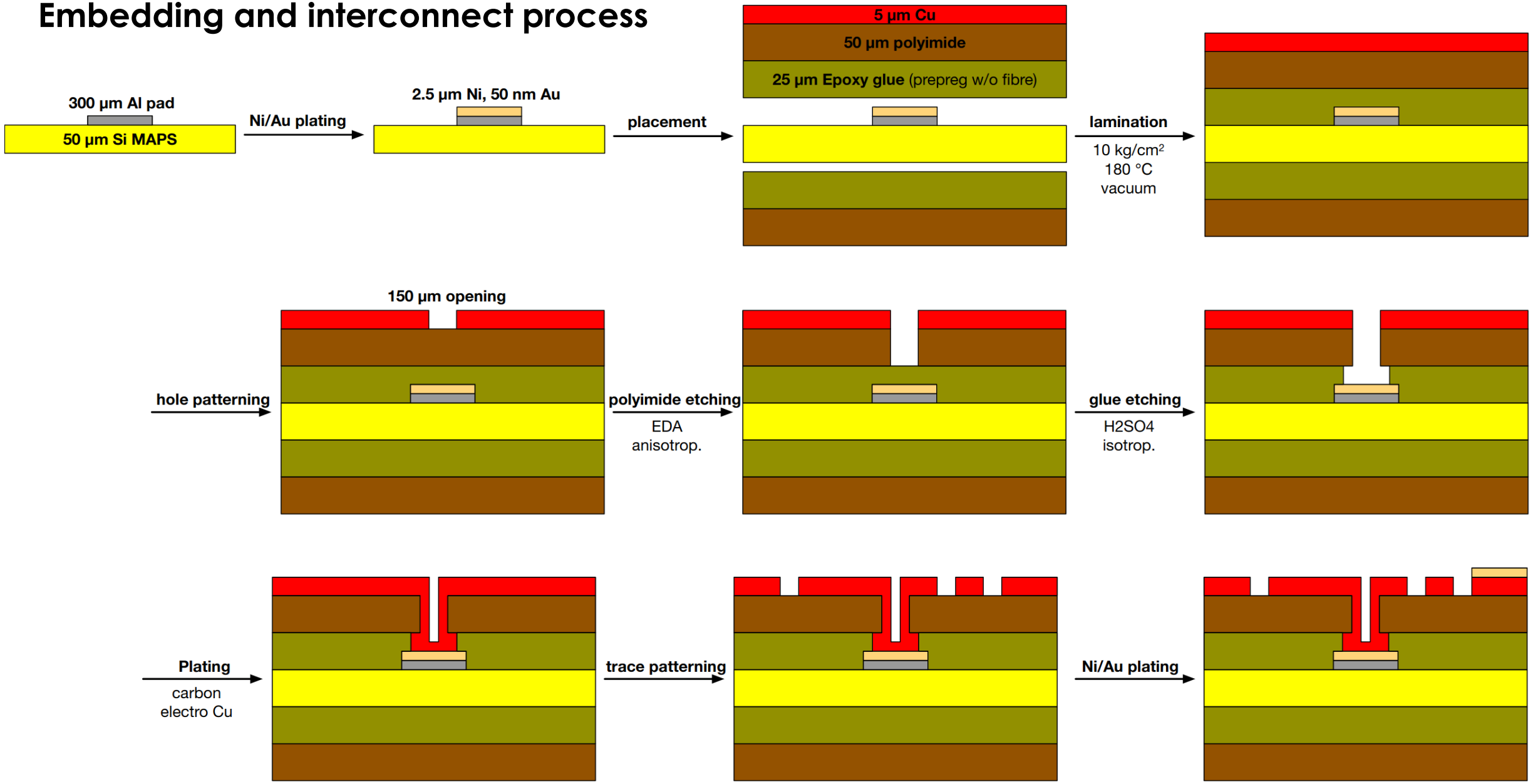
Flex embedded sensors, an old new concept

S. Beol´e, F. Carnesecchi, G. Contin, R. de Oliveira, A. di Mauro, S. Ferry, H. Hillemanns, A. Junique, A. Kluge and L. Lautner, et al. “**The MAPS foil**”

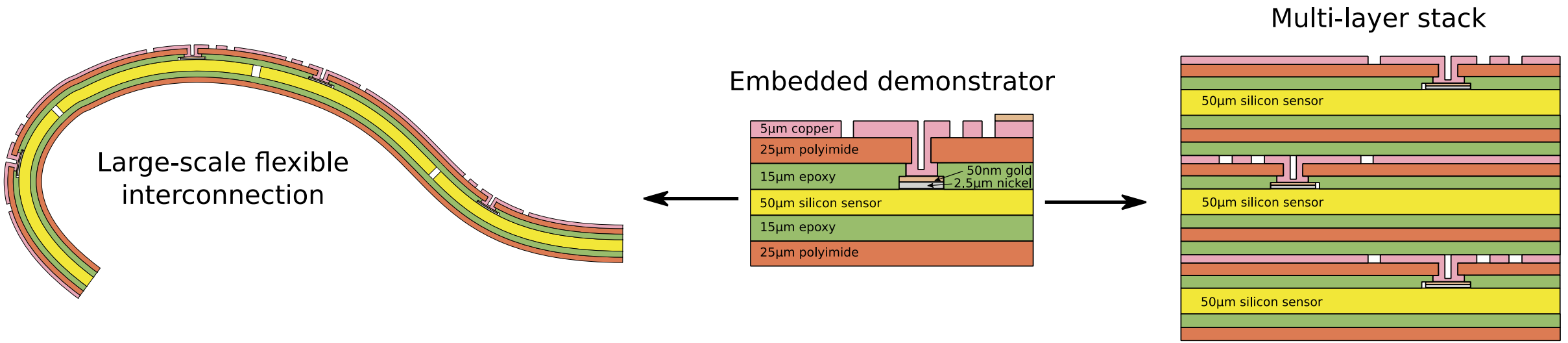


ALICE ITS3 mechanical bent prototype

Embedding and interconnect process



The stack



Equipment and facilities

Small scale lab press

- Few tons of applied pressure
- Few C precision in applied temperature
- Require a lot of modification from original model

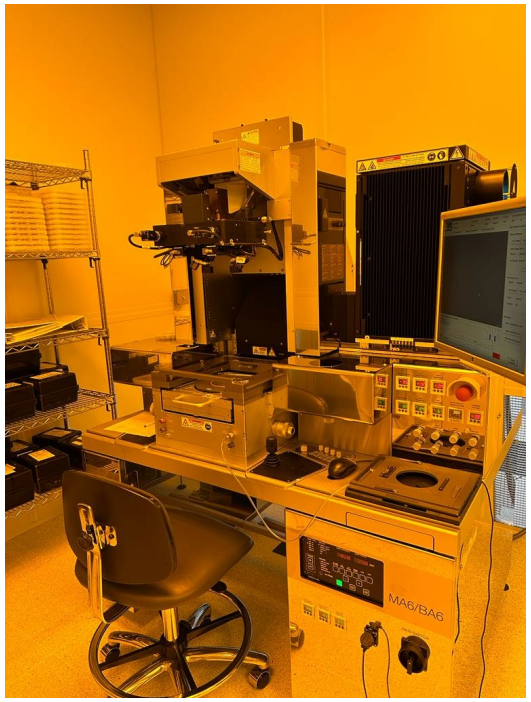
General purpose press

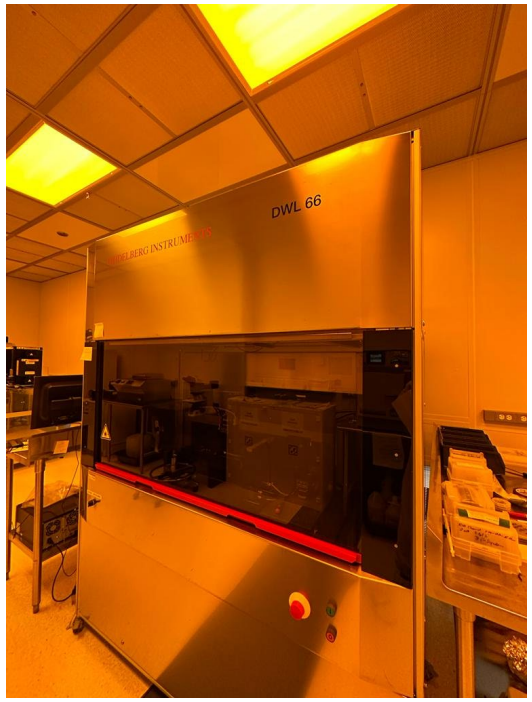
- 5 Ton max pressure
- 300 C temperature range
- Excellent passive planarity (sufficient for 4" wafer-to-wafer bonding)
- Clean room integration

"Fancy" fine placer

- 10g precision on force applied up to 200kg
- Very precise Temperature control
- +- 1µm post-bonding precision
- Excellent actively corrected planarity
- Can precisely dispense fluid
- 105x105mm working area

Equipment and facilities





Lithography and mask alignment

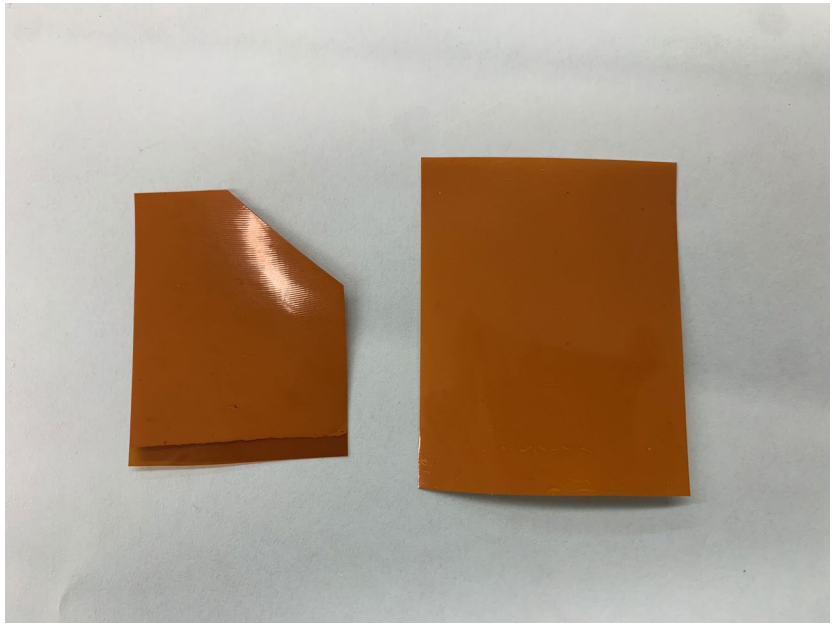
- Allow for development of metal traces, etch area on samples up to 4”

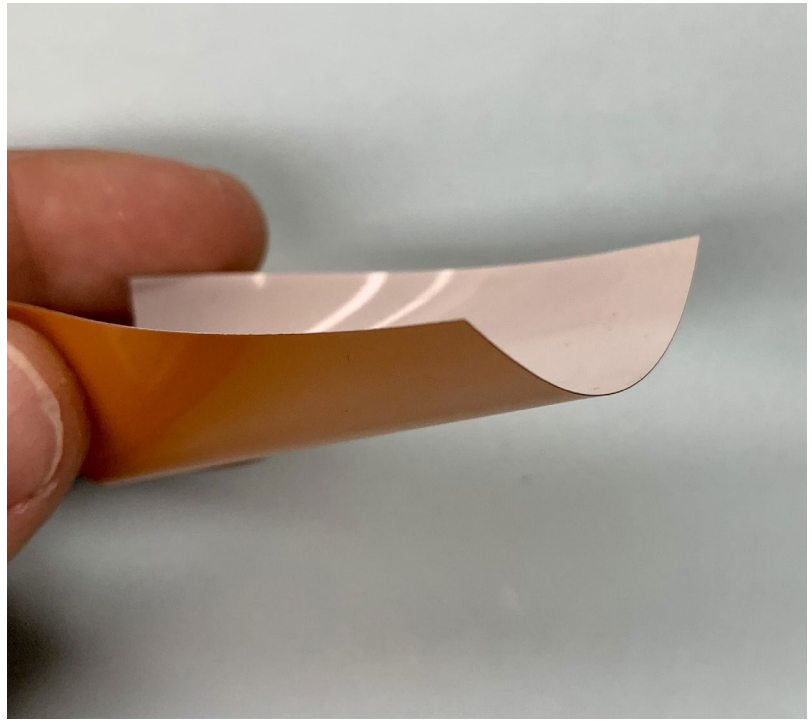
Sputtering, wet chemistry, etching

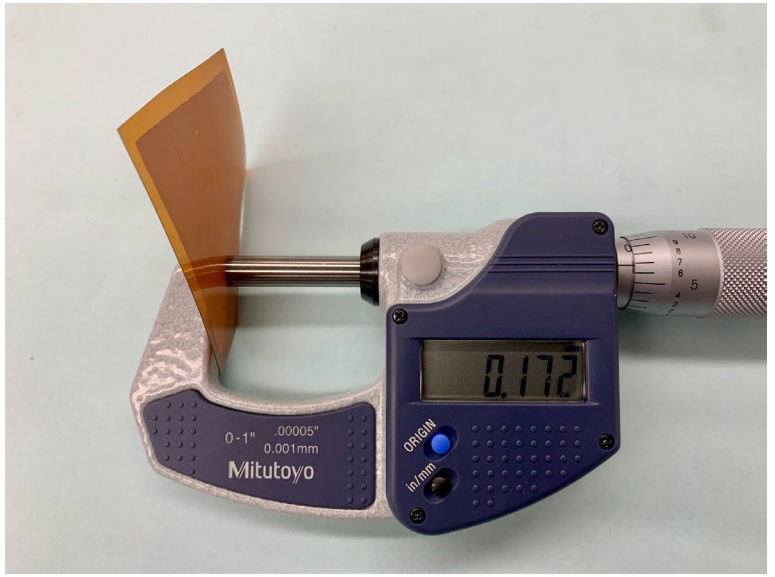
- Allows the metallization, etching and pattering of interconnect of our prototypes
- Ex: ENIG deposition on pads, etching of metals, Kapton and epoxy

ORNL Physics Division granted access to CNMS facilities

First trials





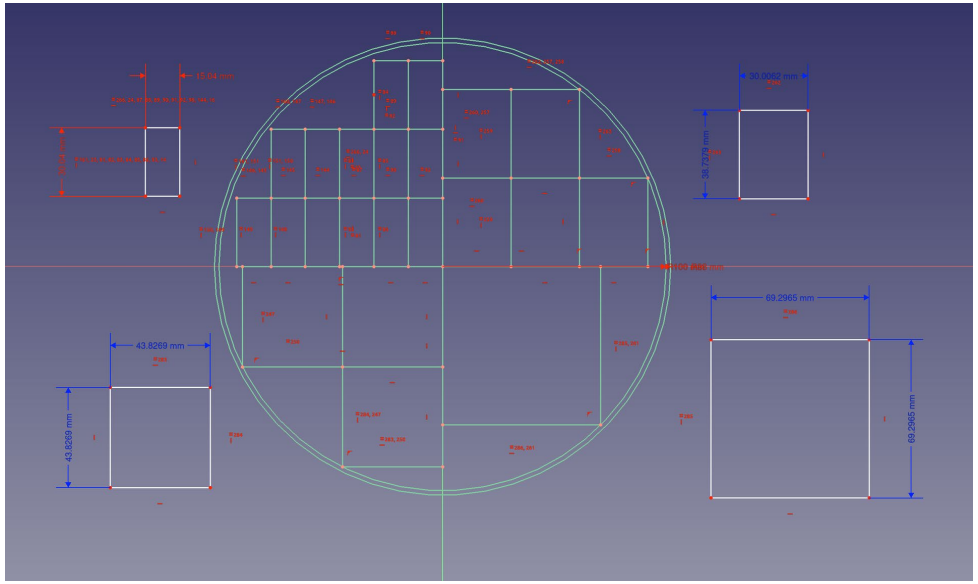


First baby steps with 50um Kapton and 25um Epoxy for now, sans silicon

- epoxy is DuPont Pyralux HP250000 for the 25um
- HP125000 for the 12.5um (yet to be tested)
- Very useful to optimize temperature ramping parameters, pressure and time required to obtain mechanically stable assemblies
- Next step to be performed on ~cm scale Silicon dummies

Mechanical and Electrical dummies

- We purchased thinned Silicon wafer to produce mechanical and electrical dummies for the optimization of the Kapton embedding process
  - Dicing performed in-house
- Next step will be the pattering of a metal layer to form pads and trace
  - Test thermal properties via heaters
  - Test interconnect yield via daisy-chained test structure



Next steps and challenges

- **Production of first mechanical and electrical prototypes**
  - Targeting few cm size samples
  - Mechanical samples to be used to optimized thermo-compression process
  - Electrical samples to be used to measure interconnect properties
- **Challenges**
  - Achievable large area, interconnect density and pitch
  - Mechanical stability, aging and long-term stability
  - Radiation, environment hardness
  - Achievable thermal and electrical properties
    - What signal speed can we handle
    - What power can we deliver and dissipate
  - Demonstrate functional bent detectors
  - Explore partnership with industry for Technology transfer, alternative bonding methods

Conclusion

- The embedding of ultra-thin silicon MAPS detectors in Kapton-Flex is being developed at ORNL for the purpose on making self-supported detector layers for ePIC SVT detector
  - Embedding provide low-cost support, interconnect and mechanical protection of the fragile thin MAPS detectors
  - Generic detector R&D : can easily be applied to any MAPS
- Lots of opportunities for a collaborative approach
  - Interested in testing various MAPS, providing samples to collaborators for characterization
  - Electrical design of Kapton flex for interconnection
  - Sharing of lessons learned, process steps, common technological transfer to institution and industry
  - Exploring various interconnect methods