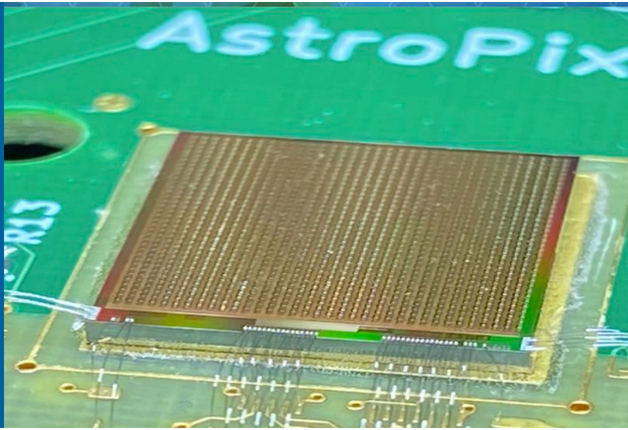
ASTROPIX: LOW POWER CMOS DETECTORS



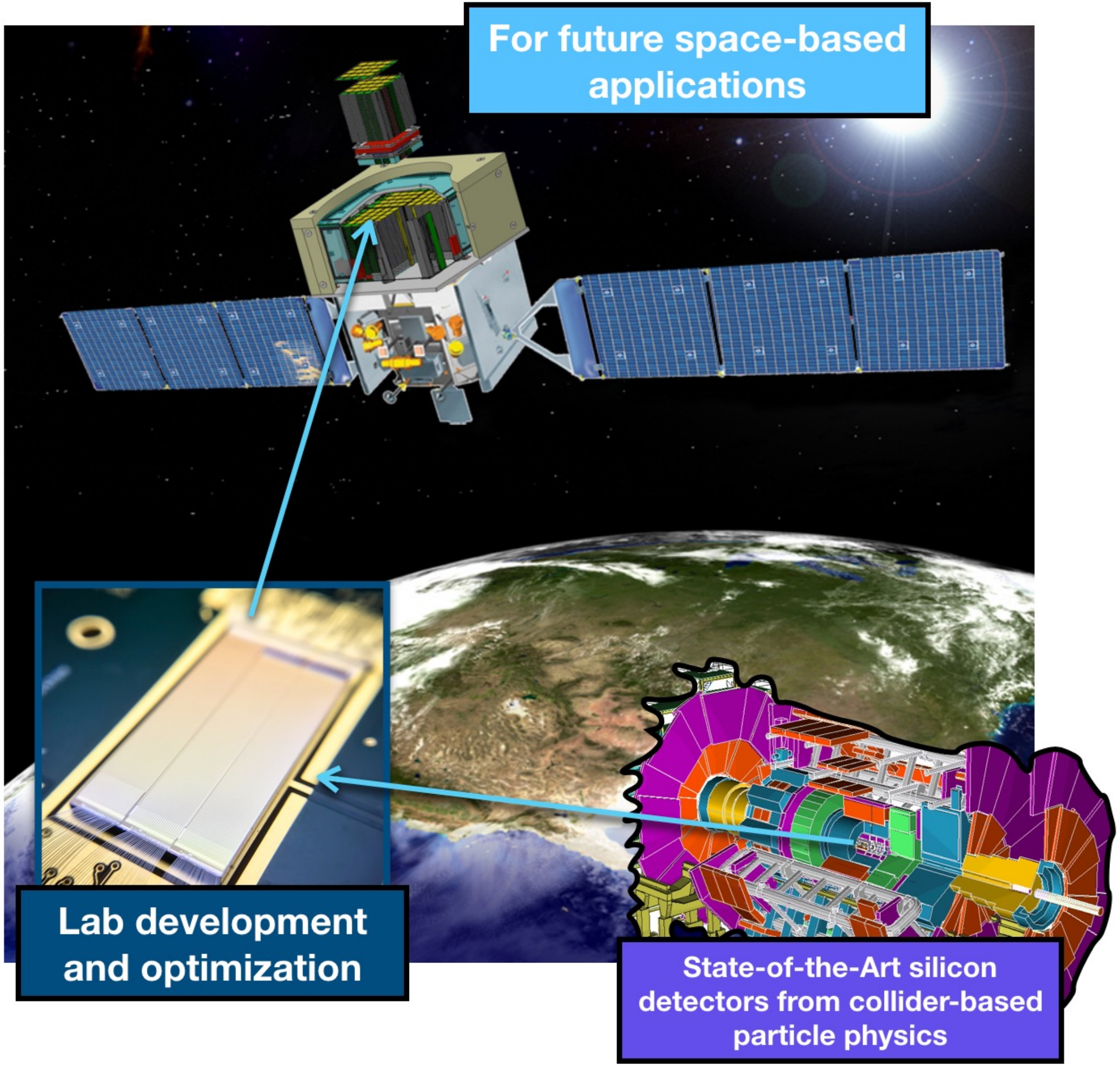
JESSICA METCALFE

November 8, 2023
CPAD, SLAC

ASTROPIX

AstroPix is a monolithic CMOS sensor developed for space-based applications

- Concept was to leverage the development work done by HEP
- Grew from the ATLASPix development
- NASA technology development project
- Several AstroPix development cycles to date



AMEGO-X

What is AMEGO-X?

- Gamma ray telescope
- ‘Next generation’ Fermi Telescope
- Target the MIDEX size instrument → ~$400M budget
- Expected proposal (similar to CD-2 phase) in 2026
- 4 towers, 40 layers each, 0.5 m x 0.5 m

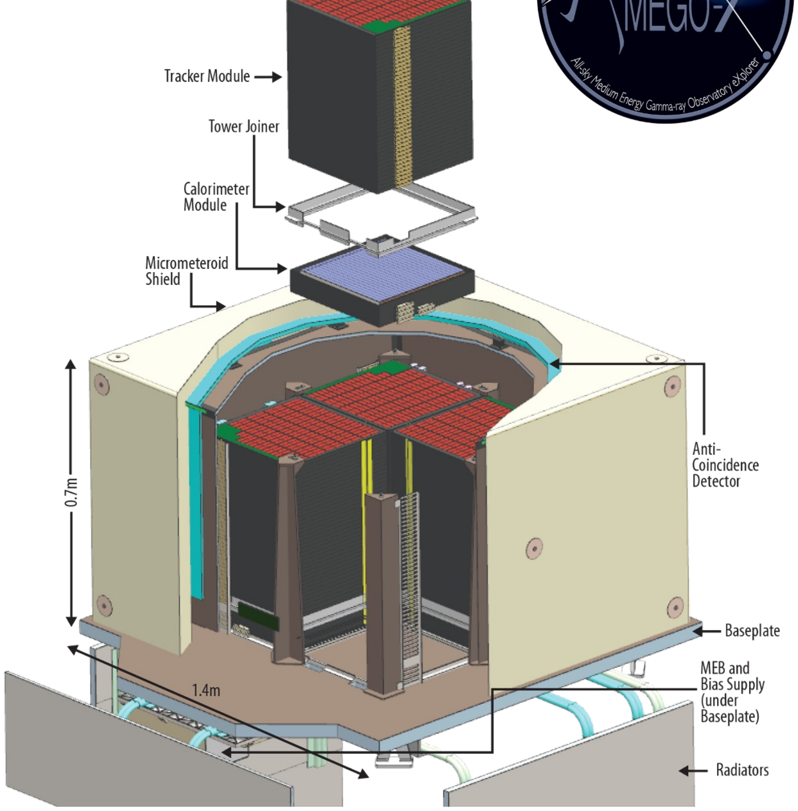


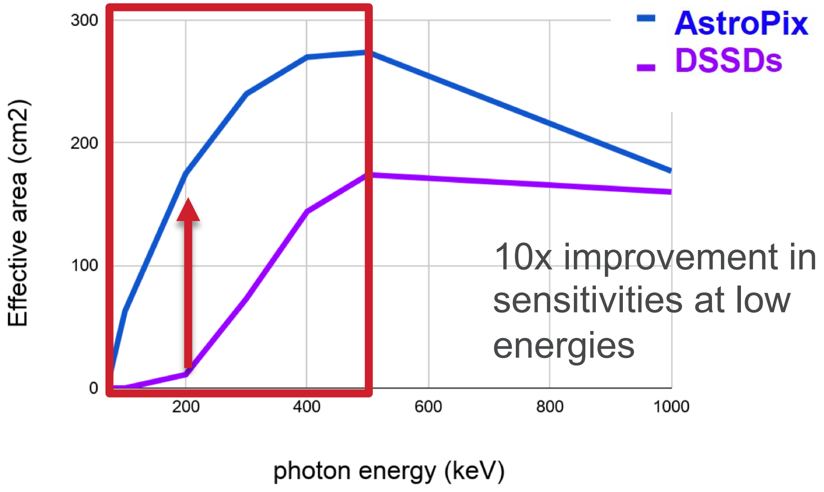
Table 1: The Gamma-Ray Telescope baseline capabilities.

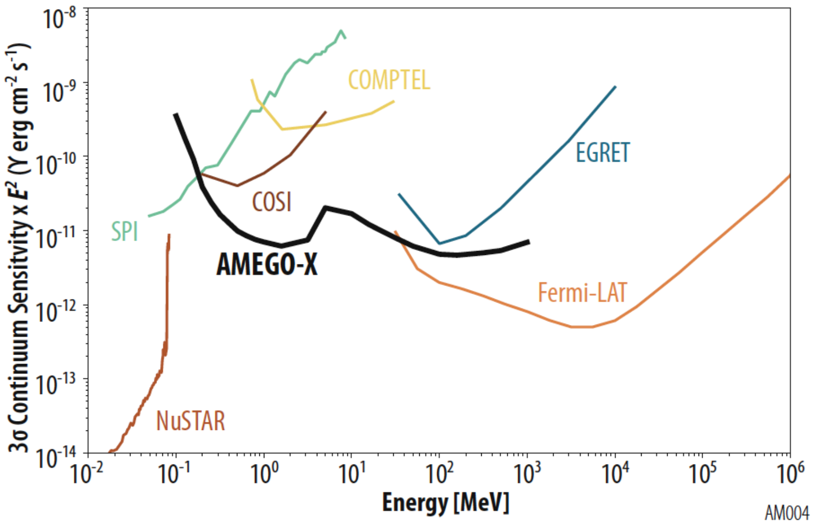
Parameter	
Energy Range	25 keV – 1 GeV
Energy Resolution	5% FWHM at 1 MeV, 17% (68% containment half width) at 100 MeV
Point Spread Function	4° FWHM at 1 MeV, 3° (68% containment) at 100 MeV
Localization Accuracy	transient: 1° (90% CL radius), persistent: 0.6° (90% CL radius)
Effective Area	1200 cm^2 at 100 keV, 500 cm^2 at 1 MeV, 400 cm^2 at 100 MeV
Field of View	2π sr (<10 MeV), 2.5 sr (>10 MeV)

R. Caputo *et al*, 2022

AMEGO-X PHYSICS

- Target MeV scale physics
  - Move to a lower energy regime to provide improved sensitivity
  - Provide better pointing resolution for **multi-messenger** physics
- AstroPix replaced double-sided strip detectors as the new baseline
  - Provides a pixelated readout
  - Lower energy threshold
  - Room temperature readout
  - Affordable





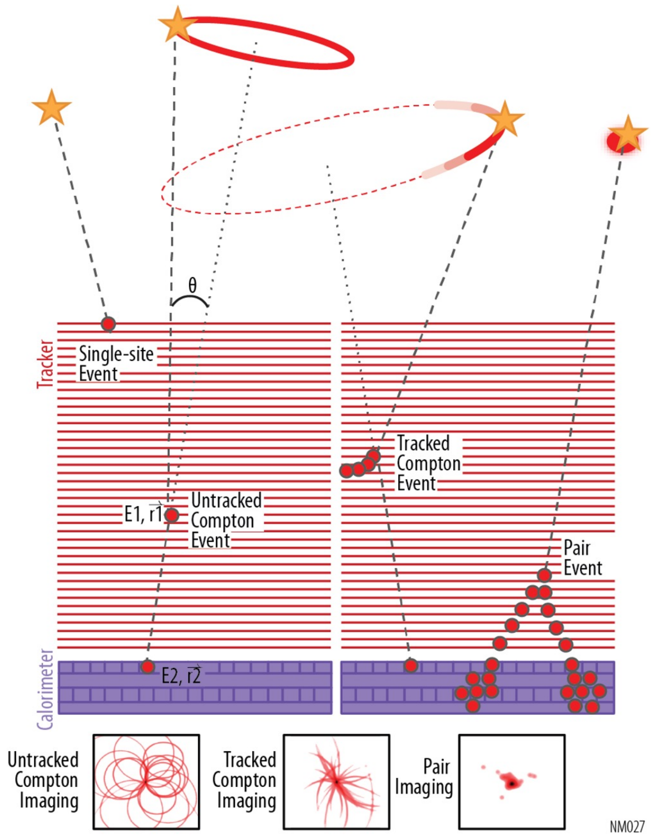
MEV INSTRUMENT CHALLENGES

Original AstroPix Design Goals:

Observe Compton scattering in the MeV range

- Low Power
  - limited by solar panels & payload
  - fewer/larger pixels, slower readout
- Energy Resolution:
  - aim for low energy gamma rays
  - thicker sensors
- Low Mass
  - Avoid photon conversions in dead material
- High Position Precision
  - Pixelated tracking

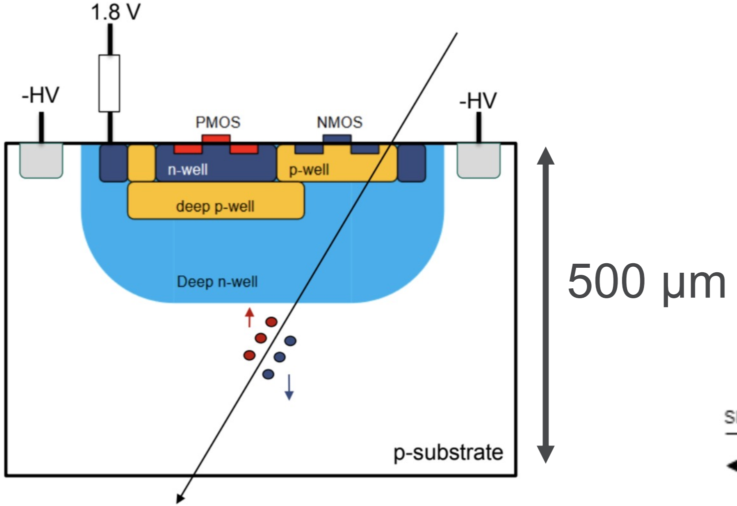
Parameter	**Goal**
$\mathbf{E}_{Res}$	<10% at 60 keV
Power Usage	$<1\ \mathrm{mW/cm^2}$
Passive Material	<5% on the active area of Si
Pixel Size	$500 \times 500\ \mu m^2$
Si Thickness	$500\ \mu m$
Time Tag	$\sim 1\ \mu s$

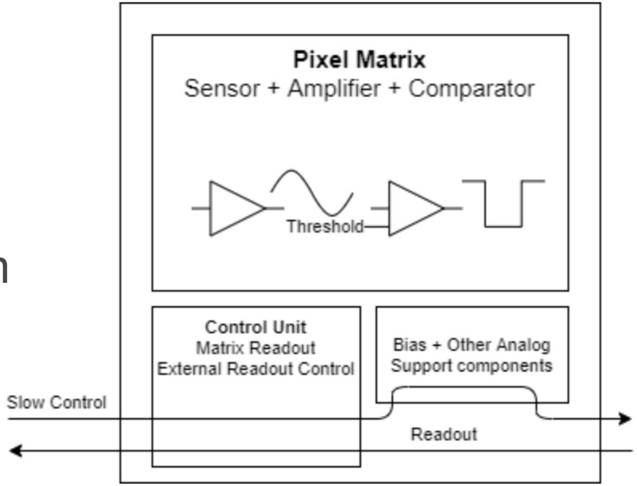


ASTROPIX: MONOLITHIC HVCMOS SENSOR

Current AstroPix Specs:

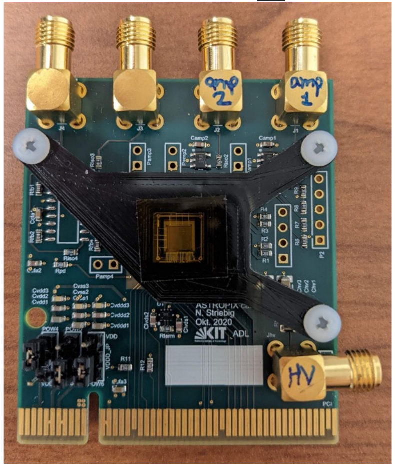
- 180 nm CMOS at TSI in California
  - Moving to AMS or other foundry
- 500 μm x 500 μm pixels;
- 700 μm thick
- Power consumption: ~1.5 mW/cm^2
- Energy resolution target (single sensor) 2% @ 600keV

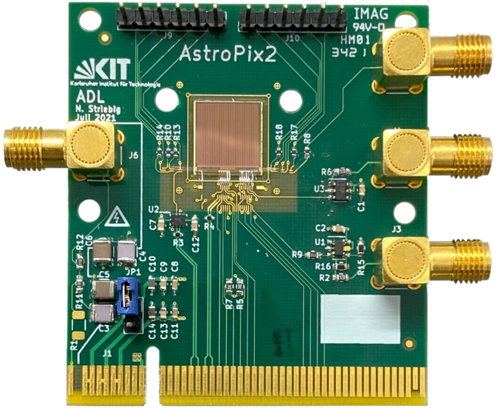




ASTROPIX DEVELOPMENT

ATLASPix	AstroPix_v1	AstroPix_v2	AstroPix_v3



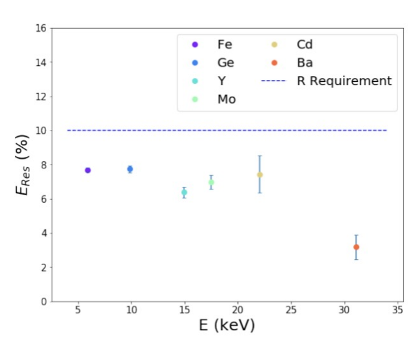


100 µm thick wafer	--720 µm thick wafer --		
40 x 130 μm^2 pitch	175 x 175 μm^2 pitch	250 x 250 μm^2 pitch	500 x 500 μm^2 pitch
0.3 x 1.6 cm^2 chip	0.5 x 0.5 cm^2 chip	1 x 1 cm^2 chip	2 x 2 cm^2 chip
150 mW/cm^2	14.7 mW/cm^2	3.4 mW/cm^2	1.06 mW/cm^2

(Power numbers represent amplifier+comparator only, not full digital power. Full v3 power draw = 4.12 mW/cm^2)

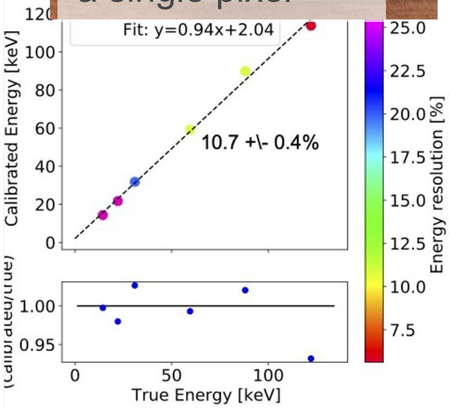
ASTROPIX DEVELOPMENT

ATLASPix



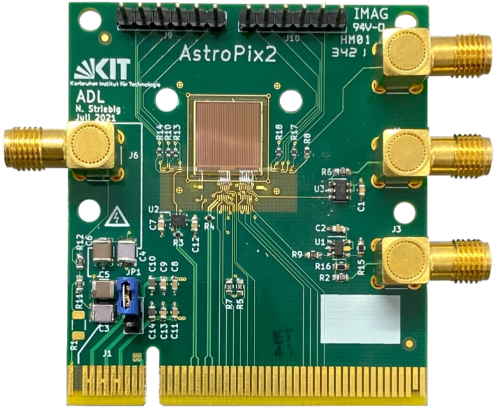
I. Brewer *et al*, 2021

AstroPix_v1

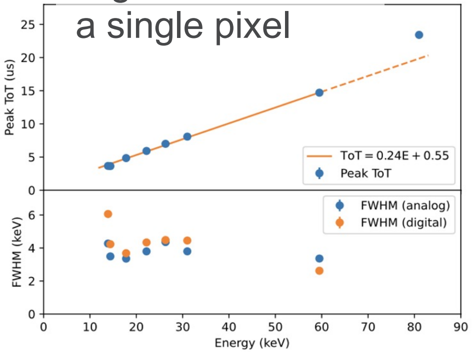


A. Steinhebel *et al*, 2022

AstroPix_v2

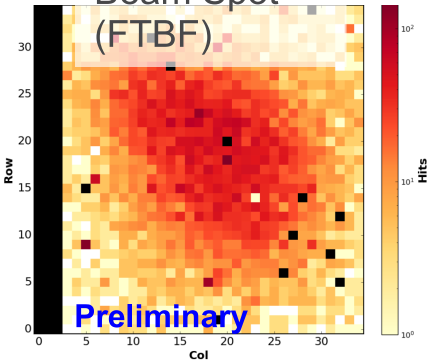


Digital data from
a single pixel



Y. Suda *et al*, 2023

AstroPix_v3



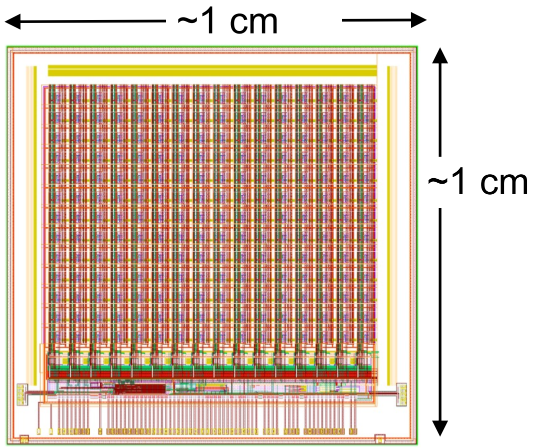
ASTROPIX: V4

AstroPix Features (v4):

- Potentially the final design in small size 1 cm x 1 cm
- 500 um pixel pitch
- Wafers recently delivered by foundry
- Previous versions needed to meet certain 'flyable' specifications like low power
- Implement more features for better performance

Features:

- Time stamp w/ 3.125 ns time resolution
- Row & Column from individual pixel hitbuffer
- Increase Time-Over-Threshold (ToT) bits
- Improve Threshold tuning (5-bit)
- Mask noisy pixels
- Pass hits to next chip (daisy chain)
- Self-triggered (only read out active hits)

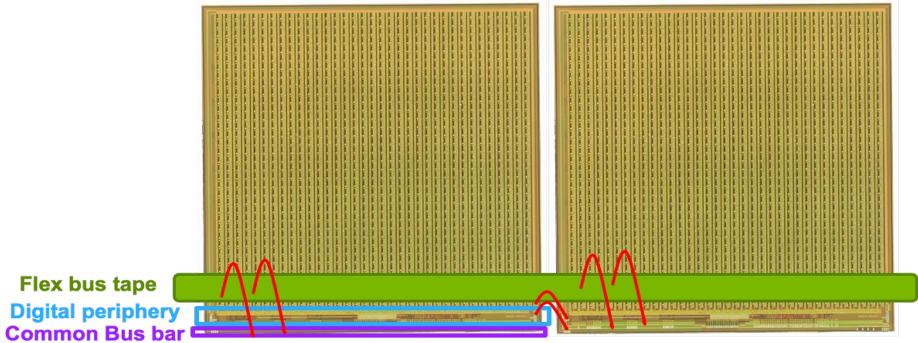


N. Striebig *et al*, in prep

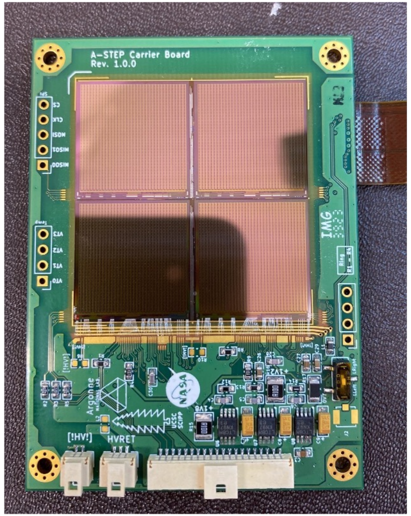
ASTROPIX: NEXT STEPS

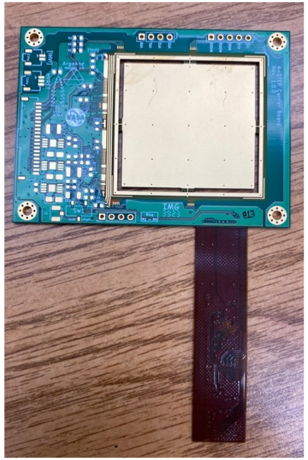
Several Features to Validate Performance:

- Daisy chain readout
  - Multi-chip module read-out board
  - Check for data loss/max occupancy
- Sensor efficiency between pixels, depth
  - Preparing for edge-TCT measurements
  - Charge collection efficiency
- Flex bus tape design
- DAQ development
- Update previous results with v4
  - Test Beam
  - Irradiation: SEU, LET, Total Dose

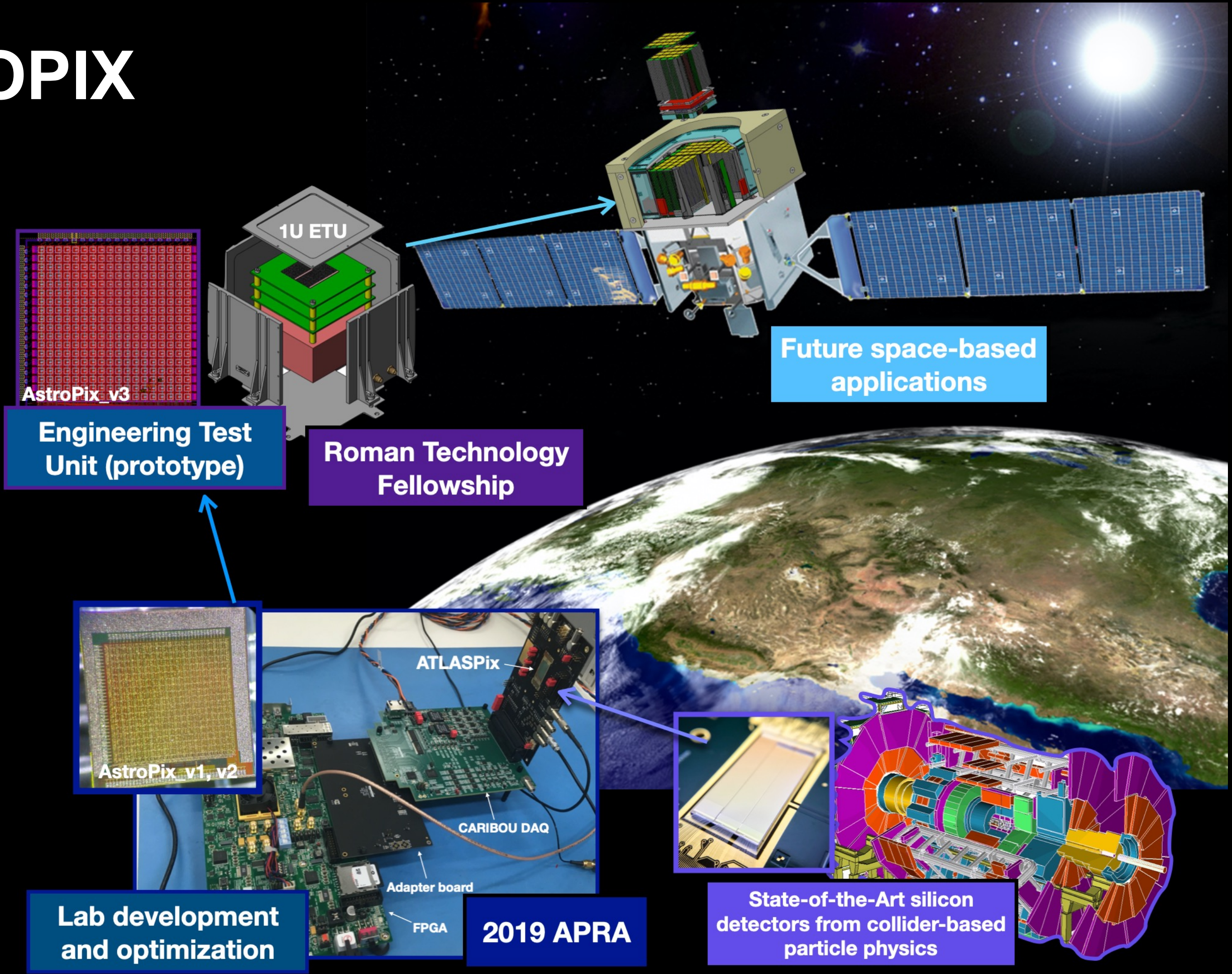


- Command/Power is distributed through a bus tape
- Wire bonded from bust tape
- Signals are digitized and routed out to the neighbor chip via wire bonds





ASTROPIX



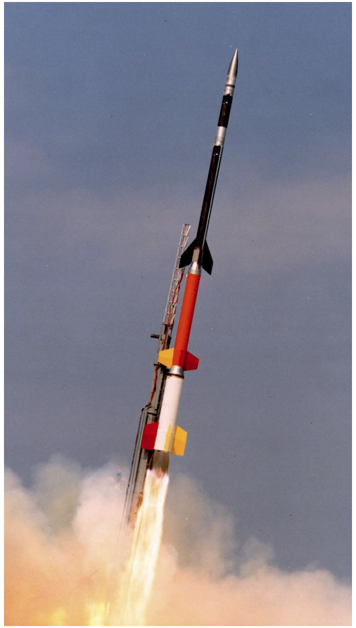
1U ETU
AstroPix_v3
Engineering Test Unit (prototype)
Roman Technology Fellowship
Future space-based applications
ATLASPix
AstroPix_v1, v2
CARIBOU DAQ
Adapter board
FPGA
Lab development and optimization
2019 APRA
State-of-the-Art silicon detectors from collider-based particle physics

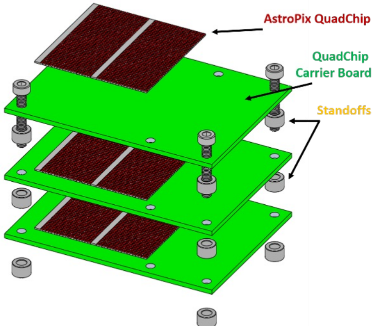
NASA LARGE-SCALE PROTOTYPES

A-STEP

Astropix Sounding rocket Technology dEmonstration Payload

- Sounding-rocket hosted flight of 3 v3 quad-chips
- Summer 2025





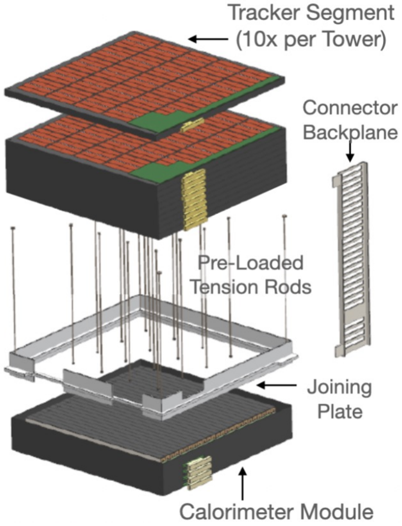
A. Steinhebel *et al*, 2023

D. Violette *et al*, in prep

ComPair 2

Compton-Pair telescope prototype

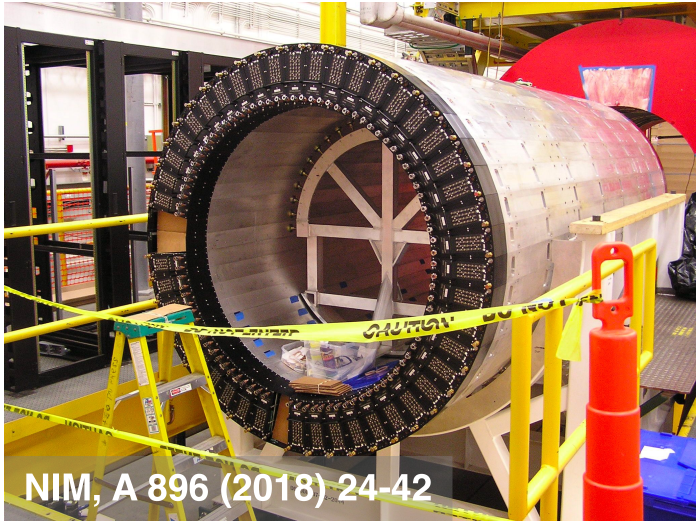
- High-altitude balloon hosted flight
- Prototype of AMEGO-X tower
- Instrument integration and gamma-ray beam test end of 2026



ASTROPIX

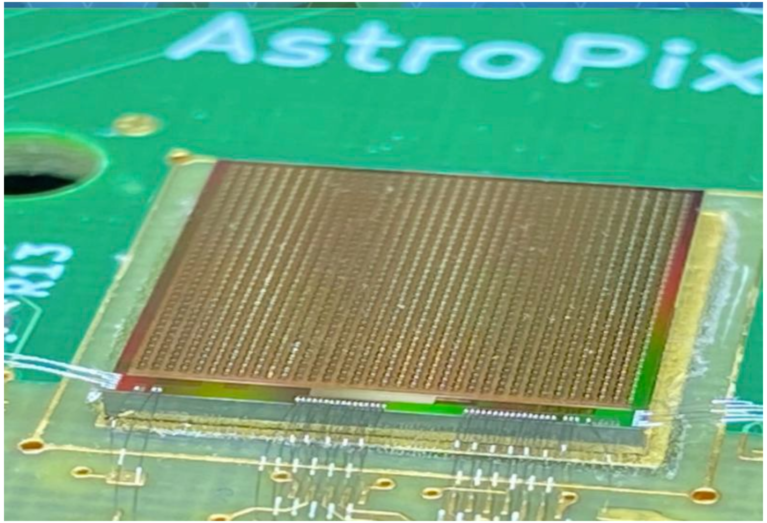
AMEGO-X
Future space-based applications
1U ETU
AstroPix_v3
Engineering Test Unit (prototype)
Roman Technology Fellowship
BIC@ePIC
AstroPix_v1, v2
ATLASPix
CARIBOU DAQ
Adapter board
FPGA
Lab development and optimization
2019 APRA
State-of-the-Art silicon detectors from collider-based particle physics

BARREL IMAGING CALORIMETER FOR EIC



GlueX Pb/SciFi sampling calorimeter

+



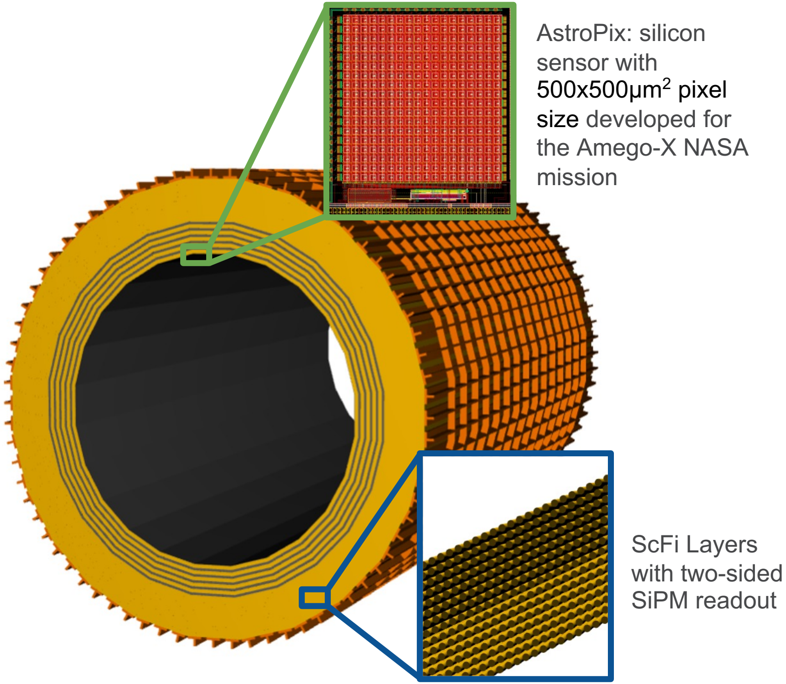
AstroPix tracking layers to capture 3D image of shower development

BIC

Addressing the unique challenges for the barrel region in ePIC

Hybrid concept: 6(4 now) layers of Astropix interleaved with the first 5 Pb/ScFi layers, followed by a large volume with the rest of the Pb/ScFi layers

- ✓ Deep calorimeter (21 X_0) but still very compact at ~ 40 cm
- ✓ Excellent energy resolution ($5.2\% / \sqrt{E} \oplus 1.0\%$)
- ✓ Unrivaled low-energy electron-pion separation by combining the energy measurement with shower imaging
- ✓ Unrivaled position resolution due to the silicon layers
- ✓ Deep enough to serve as inner HCal
- ✓ Very good low-energy performance
- ✓ Wealth of information enables new measurements, ideally suited for particle-flow
- ✓ Makes the tracking MPGD layer behind the DIRC unnecessary



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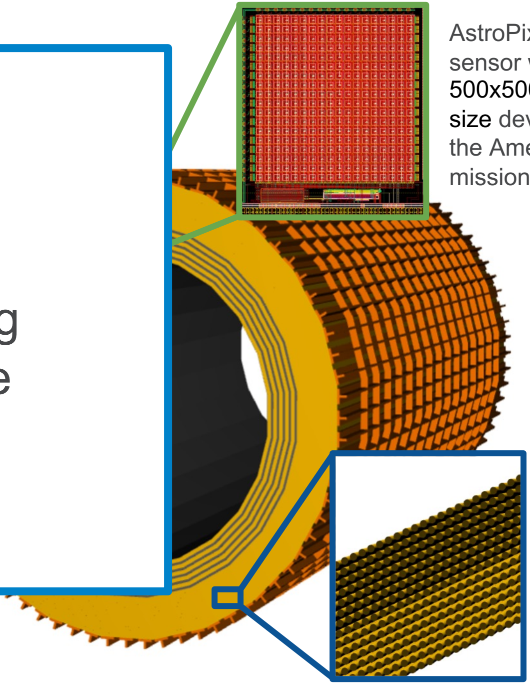
- ✓ Makes the tracking MPGD layer behind the DIRC unnecessary

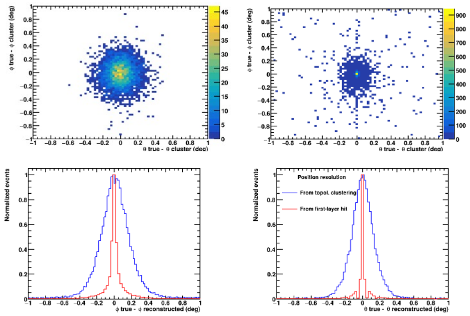
BIC Tracker

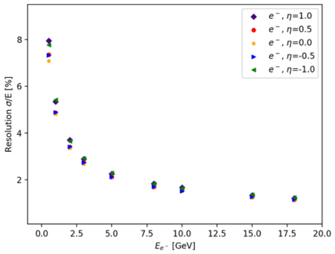
- ~100 m^2 of silicon
- ~5,000 wafers
- ~250,000 chips
- Optimize the design & building procedures for industrial scale production
  - 1 module flavor x31,200
  - 1 stave flavor x2,400

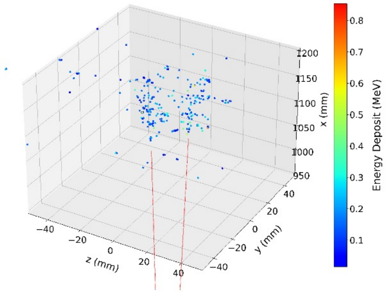


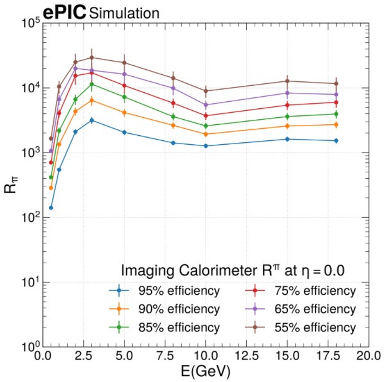
BIC PERFORMANCE

- Full simulation
- Implemented with AstroPix specs

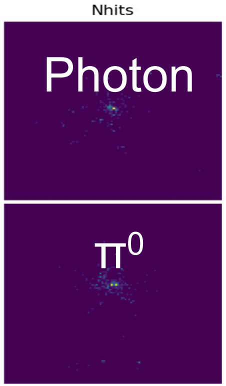


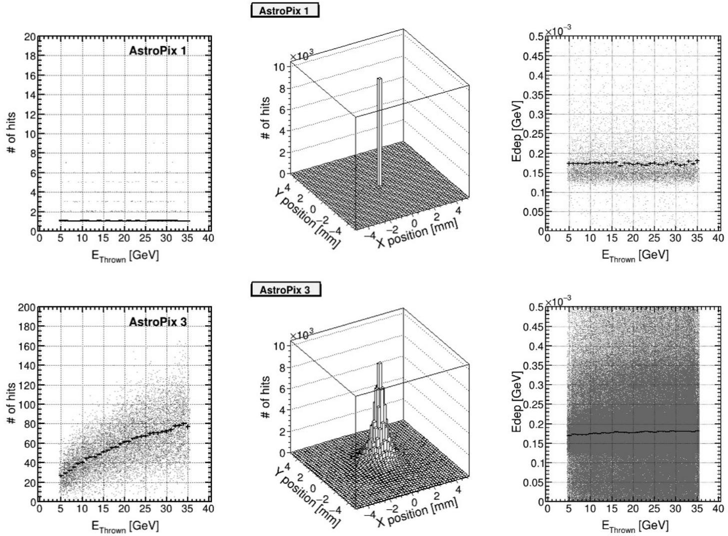






- 3D shower images
- Excellent electron/pion separation





SUMMARY

- AstroPix has its roots in HEP CMOS development
- Adapted for low mass → low inactive material detector design
- AstroPix design is relatively mature now
  - Expect v4 could be a final design
  - Full size chip fabrication run submission in about 1 year
- Work ongoing for large-scale proto-types
  - A-STEP rocket launch
  - COMPAIR-2 balloon launch
  - BIC Pb-SciFi + AstroPix segment prototype

Thank You

USA

- Argonne National Laboratory
- NASA Goddard Space Flight Center
- Oklahome State University
- University of Connecticut
- University of California Santa Cruz

Canada

- University of Manitoba
- University of Regina
- Mount Allison University
- NSERC
- Canada Fund for Innovation

Korea

- Kyungpook National University
- Yonsei University
- University of Seoul
- Pusan National University
- Korea University
- Sungkyunkwan University
- Hanyang University
- Gangneung-Wonju National University

Germany

- Karlsruhe Institute of Technology
- University of Giessen

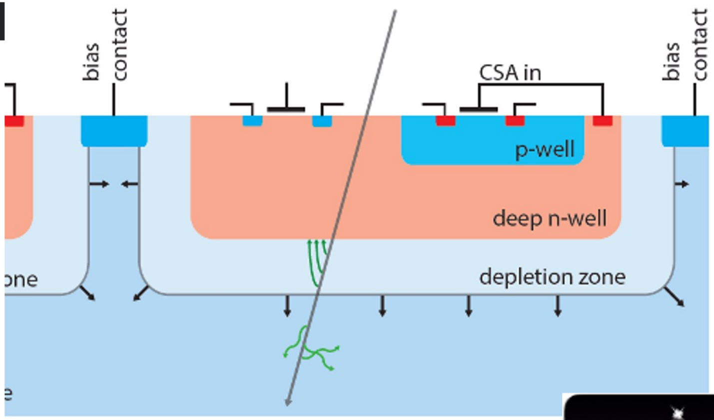
ePIC BIC Detector Subsystem Collaboration

AstroPix Collaboration:

- Hiroshima University
- Nagoya University

BACKUP

SENSORS: MONOLITHIC HVCMOS
(MONOLITHICS ACTIVE PIXEL SENSOR (M



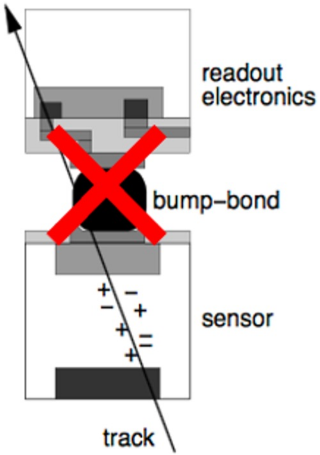
Monolithic: combines a traditional silicon pixel sensor wafer and the Front-End ASIC in a single wafer

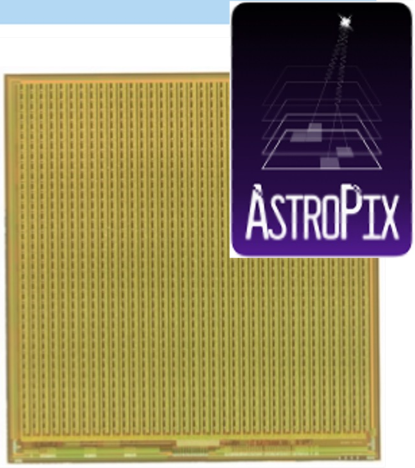
- Each pixel has it’s own amplifier in a deep n-well
- High-resistivity substrates enable sensor depletion for collection via drift rather than diffusion
- Technology uses more typical CMOS wafer processing for cost effective production
- Single wafer enables shorter design cycle

History: HVCMOS developed by Ivan Peric at Karlsruhe Institute of Technology (KIT). He has designed MuPix, ATLASPix, AstroPix, etc.

AstroPix: initially for space-based applications

- Upgrade to the next generation Fermi Telescope—AMEGO-X





ASTROPIX TIMELINE & PRODUCTION

AstroPix versions

- v1 early prototype
- v2 current test bench & test beam studies
    - extensive test bench characterization
    - higher noise due to larger pixel size
    - LET radiation testing
    - first test beam run a few weeks ago
- v3 full size chip
    - minor fixes from v2
    - OR’d rows & columns
    - just received
- v4 new features for better performance (MPW)
    - ‘final version’, but smaller chip (1 cm x 1 cm)
    - plan to submit in May 2023
    - better noise/threshold performance
    - per pixel hitbuffer
- v5 full size chip
    - fix any bugs from v4
    - Final production version
    - chips available November 2024

Design Validation

- test bench characterization complete
- LET irradiations done
- test beam measurements on-going
- multi-chip DAQ development
- daisy chain readout validation
- compare-1 NASA balloon test Fall 2023
    - DSSD’s
- A-STEP sounding rocket January 2025
- ComPair-2 balloon launch 2026

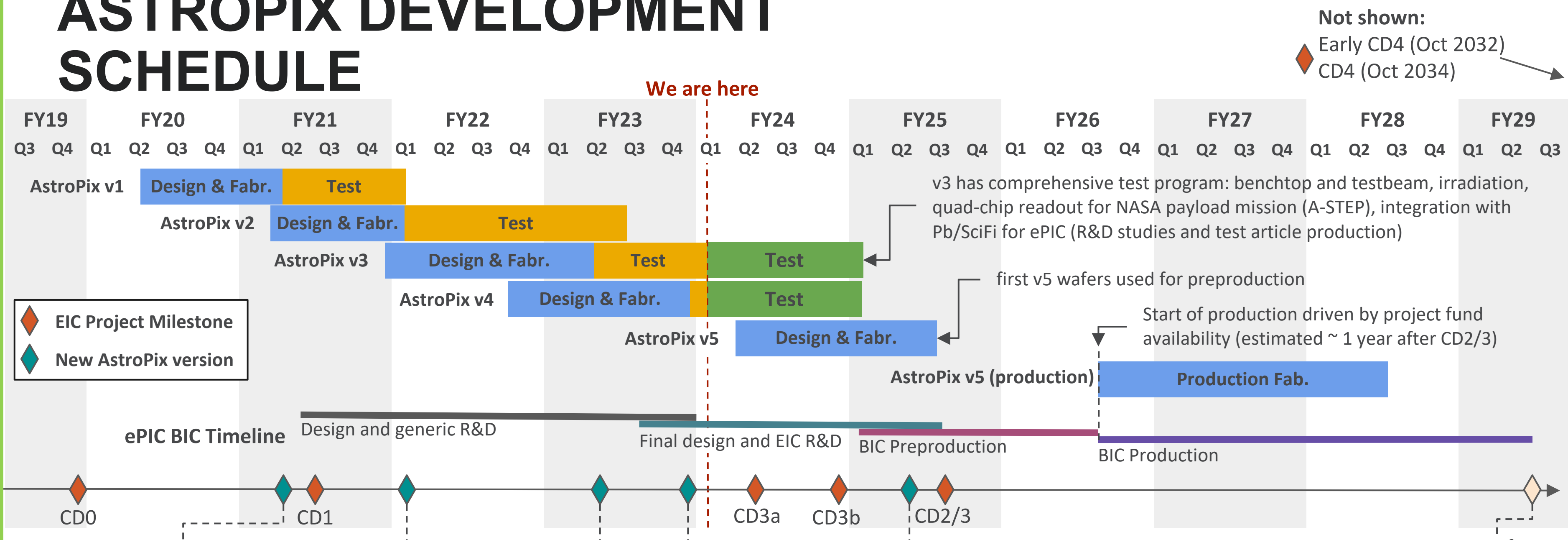
Multi-layer calorimeter prototype (ANL)

- full scale prototype to be built and tested w/ v3
- DAQ development joint with NASA

Production

- fabrication by TSI
    - AMS is a backup, but need a large order

ASTROPIX DEVELOPMENT SCHEDULE



AstroPix v1

HV-CMOS MAPS based on ATLASPix3, designed for the AMEGO-X NASA mission, optimized for power dissipation and energy resolution

Nucl.Instrum.Meth.A 1019 (2021) 165795

0.45 x 0.45 cm² chip, 175 µm pixel pitch
18 x 18 pixel matrix
Power dissipation 14.7 mW/cm²

AstroPix v2

1 x 1 cm² chip, 250 µm pixel pitch
35 x 35 pixel matrix
Row/column readout
Power dissipation 3.4 mW/cm²

AstroPix v3

First full-size chip

2 x 2 cm² chip, 500 µm pixel pitch
Row/column readout
Power dissipation <1 mW/cm²
2.5 MHz timestamp, 200 MHz ToT

AstroPix v4

Final design but smaller size

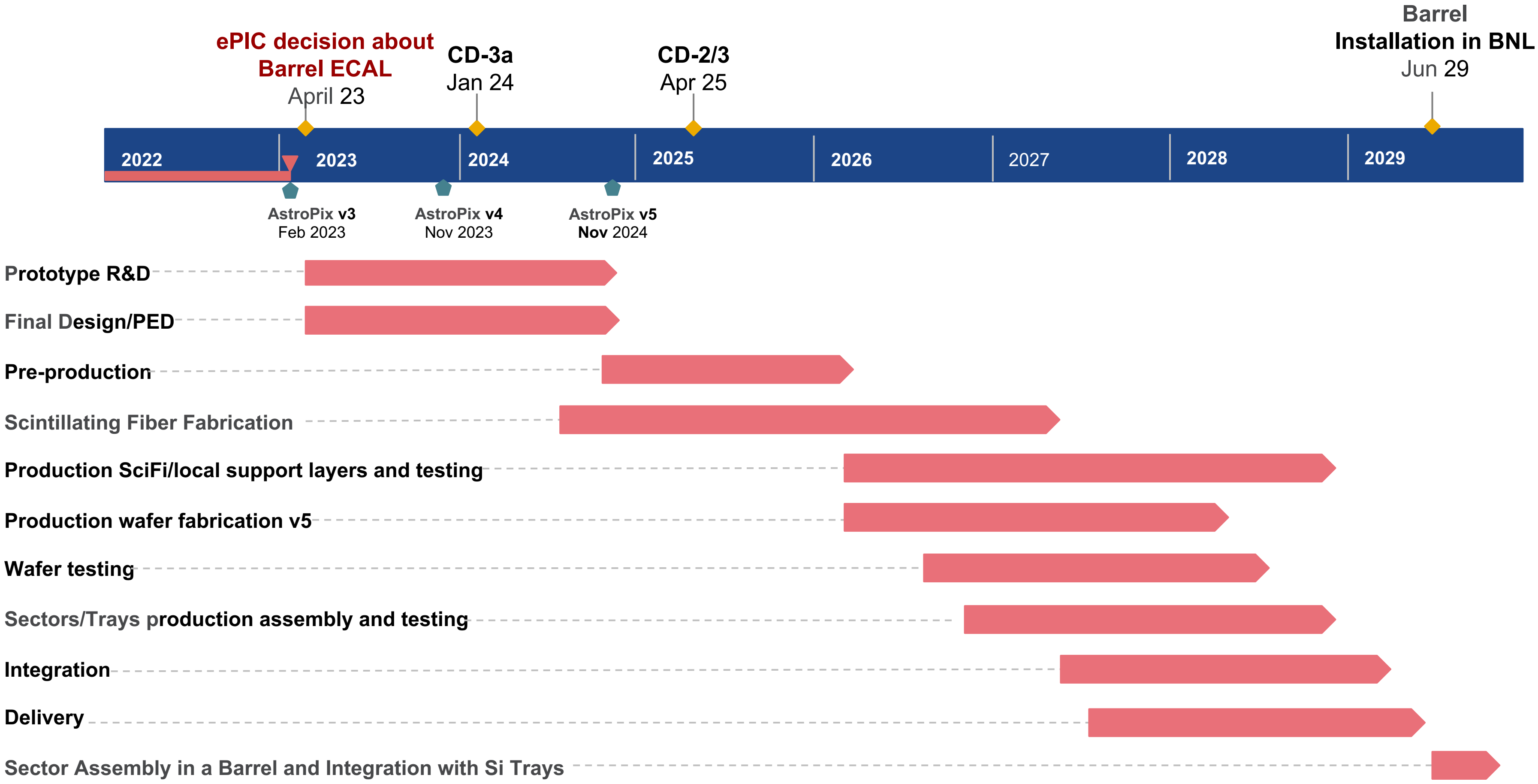
1 x 1 cm² chip, 500 µm pixel pitch
Individual pixel readout
3 timestamps, 3.25ns time resolution
TuneDAC for pixel-by-pixel thresholds

AstroPix v5

Full-size production chip

2 x 2 cm² chip, 500 µm pixel pitch
Design identical to v4 (with bug fixes)

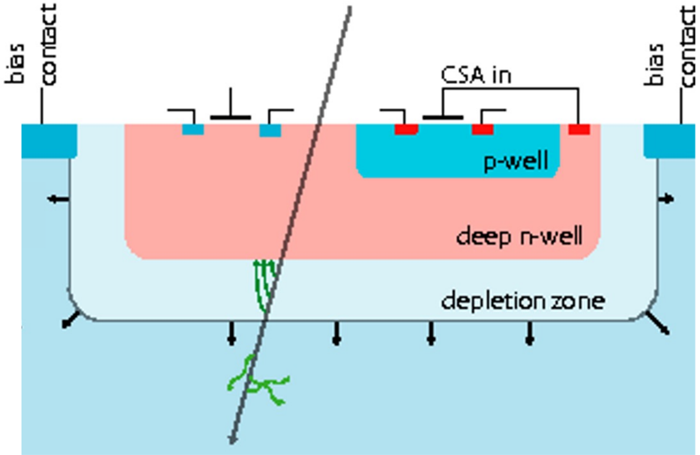
BIC HIGH-LEVEL SCHEDULE



AstroPix

HV-CMOS Monolithic Active Pixel Sensor (MAPS):

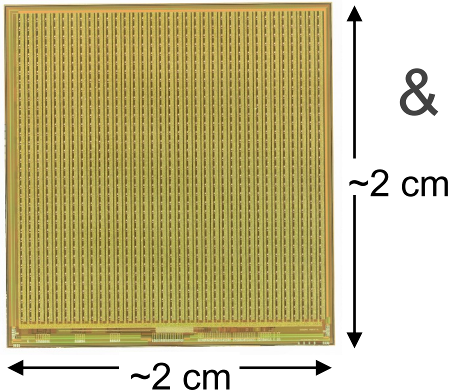
- Combination of silicon pixel & Front-End ASIC
- On-pixel charge amplification and digitization
- Technology uses more typical CMOS wafer processing for cost effective mass production
- Fabrication on single wafer enables shorter design cycle
- No need to bump-bond to each pixel - improves yield



AstroPix (based on **ATLASPix3** **arXiv:2109.13409**)

- 180nm HV-CMOS MAPS sensor
  designed at KIT (also designed ATLASPix, MuPix, etc.)
- Developed for AMEGO-X GSFC/NASA mission
  (Upgrade to the Fermi's LAT)
- Power consumption <1.5 mW/cm^2
- Energy resolution target of 2% @ 662keV

AstroPix v3 (Under test)



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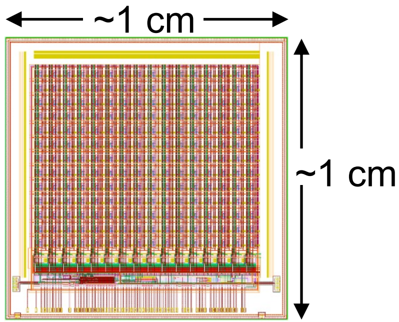


AstroPix v4
(MPW - delivered)

AstroPix Developments

AstroPix v1 - January 2021

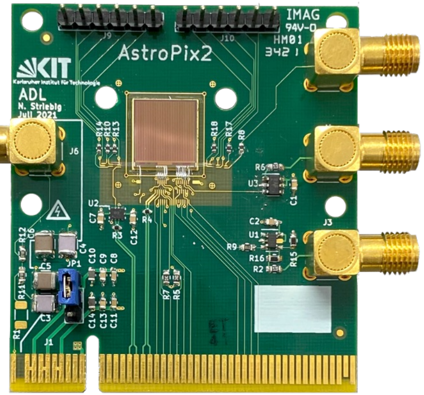
- 0.45 × 0.45 cm² chip, 175 µm pixel pitch
- 18 × 18 pixel matrix
- Power dissipation ~14.7 mW/cm²

AstroPix v2 - December 2021

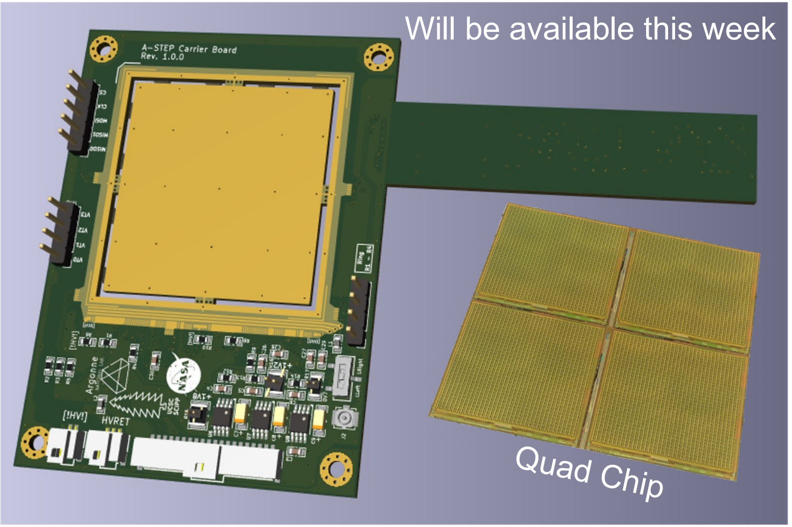
- 1 × 1 cm² chip with 250 µm pixel pitch
- 35 × 35 pixel matrix
- Hit identification with Row/Column readout
- Power dissipation ~3.4 mW/cm²

AstroPix v3 - February 2023

- 2 × 2 cm² chip with 500 µm pixel pitch
- Power dissipation <1 mW/cm² (targeted)
- Timestamp clock 2.5MHz, ToT 200 MHz
- 10 byte data frame per hit



AstroPix v2



AstroPix v3 Quad-chip Carrier Board

AstroPix v4/v5

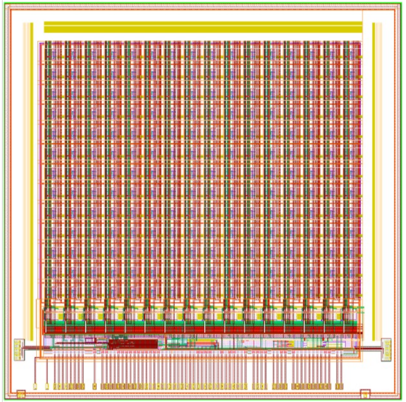
AstroPix v4 : Final design version will small size

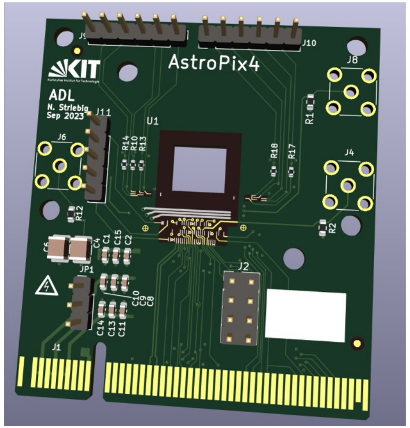
- Chip size 1 × 1 cm^2; Thickness 700 μm, V_{BD} ~ 400V
- Pixel pitch 500 μm with pixel size 300 μm, 16 × 16 pixel matrix
- Individual pixel readout with individual hit buffer
  - No identification issue due to ghost hits
- 3 Timestamps - 2.5MHz (TS), 20 MHz (Fine TS), and 16 bit Flash TDC
  - Fast ToT and Timestamp with 3.125 ns time resolution
- TuneDACs - Pixel-by-pixel threshold tuning and pixel masking
- Daisy Chain readout - pass hits to next chip through QSPI
- Self-triggered (reads out active hits)

AstroPix v5 : Full size final design

- No planned design changes
- Fix any bug from v4
- Full size chip - 2 × 2 cm^2, pixel pitch 500 μm,
- 35 × 35 pixel matrix → 1225 hit buffers

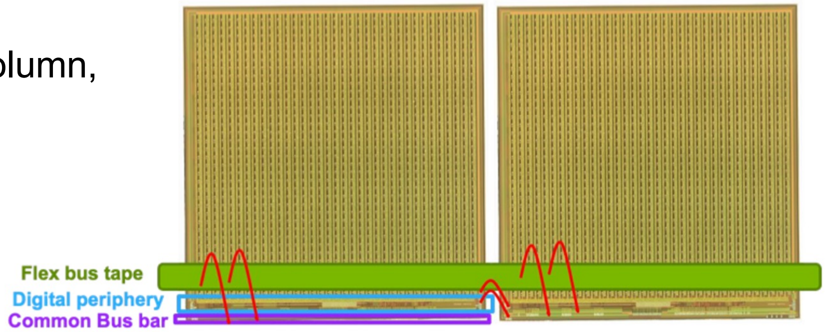
AstroPix v4

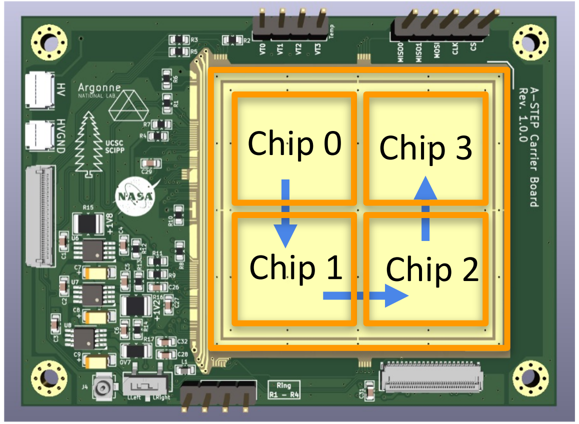




AstroPix Readout

- 8 bytes data per hit - header (chipID, payload), row/column, timestamp, ToT
- SPI I/O daisy chained - chip-to-chip signal transfer
  - signals are digitized & routed out to the neighboring chip using 5 SPI lines via wire bond
- Power/Logic I/O distribution on the module (through a bus tape)
  - 4 power lines (LV, HV), ~20 Logic I/O (SPI, clk, timestamp, interrupt, digital Injection, etc.)
  - HV, VDDA/VDDD(1.8V), VSSA(1.2V), Vminuspix(0.7V)
  - power distribution can be controlled using voltage regulators
  - mostly part of end of the stave services
- Data will be received by FPGA at the end of stave
  - FPGA aggregates data before sending off-detector
- Low heat load at chip, only cooling of end of the stave card
- Operational temperature for AstroPix is at room temperature and considered to be operated at 22 ℃





AstroPix v3 quad-chip carrier board
- Demonstrate required services
- Daisy chaining

AstroPix at ePIC

Low Rates

- The expected hit rate for **all imaging layers together** is well below < 3×10^7 Hz
- This translates to a maximum hit rate per tracker stave (1 x 104 chips) < 36 kHz

Zero-suppression below threshold 20 keV (4 × noise floor) well suited for EIC electromagnetic showers

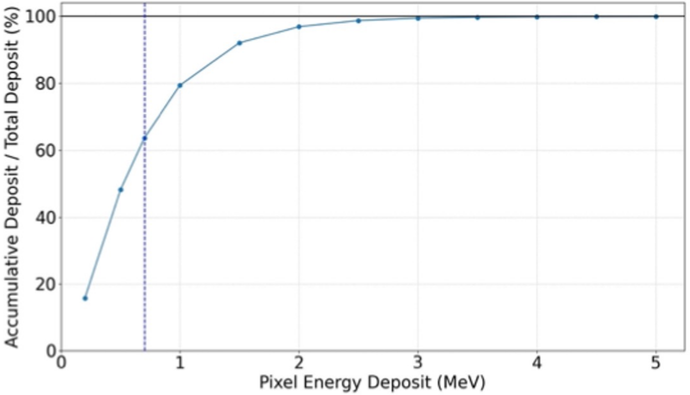
Timing requirement: 3.125 ns (v4/v5) - **driven by 10 ns bunch crossing**

Low Ionization radiation dose and neutron flux

- The maximum **ionizing radiation dose < 1 kRad/year** for the barrel region
- Max neutron flux - order of **10^9 $n_{equivalent}$/cm^2 per year**

Dynamic range (see plot for 2 GeV e^-)

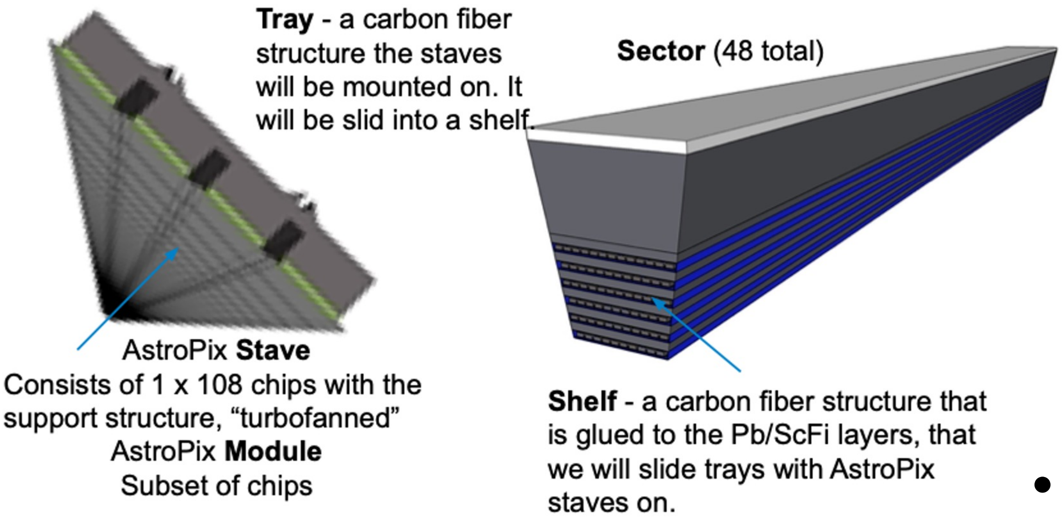
~ 3 MeV



Accumulative energy deposit to the total energy deposit for 2 GeV electrons.

- About 63% of the energy deposit was made through hits with deposit < 700 keV
- hits with deposit < 3 MeV contribute to 99% of the total energy deposit

AstroPix Assembly



*The designs presented on these slides are not final but for illustration only

Module Strategy

- QC testing with wafer probing + Module and stave level QC testing and tuning
- “Baseline” model of Modules on Stave
  - Module - 8 single chips
  - Stave - 13 Modules - 104 chips
  - 12 or 14 Staves per AstroPix layer per Calorimeter Sector
  - Total 249600 chips
- All staves are identical and gets combined in a separate production step
- Data transmitted to end of the Stave card using flex base tape
- Institutions - ANL, GSFC/NASA, KIT ,UCSC, Korea, Oklahoma State

AstroPix Timeline and Production

v3 full size chip (ongoing testing)

- Test bench characterization (ongoing)
- Testbeam performance studies
- Active and passive irradiation **~10^{15} $n_{equivalent}$/cm^2**
- **Quad-chip readout (ready to test)** for NASA's hosted payload mission (A-Step) - **January 2025**
- Integration with Pb/SciFi - FY2024

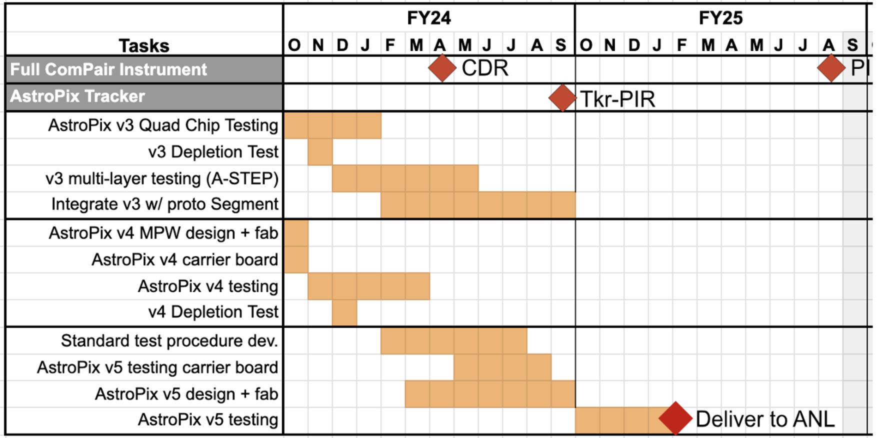
v4 new features for better performance (MWP)

- **Final design version**, smaller chip (1cm × 1cm)
- Fabricated wafers **delivered last week**
- Chip carrier board design for bench test is ready for the PCB fabrication

v5 full size final chip

- Fix any bugs from v4
- v5 chips available **November 2024**

GSFC/NASA ComPair-2 AstroPix timeline



BIC@ePIC Timeline

- **Prototype R&D** (v3) Ongoing - till Nov 24
- Pre-Production (v5) chips starts **Nov 2024**

Production

- Fabrication by TSI - with a large production order, AMS is a backup