MAPS R&D for tracking and calorimetry at future e+e- colliders

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SLAC NATIONAL ACCELERATOR LABORATORY

Stanford University | U.S. DEPARTMENT OF ENERGY

Higgs physics as a driver for future detectors R&D

The goal of measuring Higgs properties with sub-% precision translates into ambitious requirements for detectors at e+e-

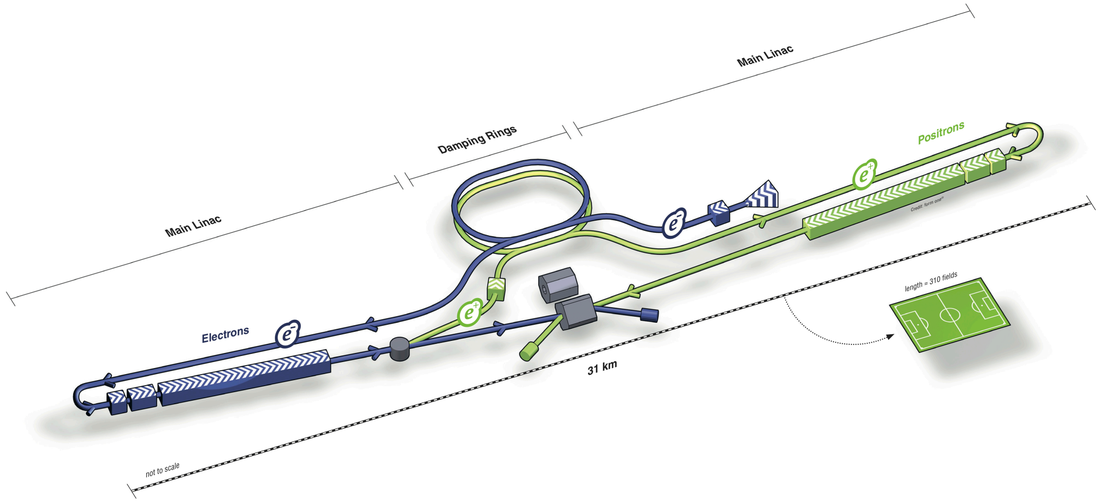
- Advancing HEP detectors to new regimes of sensitivity
- Building next-generation HEP detectors with novel materials & advanced techniques

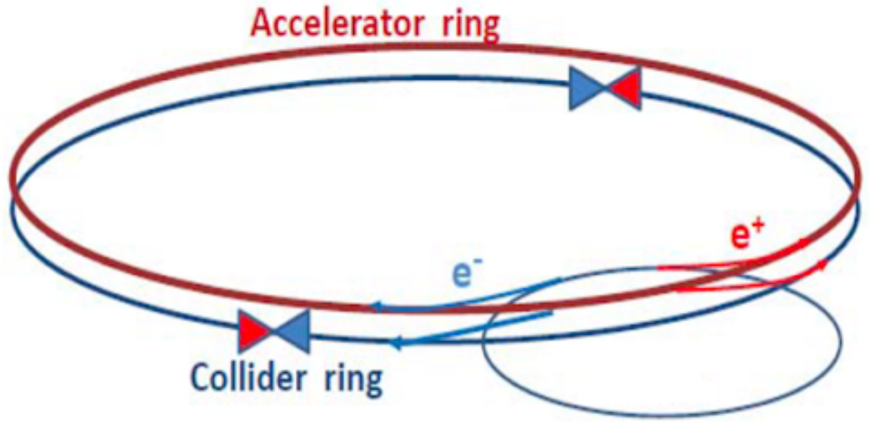
Initial state	Physics goal	Detector	Requirement
e^+e^-	hZZ sub-%	Tracker	σ_{p_T}/p_T=0.2% for $p_T < 100$ GeV $\sigma_{p_T}/p_T^2 = 2 \cdot 10^{-5}/$ GeV for $p_T > 100$ GeV
		Calorimeter	4% particle flow jet resolution EM cells 0.5×0.5 cm^2, HAD cells 1×1 cm^2 EM $\sigma_E/E = 10\%/\sqrt{E} \oplus 1\%$ shower timing resolution 10 ps
	$hb\bar{b}/hc\bar{c}$	Tracker	$\sigma_{r\phi} = 5 \oplus 15(p \sin\theta^{\frac{3}{2}})^{-1} \mu$m 5$\mu$m single hit resolution

Arxiv:2209.14111 Arxiv:2211.11084 DOE Basic Research Needs Study on Instrumentation

Linear & Circular e^+e^-

- **Linear** e^+e^- colliders
  - Reach **higher energies** (~ TeV)
  - Can use **polarized** beams
  - Relatively low radiation
  - Collisions in bunch trains
    - Power pulsing → Significant power saving for detectors
- **Circular** e^+e^- colliders
  - **Highest luminosity** collider at Z/WW/Zh
    - limited by synchrotron radiation above 350– 400 GeV
  - Beam continues to circulate after collision
    - No power pulsing, detectors need active cooling → more material
    - Limits magnetic field in detectors to 2T





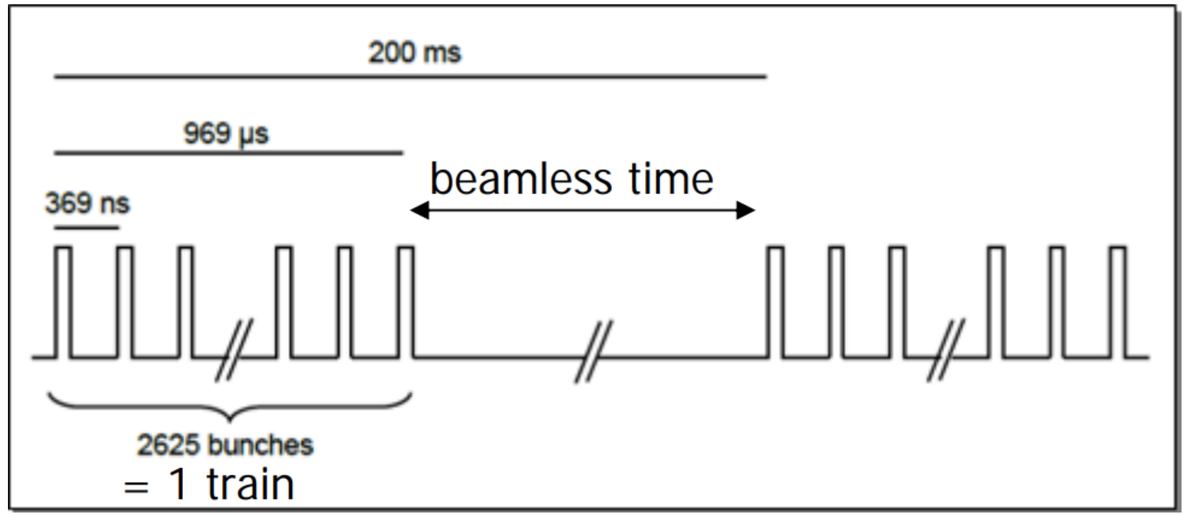
Future e+e- Colliders

Joint simulation/detector optimization effort with ILC groups Common US R&D initiative for future Higgs Factories 2306.13567

Main Candidates, either linear C³/ILC/CLIC or circular FCC/CEPC

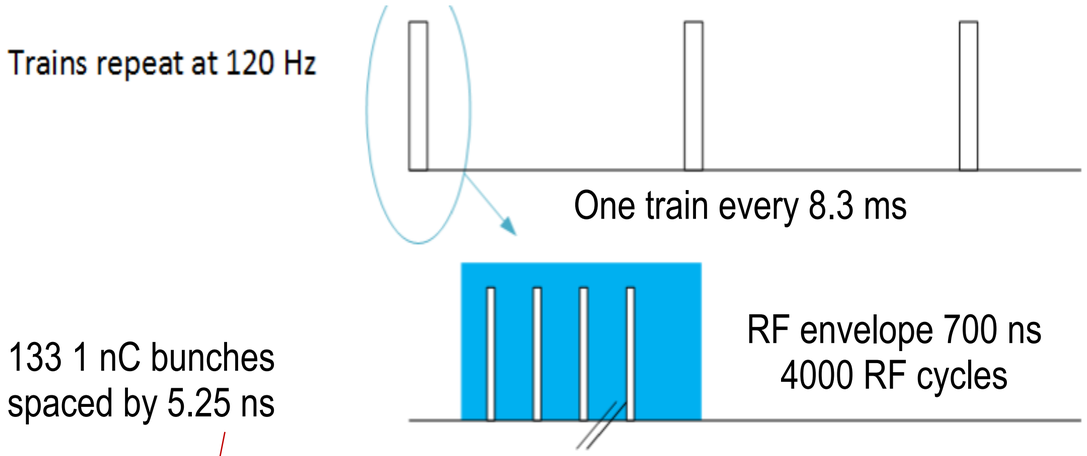
- Linear e+e- colliders are characterized by a very low duty cycle
- Power Pulsing can be an additional handle to reduce power consumption and cooling constraint
  - Factor of 100 power saving for FE analog power
- Tracking detectors don't need active cooling
  - Significantly reduction for the material budget

ILC Timing Structure



Duty Cycle = 0.48%

C³ Timing Structure



Duty Cycle = 0.03 %

~1 ns time resolution is needed

arXiv:2003.01116

Physics requirements for detectors

Precision challenges detectors

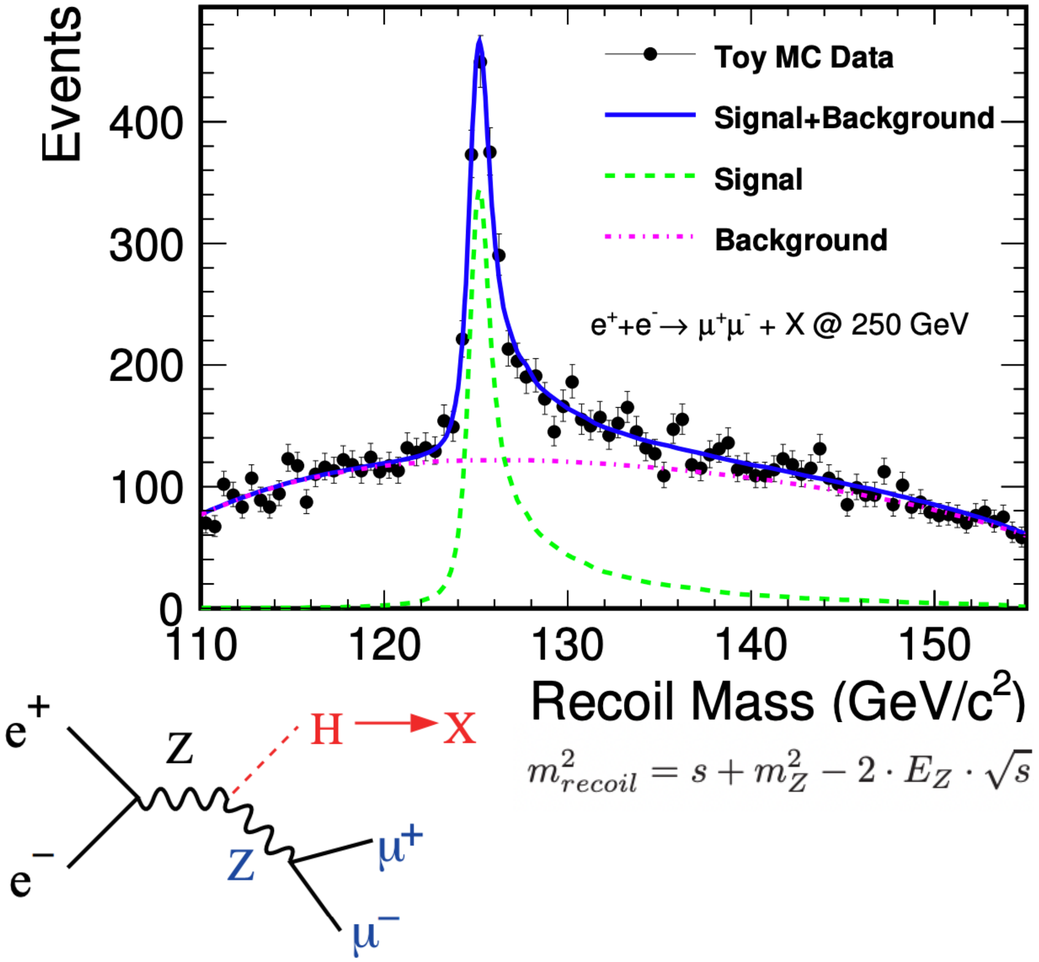
ZH process: Higgs recoil reconstructed from Z →*μμ*

- Drives requirement on charged track momentum and jet resolutions
- Sets need for high field magnets and high precision / low mass trackers

Particle Flow reconstruction

Higgs → bb/cc decays: Flavor tagging & quark charge tagging at unprecedented level

- Drives requirement on charged track impact parameter resolution → low mass trackers near IP
- <0.3% X0 per layer (ideally 0.1% X0) for vertex detector
- Sensors will have to be less than 75 *μ*m thick with at least 5 *μ*m hit resolution (17-25*μ*m pitch)



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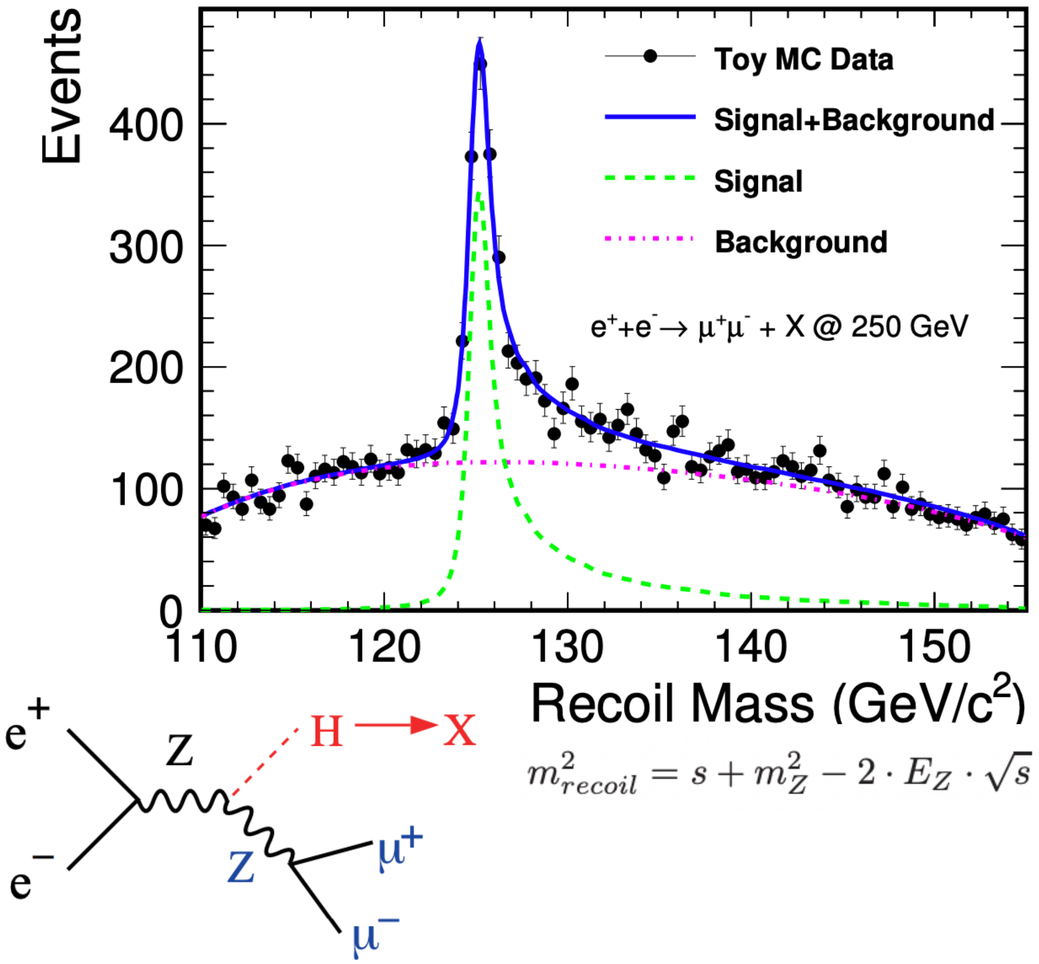


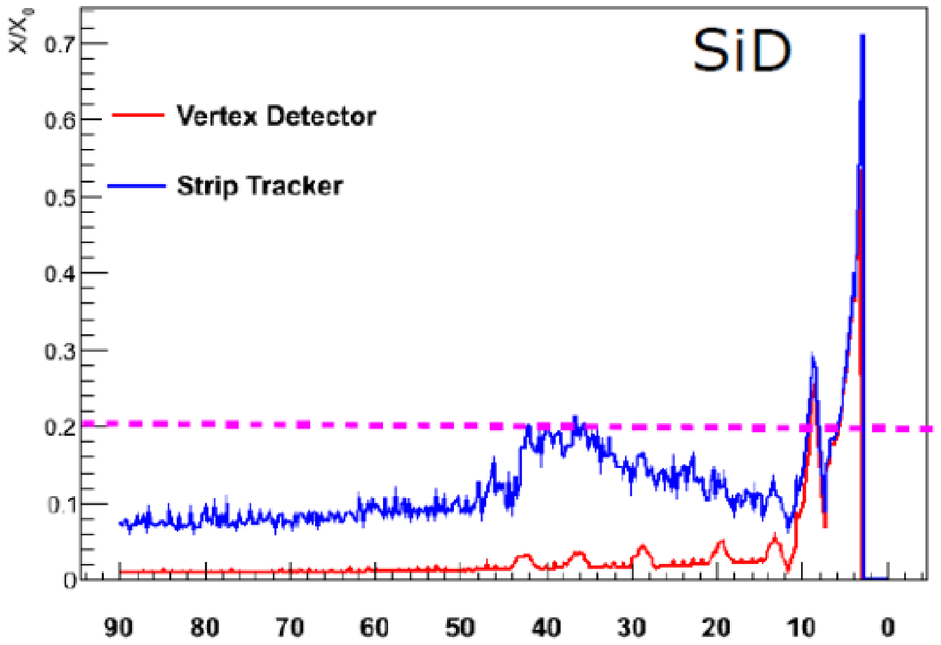
Need new generation of ultra low mass vertex detectors with dedicated sensor designs

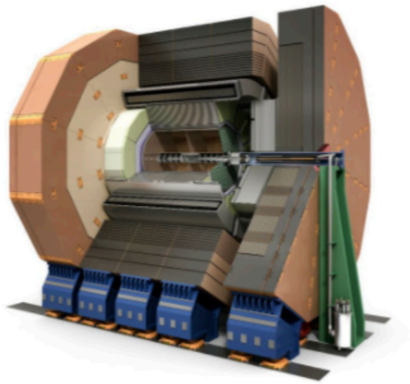
Detectors at future e^+e^-

Stringent detector requirements from ZH reconstruction

Detector designs at e^+e^- colliders are converging to very similar strategies

- Strong magnetic field 2-5 T
- (Ultra) low material budget & high granularity tracker close to the interaction point
  - <0.3% X0 per layer (ideally 0.1% X0) for vertex detector
  - <1% X0 per layer for Si-tracker
- High granularity calorimetry
  - Particle Flow reconstruction → plays a big part in many designs





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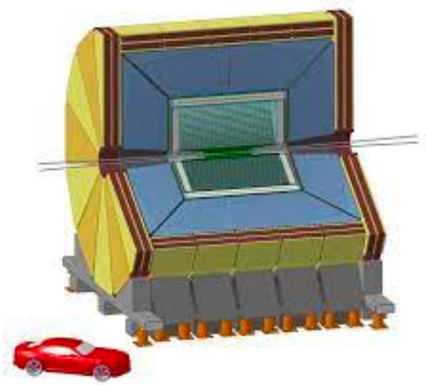


IDEA

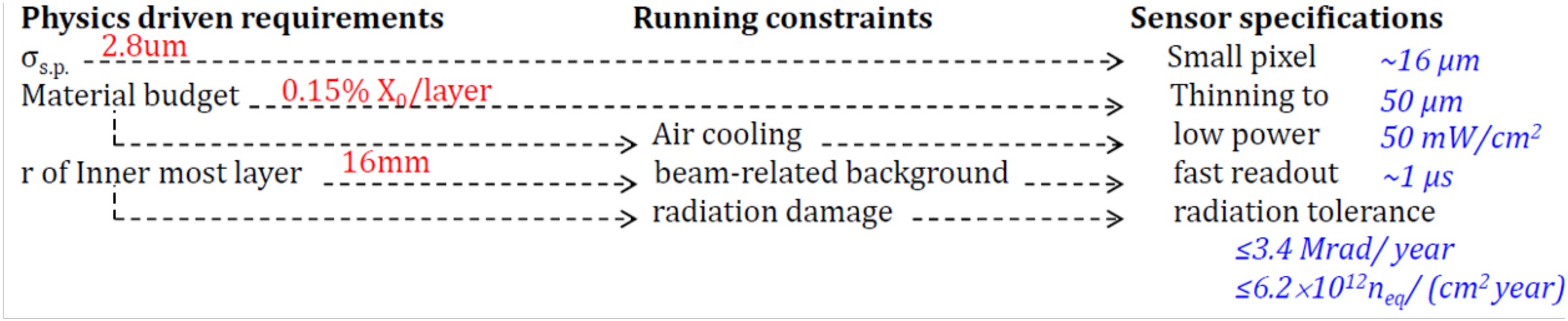
arXiv:2003.01116

Sensors technology requirements for Vertex Detector

Several technologies are being studied to meet the physics performance

Sensor's contribution to the total material budget of vertex detector is 15-30%

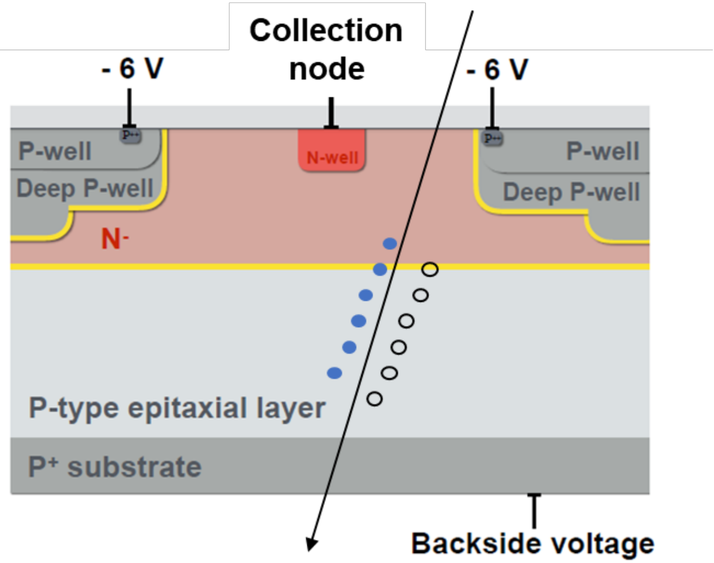
Sensors will have to be less than 75 μm thick with at least 3-5 μm hit resolution (17-25 μm pitch) and low power consumption



Monolithic Active Pixel Sensors - MAPS

A suitable technology for high precision tracker and high granularity calorimetry

- Monolithic technologies have the potential for providing higher granularity, thinner, intelligent detectors at lower overall cost.
- Significantly lower material budget: sensors and readout electronics are integrated on the same chip
  - Eliminate the need for bump bonding : thinned to less than 100μm
  - Smaller pixel size, not limited by bump bonding
  - Lower costs : implemented in standard commercial CMOS processes



Sensor optimization in TJ180/TJ65 nm process

Snowmass White Paper 2203.07626
Common US R&D initiative for future Higgs Factories 2306.13567

Current effort

Co-design approach: close interaction between physics studies and technology R&D [4]

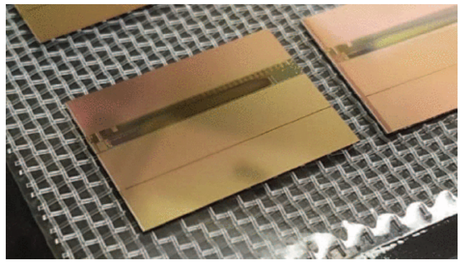
- Novel CMOS process for MAPS has recently become available, CERN (WP1.2 Collaboration) provides access to scientific community: TowerJazz-Panasonic (TPSCO) 65 nm CMOS imaging process with modified implants
  - Builds on sensor optimization done for the TJ180 process[1-2], excellent charge collection efficiency and low capacitance [3]
    - Increased density for circuits: Higher spatial resolution, better timing performance at same power consumption.
  - Supports stitching: enable wafer-scale MAPS →**potential to greatly reduce costs of future experiments**
- ALICE ITS3 upgrade is the main driver of CERN WP1.2 efforts
  - SLAC is the only US institute involved in Enginering Runs fabrication
- Several challenges towards wafer-scale devices → **large international effort needed to address all of them**
  - Large collaboration is interested in designing solutions for power distribution compatible with stitching and enabling O(ns) timing precision

[1] M. van Rijnbach *et al., Radiation hardness and timing performance in MALTA monolithic pixel sensors in TowerJazz 180 nm*, 2022 *JINST* C04034
[2] M. Munker *et al., Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance,* 2019 *JINST* 14C05013
[3] S. Bugiel *et al., Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology, NIMA Volume 1040, 1 October 2022, 167213*
[4] J. E. Brau et al., *The SiD Digital ECal based on Monolithic Active Pixel Sensors*, https://agenda.linearcollider.org/event/9211/sessions/5248, 2021.

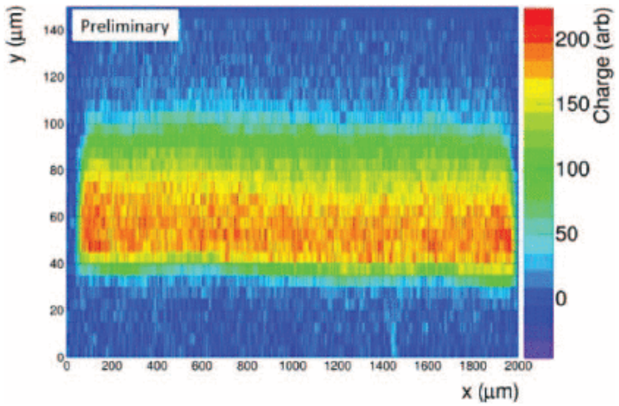
Large area MAPS – SLAC expertise

- SLAC has many years of experience in MAPS, developed detectors in several technologies[1-4]
- MAPS developments leverage large synergy with other core mission at SLAC: X-ray detectors (BES)
- Two most recent examples:

CHESS-II (AMS-350nm): prototype for strip detector for ATLAS

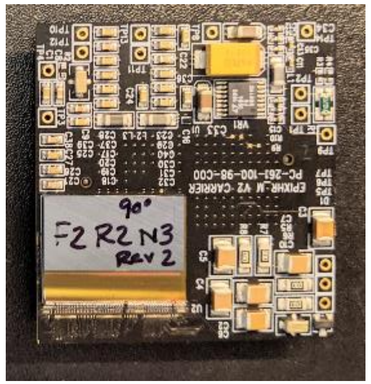


Photograph of the CHESS-II die

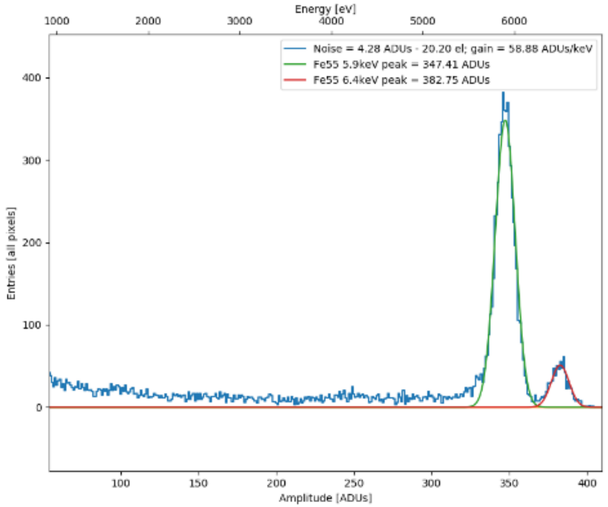


Collected charge at different x-widths and y-depths obtained with an Edge-TCT setup with a neutron fluence Φ=3×10^{14} neq/cm^2.

ePixM (LF 150nm): soft X-ray detector for LCLS-II



ePixM readout board



Fe55 spectrum measured with ePixM

[1] W. Snoeys, J.D. Plummer, S. Parker and C. Kenney, *Pin detector arrays and integrated readout circuitry on high-resistivity float-zone silicon*, IEEE Trans. Electron Devices 41 (1994) 903.
[2] J. D. Segal et al., *Second generation monolithic full-depletion radiation sensor with integrated CMOS circuitry*, in proceedings of IEEE NSS-MIC, Knoxville, U.S.A., 30 October–6 November 2010, pp. 1896–1900
[3] L. Rota et al., *Design of ePixM, a fully-depleted monolithic CMOS active pixel sensor for soft X-ray experiments at LCLS-II,* Journal of Instrumentation, Volume 14, December 2019
[4] C. Tamma et al., *The CHESS-2 prototype in AMS 0.35 µm process: A high voltage CMOS monolithic sensor for ATLAS upgrade,* doi: 10.1109/NSSMIC.2016.8069856

Enabling technical capabilities at SLAC

Microwave Annealing & Device modeling and simulations

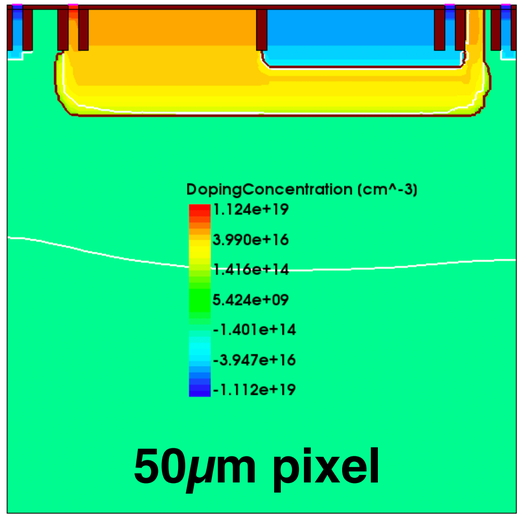
AXOM Microwave Annealing System in SLAC cleanroom

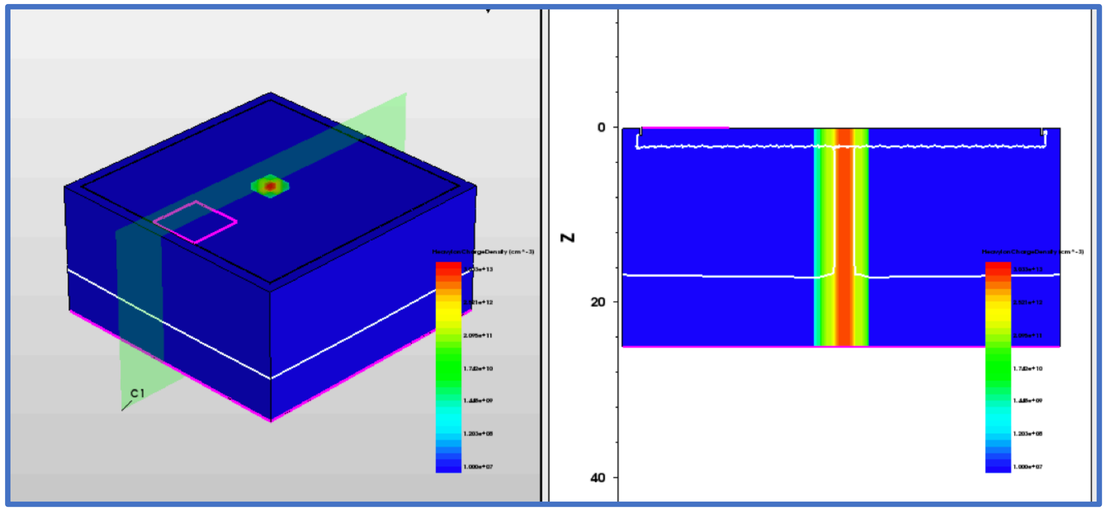
- Optimization of material to obtain desired properties (semiconductors, ceramics, polymers) often requires annealing (heat)
  - Heat may change, damage or destroy other elements of a structure
  - Heating materials is energy intensive process
- Microwave annealing (MWA) is a non-equilibrium annealing technique which selectively transfers energy to defects, dopants, interfaces or impurities
  - Tool facilitates development of novel device structures for sensors, ASICs
  - SLAC has developed several HEP applications using microwave annealing
  - MWA is compatible with CMOS processing, allowing advanced integration
- Experience in Device modeling and simulations
  - TCAD full characterization of new processes

MAPS on novel CMOS technologies

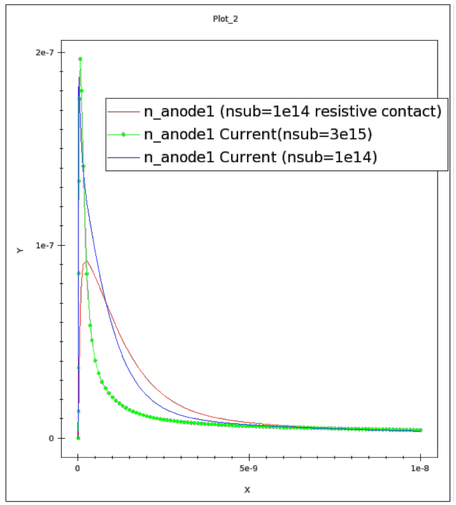
Blue-sky R&D on CMOS 22nm FDSOI

- Fully-Depleted Silicon-On-Insulator process enables implementation of sensor in substrate
- Promising CMOS process with excellent mixed-signal performance
- TCAD simulations and initial pixel design to evaluate key performance parameters:
  - Detector capacitance
  - Charge collection time
  - Cross-talk





3D Charge collection simulations (MIP)



Read-out current:
compare three process options

Large area MAPS – Highlights & Next Steps

Approach:

- Engaged with the scientific community to share know-how
- Focus on long-term R&D, targeting simultaneously:
  - ~ns timing resolution
  - Power consumption compatible with large area and low material budget
  - Fault-tolerant circuit strategies for wafer-scale MAPS

Highlights:

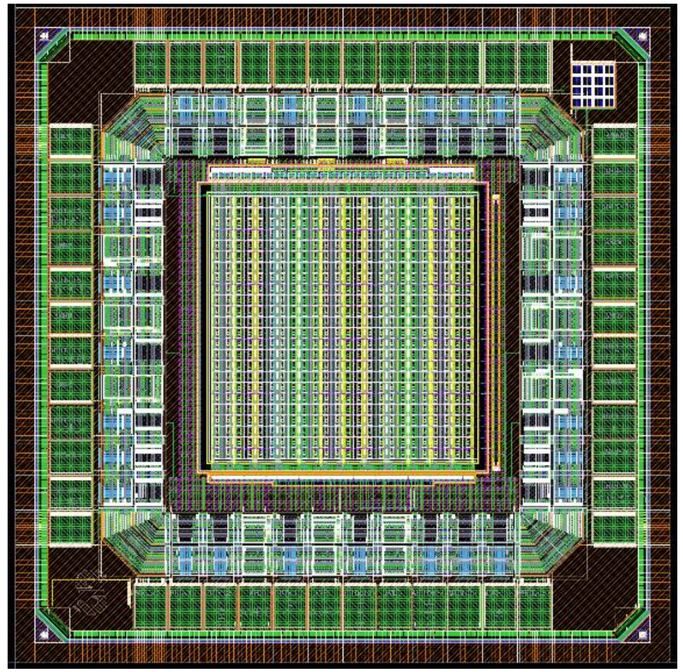
- Designed pixel architecture with binary readout optimized for linear colliders
- Submitted a small pixel matrix for fabrication on CERN WP1.2 shared run
- Architecture will allow us to evaluate technology in terms of defects and RTS

Next steps:

- Evaluate performance of 1st SLAC prototype on TJ65nm (2023).
- New design combining O(ns) timing precision and low-power (2024/2025).
- **Stretch Goals:** design of a wafer-scale ASIC (2025/2026, design only)

Engagement :

- Higgs Factory detector initiative R&D
- DRD 7.6 on common issues of power distributions compatible with stitching

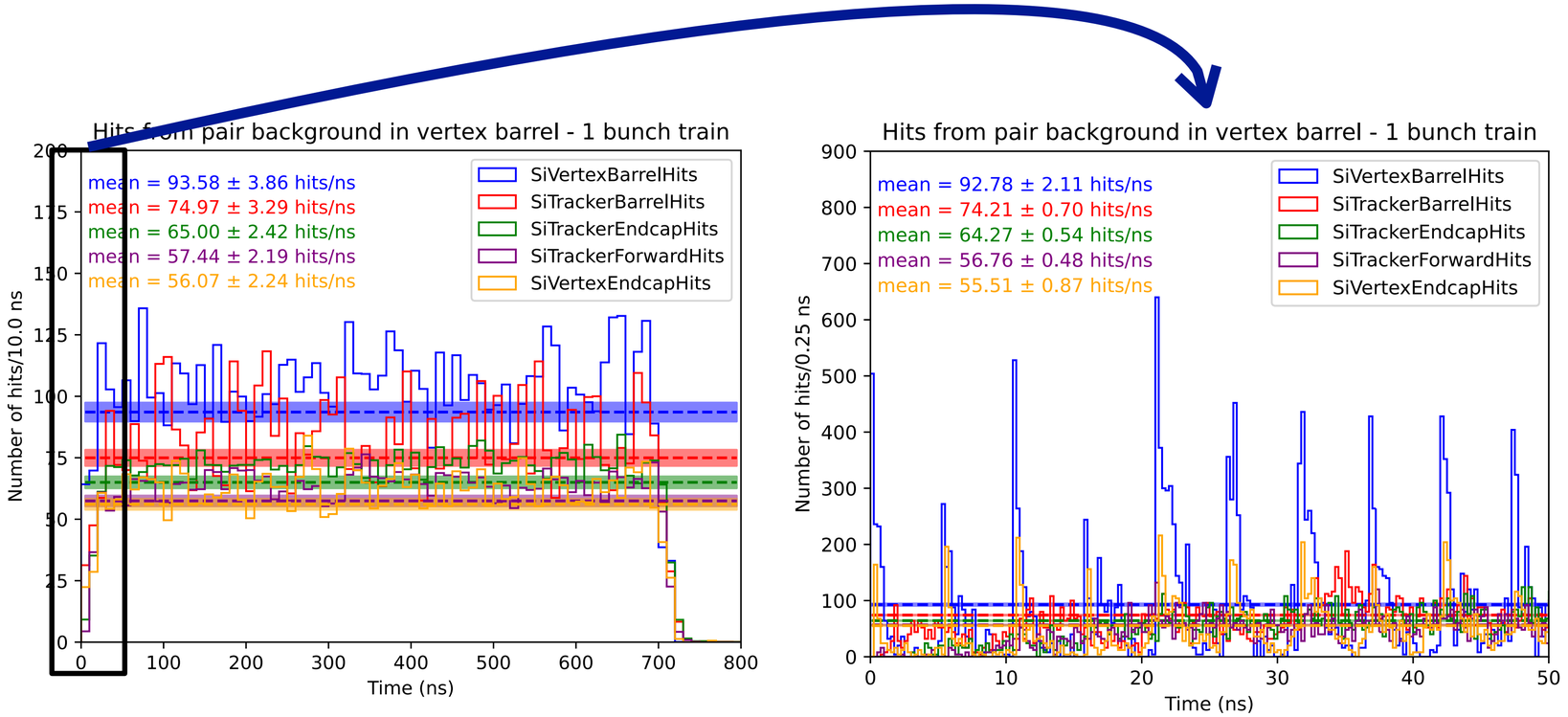


Layout of SLAC prototype for WP1.2 2022 shared submission on TowerSemi 65nm

Tracking performance

O(ns) timing capabilities as an additional handle to suppress beam induced backgrounds

Time distribution of hits per unit time and area: $\sim 4.4 \cdot 10^{-3}$ hits/(ns·mm^2) $\simeq$ 0.03 hits/mm^2 /BX
in the 1st layer of the vertex barrel SiD-like detector for ILC/C^3



Parameter	Value
Time resolution	1 ns-rms
Spatial Resolution	7 μm
Expected charge from a MIP	500 – 800 e/h
Minimum Threshold	200 e-
Noise	< 30 e-rms
Power density	< 20 mW/cm^2
Maximum particle rate	1000 hits/cm^2

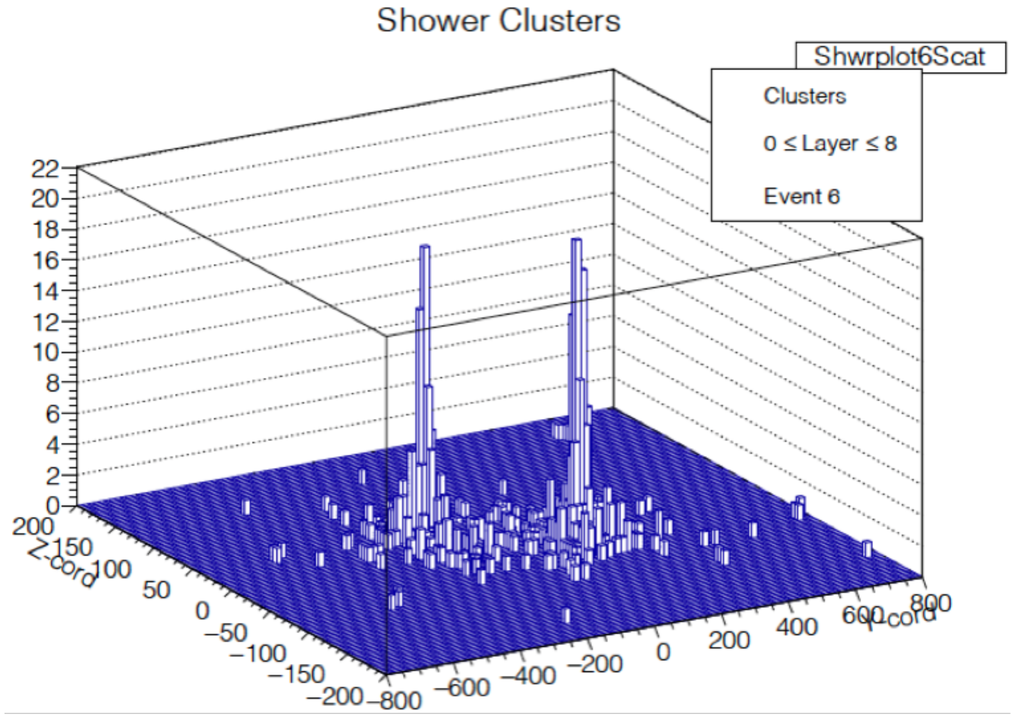
D. Ntounis talk on beam background simulations at ECFA 2023

MAPS for ECal

See J. Brau's talk

Fine granularity allows for identification of two showers down to the mm scale of separation

- SiD detector configuration with 25x100 μm^2 pixel in the calorimeter at ILC
  - With no degradation of the energy resolution
- ***The design of the digital MAPS applied to the ECal exceeds the physics performance as specified in the ILC TDR***
- The 5T magnetic field degrades the resolution by a few per cent due to the impact on the lower energy electrons and positrons in a shower
- Future planned studies include the reconstruction of showers and π^0 within jets, and their impact on jet energy resolution



GEANT4 simulations of Transverse distribution of two 10 GeV showers separated by one cm

See A. Habib's talk

Target Specs vs. State of the Art

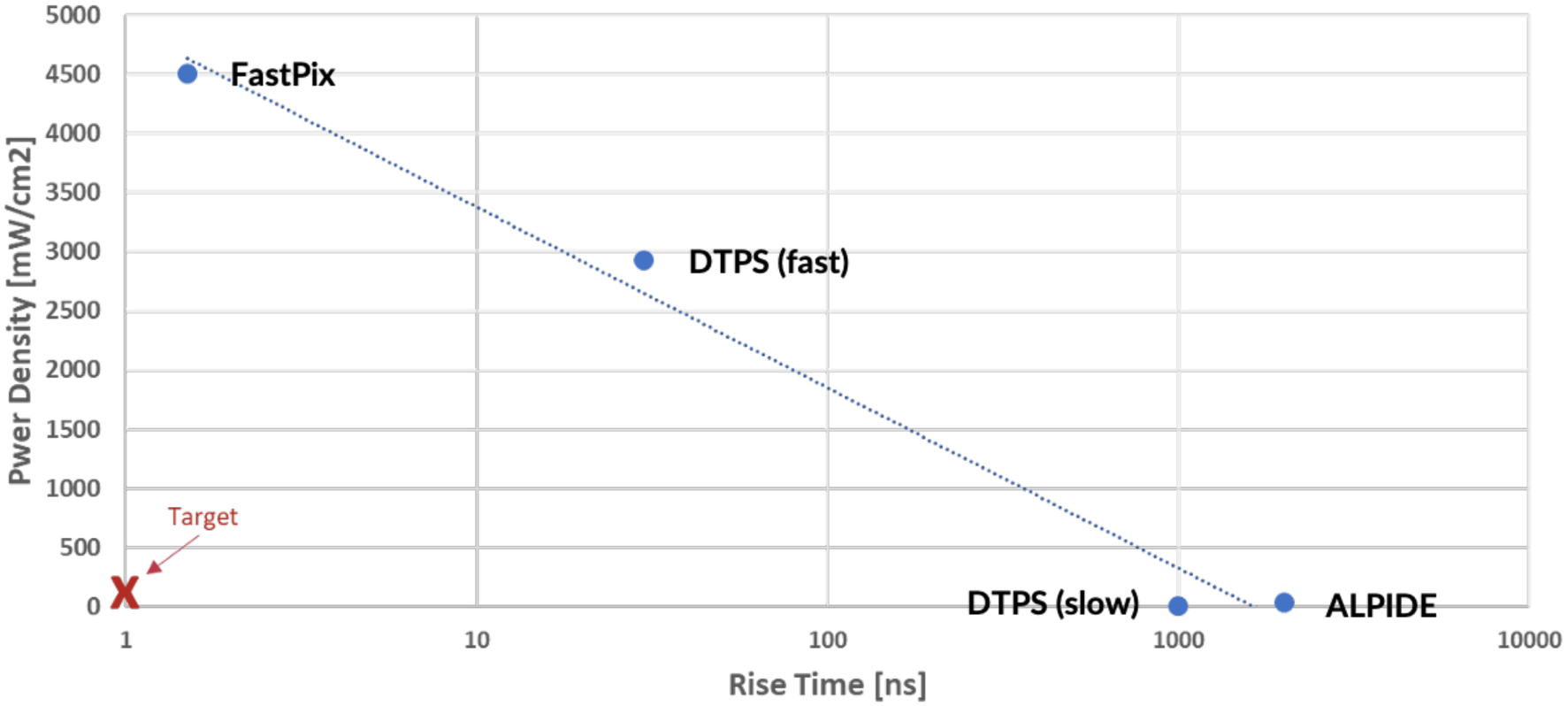
Chip name	Technology	Pixel pitch [μm]	Pixel shape	Time resolution [ns]	Power Density [mW/cm^2]
Target Specification	**?**	**25 x 100**	**Sq / rect**	**1**	**< 20**
ALPIDE [2][3]	Tower 180 nm	28	Square	< 2000	5
FastPix [4][5]	Tower 180 nm	10 - 20	Hexagonal	0.122 – 0.135	>1500
DPTS[6]	Tower 65 nm	15	Square	6.3	53
Cactus [7]	LF 150 nm	1000	Square	0.1-0.5	145
MiniCactus [8]	LF 150 nm	1000	Square	0.088	300
Monolith [9][10]	IHP SiGe 130 nm	100	Hexagonal	0.077 – 0.02	40 - 2700

No design fulfills all target specification → The need to develop a custom design

We decided to go with the Tower 65nm technology, which has been optimized by CERN WP1.2 to have low sensor capacitance allowing very good performance with low power consumption.
+ it has the possibility of a wafer-scale stitched sensor
+ it has been proven to be radiation tolerant

See A. Habib's talk

Target Specs vs. State of the Art



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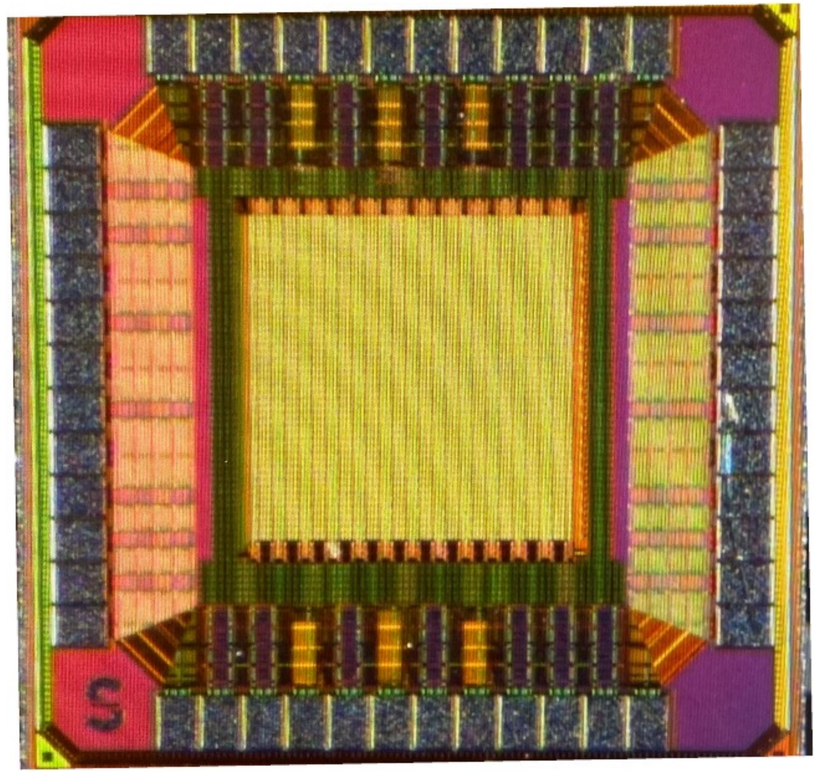
See A. Habib's talk

NAPA_p1: **NA**nosecond **P**ixel for large **A**rea sensors – **P**rototype **1**

First prototype in TJ 65nm

- The prototype design submitted with a total area 5 mm x 5 mm and a pixel of 25 μm 25 μm, to serve as a baseline for sensor and pixel performance.
- Design motivation ➔ simple architecture with minimum global signals to reduce failure risk in a large area implementation.
- Thanks to CERN WP1.2 effort on sensor optimization in TowerSemi 180 nm and 65 nm technologies

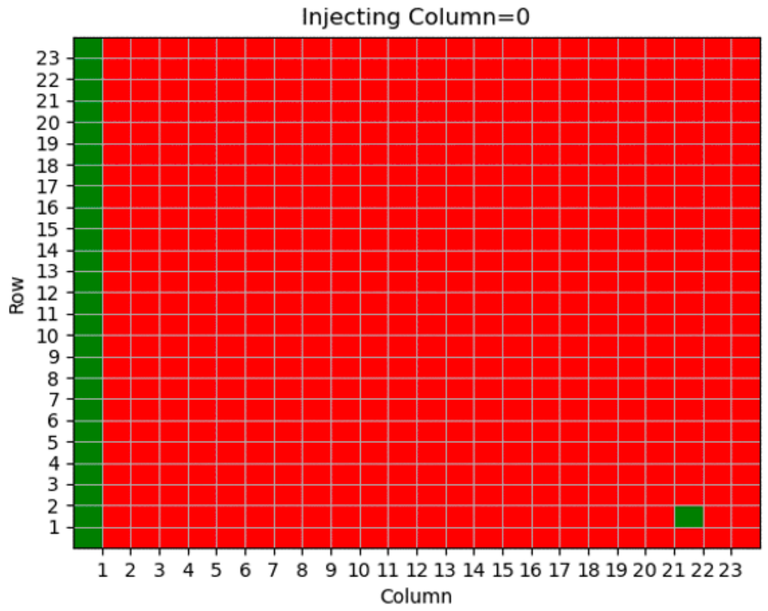


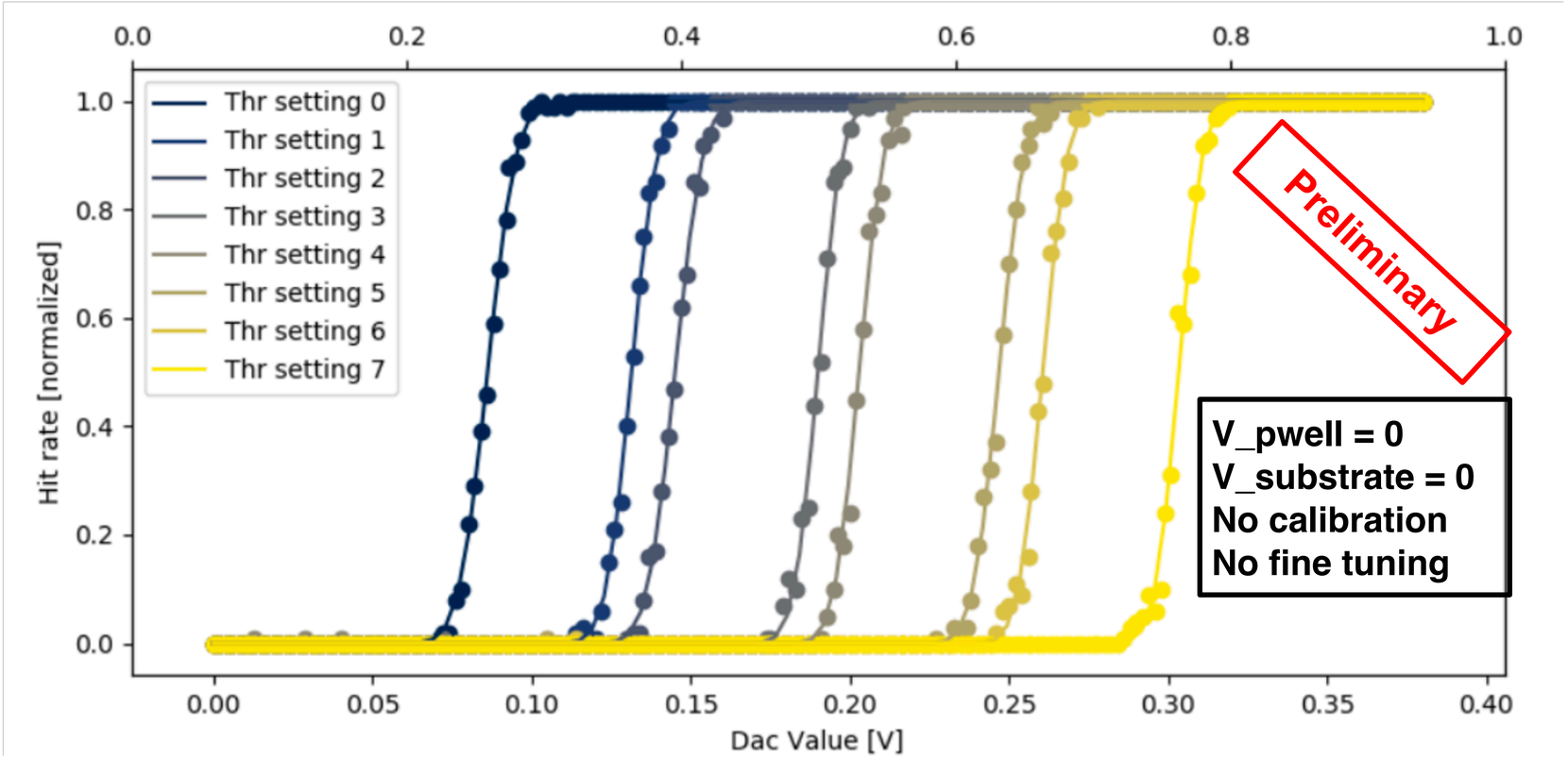
Picture of NAPA-p1 prototype from WP1.2 shared submission

See A. Habib's talk

Preliminary Characterization Results

Chip characterization is on going



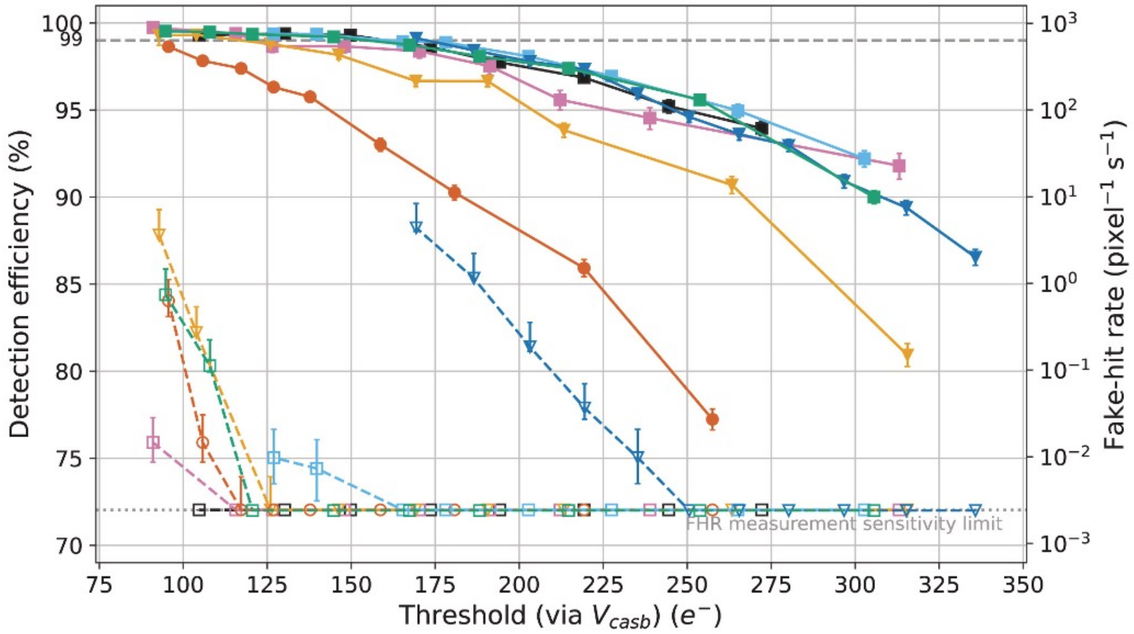


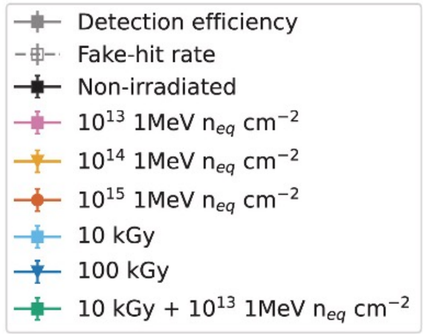
See M. Vassilev's poster

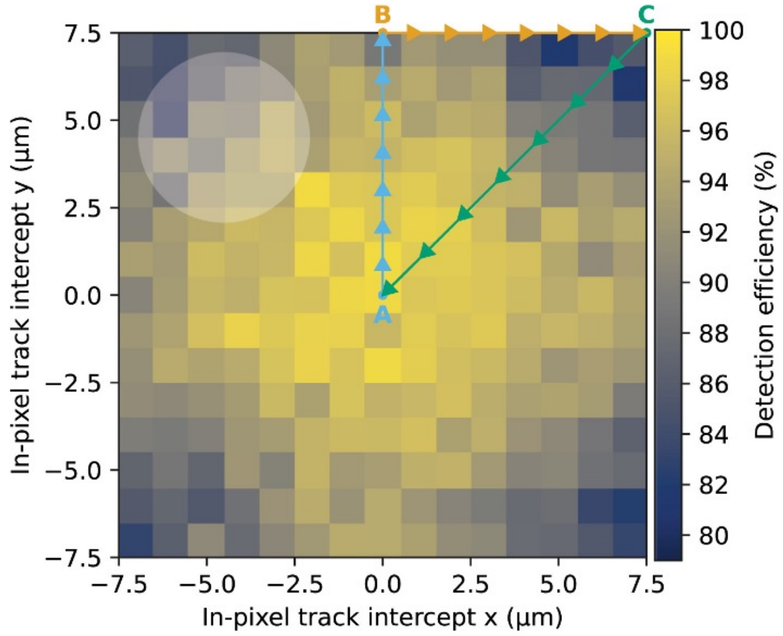
DPTS testing activities

Synergies with DPTS characterization at CERN test beam facility within ALICE Collaboration

- DPTS chips were tested in charged particle beams, such as in a 10 GeV/c positive hadron beam at CERN PS
  - Characterization done up to 10^{15} 1 MeV n_{eq} cm^{-2}





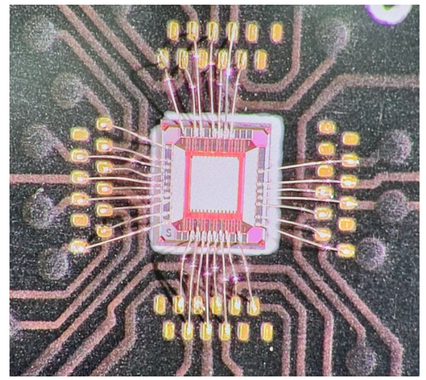


[1] *Digital pixel test structures implemented in a 65 nm CMOS process*, https://doi.org/10.1016/j.nima.2023.168589
[2] *A Compact Front-End Circuit for a Monolithic Sensor in a 65-nm CMOS Imaging Technology* doi: 10.1109/TNS.2023.3299333

Conclusions and next steps

First MAPS prototype within CERN WP1.2 collaboration targeting e^+e^- requirements is being tested

- MAPS technology is being investigated for applications at future e^+e^- colliders for both tracking and calorimetry applications
  - *Highlighted in the IF Snowmass report and US R&D initiative for future Higgs Factories*
- Developed first prototype within CERN WP1.2 based on TJ 65nm processing
  - Simulations of NAPA-p1 show that it is possible to achieve a time resolution 1 ns-rms with reasonably low power consumption of ~100 mW/cm^2 x Duty Cycle (at LC < 1%)
  - First characterization of Napa-p1 is promising - more ongoing
  - Design of NAPA-p2 has started to tackle large sensor challenges
    - NAPA-p2 will serve as a system proof of concept
- Requirements derived for LC but many of the challenges of deploying this technology are common: power distribution, low yield …
  - Technical problems which are independent of the application which require international collaboration to tackle
  - Test beam experience at CERN within the Alice collaboration testing effort for DPTS
  - Engagement within the DRD7.6 collaboration to develop specific block to be included in the next engineering run.
- SLAC expertise will be leveraged to test new processing
  - Several MAPS developments have been carried out at SLAC in the past years
  - Synergy with other programs at SLAC, e.g. Ultra-fast X-ray science
  - We are now focusing on co-design leveraging SLAC expertise across all areas: physics studies, TCAD device modeling and simulation, ASIC design, etc.



NAPA-p1

Thank you!

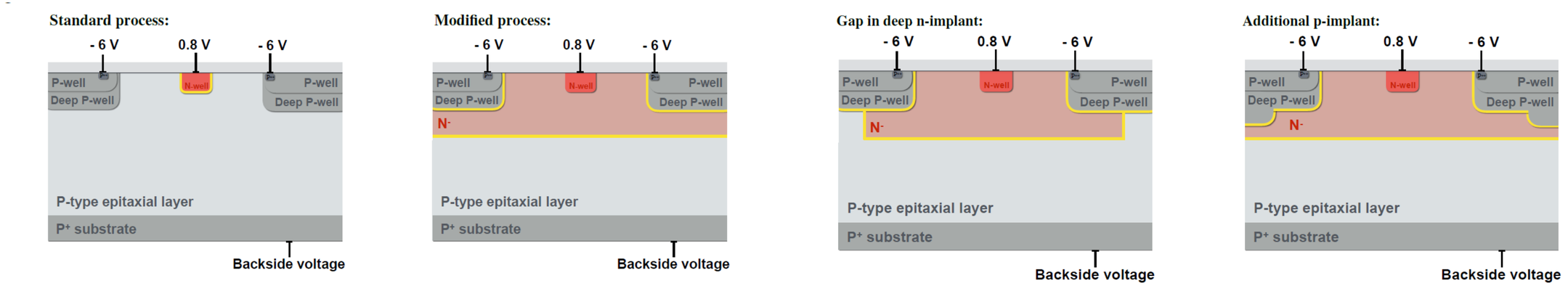
Design Approach

For a constant SNR and Q_{in} ➔ $Power \propto (C_{sensor})^m \quad with\ 2 \leq m \leq 4$ as shown in [11]

➔ **Aim for smallest possible sensor capacitance**

- Thanks to CERN WP1.2 effort on sensor optimization in TowerSemi 180 nm and 65 nm technologies [12] [13]
  - ➔ C_{sensor} of 2-3 fF is achievable while maintaining high collection efficiency

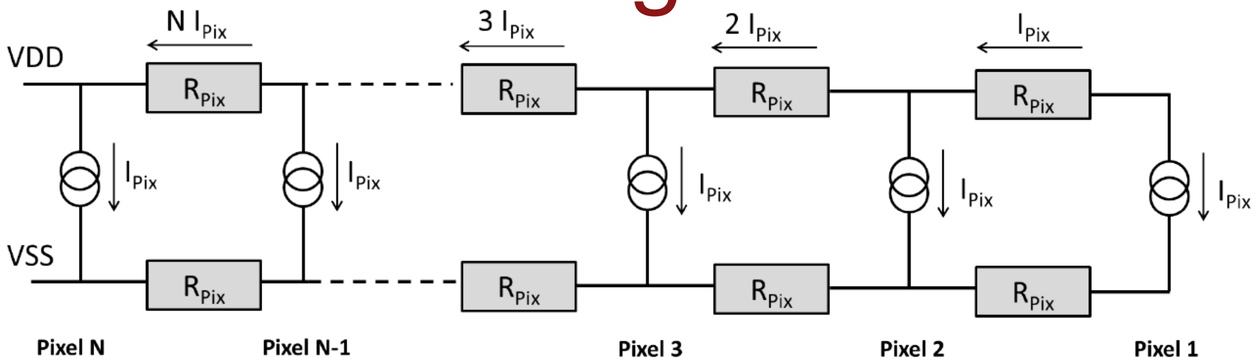
Jitter $\propto \frac{Cload}{\sqrt[n]{I}}$ with $1 \leq n \leq 2$ ➔ **Keep C_{load} to a minimum and increase the current if needed.**



Sensor optimization in TowerSemi 180 nm process from [12] and [13]

Going Towards a Large Sensor → Challenge

$$\Delta V = I_{pix} \times R_{Pix} + 2 \times I_{Pix} \times R_{Pix} + 3 I_{Pix} \times R_{Pix} + ... + N \times I_{Pix} \times R_{Pix}$$
$$\Delta V = I_{Pix} \times R_{Pix}(1 + 2 + 3 + ... + N)$$
$$\Delta V = I_{Pix} \times R_{Pix} \times \frac{N(N+1)}{2}$$



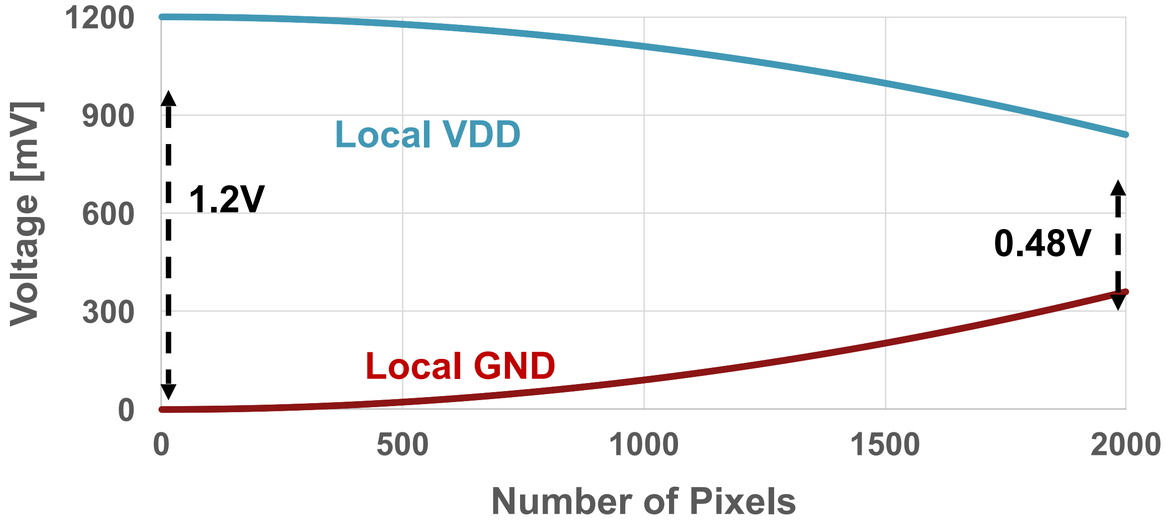
Assuming :I_{pix} = 600 nA and R_{pix} = 300 mΩ

Assuming pixel of 25 μm x 25 μm

A column of 10 cm would have 4000 pixels

Double sided powering

→ max drop length = 2000 pixels

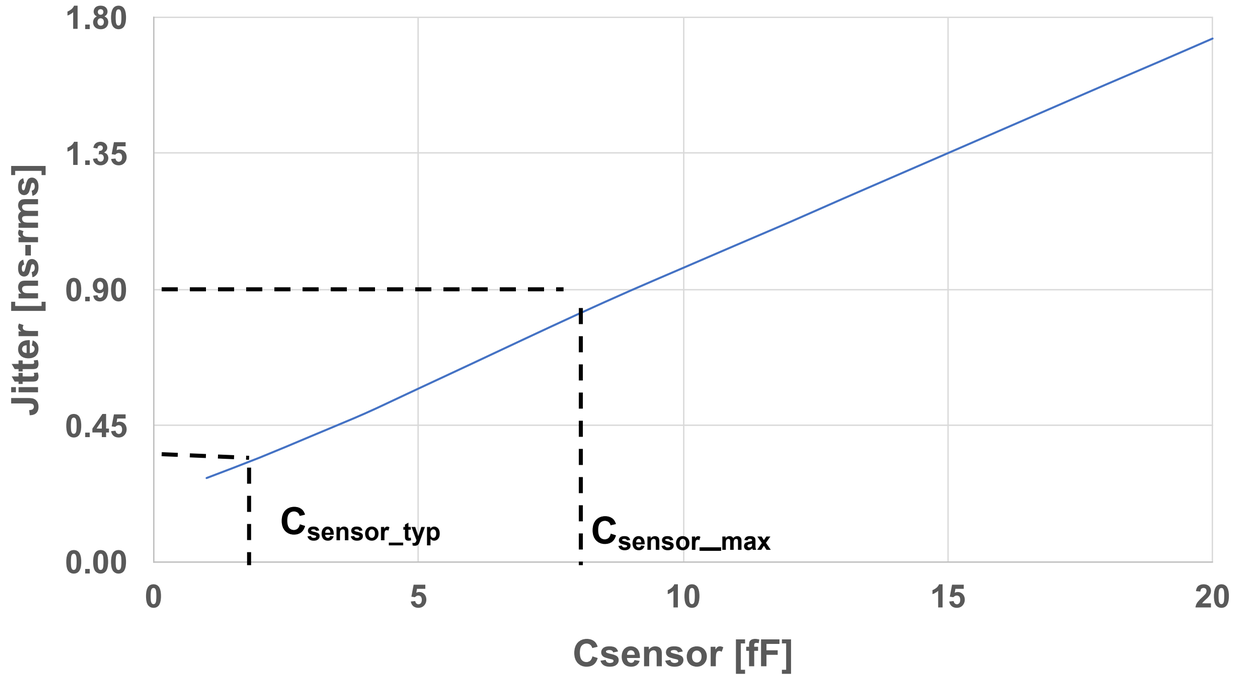


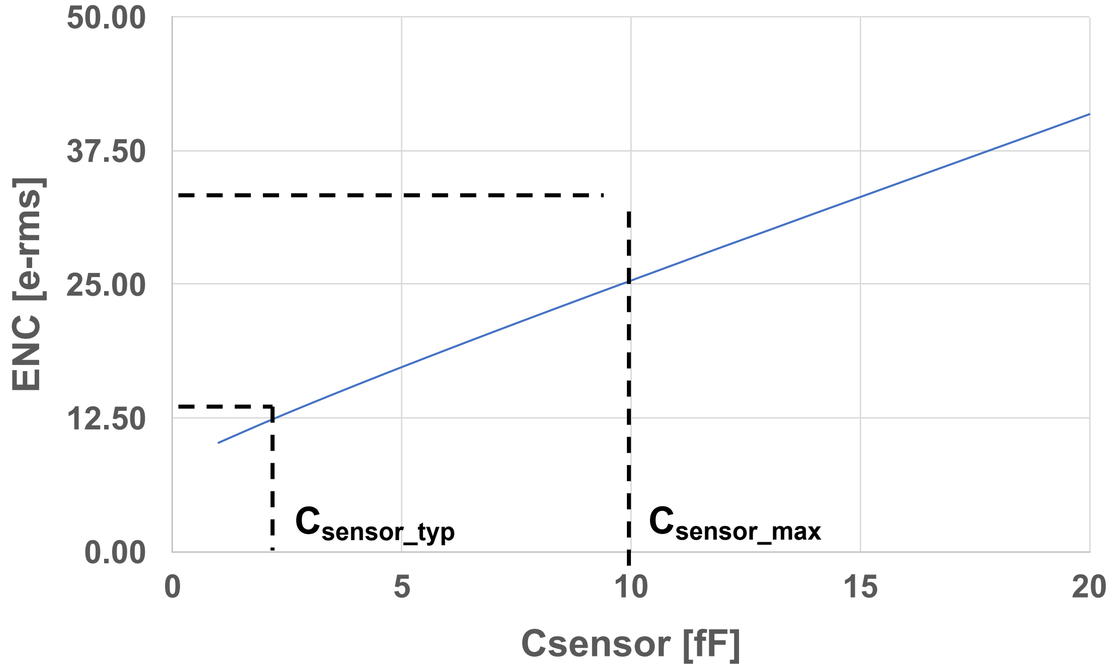
VDD-GND goes from 1.2 V near the power pads down to around 480 mV after 2000 pixels

The main limitation comes from large scale power distribution rather than cooling constraints

After 10^3 pixels (reticle, 2.5 cm), $V_{drop} \approx 0.1$ V
After 4 x 10^3 pixels (sensor, 10cm), V_{drop} = 1.5V !

Simulation of Jitter and ENC as a Function of C_{sensor}



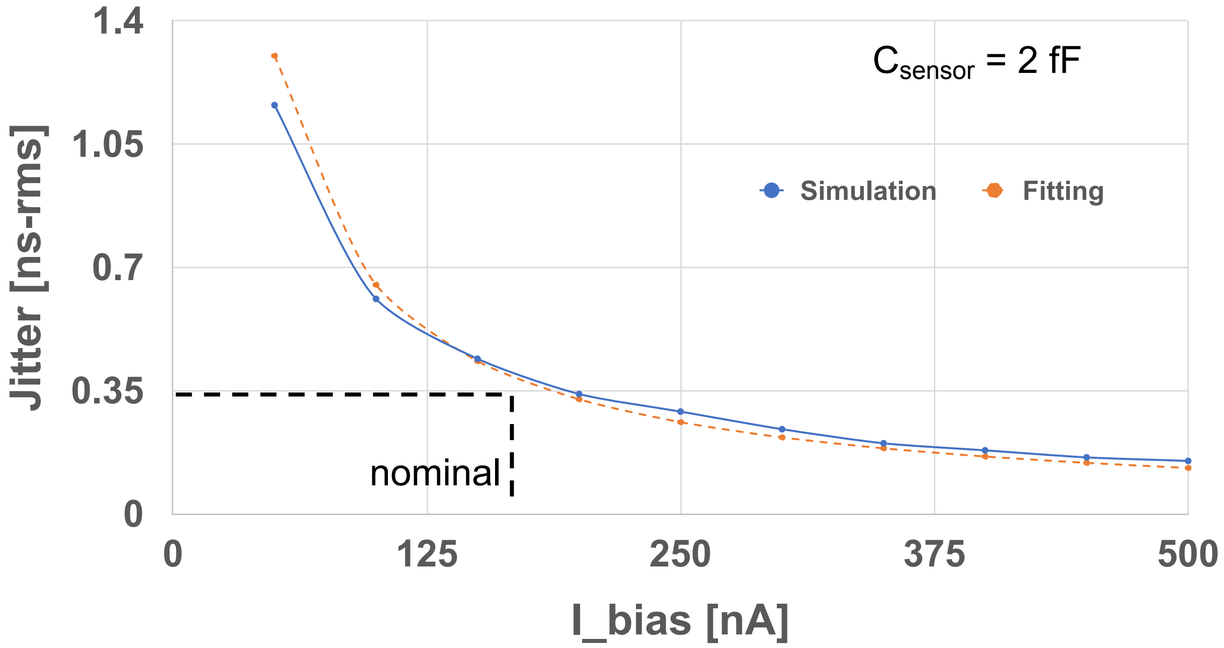


jitter = 400 ps for $C_{sensor\_typ} \approx 2$ fF → **Ok for Specs** ← **ENC = 13 e-rms for $C_{sensor\_typ} \approx 2$ fF**

These simulations are with a nominal pixel current of 600 nA → <Power density> = 115 mW/cm² x duty cycle
For e+e- machines such as ILC and C³, duty cycle is expected < 1%

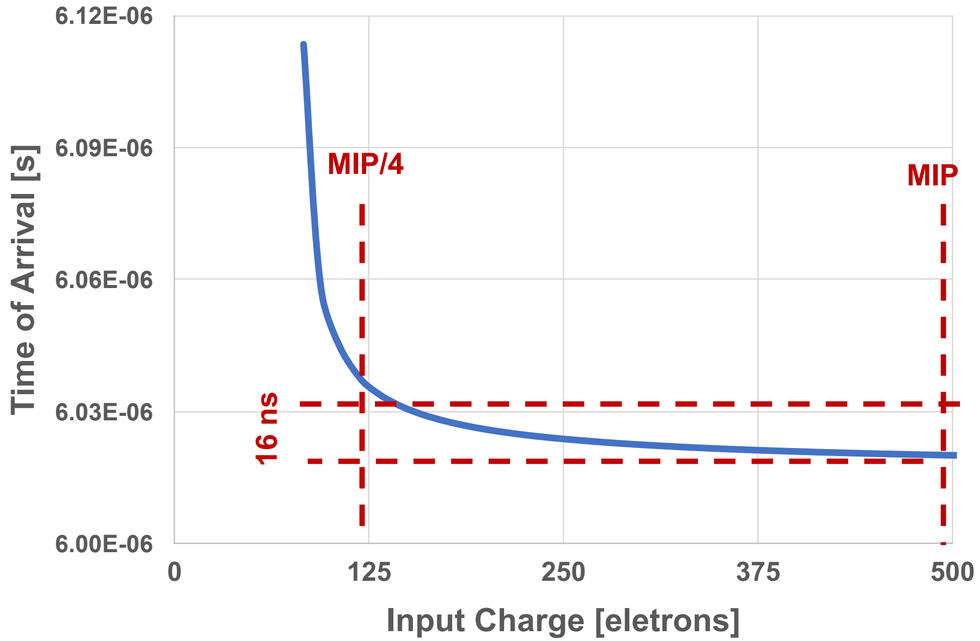
Simulation Results : Jitter and Time Walk

Jitter



I_bias = 200 nA ≡ pixel current = 600 nA
From theory we expect : $\sigma_{FE} \propto \frac{1}{(\mathrm{Power})^{\frac{1}{n}}}$ with $1 \leq n \leq 2$

Time Walk



Time walk for MIP → MIP/4 = 16 ns
Not negligible and must be corrected
(in pixel? In balcony? Offline? TBD)

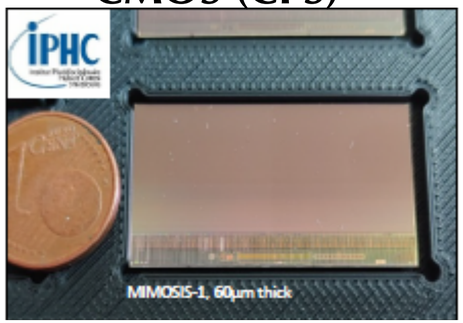
Sensors technology overview

Several possible choices for the VTX detector:

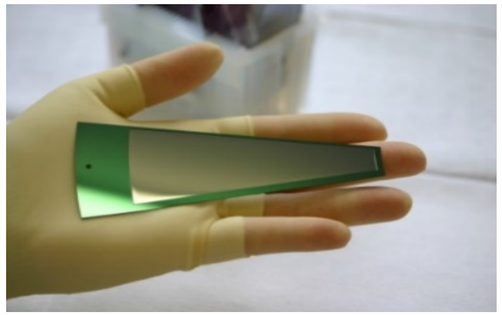
- Monolithic Active Pixels (MAPS)
  - CMOS Pixel Sensors (CPS)
  - Fully Depleted on High Resistivity Substrate (DNwel sensing)
  - Fully Depleted SOI technologies
- Depleted Field Effect Transistors (DEPFET)
- Fine pixel Charged Coupled Devices (CCD)
- 3D integration

- The general landscape is also changing rapidly with advances in microelectronics

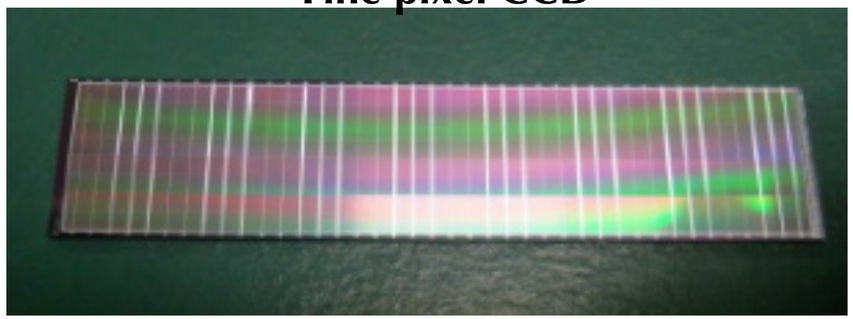
CMOS (CPS)



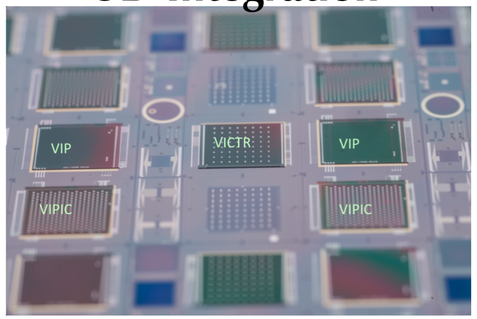
DEPFET



Fine pixel CCD

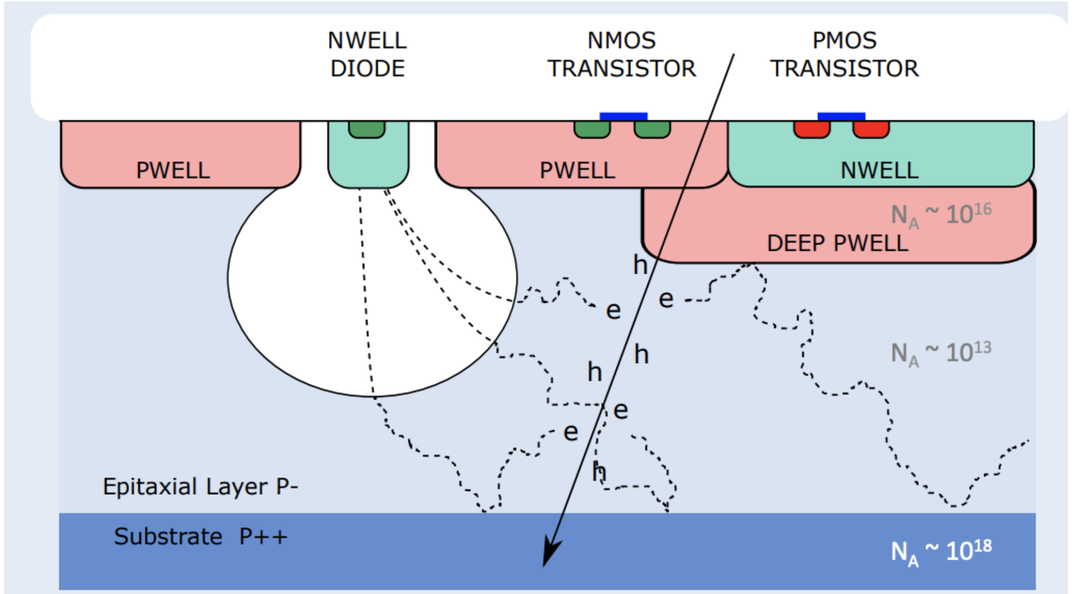


3D Integration



ALPIDE

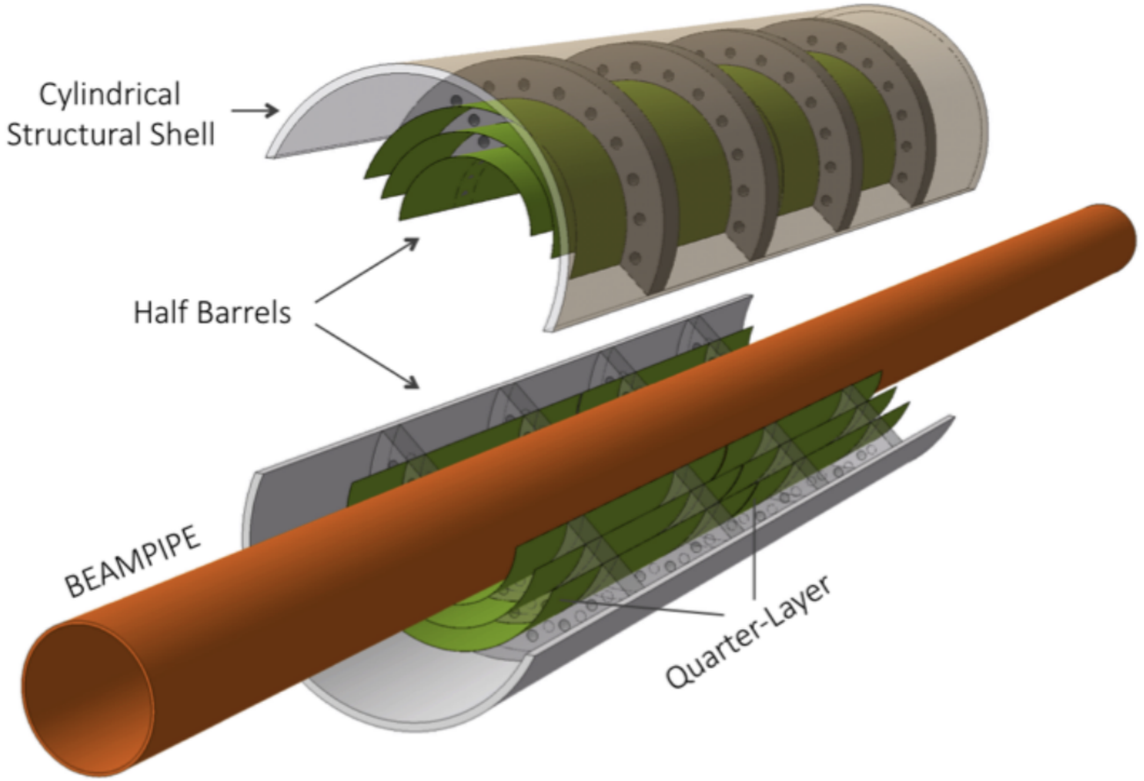
- With the current tracker upgrade ALICE redefined the new state-of-the art in CMOS MAPS technology and its applications in HEP
- ALice PIxel DEtector (ALPIDE) uses CMOS Pixel sensor used in imaging process
  - full CMOS circuitry within active area
  - Sensor thickness = 20-40 µm (0.02-0.04% X0)
  - 5µm spatial resolution
  - radiation hard to 10^{13} 1 MeV n_{eq}



V. Manzari, 2019

The used technology offers further opportunities: smaller feature size, **bending** that directly impact the key measurements that highly rely on precise vertexing and low material budget

ALICE: Bent MAPS for Run 4



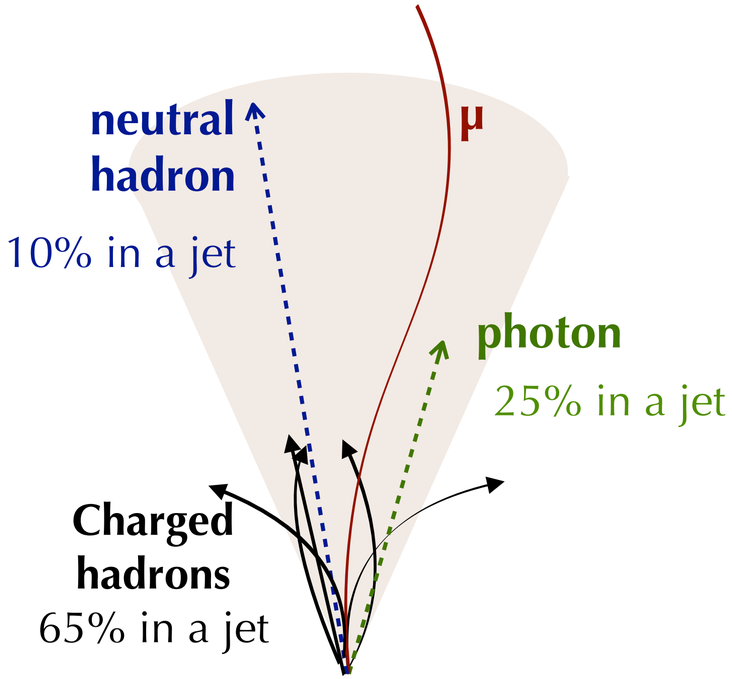
Bending Si wafers + circuits is possible

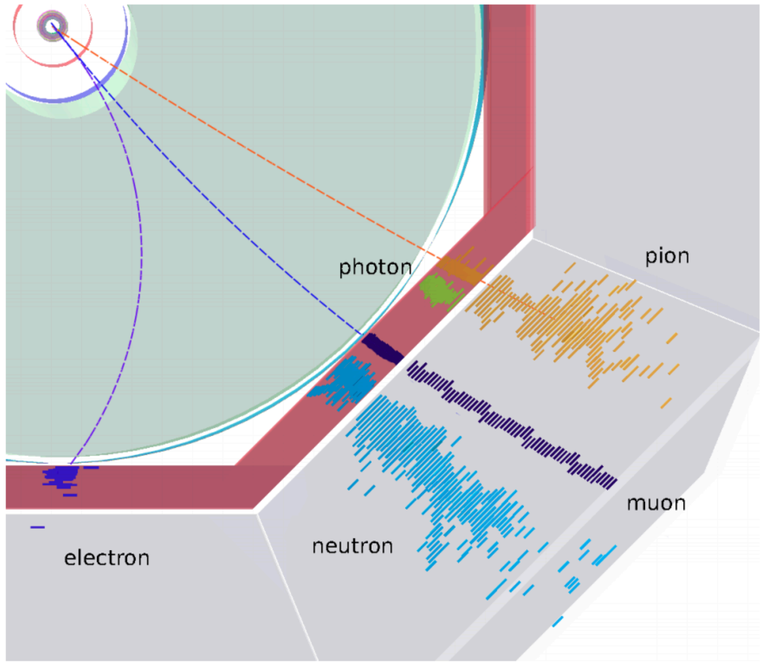
Recent ultra-thin wafer-scale silicon technologies allow:

- Sensor thickness = 20-40 µm - 0.02-0.04% X0
- Sensors arranged with a perfectly cylindrical shape
  - a sensors thinned to ~30µm can be curved to a radius of 10-20mm (ALICE-PUBLIC-2018-013)
- Industrial stitching & curved CPS along goals of ALICE-ITS3, possibly with 65 nm process

Particle Flow Calorimeters

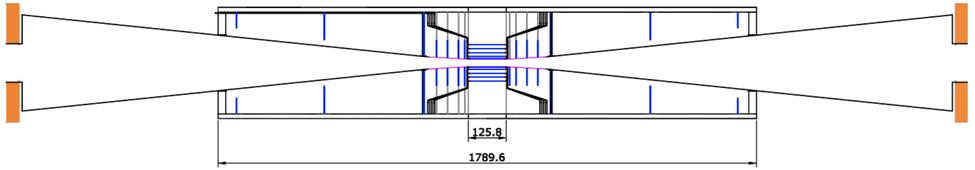
- CALICE collaboration: development and study of finely segmented and imaging calorimeters
  - Precise reconstruction of each particle within the jet
  - Issues: overlap between showers, complicated topology, separate physics event particles from beam-induced background
- CALICE R&D inspired CMS high granularity solution HGCAL - Common test beams with the AHCAL prototype
  - New ideas/technologies being explored: high precision (ps) timing calorimeters and new sensors ideas (ex: MAPS, LGADs)





SiD

Arxiv: 1306.6329



- Compact, cost constrained detector
  - 5 T solenoid B-field with with R_{ECAL}=1.27 m
  - All silicon pixel vertex + tracking system
  - Highly granular Si calorimeter optimized for PFLOW

- Pixel Vertex detector
  - 1 kGy and 10^{11} n_{eq}/cm^2 per year
  - **Pixel hit resolution** better then 5 μm in barrel
    - Better if charge sharing is used
  - Less than **0.3% X_0** per pixel layer
    - air cooling → low-mass sensor
  - Single bunch time resolution
    - Low capacitance and high S/N allows for acceptable power dissipation for single-crossing time resolution (~ 300-700 ns)

- Outer pixel Tracker:
  - 0.1-0.15% X_0 in the central region

20x20 μm pixels in the central region
50x50 μm for the forward tracker disks

Barrel	R	z_{max}	
Layer 1	14	63	
Layer 2	22	63	
Layer 3	35	63	
Layer 4	48	63	
Layer 5	60	63	
Disk	**R_{inner}**	**R_{outer}**	**z_{center}**
Disk 1	14	71	72
Disk 2	16	71	92
Disk 3	18	71	123
Disk 4	20	71	172
Forward Disk	**R_{inner}**	**R_{outer}**	**z_{center}**
Disk 1	28	166	207
Disk 2	76	166	541
Disk 3	117	166	832