Development of CMOS Sensors for HEP with a US-based foundry

Fermilab: *A. Apresyan, M. Alyari, N. Bacchetta, D. Berry, T. England, F. Fahim, R. Lipton;*
Purdue: *M. Liu, M. Jones;* ***University of Chicago***: *K. Di Petrillo;*
University of Illinois Chicago: *C. Mills*

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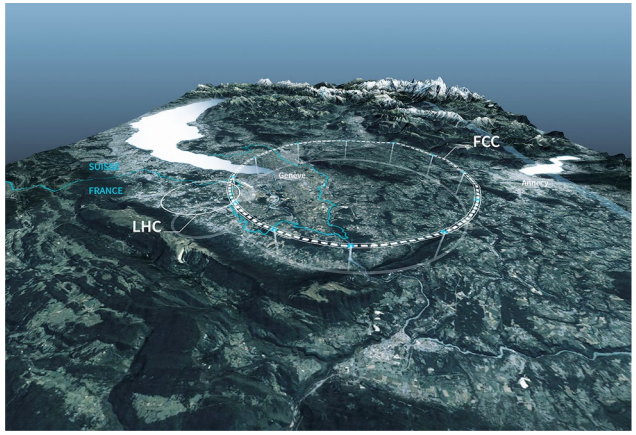
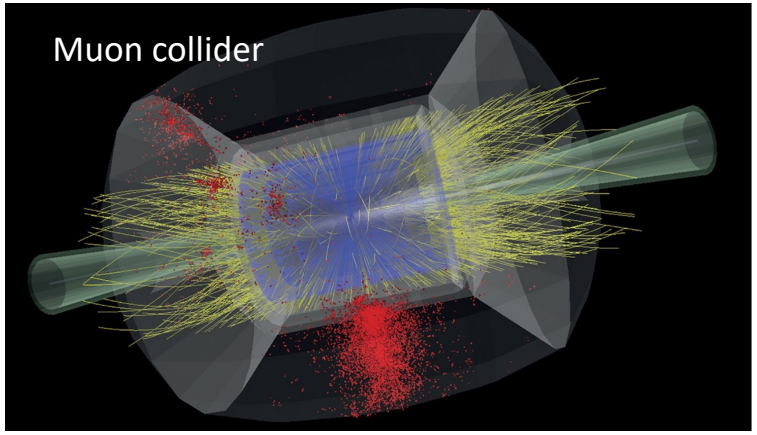
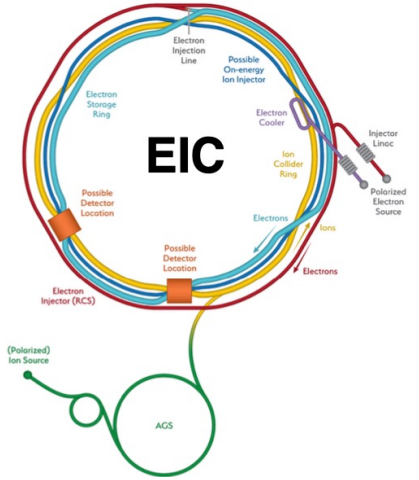
Motivation

- The HEP community is planning the next major collider
  - **Higgs factory, FCC_{ee}** recommended by Snowmass
- Tracking system will play decisive role for FCC_{ee} physics goal
  - A **low mass tracker** is required to provide measurements with a low enough systematic error to match the tremendous accumulated statistics
- Recent developments of low-mass, low-power and low-cost CMOS MAPS make this the preferred option for FCC_{ee}.







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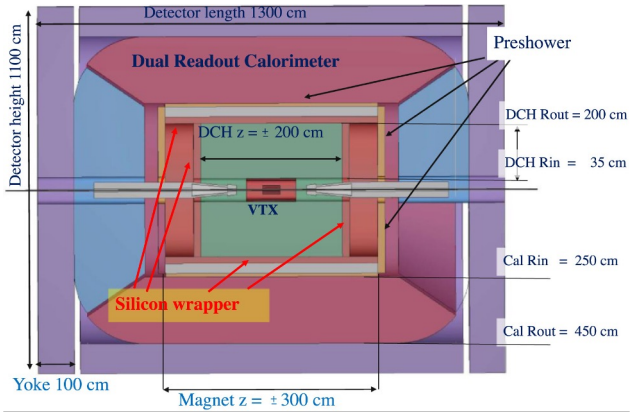
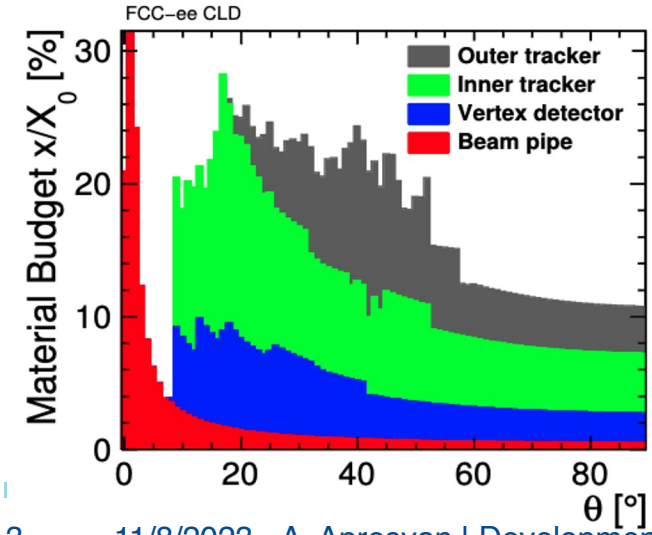
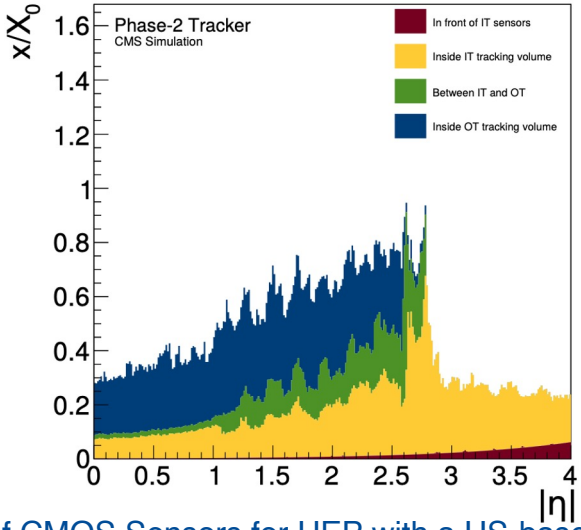
Requirements

- Physics goals
  - Identify b/c quarks and tau leptons from **Higgs**
  - Perform a precise measurements of the **Z boson**
- Require a **5 μm** spatial resolution, angular resolution of **0.1 mrad**
- Very low mass budget
  - First detector layer material budget of 0.2% X_0
  - Total tracking material budget <30% X_0
  - The upcoming CMS tracker upgrade is <80% X_0

IDEA







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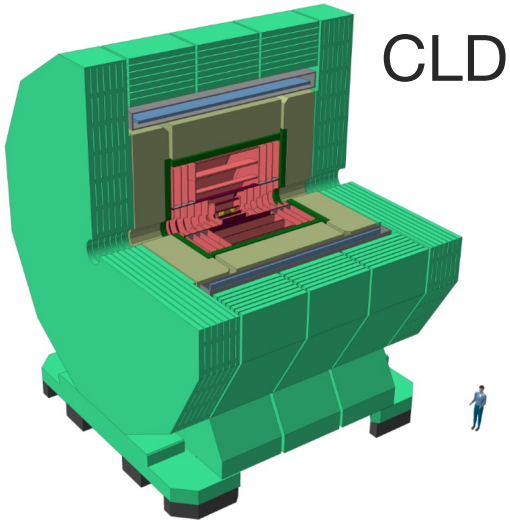

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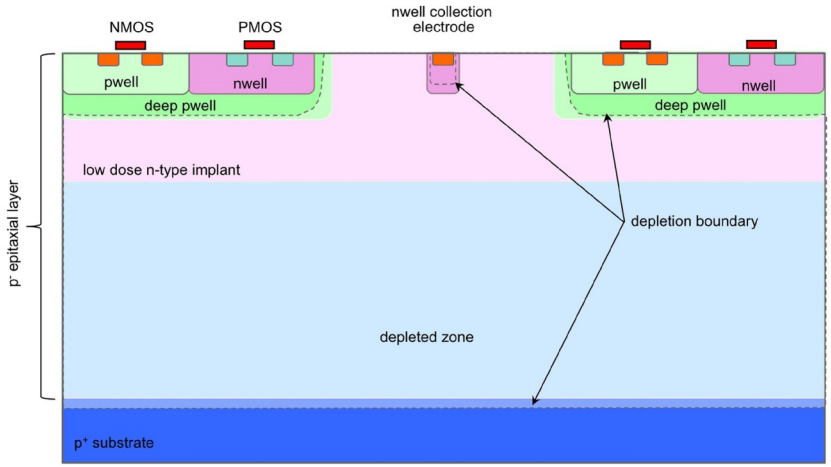
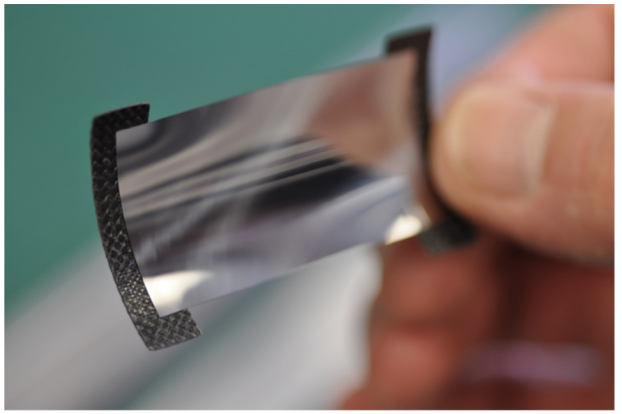
Sensor Proposal

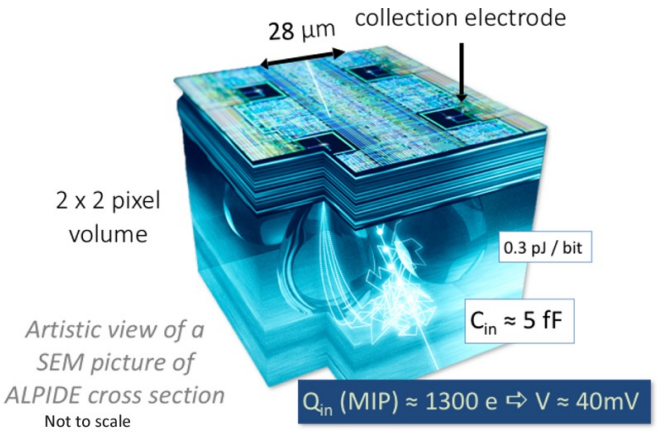
- Monolithic Active Pixel Sensors (**MAPS**), Low Gain Avalanche Diodes (**LGADs**), and Single Photon Avalanche Diodes (**SPADs**)
  - Critical components in trackers and calorimeters
- Fabricated in a standard CMOS process
  - Excellent spatial resolution (~5 μm)
  - Low-power consumptions (<40 mW/cm^2)
  - Low mass (~0.05 X_0)
  - Low cost for large volume fabrication



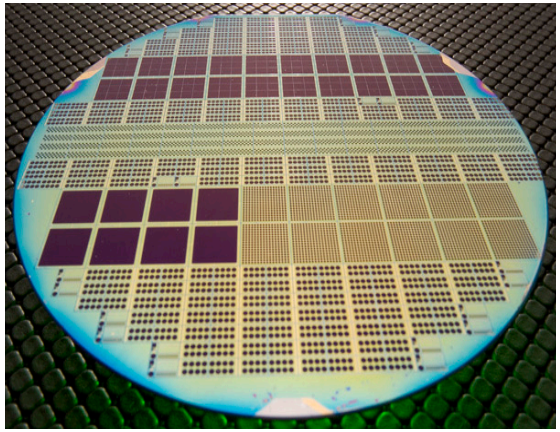


CMOS Sensors Vision

- **GOALS**
  - US manufactured sensor capability for HEP experiments
  - Optimize the process towards HEP sensors
  - Co-design sensor and readout electronics
  - Broad adoption of development in community



- **HOW?**
  - Partner with Skywater Technologies
  - Strong support from UC, UIC, Purdue, UIUC, Cornell, for device simulation and testing
  - Engineering run with various designs
  - Testing of sensors at Fermilab and partners



Commercial Partner

- Most **advanced process** among HEP MAPS
  - Fabricated on SkyWater's **90 nm** process
  - Demonstrate domestic production for future HEP experiments

- We will work with SkyWater to modify their standard epitaxial silicon layer
  - Adapt and optimize SkyWater process to develop particle detectors
  - Use thicker, higher-resistivity epitaxy with deep-well implants on a standard CMOS substrate
  - The standard CMOS process flow can then be used to fabricate IC resulting in a monolithic sensor with integrated signal processing

HEP CMOS Sensors vs CMOS Image Sensors (CIS)

- Although similar in concept HEP CMOS sensors differ from CIS devices
  - Charge generated in HEP sensors is distributed along a particle track → no need for a transparent entrance window. As much of this charge as possible should be collected.
  - Pixels can be large: 20 – 50 μm
  - The collection region should be fully depleted if possible. We aim for ~ ns charge collection.
  - The collection well contains complex circuitry: amps, discriminators, logic…
  - Fields near the n-well limit the applied bias due to breakdown to the epi. HVCMOS can be used extend the bias voltage. This effect can also be mitigated by additional deep implants.

CMOS MAPS variants for DOE HEP

a. MAPS

b. MAPS for timing

c. LGADs

d. CMOS LGADs

e. SPADs

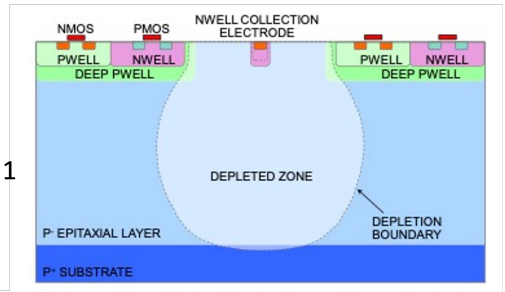
Unbiased small n-well collection electrode surrounded by deep p-wells

N-well collection electrodes with embedded CMOS

Small collection electrode with n-type “buffer” implant.

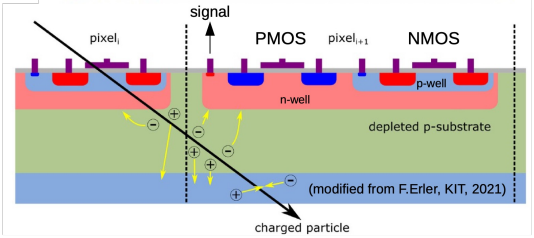
Others as well

1



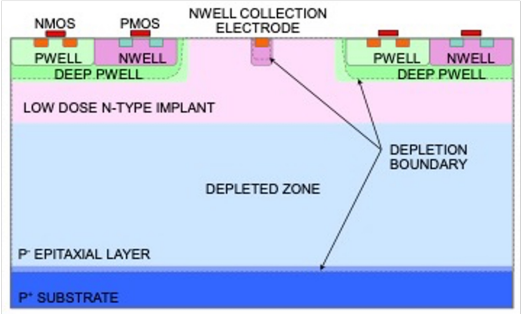
Slow speed
Low capacitance
Rad soft

2



Fast, high load capacitance

3



Fast, Low capacitance
Delicate design

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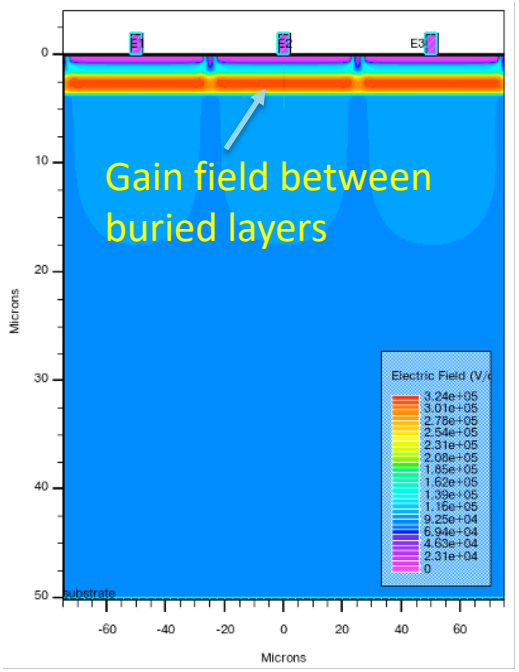
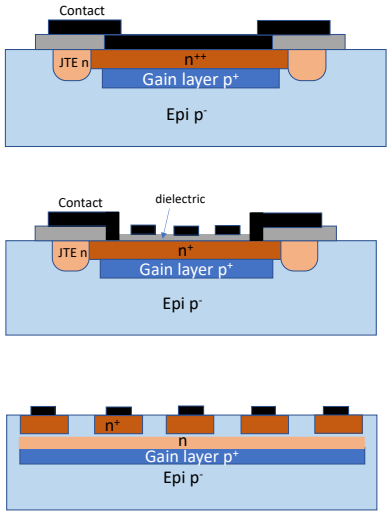
LGADs

- Low Gain avalanche diode
  - MAPS devices with linear gain
  - Deep buried junction to isolate gain field from CMOS wells
- High energy implants or graded epitaxy

Electric Field, CMOS LGAD



LGAD variants



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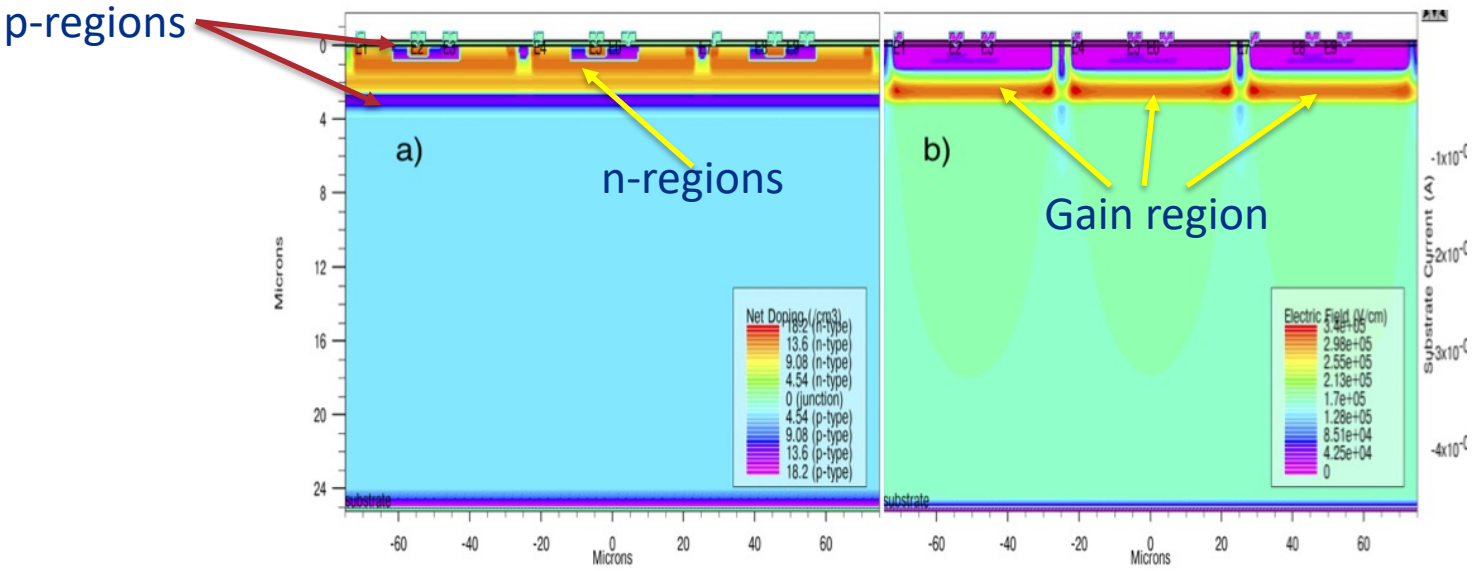
Simulations

- TCAD simulations were used to establish the feasibility of the proposed work, and we started discussions with SkyWater.
  - The initial TCAD studies for SkyWater CMOS are based on our previous work to establish designs for 8” sensor wafer production



Net doping density of the structure

Electric field profile

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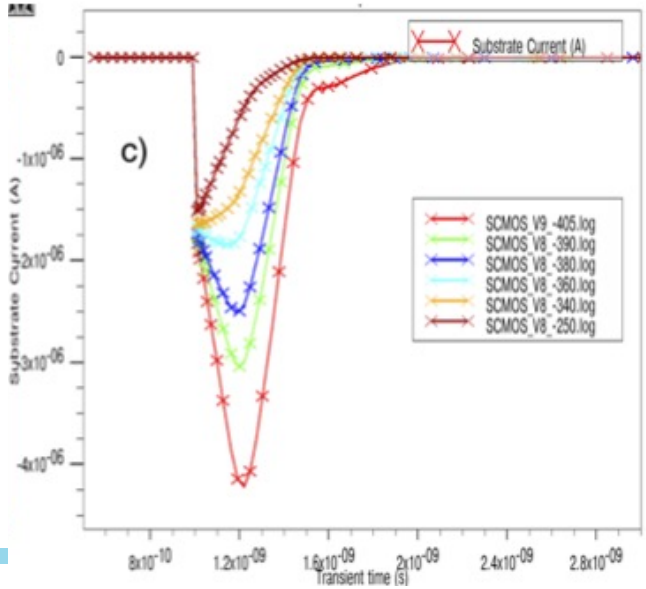
Simulations

- Depleted CMOS sensor operation can be limited by the fields in the region of the deep wells causing breakdown or affecting transistor operation.
  - Processes designed for HV operation have been studied in RD50
  - While the SkyWater 90 nm process is not an explicit HV design, it is likely compatible with the fields in fully depleted sensors
  - Can mitigate the fields near the wells with deep n-implant



- Substrate current pulses for bias voltages from 250 (brown) to 405 (red) volts showing the onset of gain.
- Rise time of the top electrodes will be determined by the details of the CMOS well capacitance

Sensor Integrated Readout Electronics

- A critical element is fast and low-power read-out electronics, whose properties must match those of the sensors
  - Investigate IC techniques and co-design basic building blocks to facilitate the readout of various sensors.
  - Basic readout circuits to extract pixelated sensor performance
  - The design will focus on the basic analog blocks with a rolling-shutter read-out of the pixel arrays.
  - This will enable the measurement of the sensor performance and characterize variations across the pixel matrix.

Project Deliverables

- Design and manufacture sensors using SkyWater's 90 nm CMOS process
- Create a HEP specific MPW run
  - Reticle divided into dies of varying designs: ½ wafer with only sensors and ½ wafer with sensors & readout circuits
  - Perform detailed characterization of MAPS, LGAD, and SPAD detectors, and quantify their performance for HEP

- Create a US-based silicon sensor manufacturing facility for next generation HEP/NP experiments
  - Enable US-teams to lead the design and fabrication of tracking detector(s) for a future Higgs factory
  - Enable a **broad participation of university groups** in cutting edge instrumentation

Summary

- Establish a US based CMOS manufacturing process
  - Target applications are FCC_{ee} and other HEP and NP experiments that require low-mass, high-speed, precise charged particle tracking.
- Lays the foundation of CMOS sensor manufacturing in the Unites States
  - A stepping stone for the domestic fabrication of the next generation of tracking sensors
- Integration with the ongoing international efforts within DRD3 and DRD5 efforts
  - Development of **tracker** and **calorimeter** designs for the **Higgs factories**