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NAPA-p1: Nanosecond Timing Pixel for Large Area Sensors

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SLAC NATIONAL ACCELERATOR LABORATORY

OREGON

Stanford University | U.S. DEPARTMENT OF ENERGY

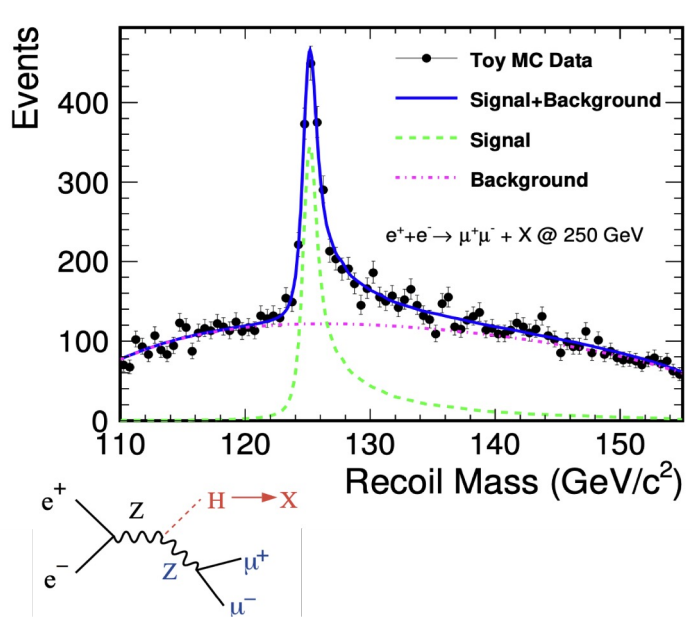
Presentation Outline

- Application: Future e+e- Colliders
- Target Specifications Vs State of the Art
- SLAC Development: NAPA_p1
- Going Towards a Large Area Sensor
- Conclusion & Perspectives

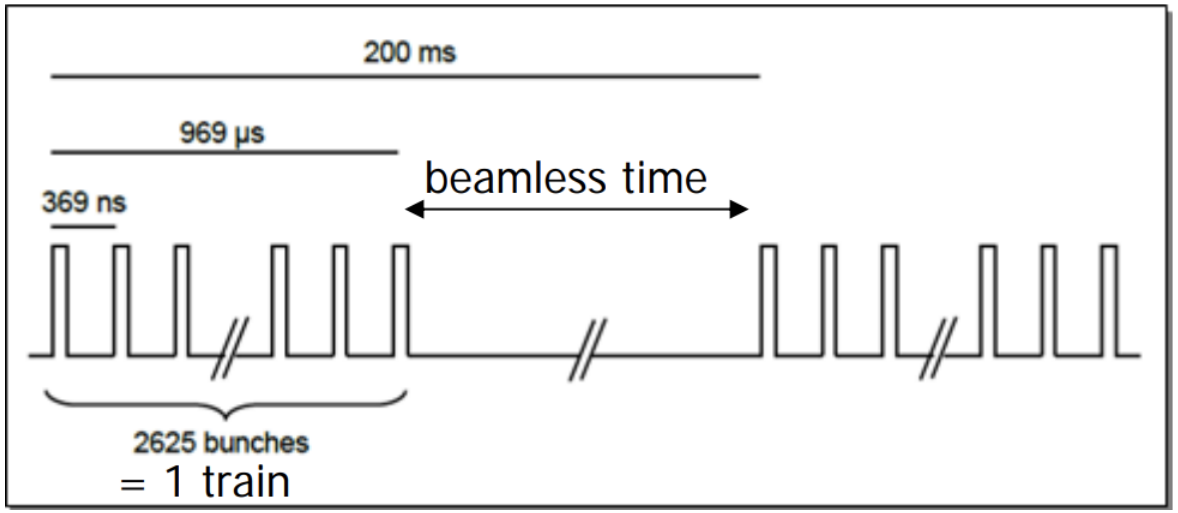
Future Linear e+e- Colliders

Designed to work ad Higgs Factory driving the requiring for detectors:

- Material budget <0.3% X_0
- Gas cooling → Very low average power consumption
- Spatial resolution: 5 μm
- Time-tagging in the order of O(1ns)

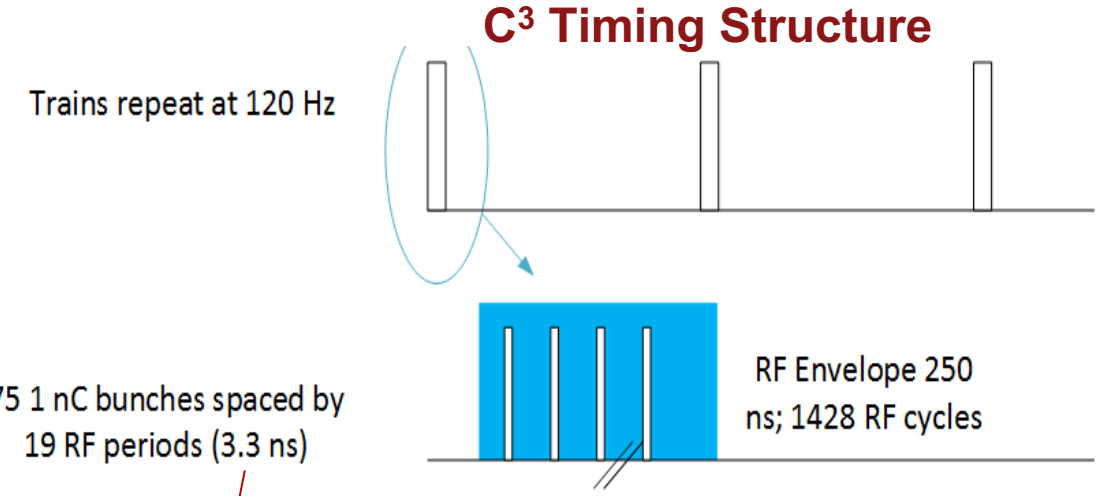


ILC Timing Structure



Duty Cycle = 0.48%

C³ Timing Structure



Duty Cycle = 0.03 %

~1 ns time resolution is needed

Specifications from Physics to Pixel

Specification	Physics	Pixel
Input charge	Minimum Ionizing Particle (MIP)	Assuming epitaxial layer of ~ 10 µm MIP goes through pixel center generates ~ 600 e- MIP shared between 4 pixels → ~ 150 e-
Noise	Negligeable fake hits	Noise < $\frac{Min\ Input\ Charge}{5}$ → ENC < 30 e-rms
Time resolution	Identity bunches within a train (C^3)	Time resolution < 1 ns-rms for whole chain considering : sensor, front-end, time walk, TDC
Average Power Consumption	Gas cooling	Depends on detector total area, used gas, and allowed increased in temperature. Initial estimation to be confirmed 20 mW/cm^2
Spatial resolution	~ 5 µm	Pixel pitch 25 µm

These initial specifications serve as a baseline for the first prototype developed at SLAC : NAPA-p1

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Target Specs Vs State of the Art

Chip name	Technology	Pixel pitch [µm]	Pixel shape	Time resolution [ns]	Power Density [mW/cm^2]
Target Specification	**?**	**≤ 25 x 100**	**Sq / rect**	**1**	**< 20**
ALPIDE [2][3]	Tower 180 nm	28	Square	< 2000	5
FastPix [4][5]	Tower 180 nm	10 - 20	Hexagonal	0.122 – 0.135	>1500
DPTS[6]	Tower 65 nm	15	Square	6.3	112
Cactus [7]	LF 150 nm	1000	Square	0.1-0.5	145
MiniCactus [8]	LF 150 nm	1000	Square	0.088	300
Monolith [9][10]	IHP SiGe 130 nm	100	Hexagonal	0.077 – 0.02	40 - 2700

No design fulfills all target specification ➔ The need to develop a custom design

We decided to go with the Tower 65nm technology, which has been optimized by CERN WP1.2 to have low sensor capacitance allowing very good performance with low power consumption.
+ it has the possibility of a wafer-scale stitched sensor
+ it has been proven to be radiation tolerant

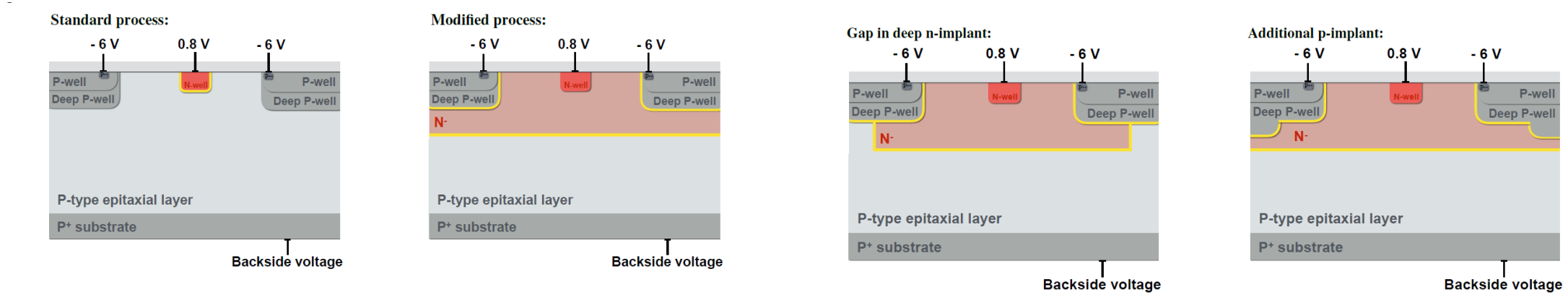
Tower Semiconductor 65 nm Imaging technology

Thanks to CERN WP1.2 effort on sensor optimization in TowerSemi 180 nm and 65 nm technologies [12] [13]

- ➔ C_{sensor} of 2-3 fF is achievable while maintaining high collection efficiency.

This is very useful from a pixel performance point of view as:

For a constant SNR and Q_{in}➔ $Power \propto (C_{sensor})^m \ \ with\ 2 \leq m \leq 4$ as shown in [11]



Sensor optimization in TowerSemi 180 nm process from [12] and [13]

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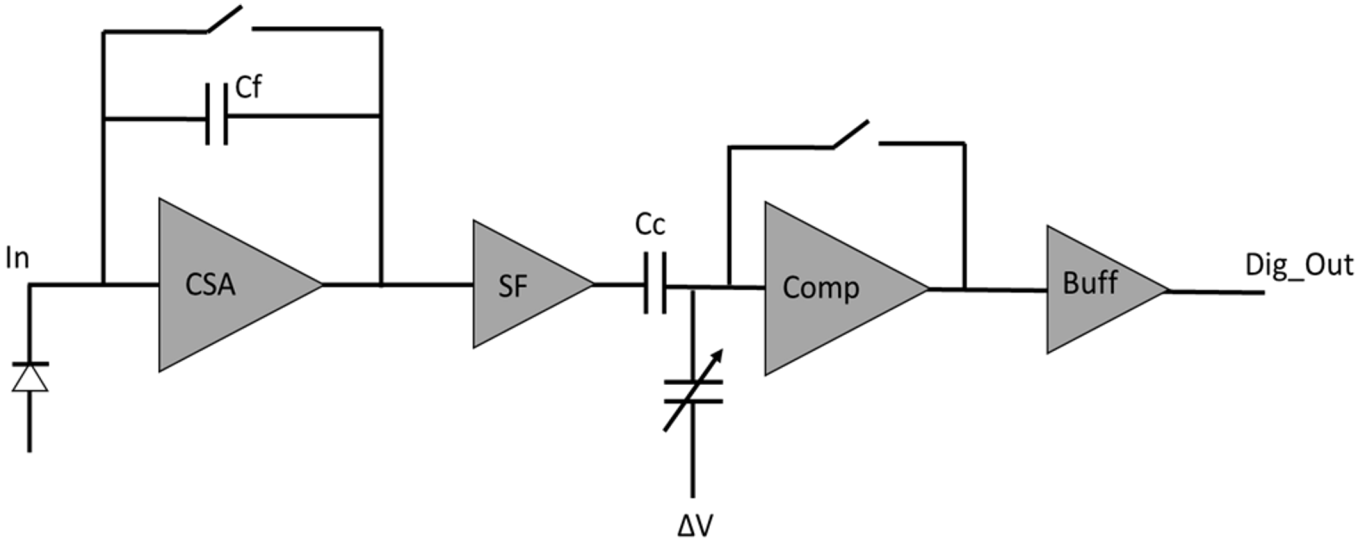
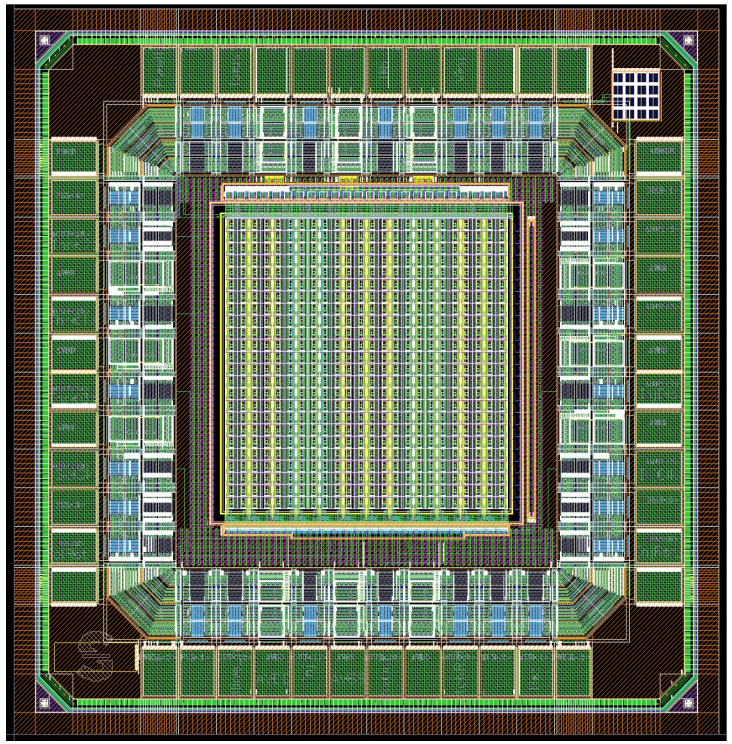
NAPA_p1: **NA**nosecond **P**ixel for large **A**rea sensors – **P**rototype **1**

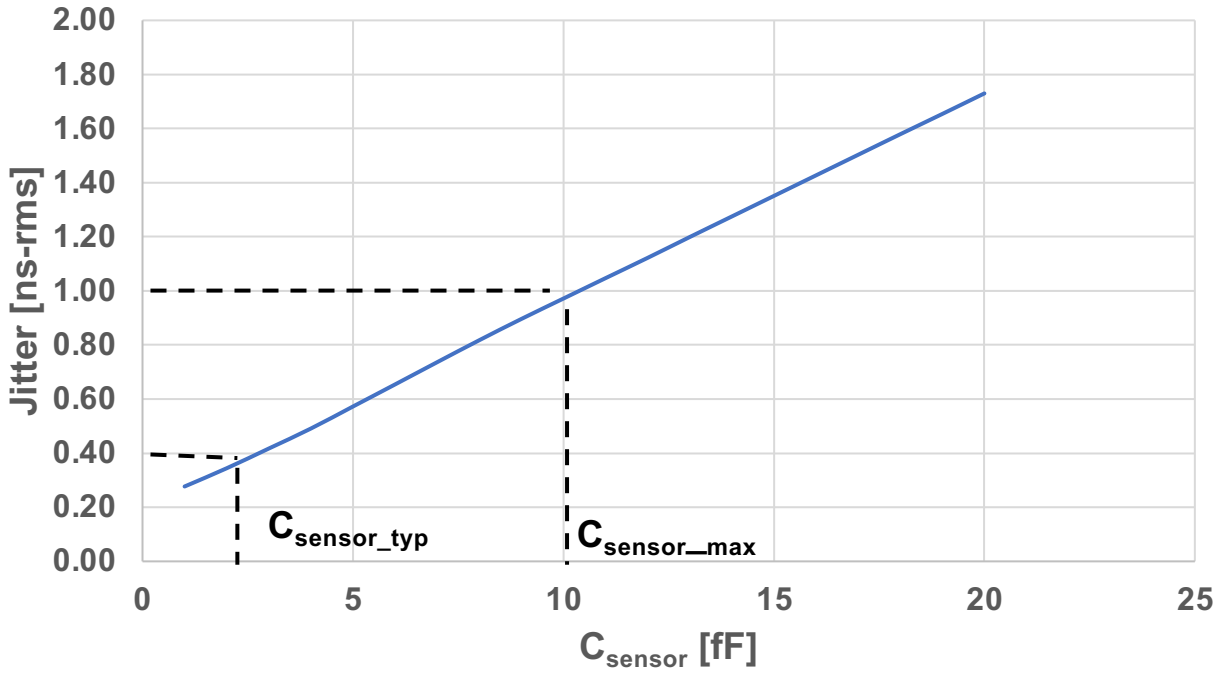
- The prototype design submitted with a total area 5 mm x 5 mm and a pixel of 25 µm × 25 µm, to serve as a baseline for sensor and pixel performance.
- Design motivation ➔ Synchronous architecture (known beam time structure), Correlated Double Sampling, eliminating low frequency noise, allowing use of minimum size transistors
- Power pulsing → reduce average power consumption by more than 100

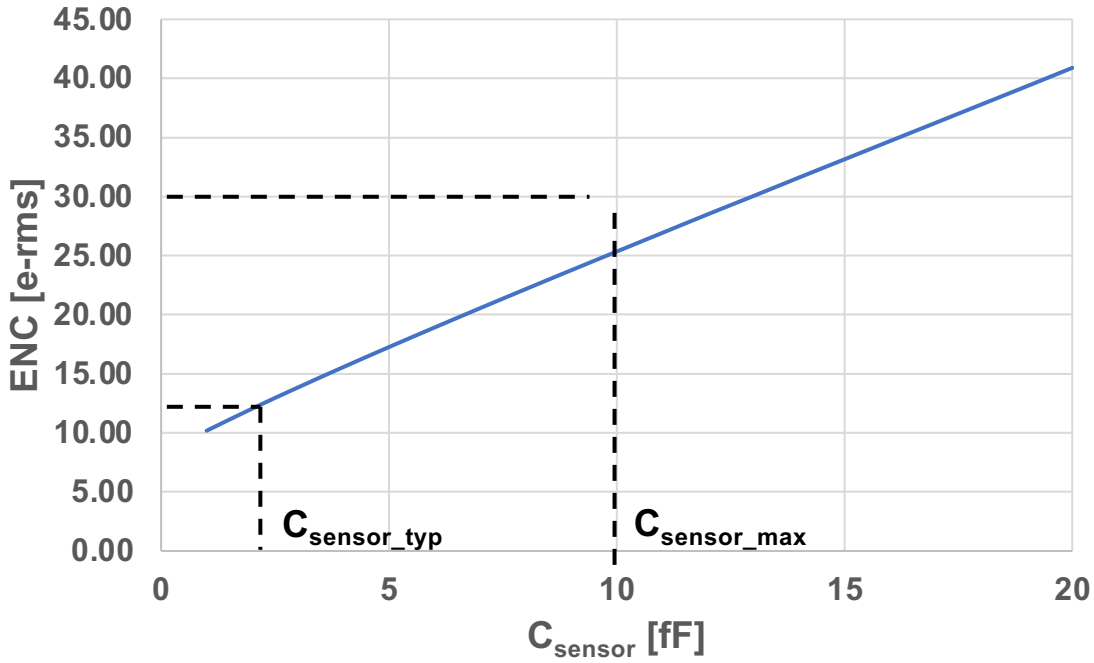




Layout of MAPS SLAC prototype for WP1.2 shared submission

Simulation of Jitter and ENC as a Function of C_{sensor}



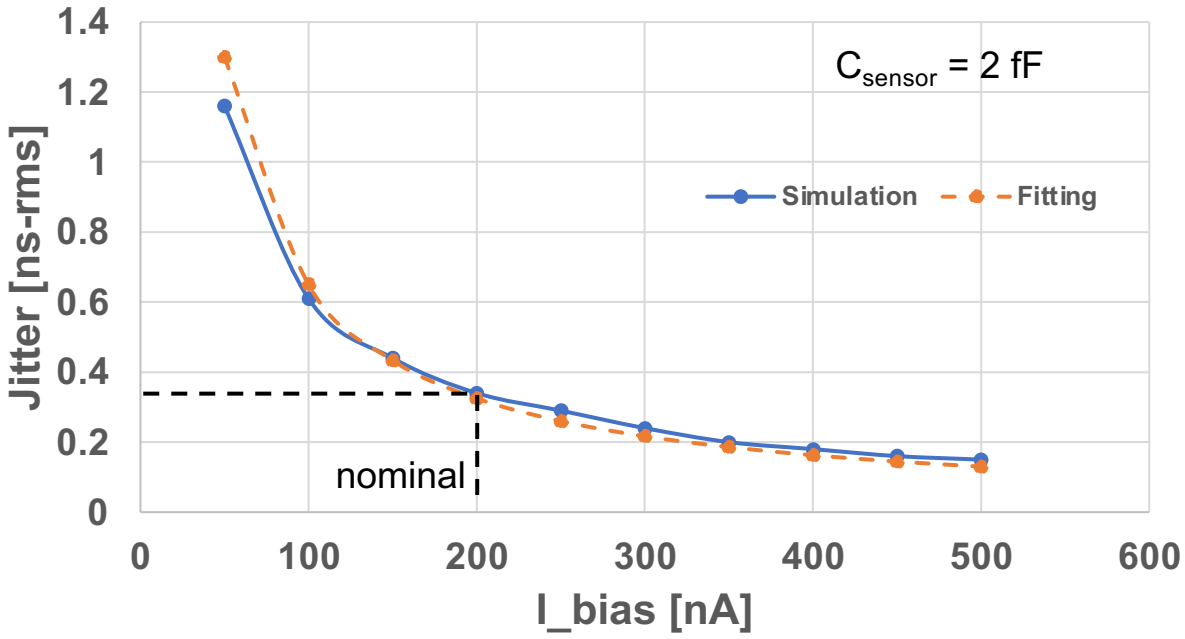


jitter = 400 ps for $C_{sensor\_typ} \approx 2$ fF → **Ok for Specs** ← **ENC = 13 e-rms for $C_{sensor\_typ} \approx 2$ fF**

These simulations are with a nominal pixel current of 600 nA ➔ <Power density> = 115 mW/cm² x duty cycle
For e+e- machines such as ILC and C³, duty cycle is expected < 1%

Simulation Results : Jitter and Time Walk

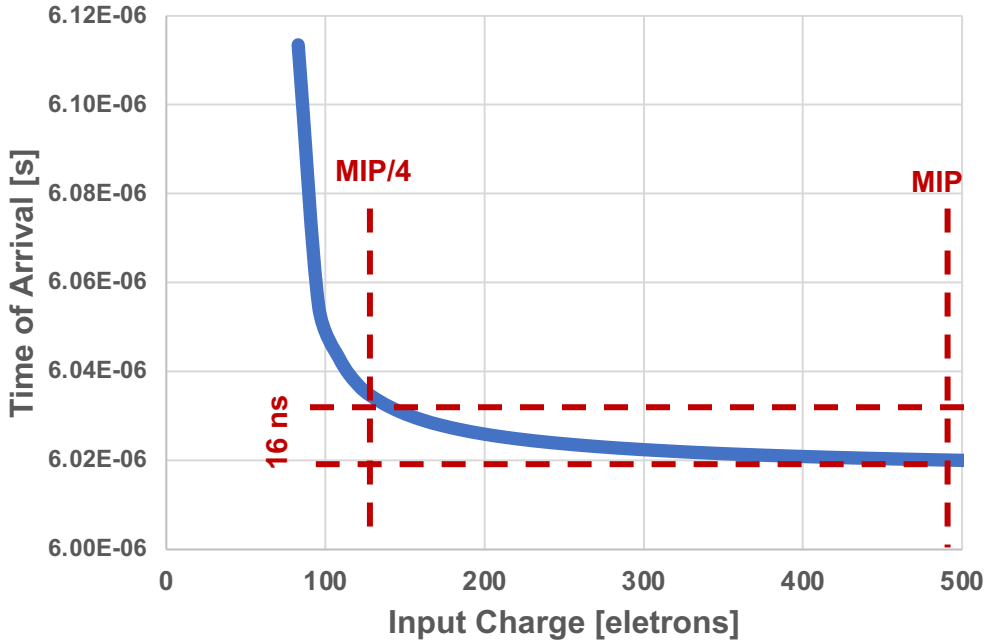
Jitter



I_bias = 200 nA ≡ pixel current = 600 nA

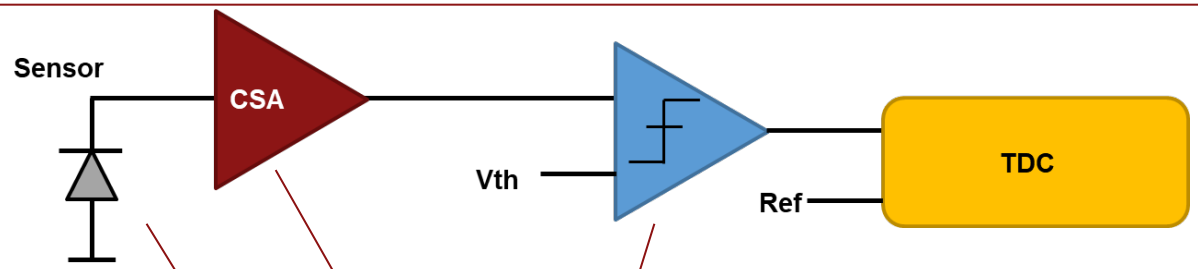
From theory we expect : $\sigma_{FE} \propto \frac{1}{(Power)^{\frac{1}{n}}}$ with $1 \leq n \leq 2$

Time Walk



Time walk for MIP → MIP/4 = 16 ns
Not negligeable and must be corrected
(in pixel? In balcony? Offline? TBD)

Timing Limits for a Complete Detection Chain



$$\sigma^2_{Total} = \sigma^2_{TOA} + \sigma^2_{FE} + \sigma^2_{Timewalk} + \sigma^2_{TDC}$$

σ_{TOA} < 150 ps-rms
For small optimized pixels based on literature

σ_{FE} < 400 ps-rms for < 1 µW/pixel

Can be corrected if we measure the ToT inside the pixel

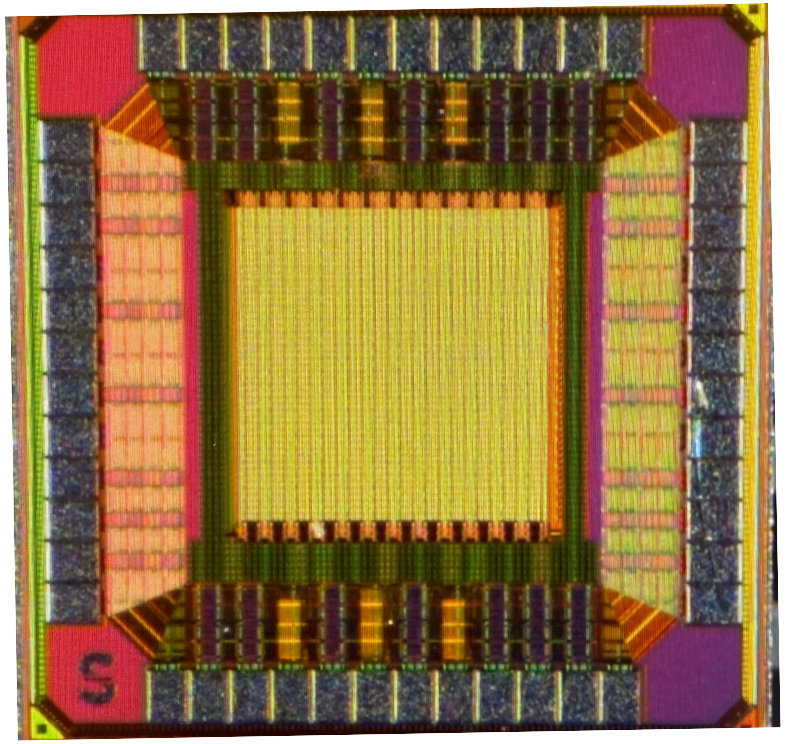
σ_{TDC} < 150 ps-rms
Limited by quantization noise

Assuming time walk is fully corrected ➔σ_{Total}~500 ps-rms with reasonable pixel power consumption, going lower will cost increasingly more power, not compatible with large area sensors
Accounting for residual time Walk after correction, and other non-idealities, it is reasonable to aim for ~1 ns-rms time resolution

Summary of NAPA-p1 Performance

	Specification	Simulated NAPA-p1
Time resolution	1 ns-rms	0.4 ns-rms ✓
Spatial Resolution	7 µm	7 um ✓
Noise	< 30 e-rms	13 e-rms ✓
Minimum Threshold	200 e-	~ 80 e- ✓
Average Power density	< 20 mW/cm^2	0.1 mW/cm^2 for 1% duty cucle ✓

The chip was received at SLAC in September 2023

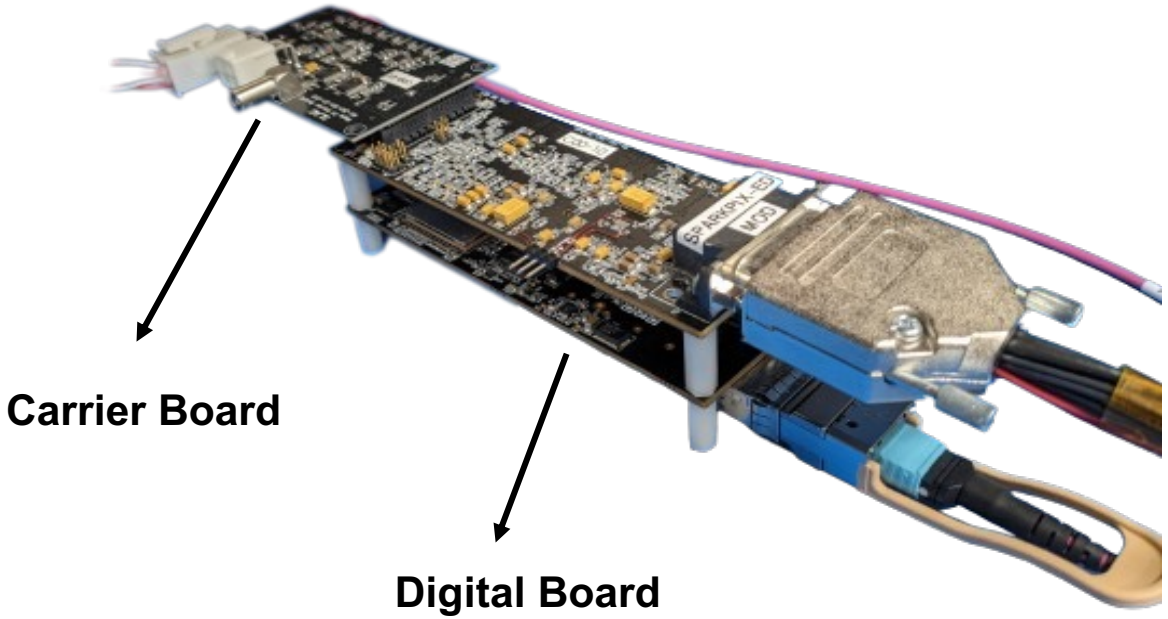


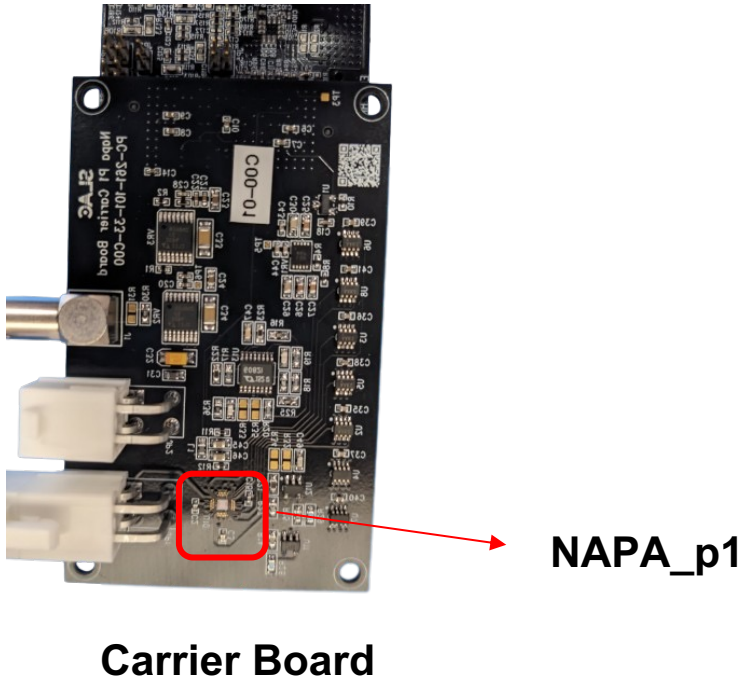
Microscope photo of NAPA-p1

Acknowledgement: to CERN WP 1.2 for the excellent cooperation: NAPA-p1 uses the pixel masked developed and optimized by CERN, and was fabricated in a shared run led by CERN

Test Setup for NAPA-p1

- A custom carrier was designed at SLAC for the NAPA-p1 chip providing all analog references
- The chip was wire-bonded at SLAC
- The carrier board connects to a digital board containing an FPGA and several DAC's

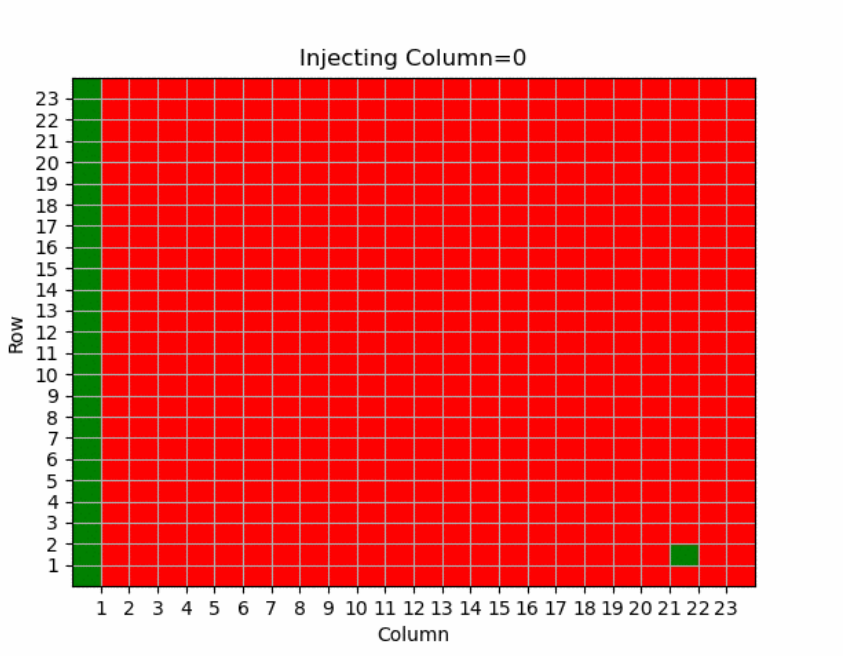




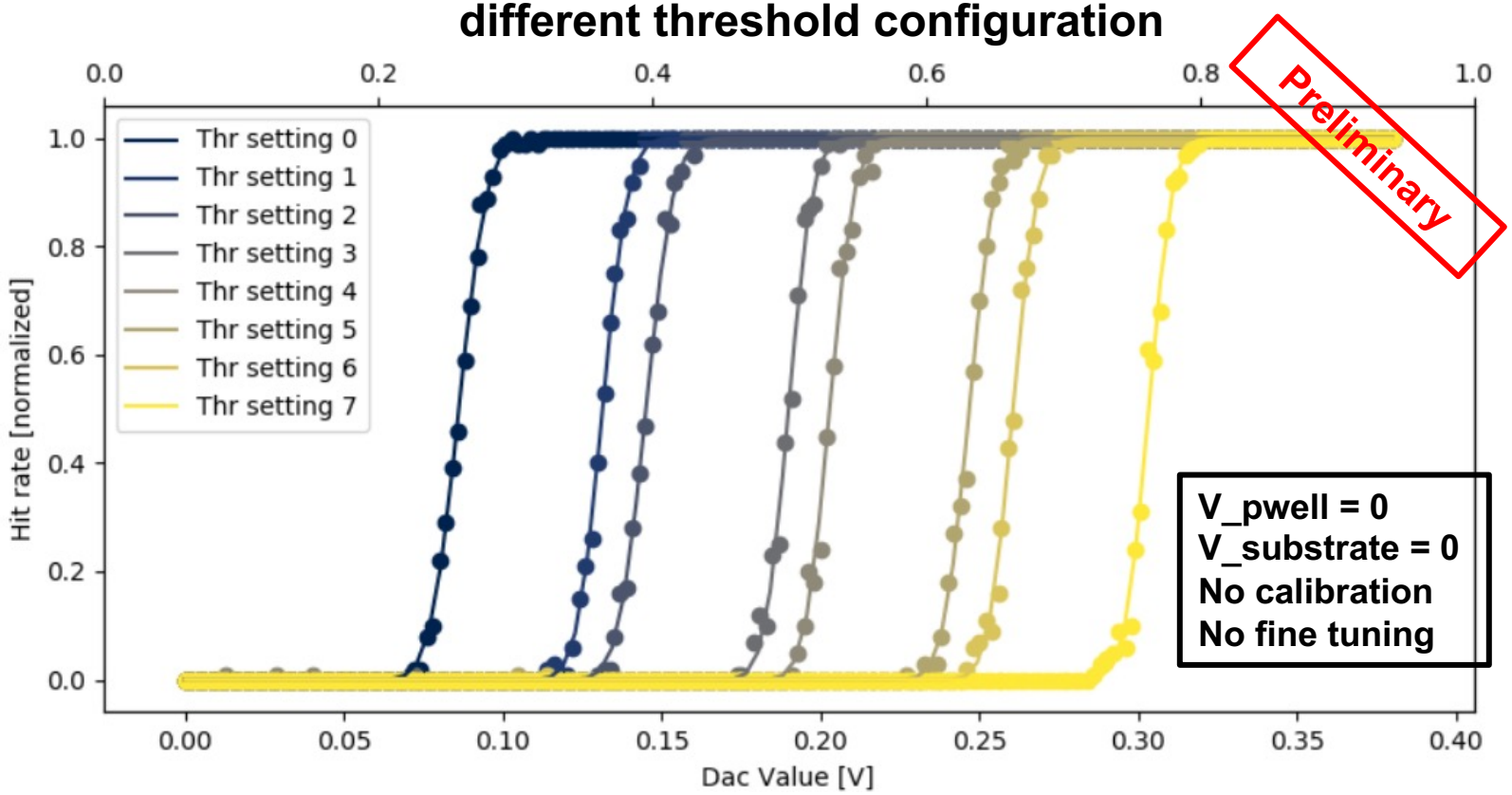
Preliminary Characterization Results

Functional Testing

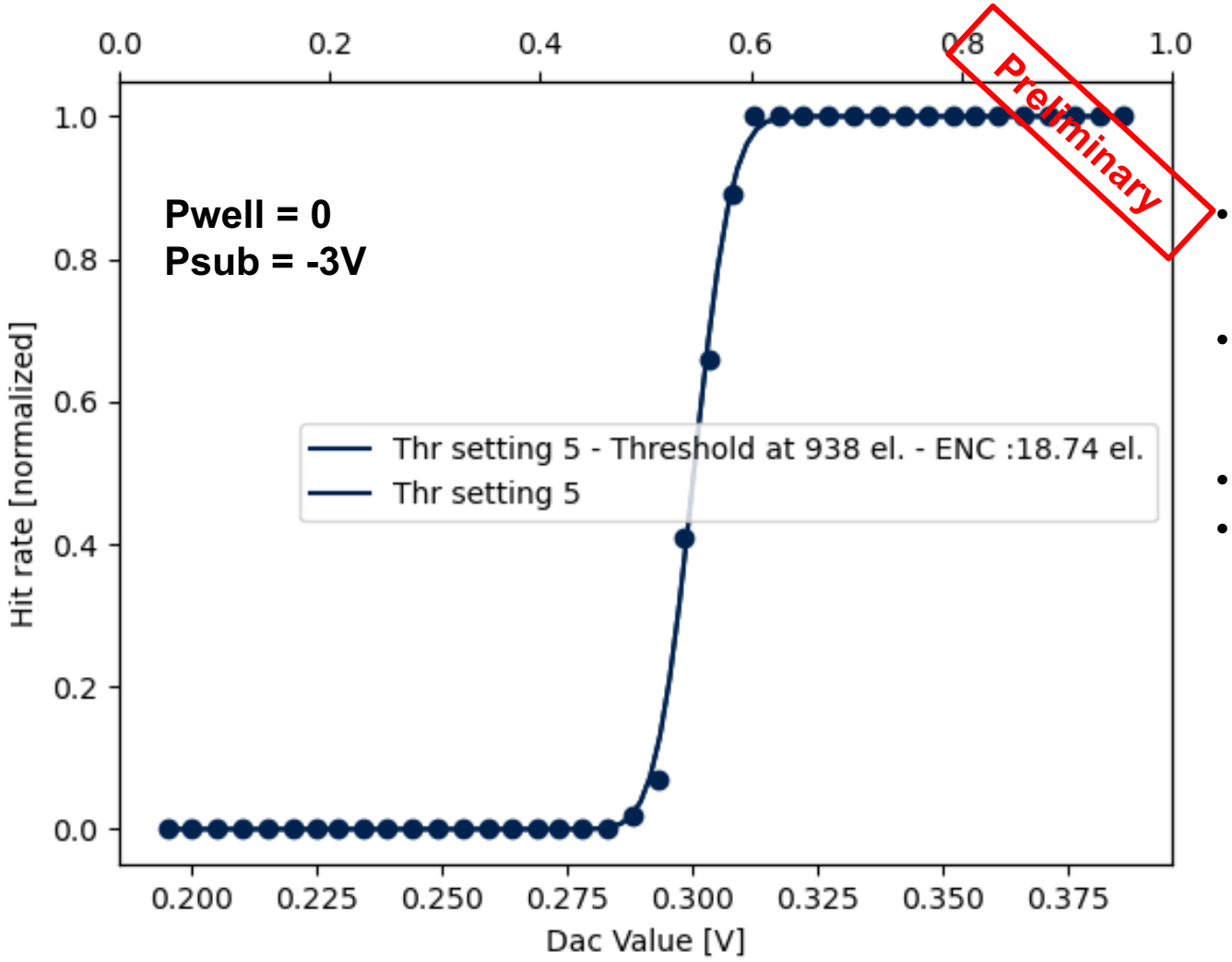
Columns Scan



Injection charge scan across different threshold configuration



ENC measurement



- **Injection cap not calibrated yet. A Laser setup is needed for that. Design value is used for C_{inj}**
- **ENC value is close to simulation ~ 13 e-rms for C_{sensor} = 2 fF**
- **ENC value satisfies the specification < 30 e-rms**
- **More measurements to be available soon**

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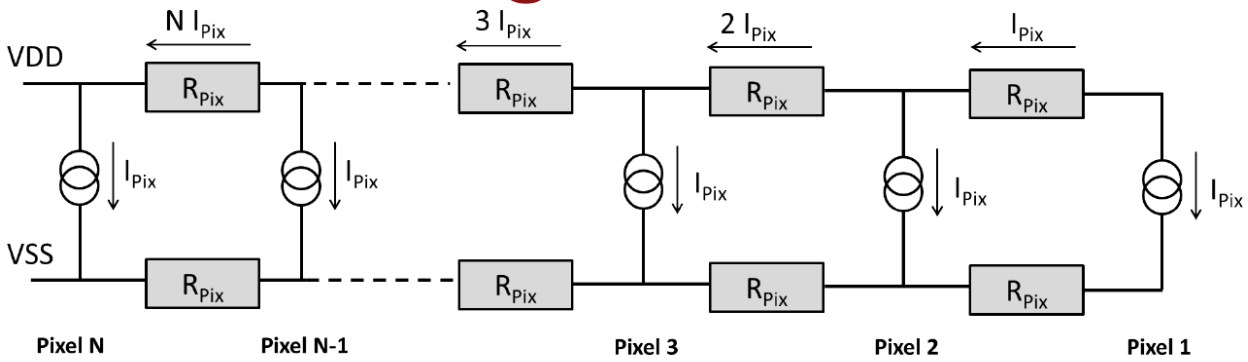
Going Towards a Large Sensor → Challenge

$$\Delta V = I_{pix} \times R_{Pix} + 2 \times I_{Pix} \times R_{Pix} + 3 I_{Pix} \times R_{Pix} + ... + N \times I_{Pix} \times R_{Pix}$$
$$\Delta V = I_{Pix} \times R_{Pix}(1 + 2 + 3 + ... + N)$$
$$\Delta V = I_{Pix} \times R_{Pix} \times \frac{N(N+1)}{2}$$



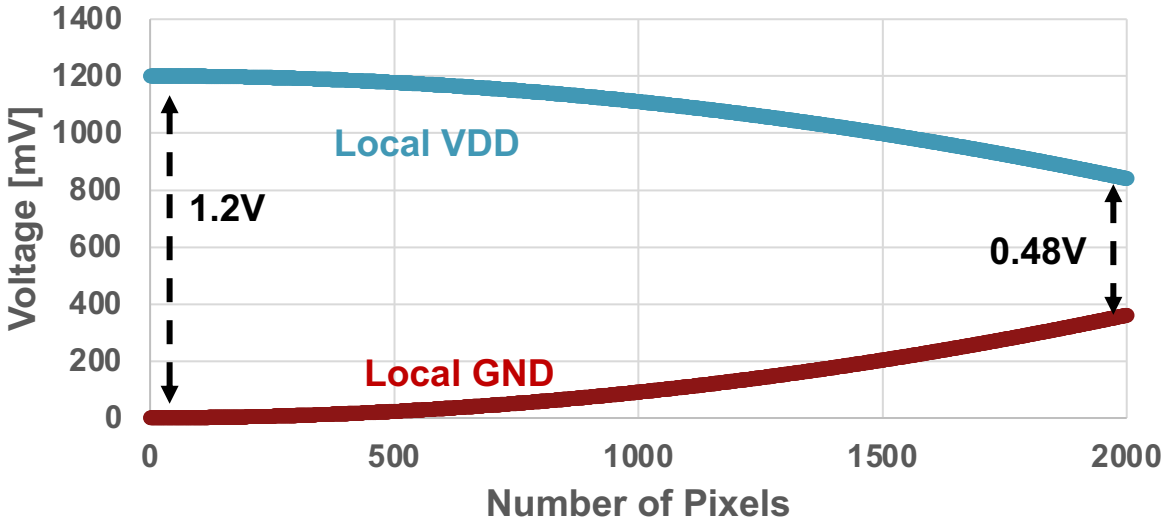
Assuming :I_{pix} = 600 nA and R_{pix} = 300 mΩ

Assuming pixel of 25 μm x 25 μm

A column of 10 cm would have 4000 pixels

Double sided powering

➔ max drop length = 2000 pixels



VDD-GND goes from 1.2 V near the power pads down to around 480 mV after 2000 pixels

The main limitation comes from large scale power distribution rather than cooling constraints

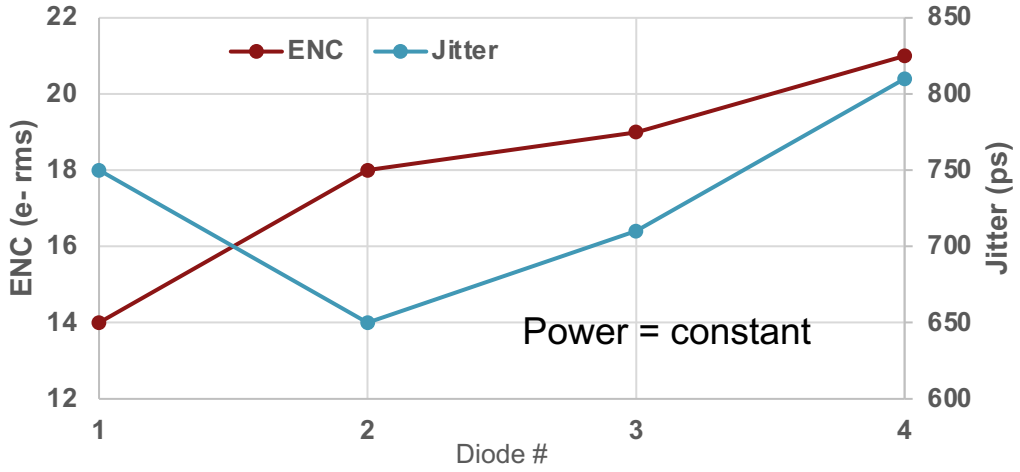
After 10^3 pixels (reticle, 2.5 cm), $V_{drop} \approx 0.1$ V
After 4 x 10^3 pixels (sensor, 10cm), $V_{drop} = 1.5$V !

Going Towards a Large Sensor → Solutions

Potential solutions to address the power distribution over a large scale:

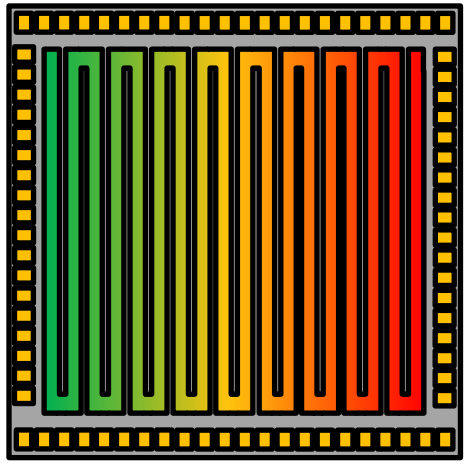
1. Decrease power density➔ Physics requirement are for a pixel of 25 µm x 100 µm. Our initial study shows that a pixel of 25 µm x 50 µm gives the best optimization for $\frac{Performance}{Power\ Density}$
2. Reduce R_{pix} ➔ Redesign of power grid
3. Keep power constant ➔ Switch from a single ended to a differential comparator
4. Reduce the column length ➔ Target sensor of 5 cm x 20 cm instead of 10 cm x 10 cm
5. Backup plan: develop capless LDO regulator ➔ ongoing shared effort with CERN WP1.2
6. ➔ NAPA-p2 design has started to tackle these challenges

Pixel Pitch vs. Performance



Simulation by Jacob Sillman

Potential Configuration of NAPA-p2



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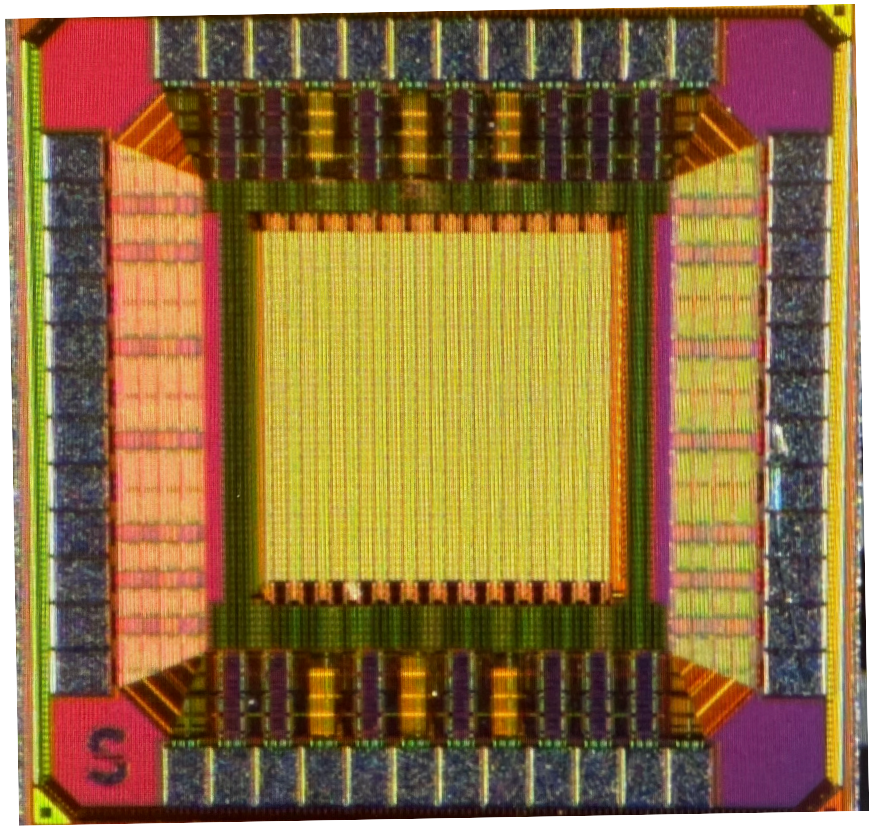
Conclusion & Perspectives

- **MAPS has great a potential to fit the future e+e- colliders requirements (tracker, calorimeter)**
- **Simulations of NAPA_p1 show that it is possible to achieve a time resolution ~ 1 ns-rms with reasonably low power consumption of ~100 mW/cm^2 × Duty Cycle. For e+e- machines duty cycles are typically < 1%**
- **We've just received the NAPA-p1 chip and the first characterization results are promising. NAPA-p1 will serve as a pixel proof of concept.**
- **Design of NAPA-p2 has started to tackle large sensor challenges. NAPA-p2 will serve as a system proof of concept.**
- **These prototypes are customized for linear lepton colliders with low duty cycle, however, many of the developed technical solutions can be of value to other applications (large area stitched sensor with increased yield, power distribution, IP blocks (capless LDO regulator, TDC,…)**



Microscope photo of NAPA-p1

Thank You For Your Attention!

References

[1] Brau JE, Breidenbach M, Habib A, Rota L, Vernieri C. The SiD Digital ECal Based on Monolithic Active Pixel Sensors. *Instruments*. 2022; 6(4):51. https://doi.org/10.3390/instruments6040051

[2] Gianluca Aglieri Rinella, "The ALPIDE pixel sensor chip for the upgrade of the ALICE Inner Tracking System, Nuclear Instruments and Methods in Physics Research, Volume 845,2017, https://doi.org/10.1016/j.nima.2016.05.016

[3] M. Mager, "ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITS upgrade", Nuclear Instruments and Methods in Physics Research, Volume 824, 2016, https://doi.org/10.1016/j.nima.2015.09.057

[4] T. Kugathasan *et al.,* "Monolithic CMOS sensors for sub-nanosecond timing", Nuclear Instruments and Methods in Physics Research, Volume 979, 2020, https://doi.org/10.1016/j.nima.2020.164461.

[5] J. Braach et al., "Performance of the FASTPIX Sub-Nanosecond CMOS Pixel Sensor Demonstrator", *Instruments* 2022, *6*(1), 13; https://doi.org/10.3390/instruments6010013

[6] G.A. Rinella *et al.* "Digital Pixel Test Structures implemented in a 65 nm CMOS process" https://doi.org/10.48550/arXiv.2212.08621

[7] Y. Degerli *et al* 2020 *JINST* 15 P06011 DOI 10.1088/1748-0221/15/06/P06011

[8] Y. Degerli *et al., "*MiniCACTUS: Sub-100 ps timing with depleted MAPS", Nuclear Instruments and Methods in Physics Research, Volume 1039, 2022, https://doi.org/10.1016/j.nima.2022.167022.

[9] S. Zambito *et al* 2023 *JINST* 18 P03047 DOI 10.1088/1748-0221/18/03/P03047

[10] L. Paolozzi "A Picosecond Avalanche Detector in SiGe BiCMOS' ULITIMA Conference 2023

[11] W. Snoeys, *Monolithic Pixel Detectors for High Energy Physics,* Nuclear Instruments and Methods in Physics Research A 731 (2013) 125–130

[12] M. van Rijnbach et al*., Radiation hardness and timing performance in MALTA monolithic pixel sensors in TowerJazz 180 nm*, 2022 *JINST* C04034

[13] M. Munker et al., *Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance,*2019 *JINST* 14C05013