Photon-to-Digital Converters: Among Steps Towards the Kilotonne Scale 0νββ Detector

S. A. Charlebois[1], S. Martel[2], L. Fabris[4], F. Retière[3], J.-F. Pratte[1]

1. Université de Sherbrooke, Sherbrooke, QC J1K 2R1, Canada
2. Teledyne DALSA Semiconductor, Bromont, QC J2L 1S7, Canada
3. TRIUMF, Vancouver, BC V6T 2A3, Canada
4. Oak Ridge National Laboratory, Oak Ridge, TN 37771, USA

3IT Institut interdisciplinaire d'innovation technologique UdS

TRIUMF

TELEDYNE DALSA Everywhereyoulook™

OAK RIDGE National Laboratory

Fraunhofer IZM

BERKELEY LAB Lawrence Berkeley National Laboratory

UdS Université de Sherbrooke

Sherbrooke: A team's work

UdS

Université de Sherbrooke

Jean-François Pratte
Serge Charlebois
Artur Turala
Frédéric Nolet
Frédéric Vachon
Gabriel Lessard
Guillaume Théberge-Dupuis
Jeanne Morehead
Jérémy Chenard
Jérôme Deshaies
Keven Deslandes
Nicolas Roy
Philippe Arsenault
Philippe Martel-Dion
Raffaele Aaron Giampaolo
Robin Scarpellini
Samuel Parent
Sean Prentice
Simon Carrier
Tommy Rossignol
Olivier Lepage
Yves-Alexandre Beebe

IZM Fraunhofer

Kai Zoschke
Thomas Fritzsch

Collaborators

Fabrice Retiere (TRIUMF)
Lorenzo Fabris (ORNL)
Stéphane Martel (TDSI)
Simon Viel (Carleton)
Peter Dennes (LBNL)
Craig Tindall (LBNL)
nEXO Collaboration
nEXO Canada

serge.charlebois@usherbrooke.ca

Building Scientific Instruments for…

- Scintillating crystal-based systems
  - Positron Emission Tomography
  - Computed Tomography
  - Neutron Imaging

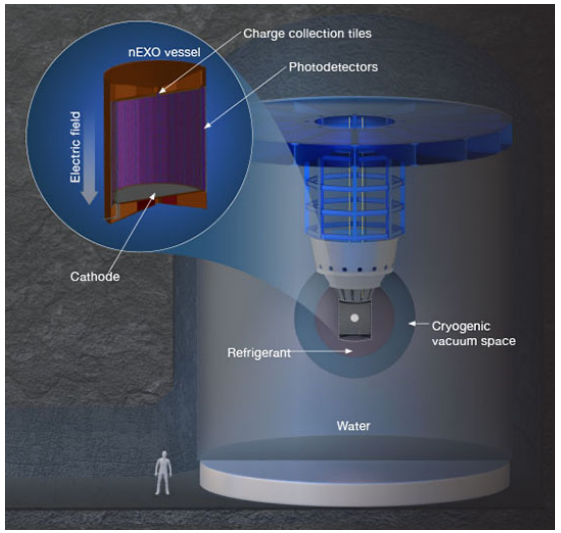
} Precise single-photon timing resolution } Visible spectrum

Mid-sized Animal LabPET II

- Noble liquid experiments (Argon and Xenon)
  - Dark matter search
  - Neutrino physics

} Large area detector (~m^2) → Low power } VUV sensitivity

5 to 100s m^2 of detector area!



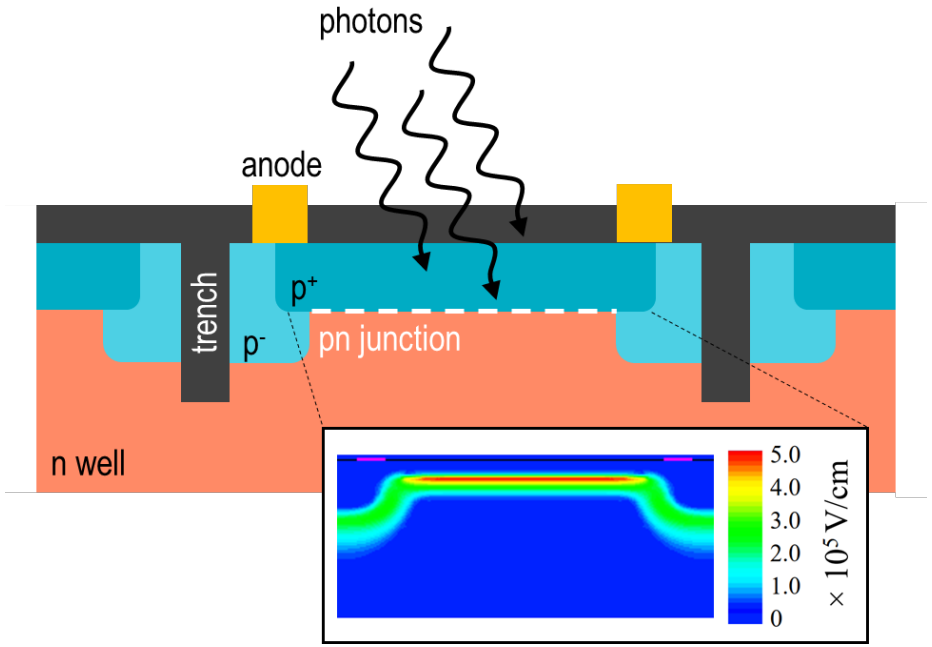
The nEXO time projection chamber (top left inset) allows measurement of energy and location of double beta decays.
https://nexo.llnl.gov

serge.charlebois@usherbrooke.ca

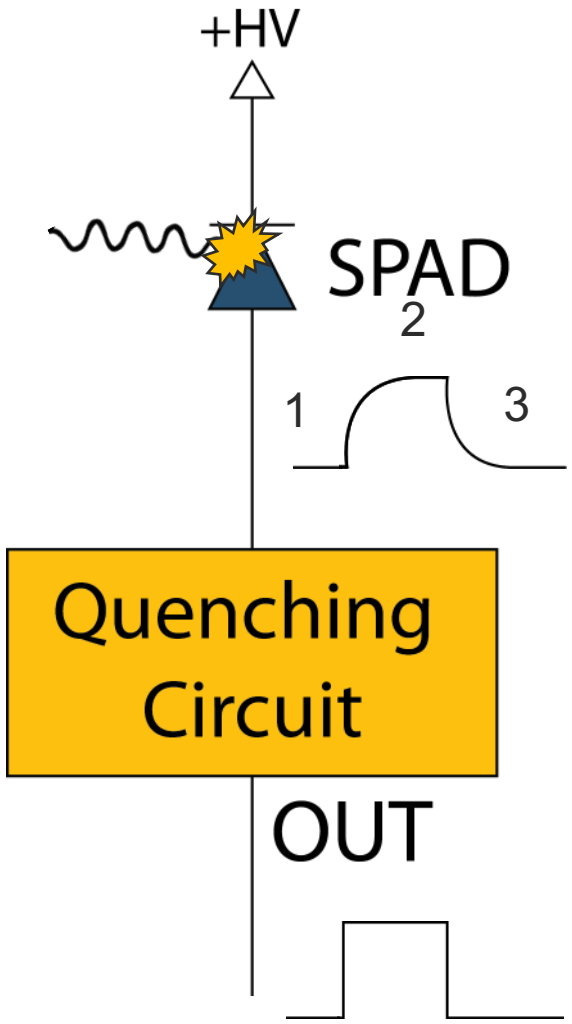
Single photon avalanche diode (SPAD)

UDS

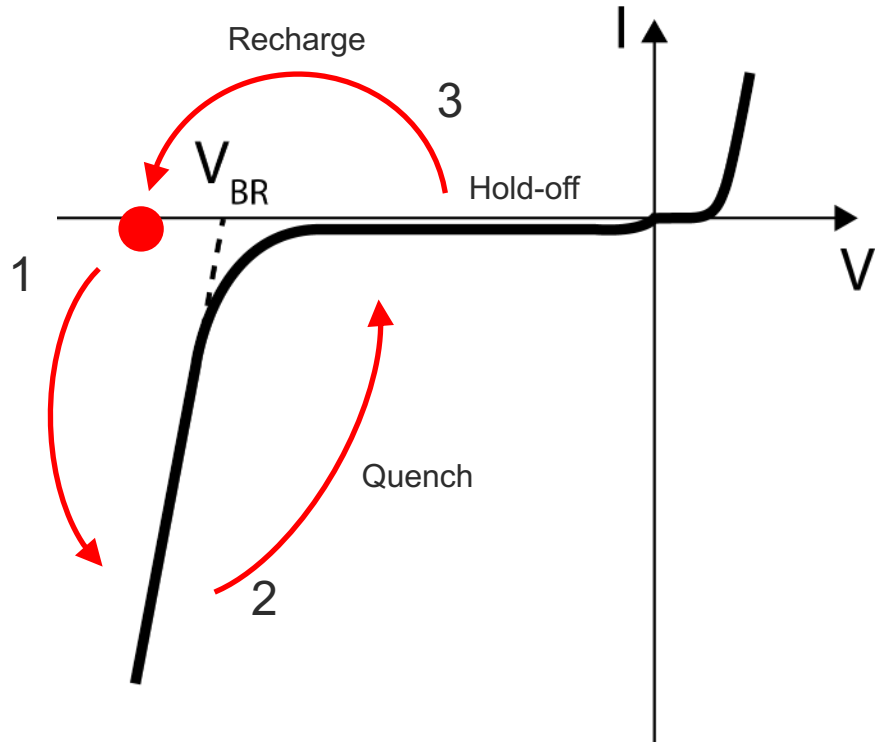
SPAD cross-section



Schematic circuit



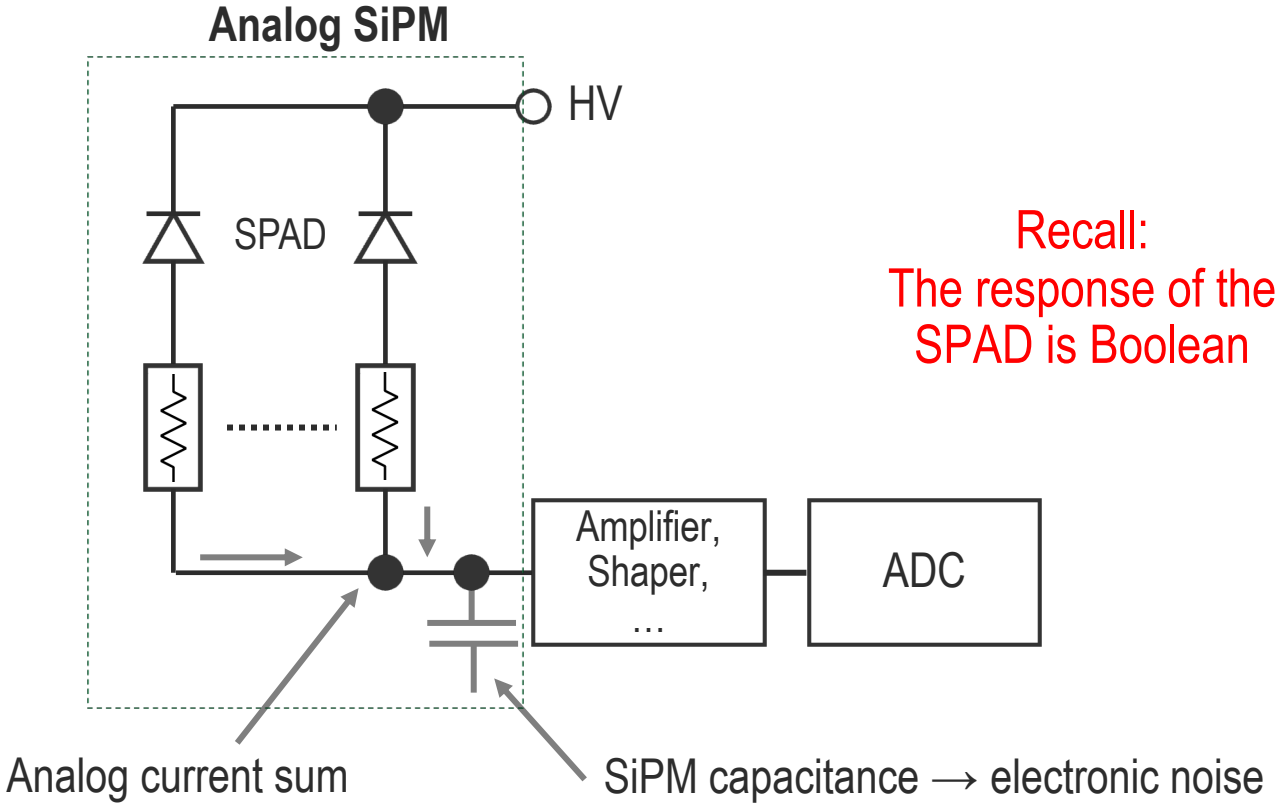
SPAD I-V curve



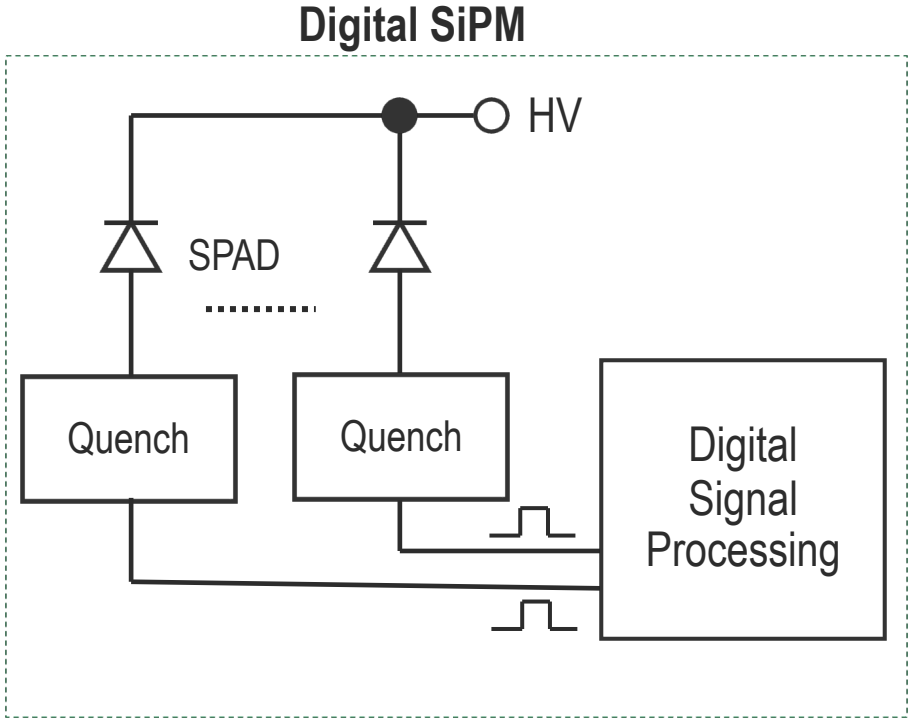
The response of the SPAD is Boolean: either **idle** or **triggered**

serge.charlebois@usherbrooke.ca

SiPM – Silicon Photo Multiplier: an array of SPADs



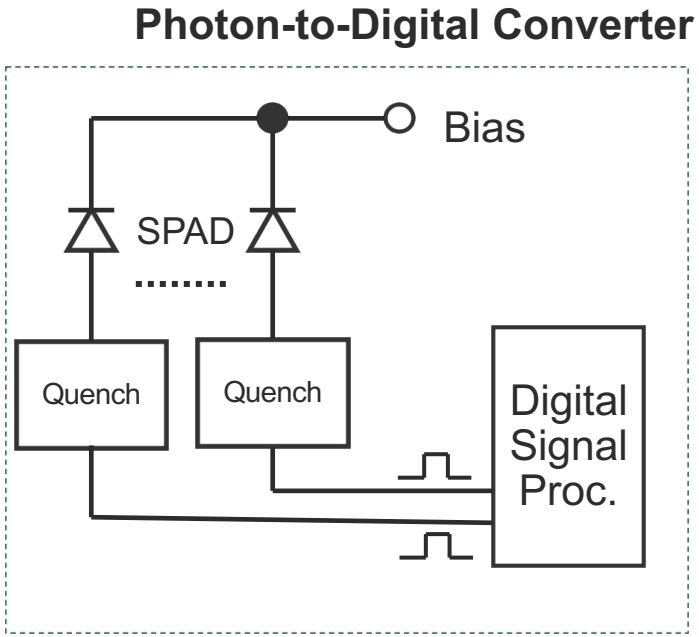
Recall:
The response of the SPAD is Boolean



The amplifier transforms charge into voltage and then BACK to digital.

Individual SPAD readout, no D/A+A/D conversion. Everything stays digital.

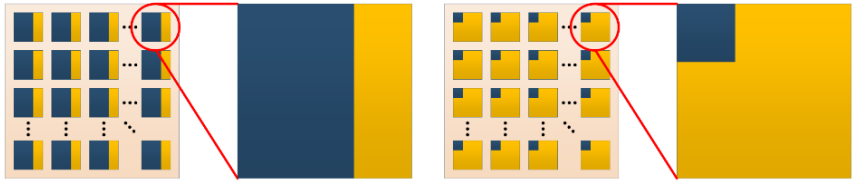
- **Digitally readout array of Single Photon Avalanche Diode (SPAD)**



- Direct digital conversion:
  - Single photon resolution on the whole dynamic range
  - Lower power consumption
- Disabling noisy SPADs: reducing noise
- Programmable hold-off delay: mitigation of afterpulsing
- Embedded signal processing: sum, dark count filters, time-to-digital conversion, etc.

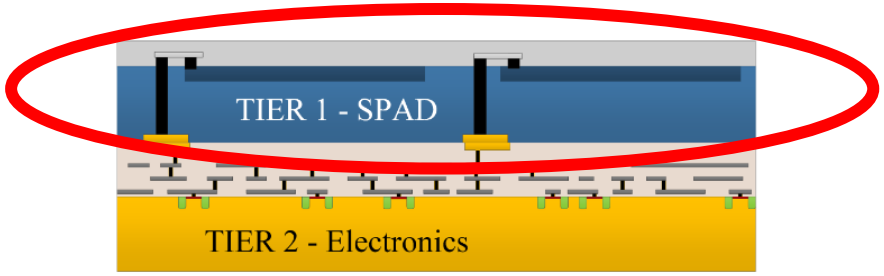
Pratte JF et al. "3D Photon-to-Digital Converter for Radiation Instrumentation: Motivation and Future Works" (2021) Sensors;21(2):598. doi: 10.3390/s21020598

- **SPAD array and CMOS readout vertically stacked (3D) to form a single detector chip**



in 2D: loosing sensitive area

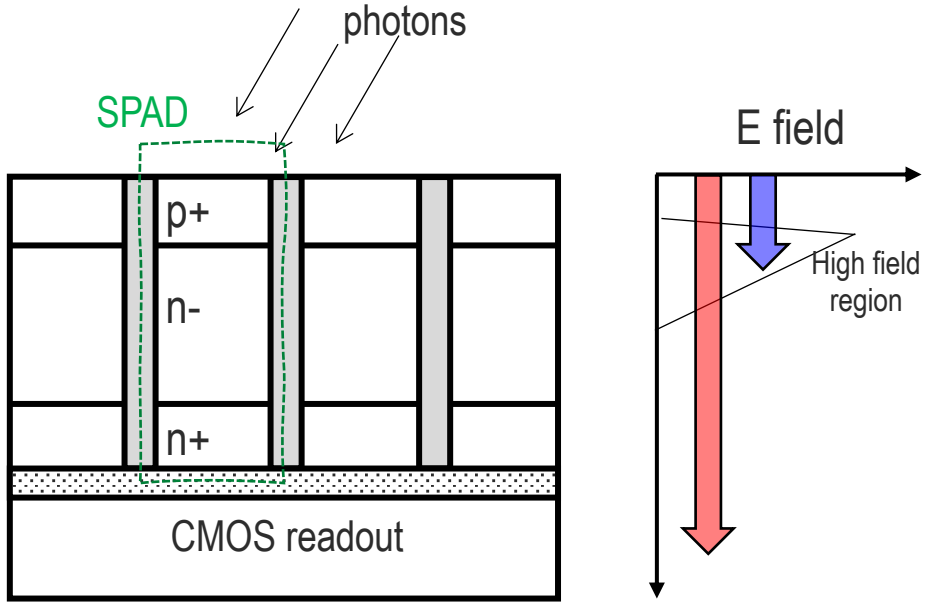
Next section



(c)

Development of the SPAD array layer

SPAD Array – Architecture Overview



- Thinned SPAD array
  - Backside connection (cathode)
  - Laterally uniform electric field
  - No through-silicon-vias (TSV)
  - Full thickness trench isolation [1]
- High Fill-Factor because no TSV

Present implementation

- Frontside illuminated p^+n SPAD:
  - junction near the photon incidence face
- For $\lambda \sim 400$ nm (violet):
  - 3/4 of photons absorbed within 100 nm from entrance face (in Si)
    - Before/in the high field region
  - Mainly electron triggered avalanches
    - Higher photodetection probability
  - Less photoelectron drift
  - Laterally uniform electric field

} High timing resolution

1. Ito, Kyosuke, et al. "A Back Illuminated 10 m SPAD Pixel Array Comprising Full Trench Isolation and Cu-Cu Bonding with Over 14% PDE at 940nm." 2020 IEEE International Electron Devices Meeting (IEDM). IEEE, 2020.

Thinned TSV-less Frontside Illuminated SPAD Array

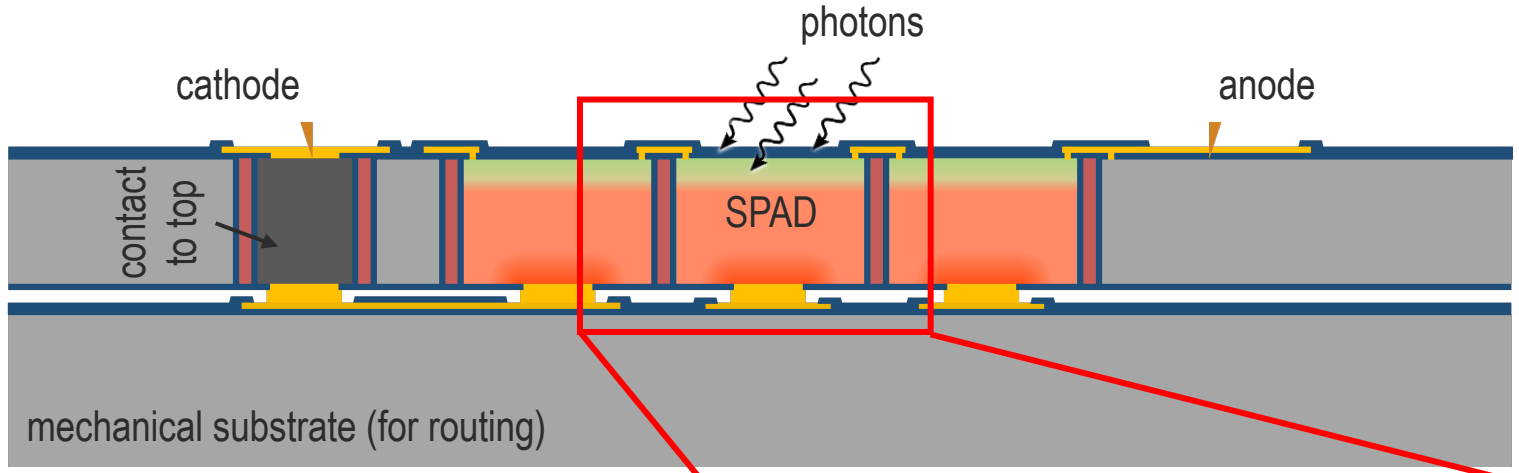
UDS

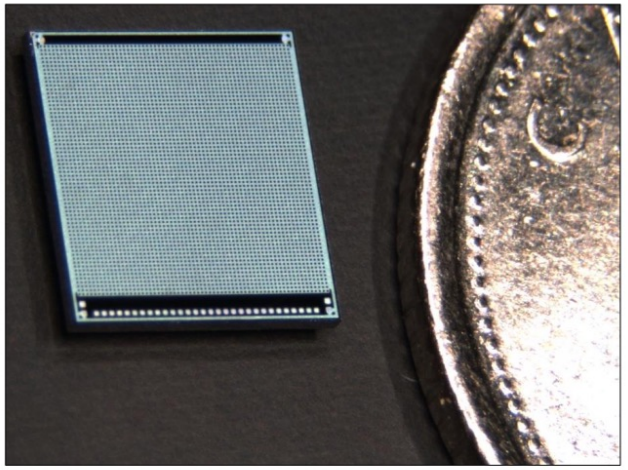
1st fabrication run completed

SPAD + thinning + 3D bonding

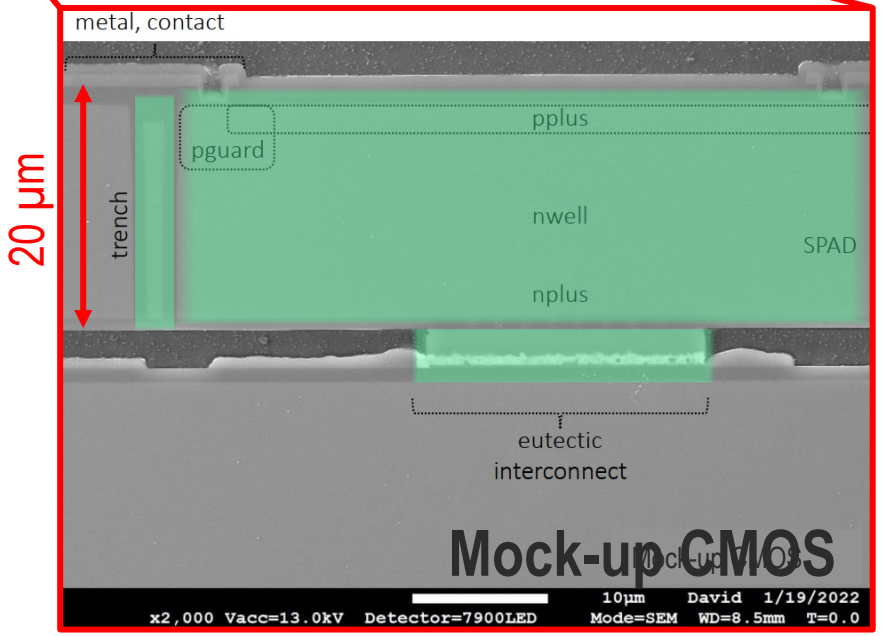
- p⁺n SPAD [1]
- 64 × 64 SPAD Array
- 78 µm pitch

- Al-Ge eutectic bonding
- Mock-up CMOS allows to test the 3D SPAD array



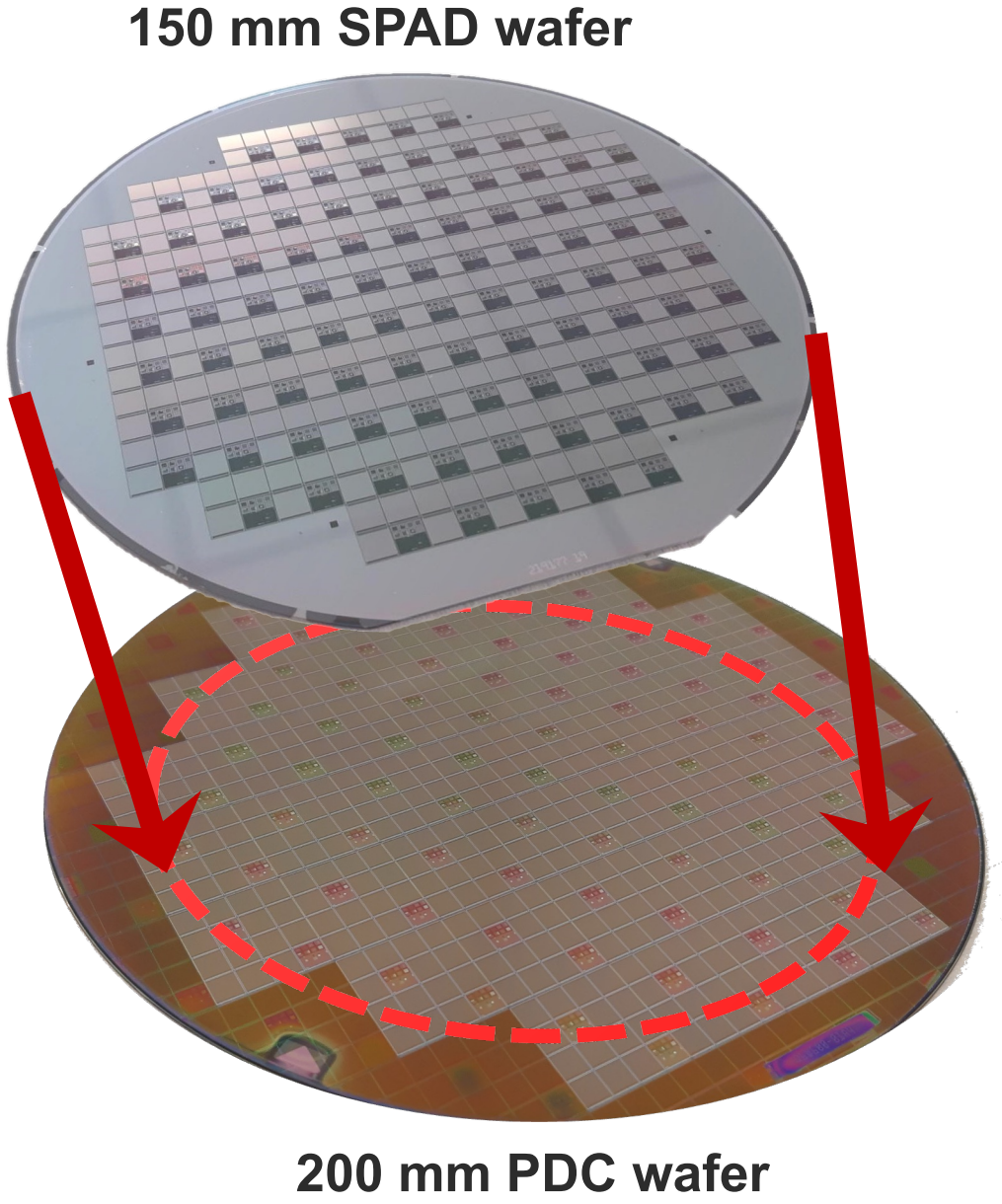


3D SPAD array
(canadian 10¢ for reference)

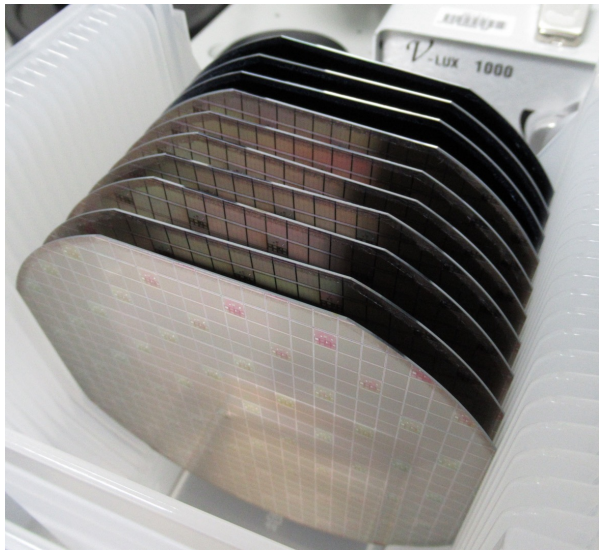


SEM cross section image

1. Parent, Samuel, et al. "Single photon avalanche diodes and vertical integration process for a 3D digital SiPM using industrial semiconductor technologies." 2018 IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings (NSS/MIC). IEEE, 2018.



- CMOS wafer cored down ready for 3D integration.



- 3D-integration in 2024 → First 3D-PDC (CMOS+SPAD)

Main Industrial Collaborator : Teledyne DALSA

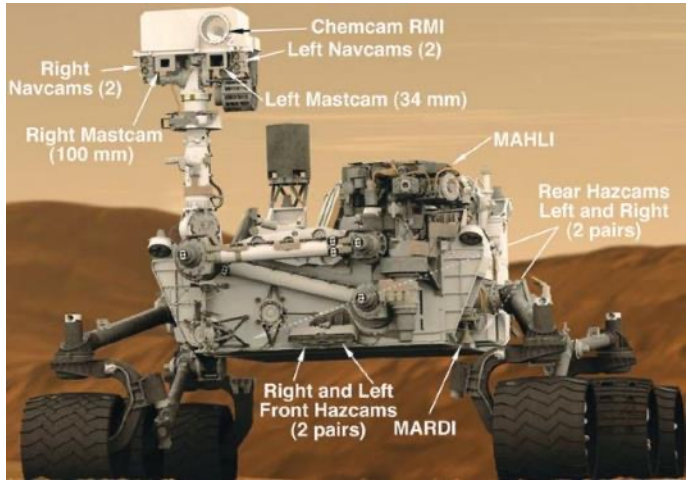
UDS

High-end CCD process line
--> excellent for SPAD R&D

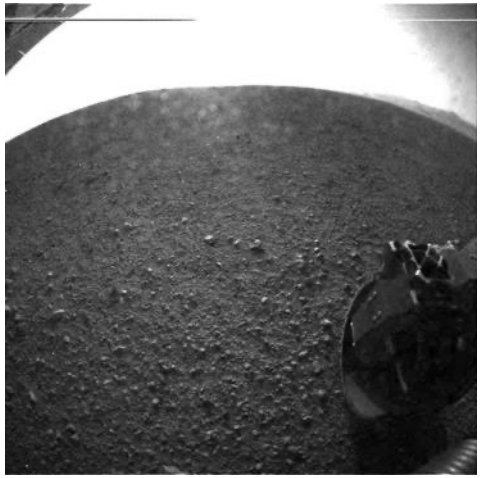
- 150 mm process line
- low contaminant / gold free clean rooms

World top 5 MEMS Foundry
--> excellent for wafer level integration

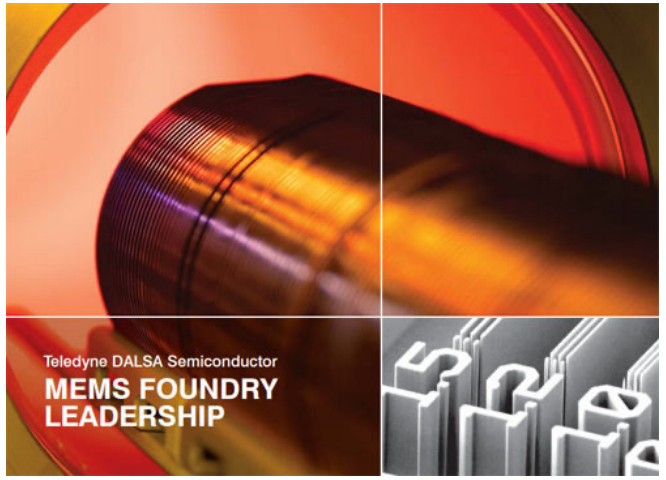
- 150 mm and 200 mm process line
- Wafer thinning, deep etching, bonding, ...



The Eyes of the Mars Curiosity Rover. Tech Briefs (2012)



Life on Mars: Rover landing gives boost to Canadian tech sector. The Globe and Mail (2012)



Courtesy of Teledyne DALSA

MEMS Foundry Rankings (2017 sales in US$M)	
STMicroelectronics	174
Teledyne DALSA	60
Silex Microsystems	50
TSMC	47
X-Fab	42

Status of the MEMS Industry 2018 Market and technology Report Yole Development (2018)

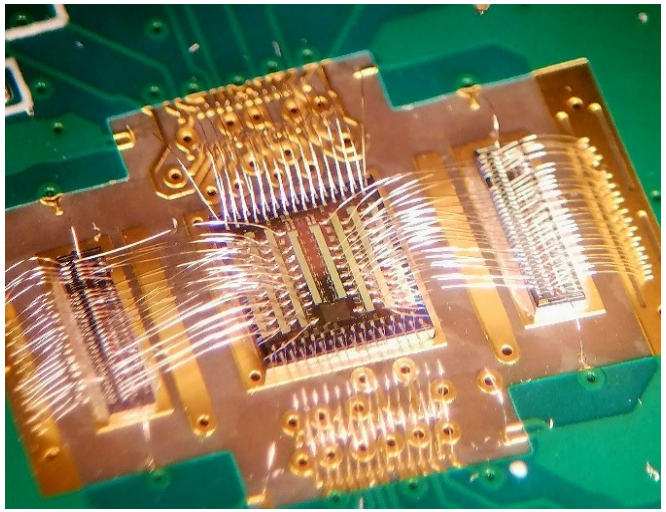
TELEDYNE DALSA
Everywhereyoulook™

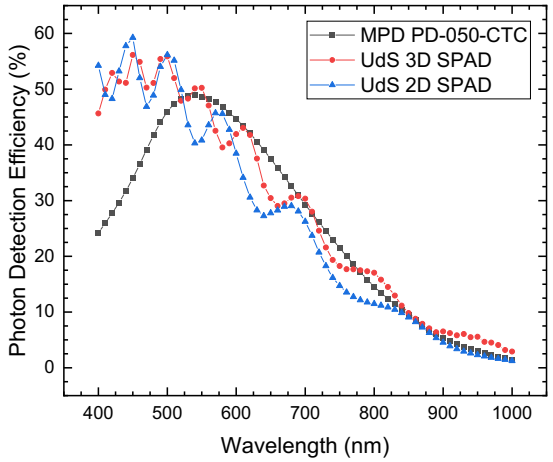
Teledyne DALSA Semiconductor (est. 1980)
~ 500 employees located at Bromont near Montreal, Canada

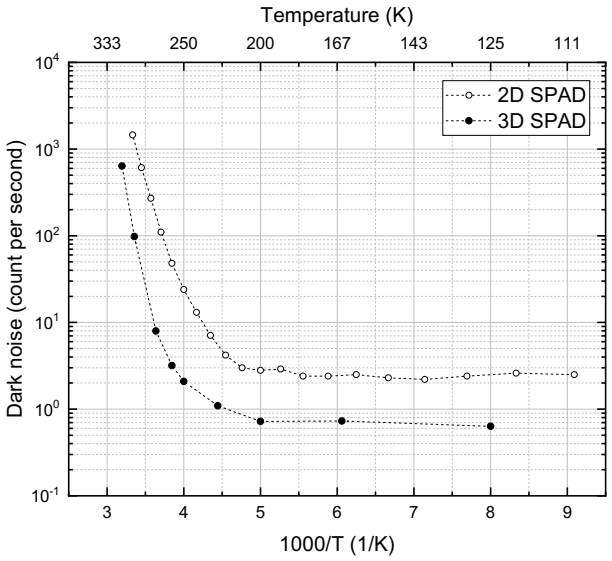
All Characterization Made in Geiger Mode

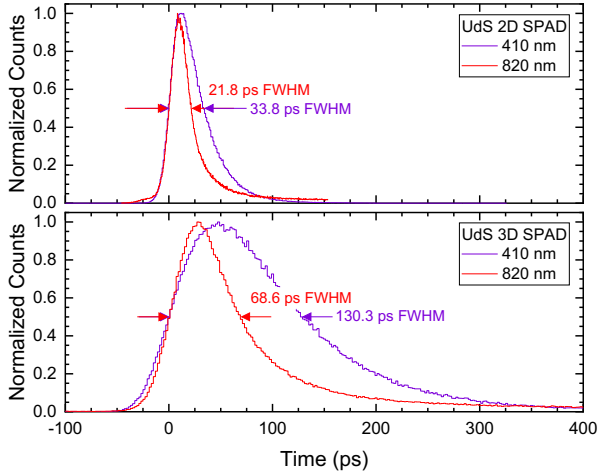
UdS

Detailed characterization using dedicated ”external” quenching circuits

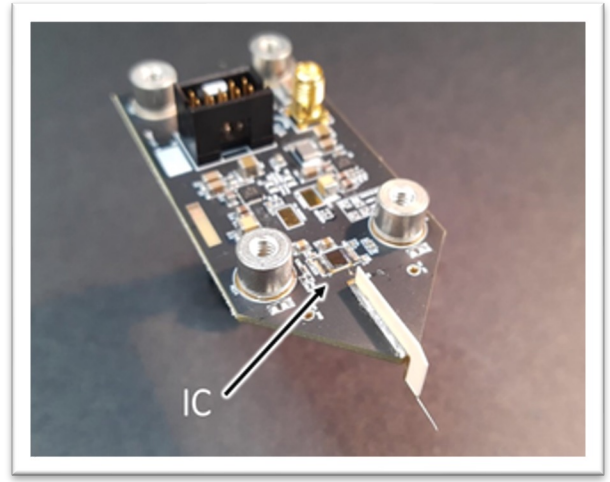


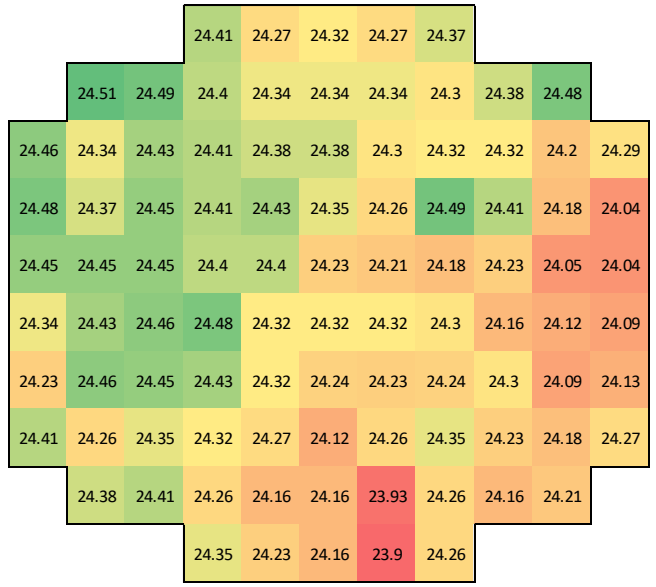






Active wafer probing to support process development





Breakdown voltage

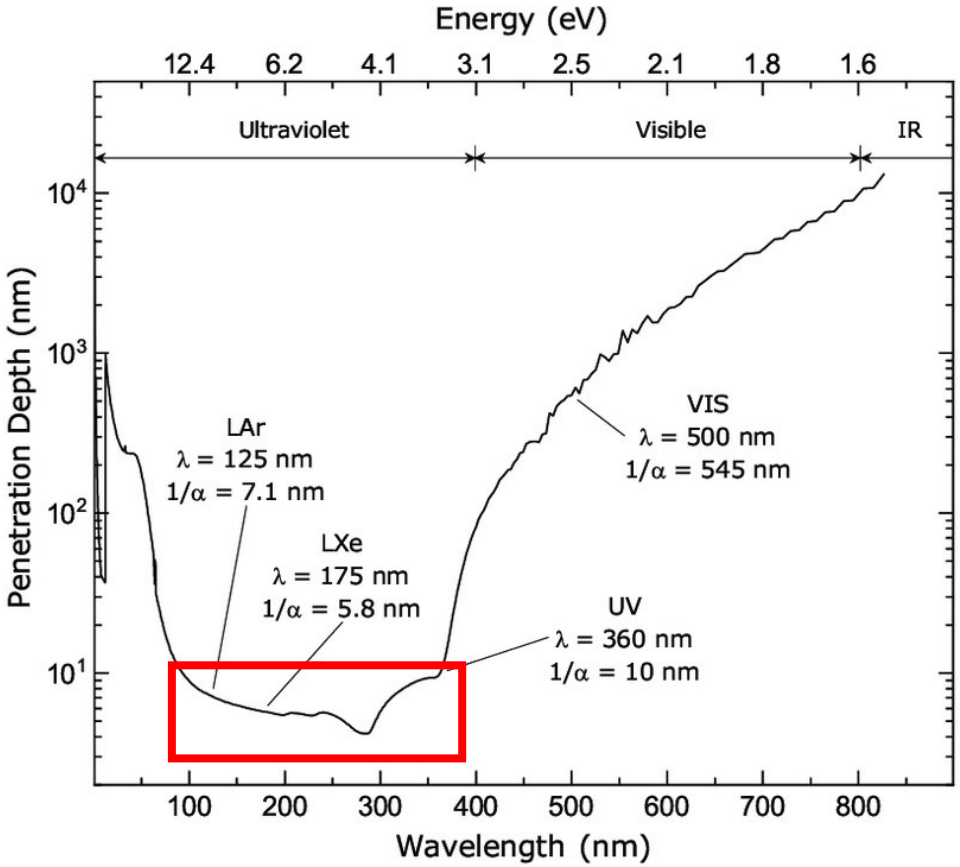
serge.charlebois@usherbrooke.ca

Enhancing sensitivity to VUV photons:

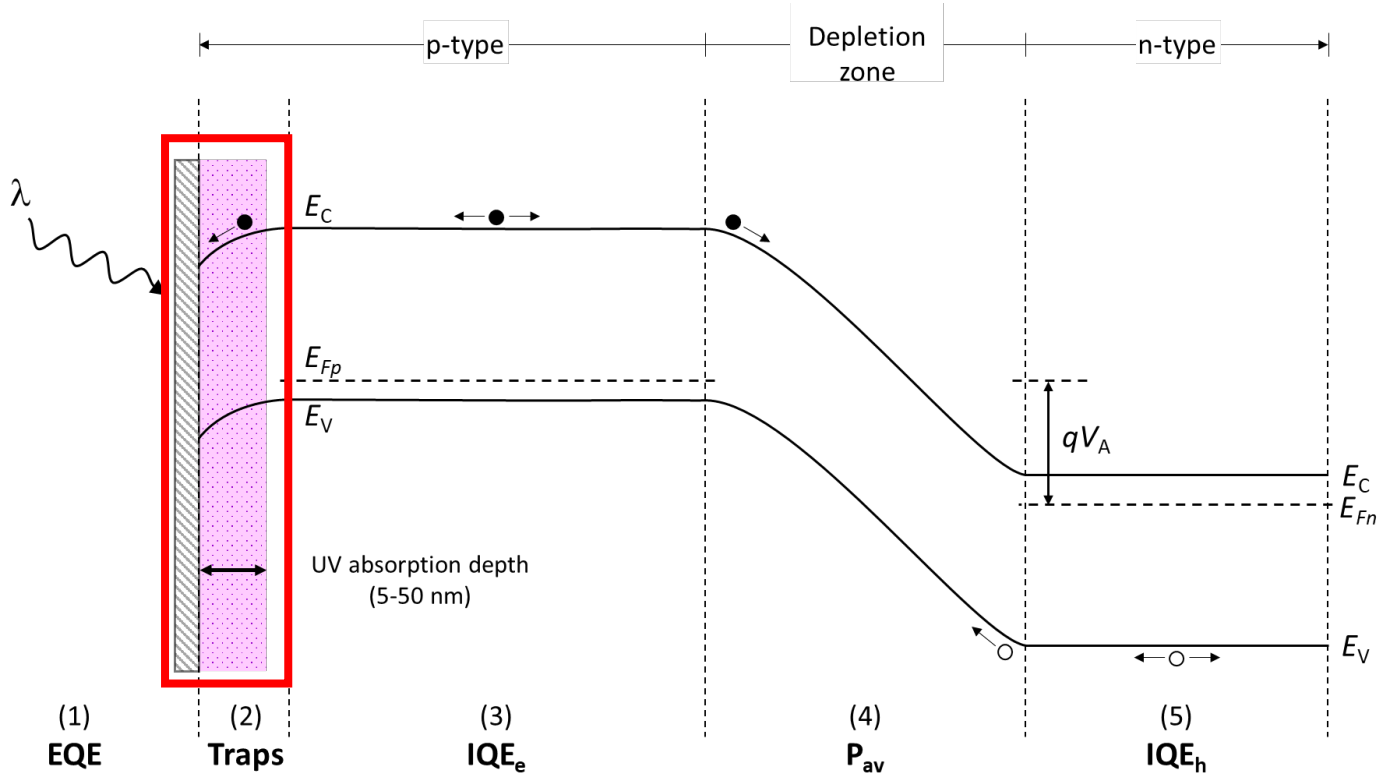
Low temperature δ-doping

with BERKELEY LAB
Lawrence Berkeley National Laboratory

Photon penetration depth and the sensitivity problem in UV



Pratte, JF. 3D Photon-To-Digital Converter for Radiation Instrumentation: Motivation and Future Works 2021

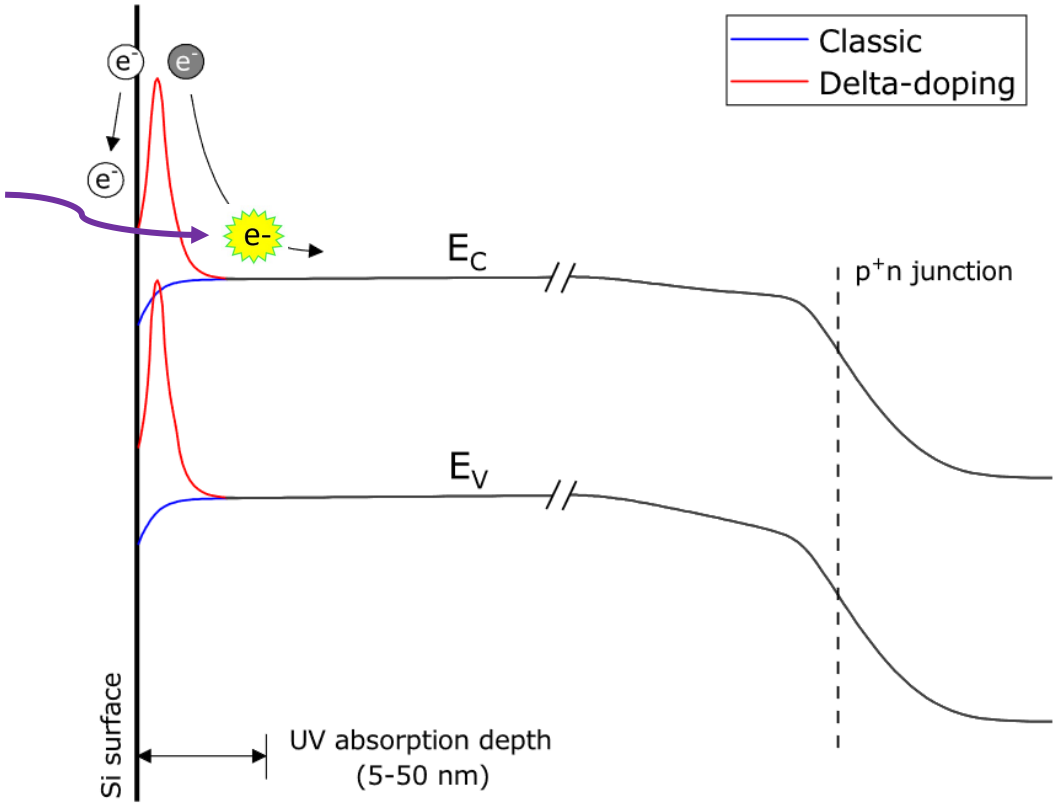


F.Vachon, Masters thesis, Université de Sherbrooke, 2021.

Delta doping – Mitigating the Surface Potential Trap

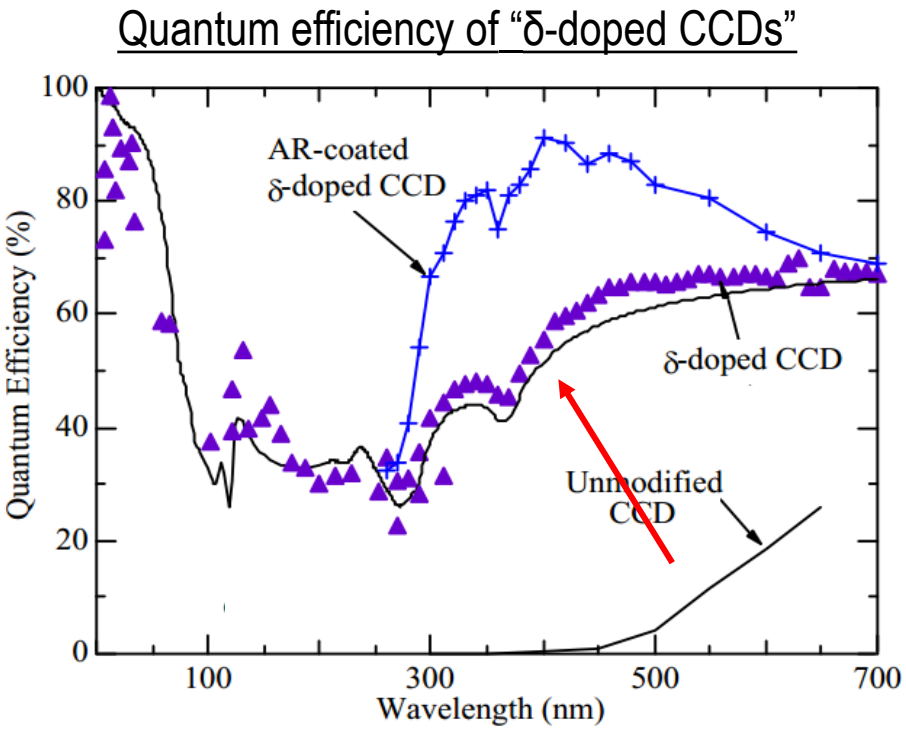
UDS

- Sharp peak of dopant (boron) “pushes” minority carriers either toward depletion zone or surface



F.Vachon, Masters thesis, Université de Sherbrooke, 2021

- JPL 1992 molecular beam epitaxy (MBE) grown δ-doped layer on backside illuminated CCDs restored unity IQE



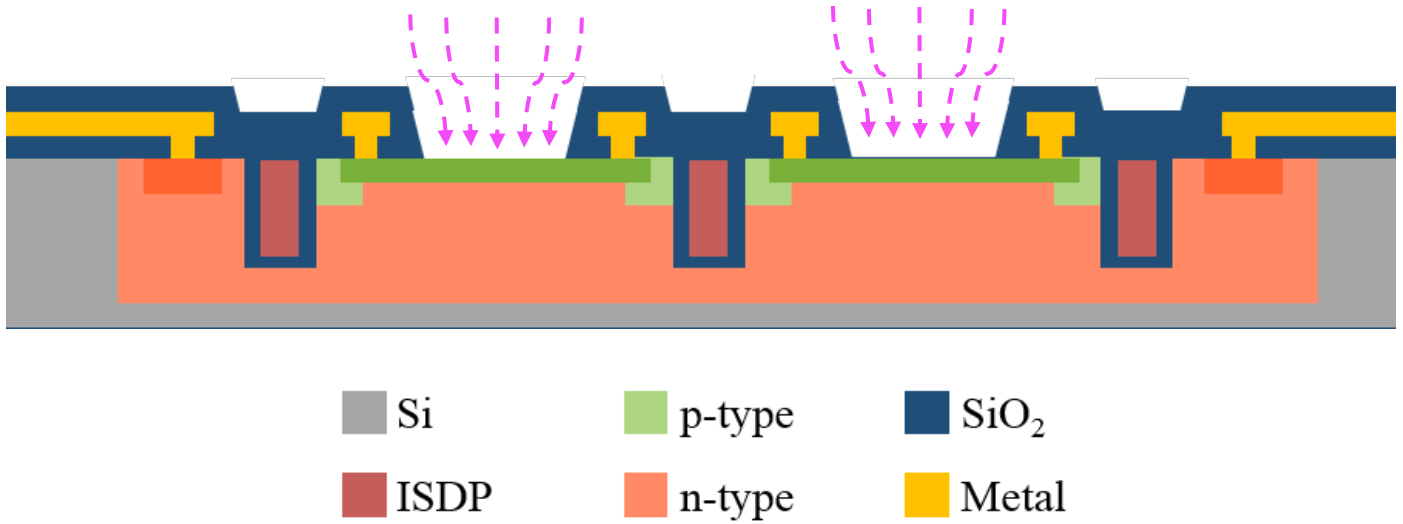
Growth of a delta-doped silicon layer by molecular beam epitaxy on a charge-coupled device for reflection-limited ultraviolet quantum efficiency. M.E. Hoenk et al. Applied Physics Letters 61, no. 9 (1992): 1084-1086.

Growth on device: process limitation(s)

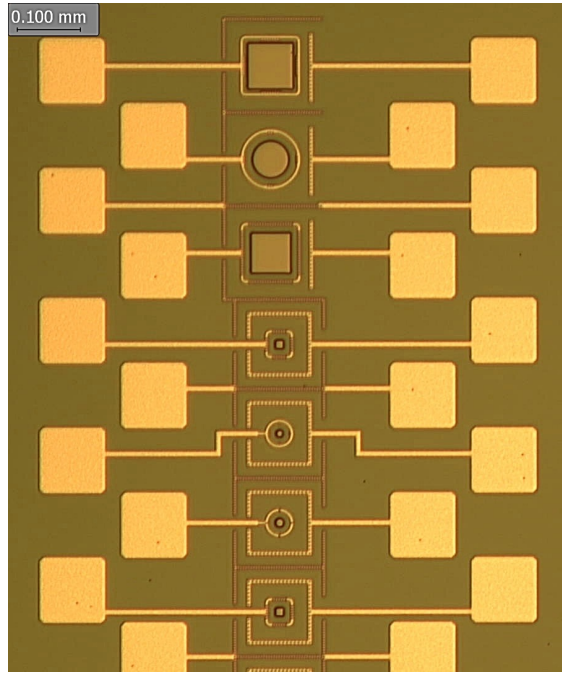
UDS

- Al contact pads and rings low diffusion T° (450°C) (spiking)

- Epitaxy on metal + oxide (frontside) patterned surface complexifies chemical cleaning (RCA, HF)



F.Vachon, Masters thesis, Université de Sherbrooke, 2021.



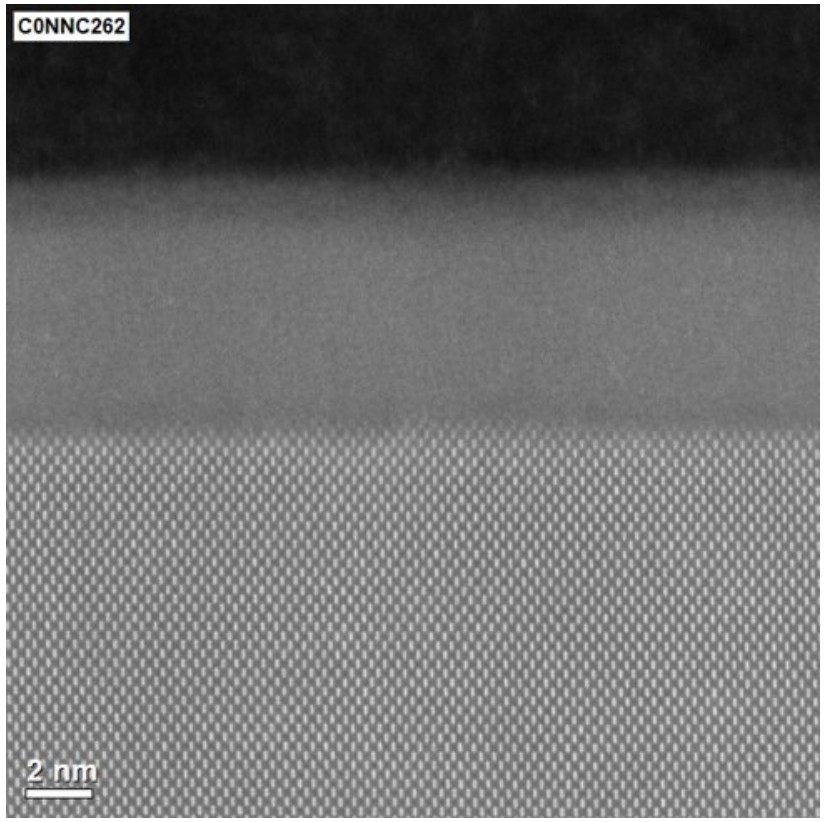
2D SPAD array test structure

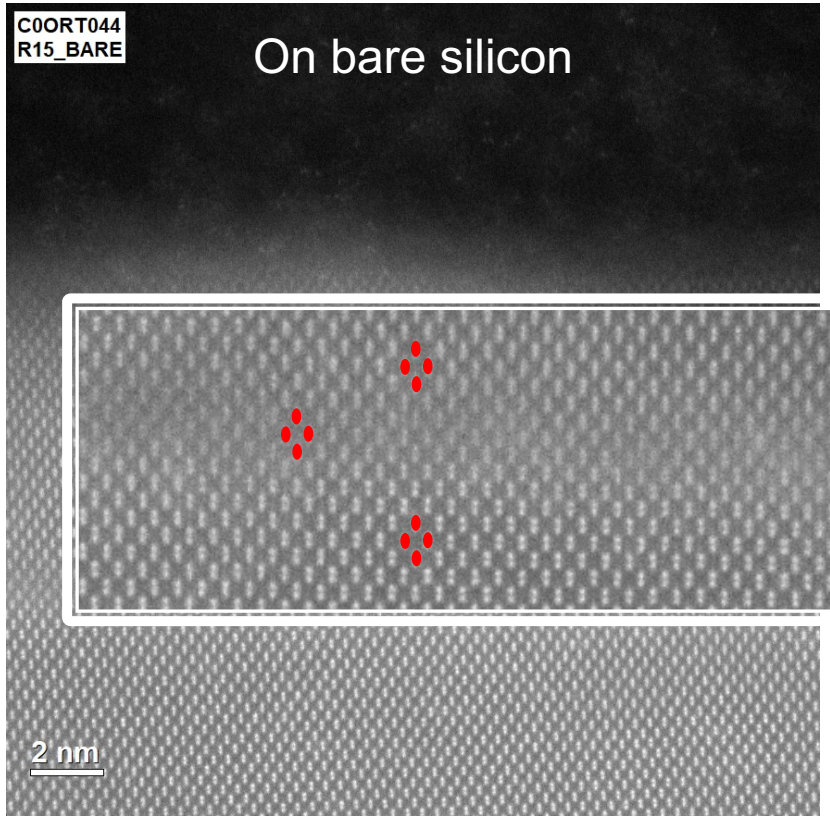
Reaching a Epitaxial Growth – A First TEM confirmation

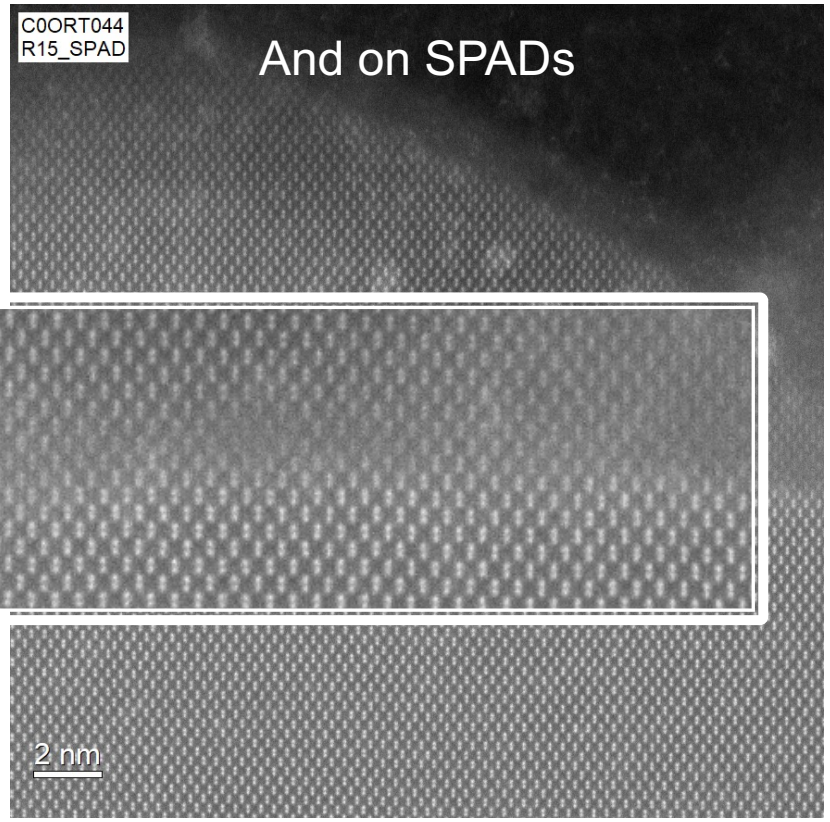
- Crystallographic orientation of layer match substrate (001)
- Interface still blurry and visible islanding

Previous runs: amorphous growth

New runs: Clustered epitaxial growth





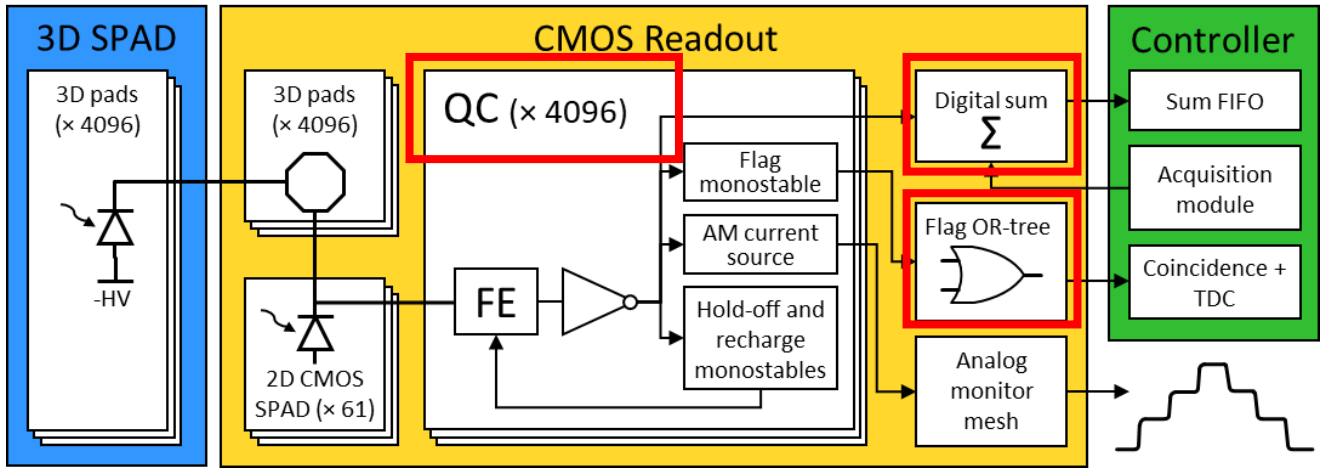


PDC designed for low power use in noble liquid experiments

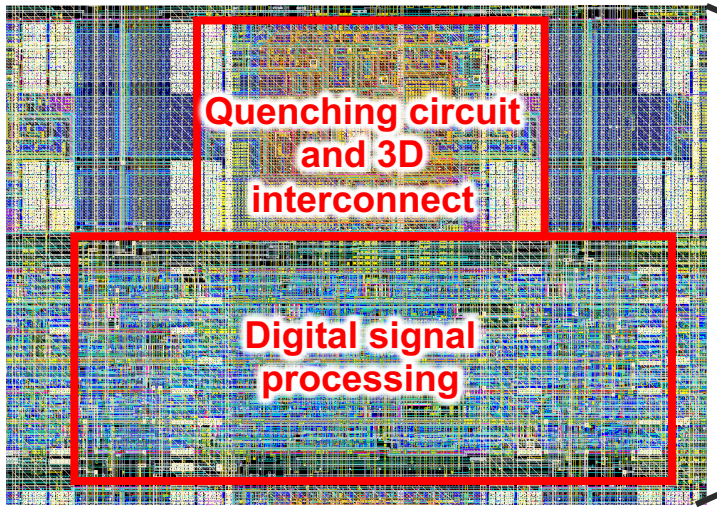
Example of Low Cost CMOS for Large-Area Experiments

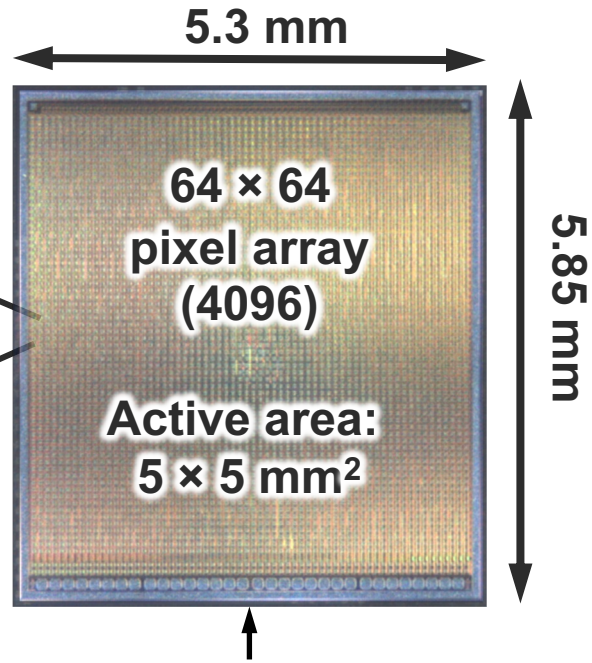
UDS

- TSMC 180 nm BCD process
- 5 x 5 mm^2 active area
- 64 x 64 pixels (4096)
- 78 µm pixel pitch
- 3-side buttable (for tiles)



A single pixel





Rossignol, Tommy. Conception d'un circuit de lecture d'une matrice de photodiodes à avalanche monophotonique pour les détecteurs de physique des particules dans les gaz nobles liquéfiés. Diss. Université de Sherbrooke, 2020.

serge.charlebois@usherbrooke.ca

Photon-to-Digital Converter: Architecture

UDS

Digital Sum

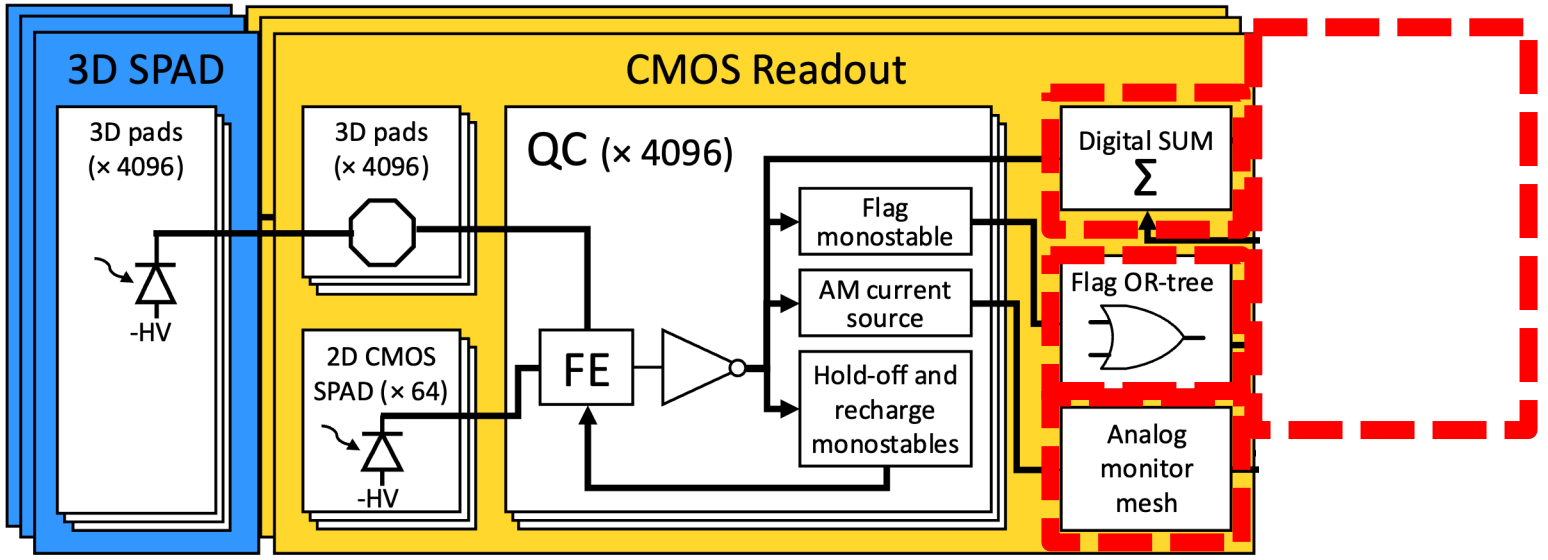
- Digital count of triggered SPADs inside a bin (dynamic range of 4096 photons).
- Adjustable bin width from 10 ns up to µs.
- Internal FIFO of 128 bins.

Flag output

- Pulsed output (adjustable from few ns to tens of ns).
- From an OR-tree.
- Timing jitter better than 100 ps RMS (i.e. external TDC).

Analog Monitor

- Current proportional to triggered SPADs.

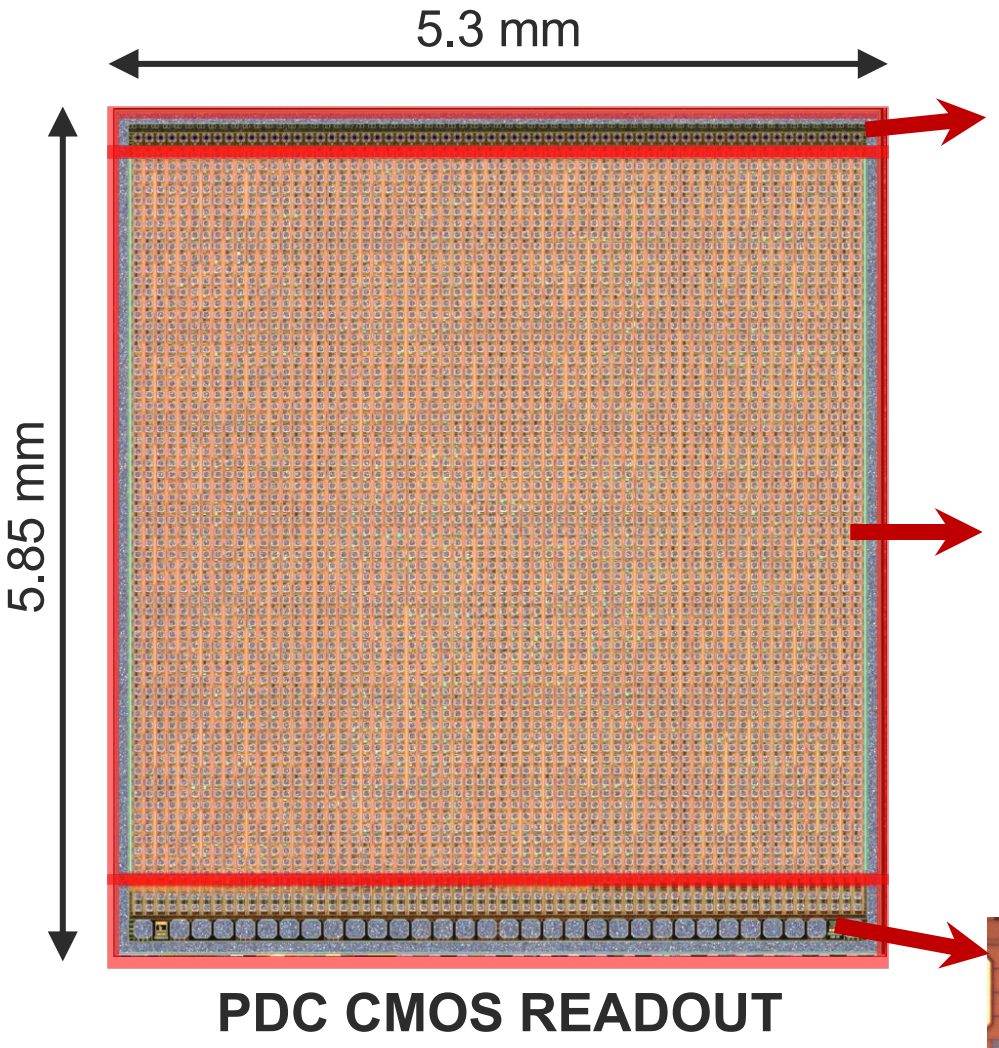


×64 PDCs/Controller

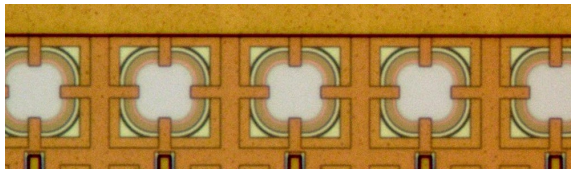
Controller (1 for 64 PDCs)

- Start PDC acquisition, based on the number of flag received to discriminate dark count.
- Bank of TDCs for timing measurements on flags.
- Receives data from PDCs and includes post-processing.
- Communicate with an external computer.

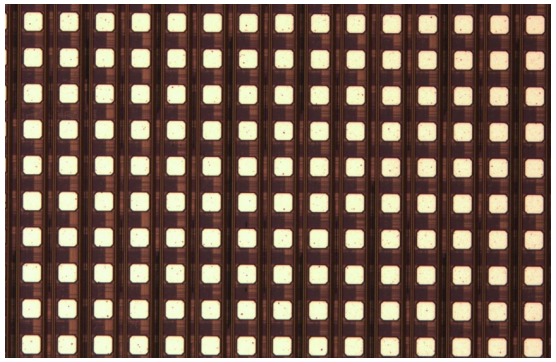
The PDC CMOS Readout Chip



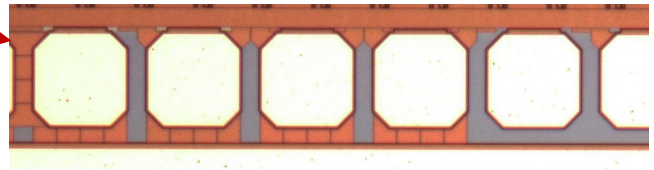
64× 2D CMOS SPADs



64×64 pixels ready for 3D integration



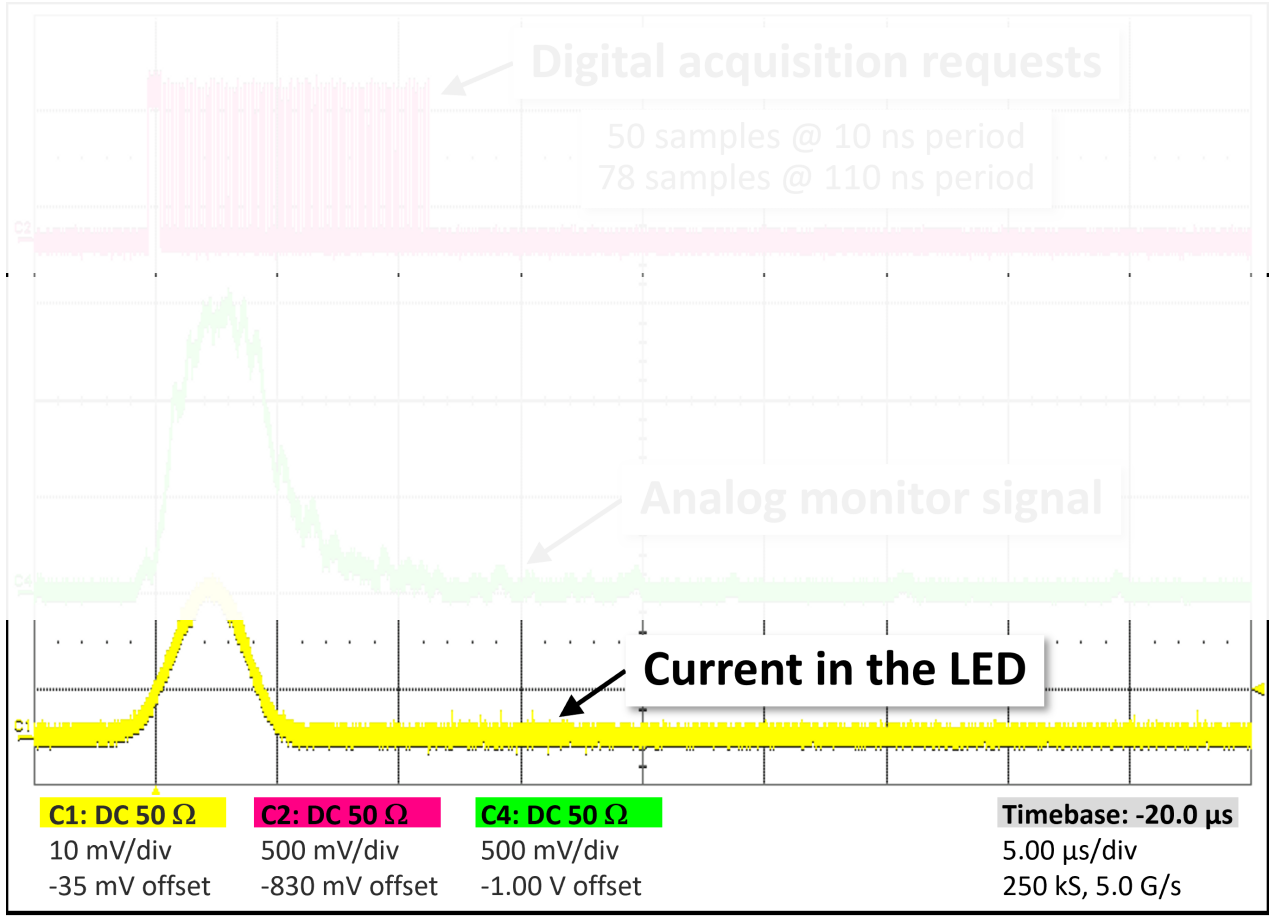
IO pads ESD protected



Key Specifications

- TSMC 180 nm BCD CMOS process.
- 78 µm SPAD-to-SPAD pitch.
- Every SPAD is controlled individually.
  - Noisy SPADs can be disabled.
- Dynamic range of 0 to 4096 photons.

2×2 Photodetection Module with LED Testing



Using embedded CMOS test SPADs of the PDC

Current in the LED to trigger the SPADs

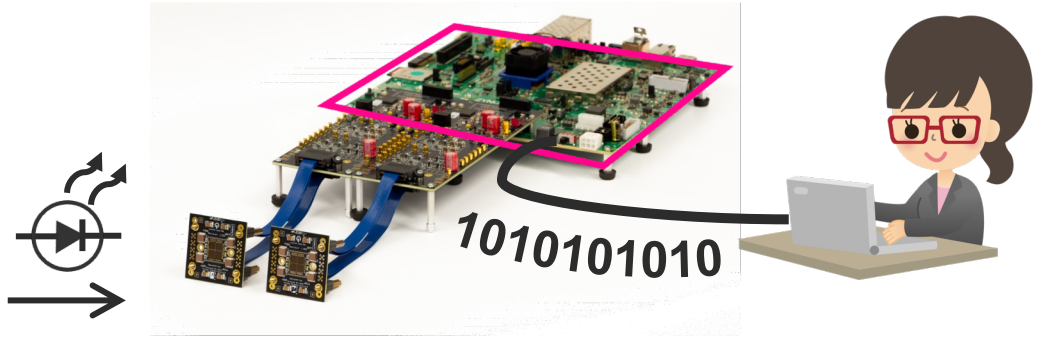
- Driven by a waveform generator

Analog Monitor

- Amplitude proportional to the number of SPADs triggered

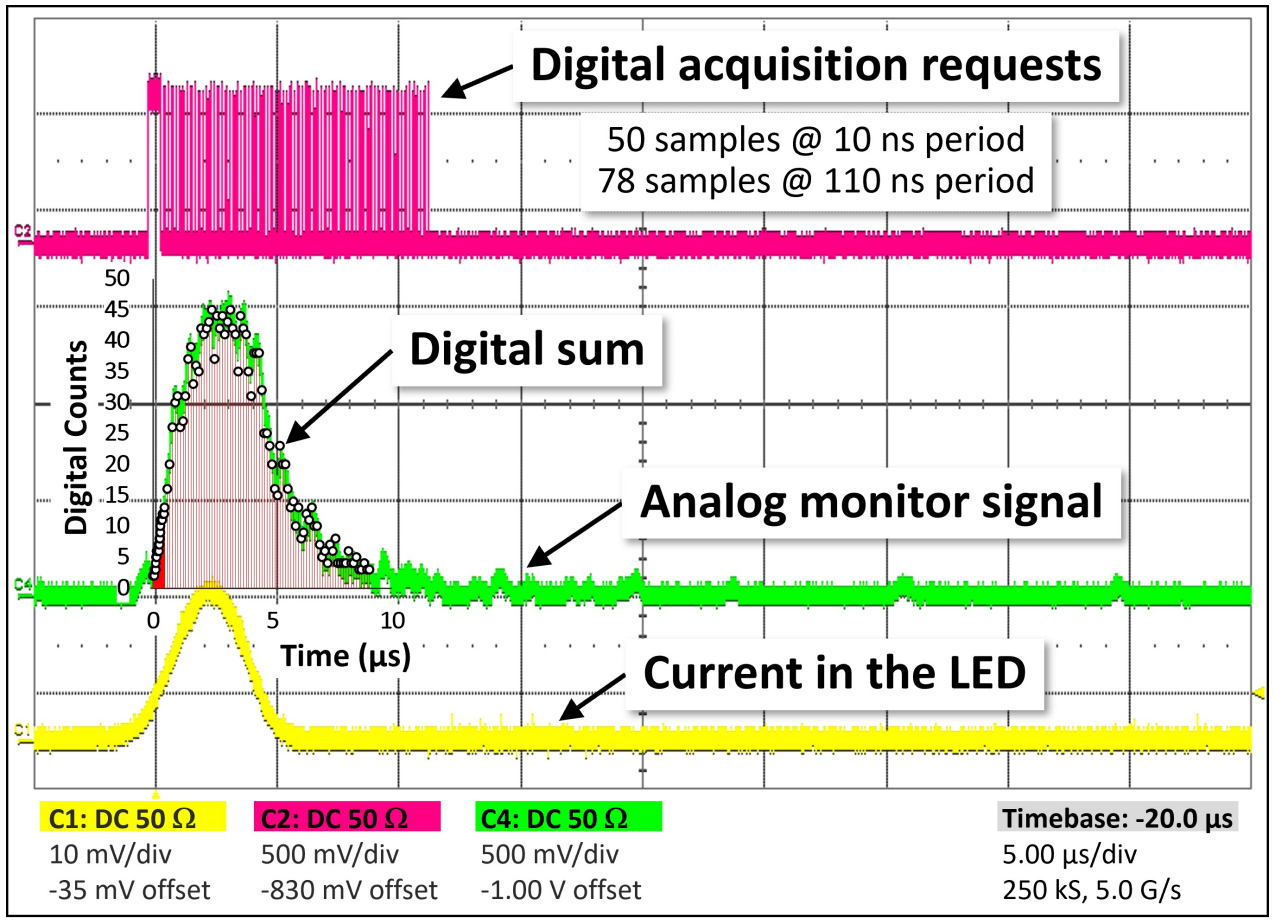
Digital Sum Acquisition

- Based on a 100 MHz readout clock
- Generated by the FPGA (Tile Controller)

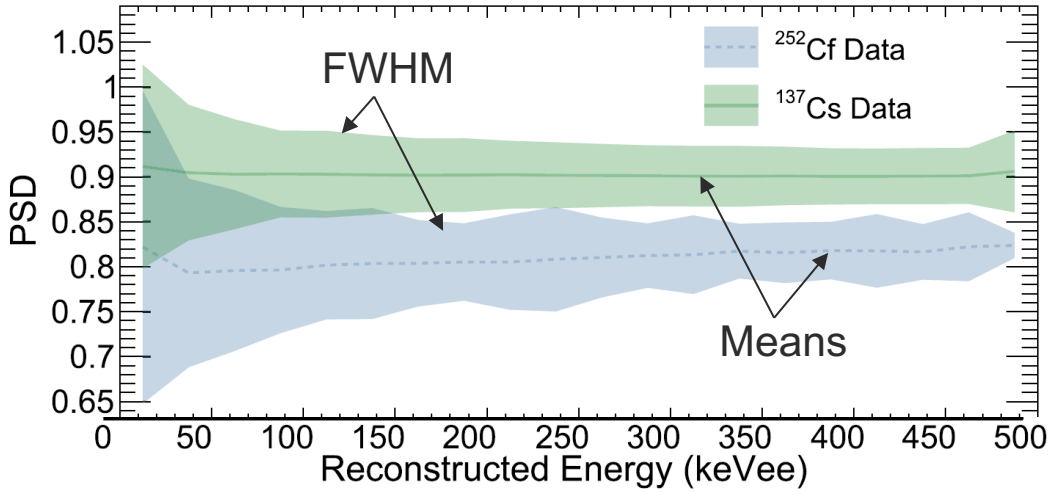


Neutron detection

2×2 Photodetection Module with LED Testing



Using embedded CMOS test SPADs of the PDC



PSD parameter as a function of energy. [1]

[1] M. R. Heath *et al.*, "Development of a Portable Pixelated Fast-Neutron Imaging Panel", DOI:10.1109/TNS.2021.3136344.

serge.charlebois@usherbrooke.ca

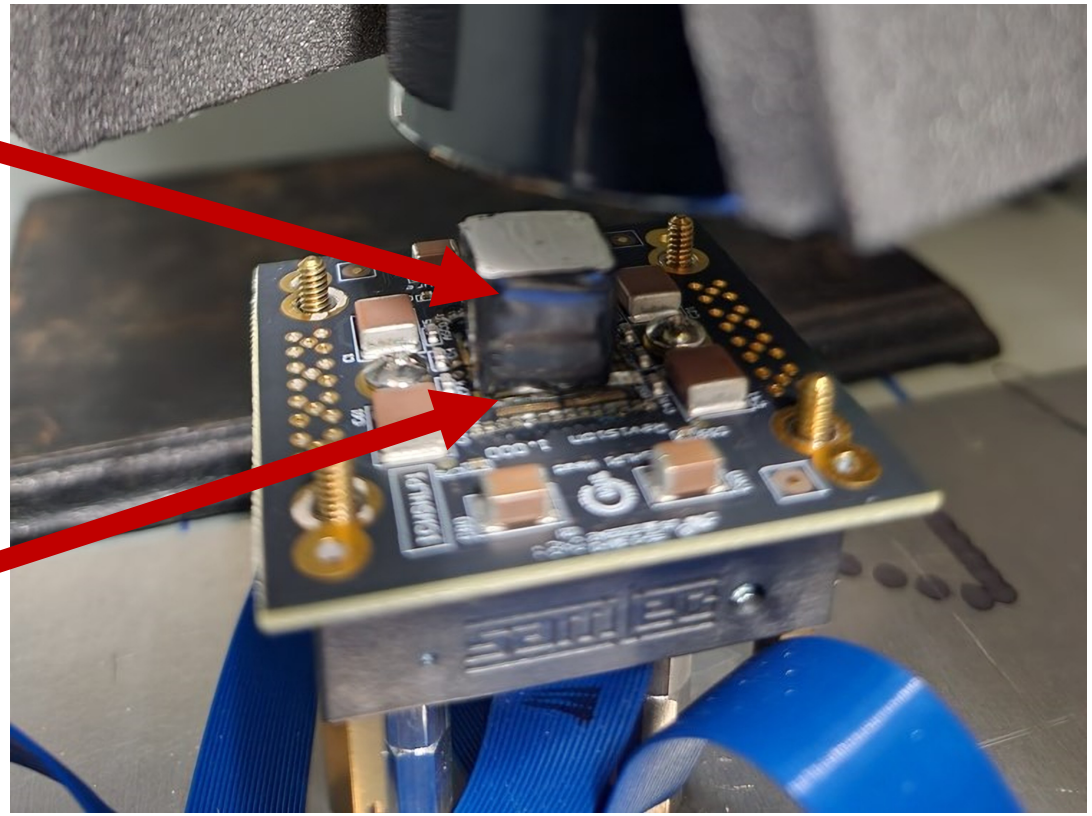
2×2 PDM with Gamma Source

UDS

Eu-152, 10 µCi
EJ-200 Plastic Scintillator

Plastic Scint.

PDCs



PMT
Hamamatsu
R9779

The light detected by the PMT triggers an oscilloscope acquisition and the flag output from the PDC is recorded.

serge.charlebois@usherbrooke.ca

2×2 PDM with Gamma Source

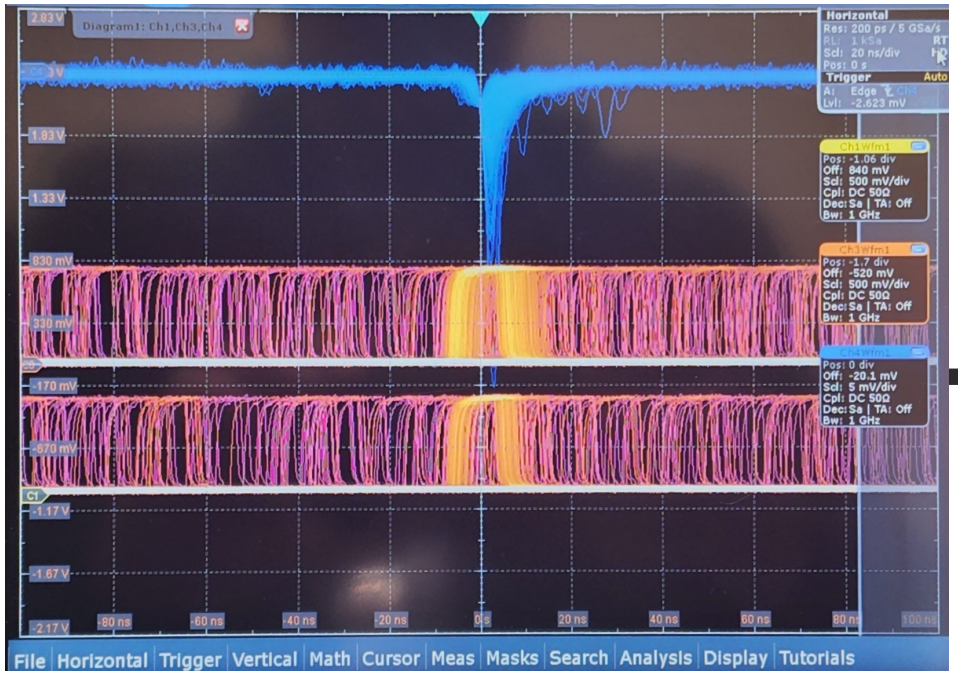
UDS

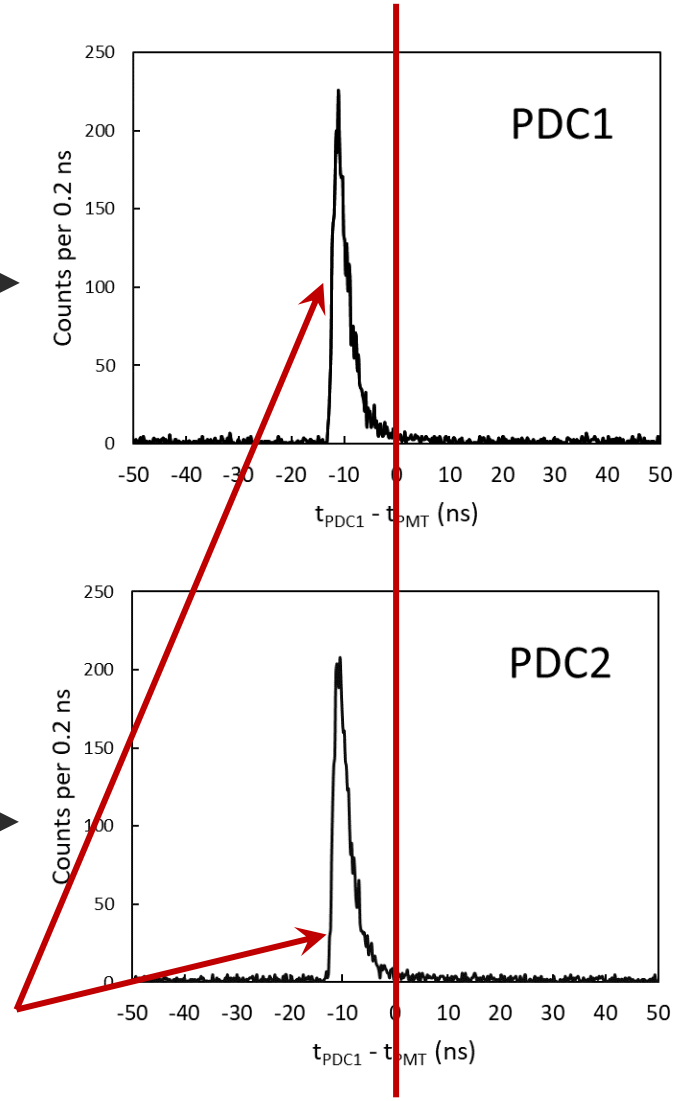
Eu-152, 10 µCi
EJ-200 Plastic Scintillator

PMT output (trigger)

Flag output (PDC1)

Flag output (PDC2)





- 20 ns/div Time Base
- Leading Edge trigger on PMT

Using embedded CMOS test SPADs of the PDC

Photons detected in coincidence between PMT and PDC

PMT Trigger @ 0ns

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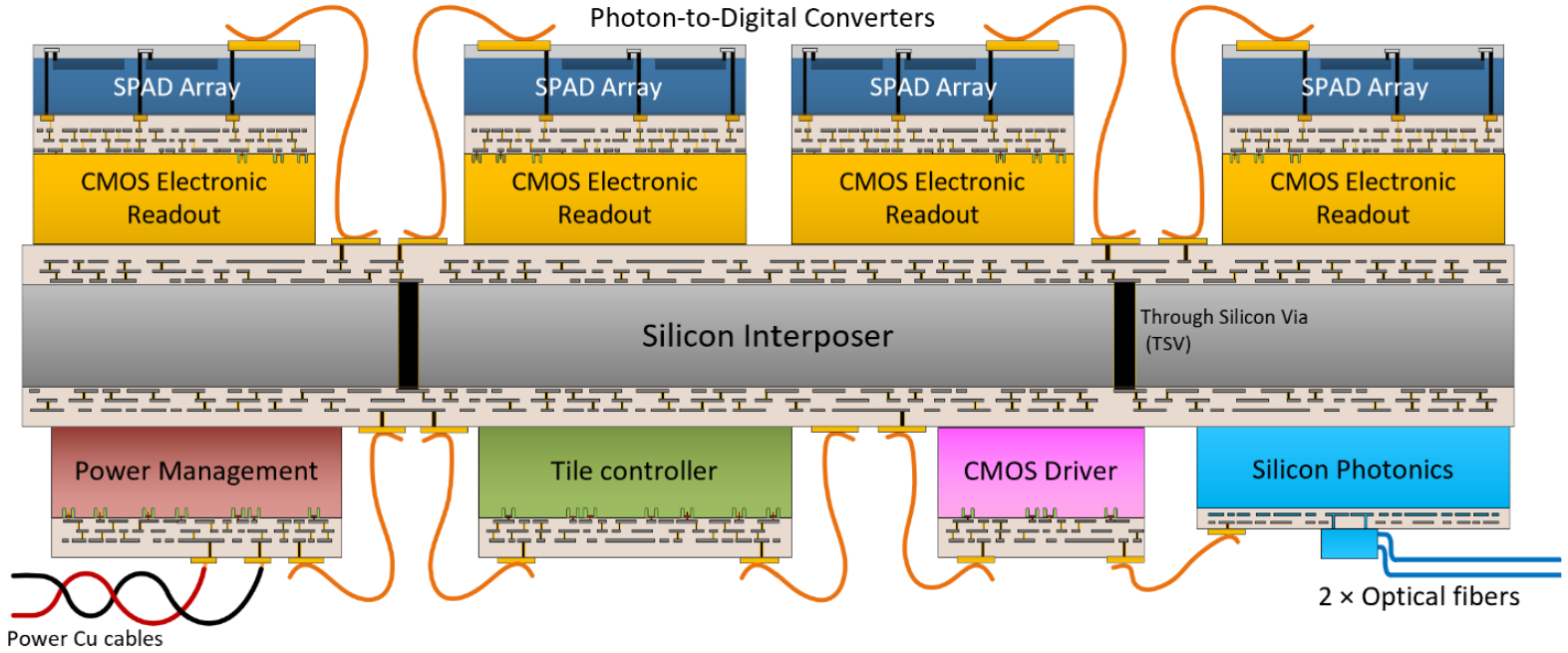
Our global research program:

Photon Detection Modules

nEXO

ARGO

Our global ambition



- Demonstrated small tile prototypes
- Silicon interposer for low background large scale integration
- Optical (digital) communication
- Embedded time-to-digital conversion

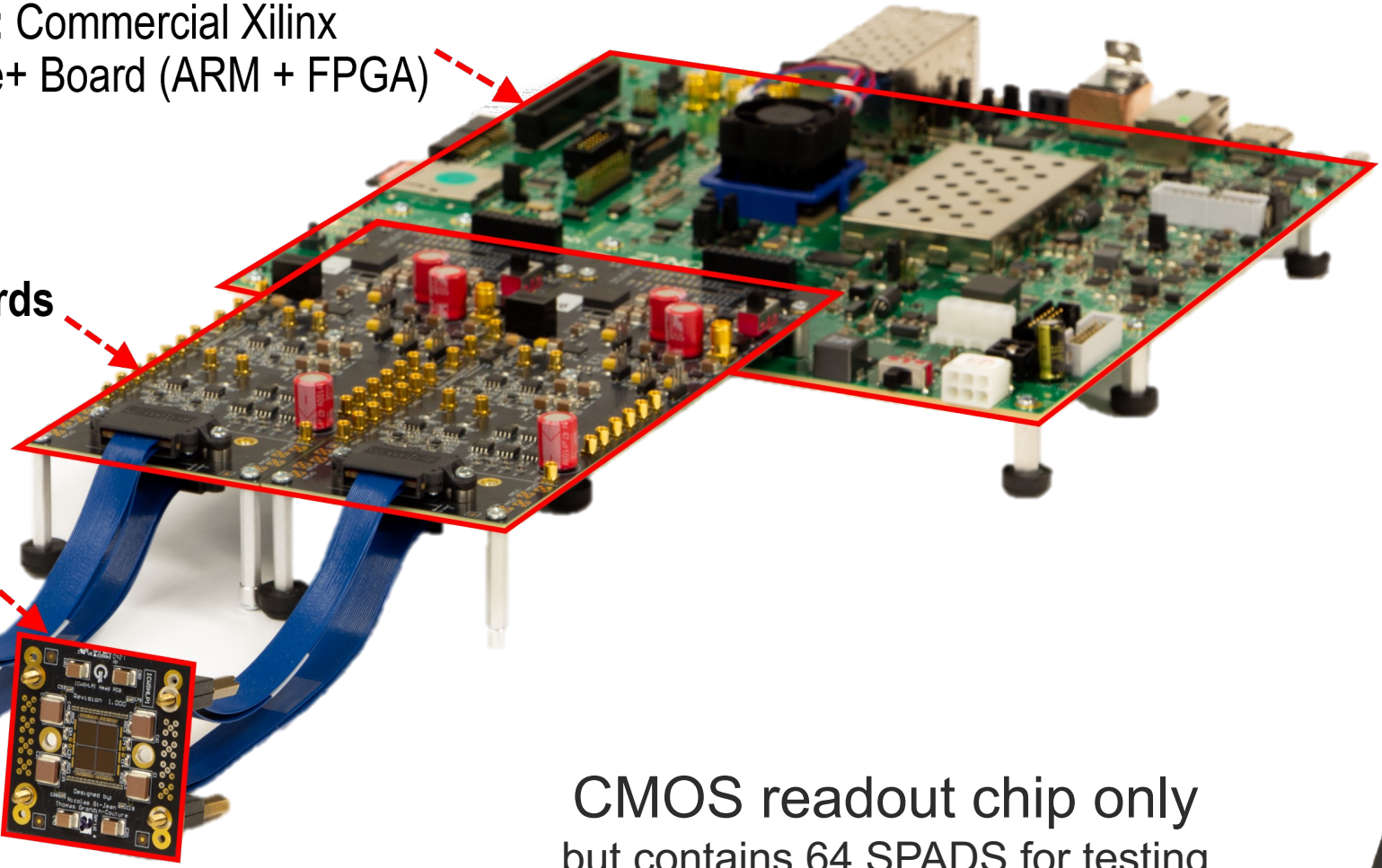
2×2 Photodetection Module

UdeS

Tile Controller: Commercial Xilinx Zynq UltraScale+ Board (ARM + FPGA)

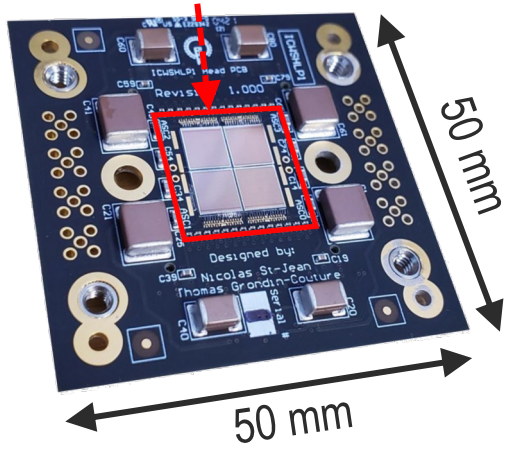
Adaptor Boards

2×2 Heads

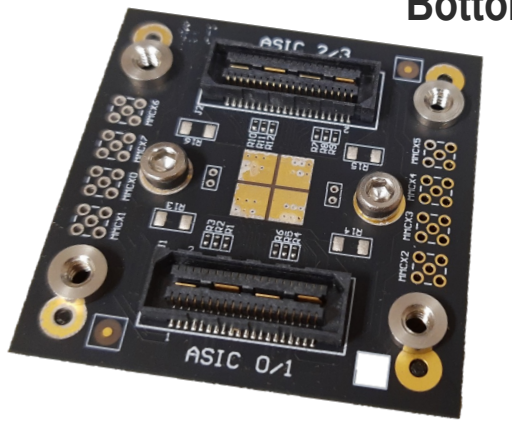


2×2 PDCs

Top



Bottom



CMOS readout chip only

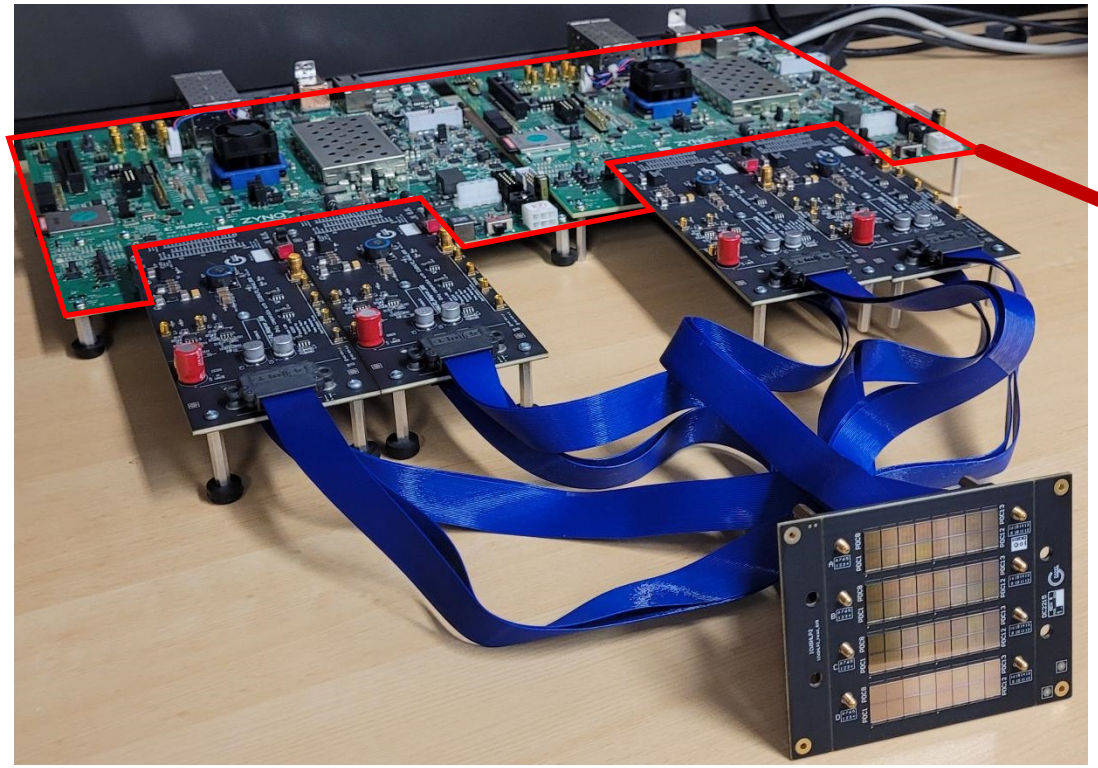
but contains 64 SPADS for testing

→ Its a « functional » detector

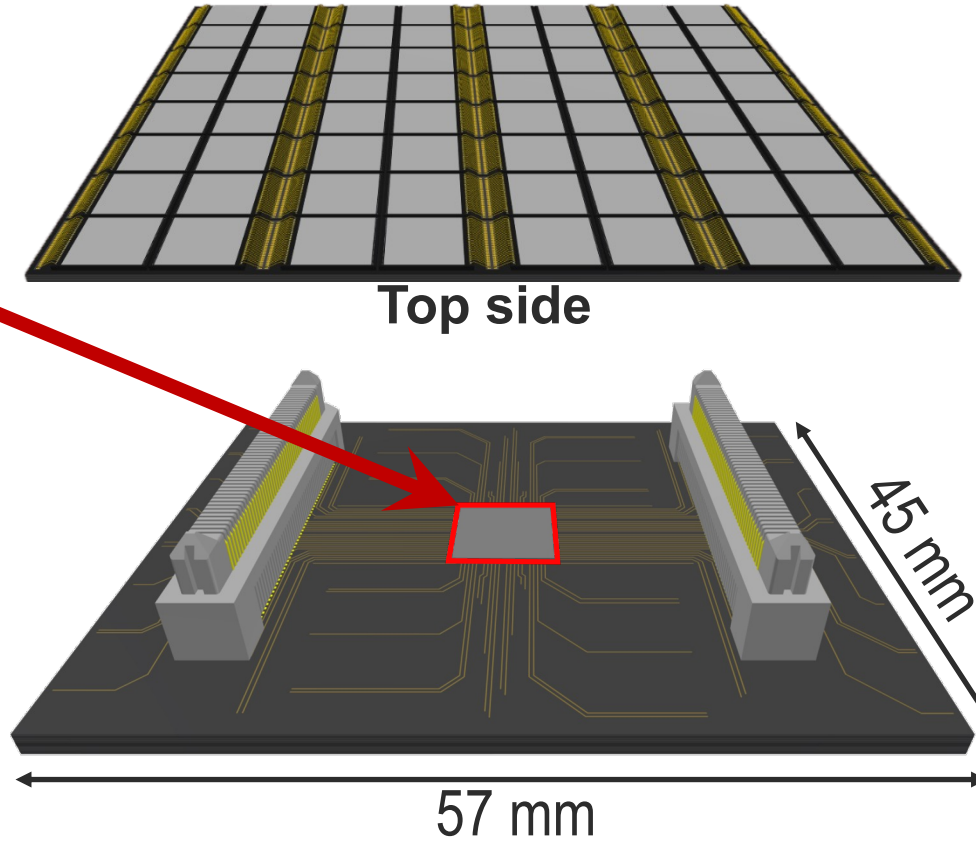
Next Step: FPGA board to a Tile controller

UDS

FPGA-based Controller



ASIC-based Controller



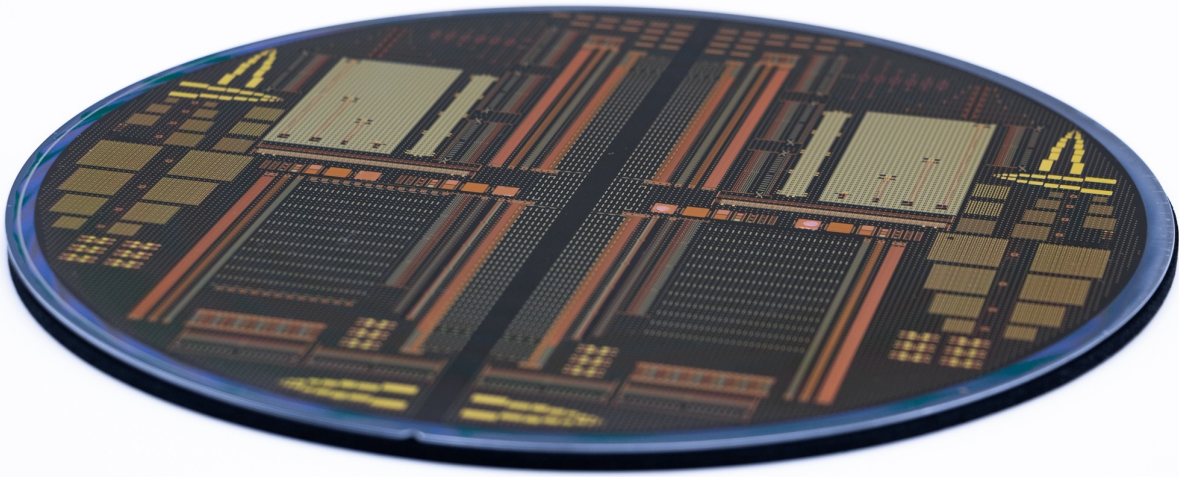
Providing a mechanical structure to the Photon Detection Module:

Large area silicon interposer

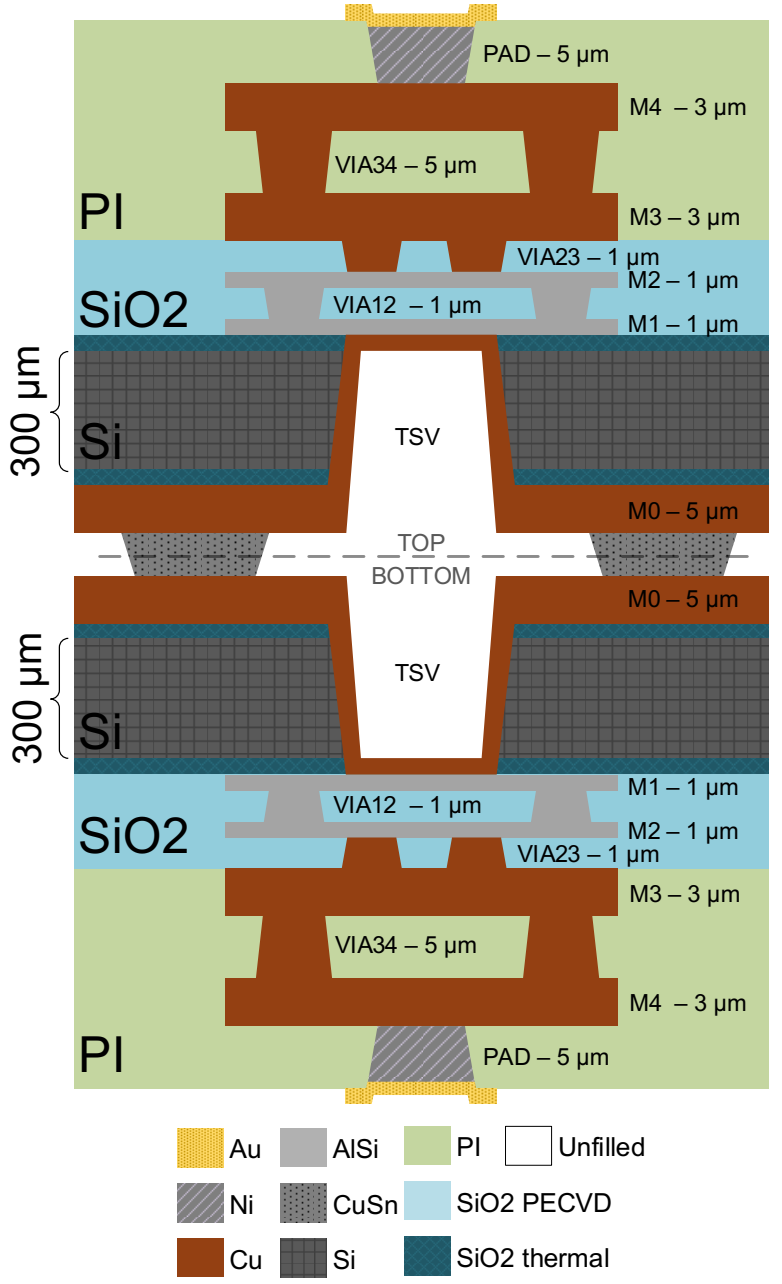
Silicon Interposer ARCHITECTURE

UDS

- 10 Redistribution Layers (RDL) passive interposer
  - 2 x 200mm Si wafers bonded (back to back)
  - TSV
- Collaboration with / Fabricated at Frauhofer IZM (Berlin)



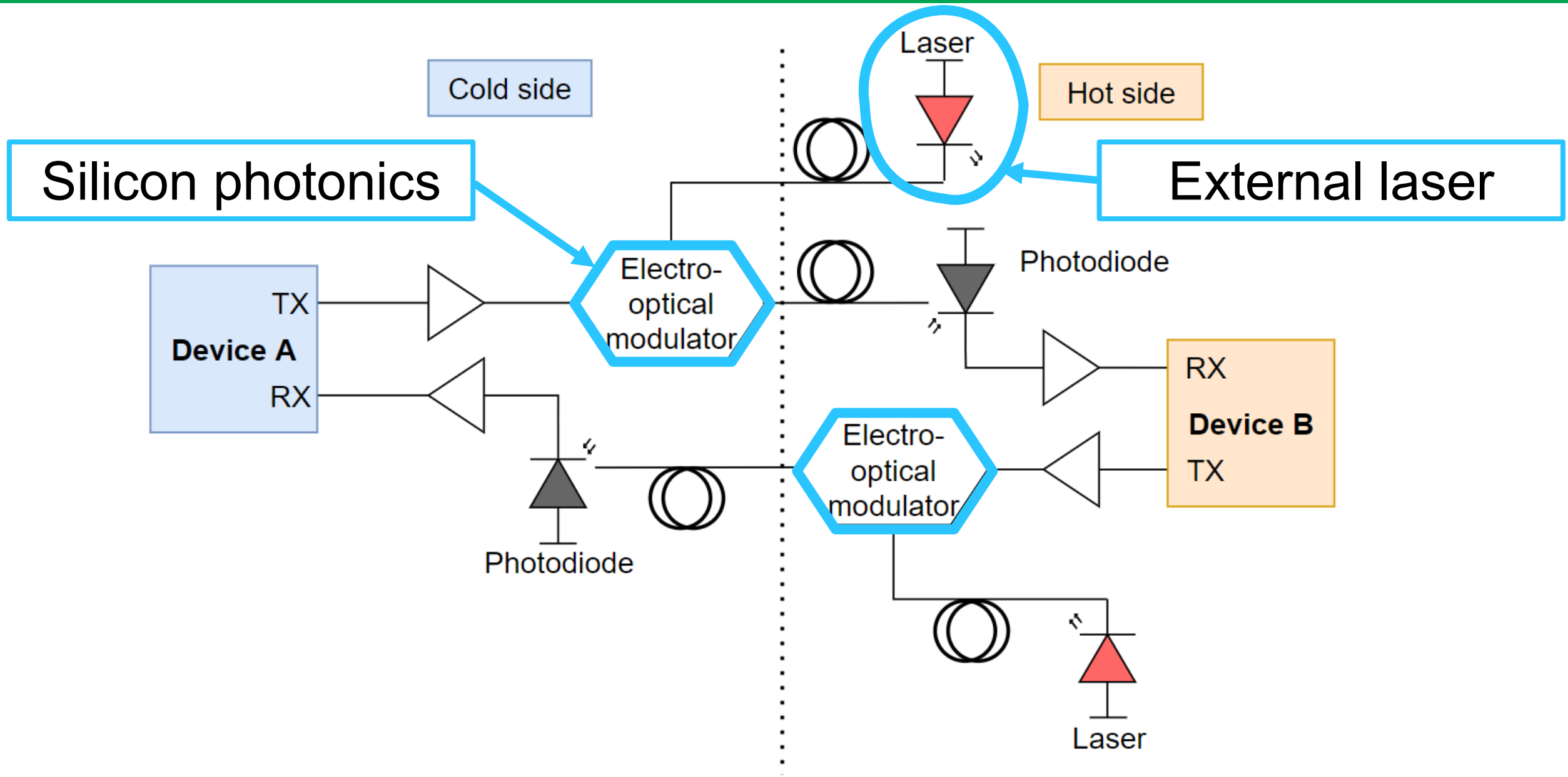
Phase 1: 200 mm test wafer
Sherbrooke-TRIUMF-IZM interposer



Fraunhofer IZM

Optical Communication

Low Power Optical Communication Link



serge.charlebois@usherbrooke.ca

[2] H. Takesue and T. Sugie, *2003*

Silicon Photonics Test Chip – Second Version

UDS

Silicon photonics V2:

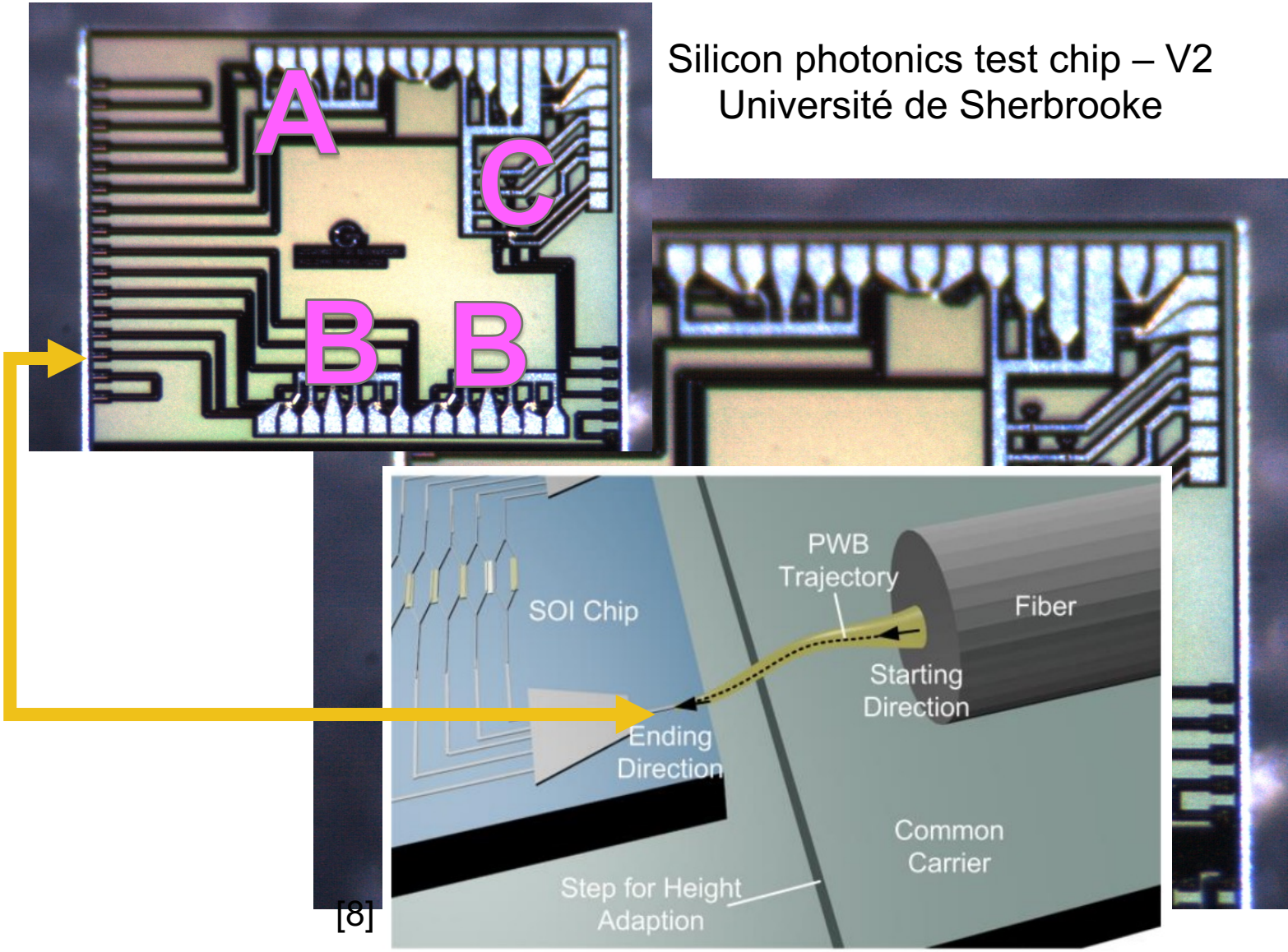
A. Individual components
   - PN Junction Microring
   - Ge Photodiode

B. Sending and receiving structures

C. Wavelength division multiplexing (WDM) test structures

ASIC driver designed

- Submission October 2023



Silicon photonics test chip – V2
Université de Sherbrooke

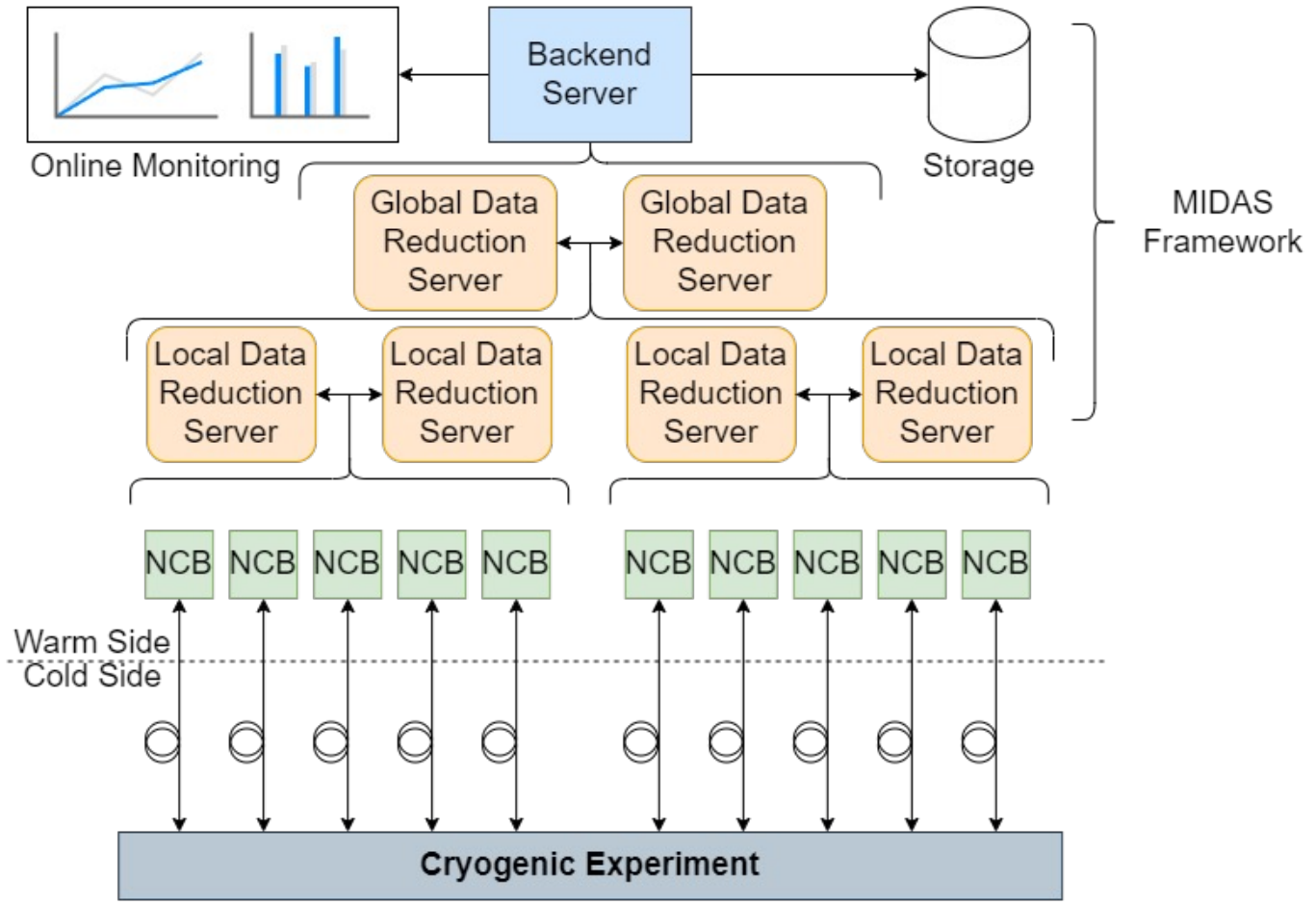
[8]

[8] N. Lindenmann *et al*, 2015

serge.charlebois@usherbrooke.ca

Considering the data path up to the DAQ

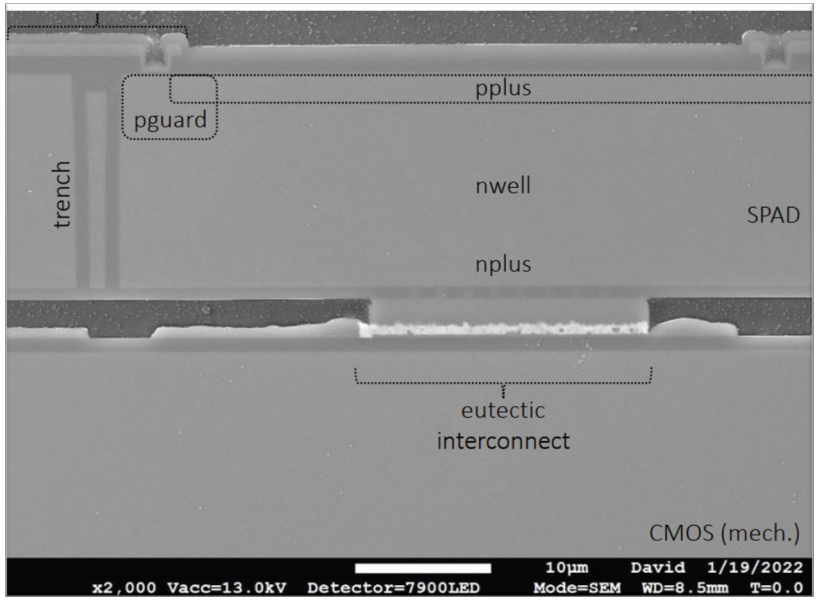
- Using COTS components
  - Scalability and ease of maintenance
- Possible stages of data reduction
  - Keeping all relevant data,
  - and not much more…?
  - AI along the path?
- Time distribution:
  - Timing requirement
  - Size of experiment
  - Power consumption



Conclusion

Conclusion

- We validated the SPAD process and its 3D assembly to a mockup CMOS
  - Wafer thinning and 3D bonding have no/little impact on performances
  - **Good mechanical integrity**
  - Process adjustments to ease manufacturability
- Now starting an optimization phase for the “final” SPAD process
  - Fill factor, junction profile, wavelength tuning (surface bands, ARC…)
- Processing CMOS wafers of the readout circuit
  - Now finalizing the CMOS preparation to allow bonding to the SPAD layer
- Expecting complete 3D Photon-to-Digital Converter and measurements next year!
  - Our dream is to offer this as Multi-Project Wafer runs to the community
- Photon detection module
  - Small tiles demonstrated
  - Started assembly of test of large 8x8 PDC tiles



Thanks for your attention !

We are recruting

Samuel Parent (TDSI)

Frédéric Vachon (UdeS)

serge.charlebois@usherbrooke.ca

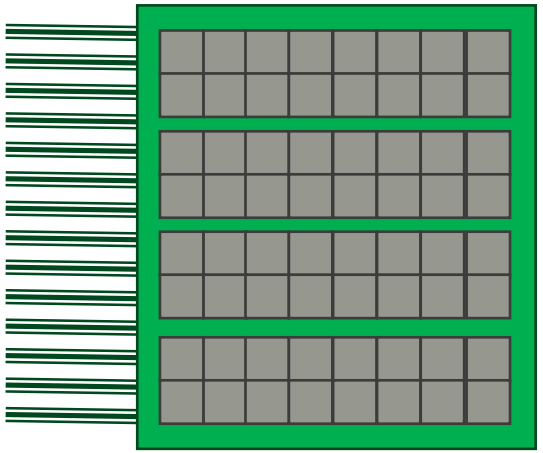
(not so) Random Comments and Ideas

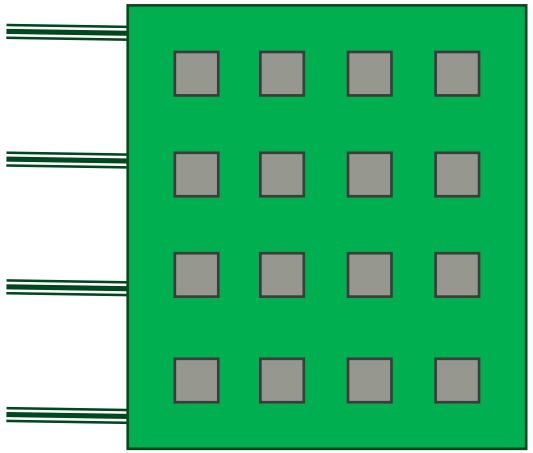
- “RGB like” light detection
  - With grouped SiPMs designs, readout electronics needs to be tuned to the SPAD/SiPM properties
    - Tuning the wavelength sensitivity (most often) influences these SPAD/SiPM properties
  - With a 1-to-1 SPAD-to-readout coupling like in digital SiPM
    - The quenching circuit (~front-end electronics) is essentially insensitive to the SPAD properties
  - With digital SiPM based light detection system, one can think dedicating some PDCs to certain wavelengths
  - The question being:

    Is there physics or discrimination potential in looking at wavelengths other than LXe scintillation?

- VUV sensitivity enhancement
  - Plausible maximum 40% PDE, 50% with tuned antireflective coating
  - In Geiger mode operation: no need for p-e yield calibration (issue with CCDs)
- With a fully digital system
  - Physical channels and the granularity of the light readout can be decoupled: ex. dynamically get more detailed spatial info where there are more photons
- Reduced need for sensor calibration
  - The avalanche gain fluctuations affects the photon detection efficiency
  - No impact on the tuning of the readout electronics to have single photon resolution

Pure scaling

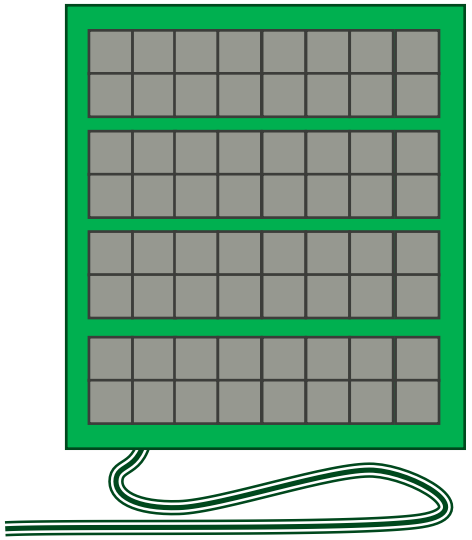




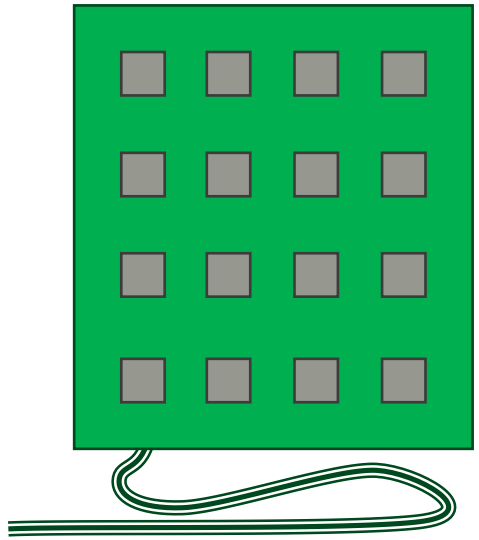
- N channels
- M wires
- P power

- N/4 channels
- M/4 wires
- P/4 power

Looking further or wider when optimizing the detector



With local readout and digital conversion

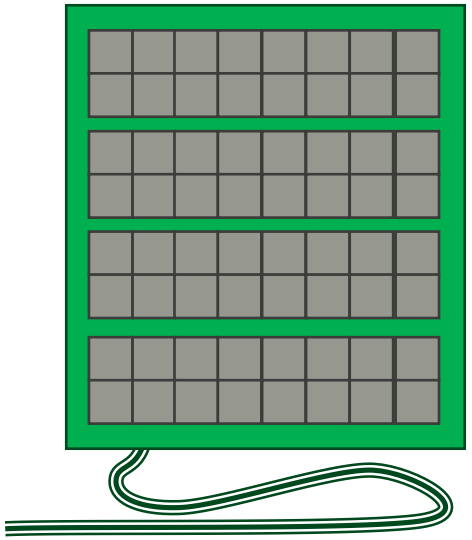


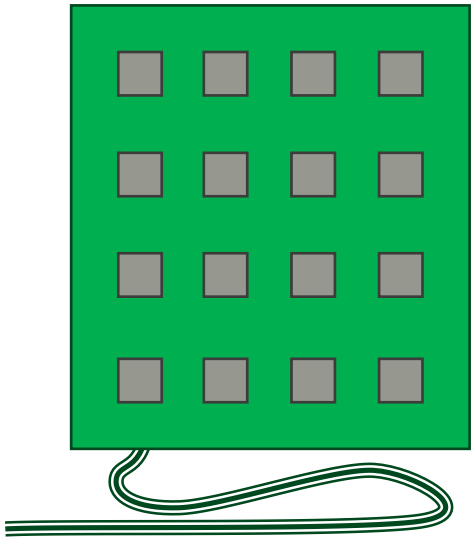
- N channels
  - ~100% light detection coverage
- Power:
  - 50% on data transmission
  - 50% for light readout

- N/4 channels
  - only 25% coverage
- Power
  - Same power for transmission: only 2 bits less needed
  - But power reduced by only 3/8 ~ 37%

Looking further or wider when optimizing the detector

With PDC
or digital SiPMs





- N channels
  - ~100% light detection coverage
- Power:
  - 75% on data transmission
  - 25% for light readout

- N/4 channels
  - only 25% coverage
- Power:
  - Same power for transmission: only 2 bits less needed
  - **But power reduced by only 3/16 ~ 19%**

- A comprehensive light detection system development plan
  - PDC design and fabrication: first devices in 2024
    - Noise and PDE optimization is starting
    - VUV enhancement (collaboration with LBNL)
  - Silicon interposer: low background, thermal expansion matched, scalability
  - Optical communication: low power, high bandwidth, low background, scalability
  - Industrialization:
    - Moving production from 150 mm to 200 mm wafer size
- Large scale experiments (LAr, LXe, GXe) call for significant technology development
  - Most likely similar technology wise
  - With specific optimization and mode of operation
  - Making the investment in Xe worth the cost!

Références and links

- Pratte, J.-F., et al. "3D Photon-to-Digital Converter for Radiation Instrumentation: Motivation and Future Works" (2021) Sensors;21(2):598. doi: 10.3390/s21020598
- Ito, K., et al. "A Back Illuminated 10 m SPAD Pixel Array Comprising Full Trench Isolation and Cu-Cu Bonding with Over 14% PDE at 940nm." 2020 IEEE International Electron Devices Meeting (IEDM). IEEE, 2020
- Parent, S., et al. "Single photon avalanche diodes and vertical integration process for a 3D digital SiPM using industrial semiconductor technologies." 2018 IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings (NSS/MIC). IEEE, 2018.
- Parent, S., et al. “Characterization and Monitoring Platform for Single-Photon Avalanche Diodes in the Development of a Photon-to-Digital Converter Technology.”, 2022 IEEE International Conference on Microelectronic Test Structures Proceedings (ICMTS). IEEE, 2022.
- Giudice et al., High-rate photon counting and picosecond timing with silicon-spad based compact detector modules”, Journal of Modern Optics, 54(23):225–237, 2007
- Parent, S., “Design of a Vertically Integrated Single-Photon Avalanche Diodes, Manufactured at Wafer level, for a Photon-to-Digital Converter Technology”, PhD Thesis (to be published), 2022.
- Jackson et al., “High-volume silicon photomultiplier production, performance, and reliability”, Optical Engineering, 53(8): 081909, 2014.
- Hoenk, M.E. et al., “Growth of a delta-doped silicon layer by molecular beam epitaxy on a charge-coupled device for reflection-limited ultraviolet quantum efficiency”, Applied Physics Letters 61, no. 9 (1992): 1084-1086.
- Vachon, F., Masters thesis, Université de Sherbrooke, 2021.
- Nolet, F. et al., “Quenching Circuit and SPAD Integrated in CMOS 65 nm with 7.8 ps FWHM Single Photon Timing Resolution”, Instruments 2018, 2, 19.
- Nolet, F. et al., “Digital SiPM channel integrated in CMOS 65 nm with 17.5 ps FWHM single photon timing resolution”, Nuclear Instruments and Methods in Physics Research Section A, 912, 29-32, 2018.
- Nolet, F. et al., “A 256 Pixelated SPAD readout ASIC with in-Pixel TDC and embedded digital signal processing for uniformity and skew correction”, Nuclear Instruments and Methods in Physics Research Section A, 949, 162891, 2020.
- Lemaire, W. et al., “Embedded time of arrival estimation for digital silicon photomultipliers with in-pixel TDCs”, Nuclear Instruments and Methods in Physics Research Section A, 959, 163538, 2020.
- Roy, N., et al. “Low Power and Small Area, 6.9 ps RMS Time-to-Digital Converter for 3-D Digital SiPM”, IEEE Transactions on Radiation and Plasma Medical Sciences, 1(6) 2017.
- Therrien, A. C., et al. “Energy discrimination for positron emission thomography using the time information of the first detected photons”, Journal of Instrumentation, 13, 2018.
- Rossignol, T. “Conception d’un circuit de lecture d’une matrice de photodiodes à avalanche monophotonique pour les détecteurs de physique des particules dans les gaz nobles liquéfiés”. Dissertation, Université de Sherbrooke, 2020.
- Loignon-Houle, F., et al., “DOI estimation through signal arrival time distribution: a theoretical description including proof of concept measurements”, Physics in Medicine and Biology, 66(9), pp. 095015, 2021.
- Gundacker, S., et al. “Experimental time resolution limits of modern SiPMs and TOF-PET detectors exploring different scintillators and Cherenkov emission”, Physics in Medicine and Biology, 65(2), pp. 025001, 2020.
- Pagano, F., et al., “A new method to characterize low stopping power and ultra-fast scintillators using pulsed X-rays”, Physics in Medicine and Biology, 67(13), pp. 135010, 2022.
- Herweg, K., et al., “On the Prospects of BaF2 as a Fast Scintillator for Time-of-Flight Positron Emission Tomography Systems”, IEEE Transactions on Radiation and Plasma Medical Sciences, 7(3) 2023.

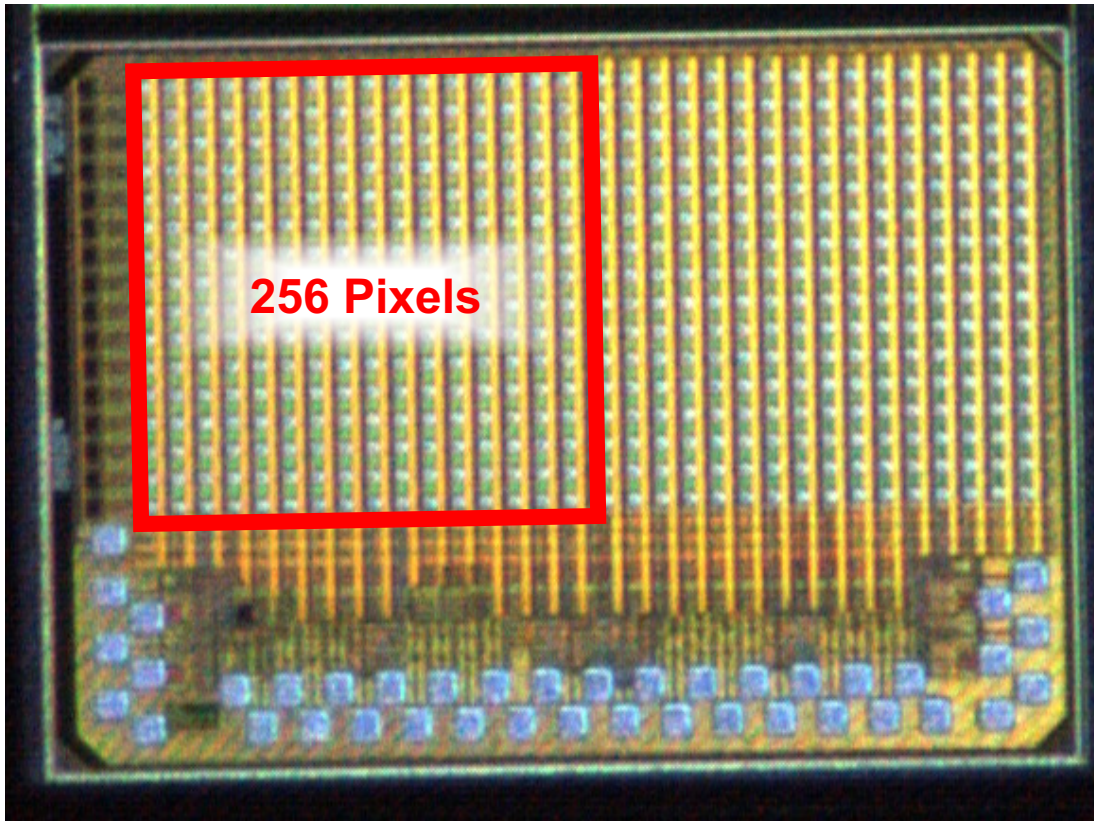
serge.charlebois@usherbrooke.ca

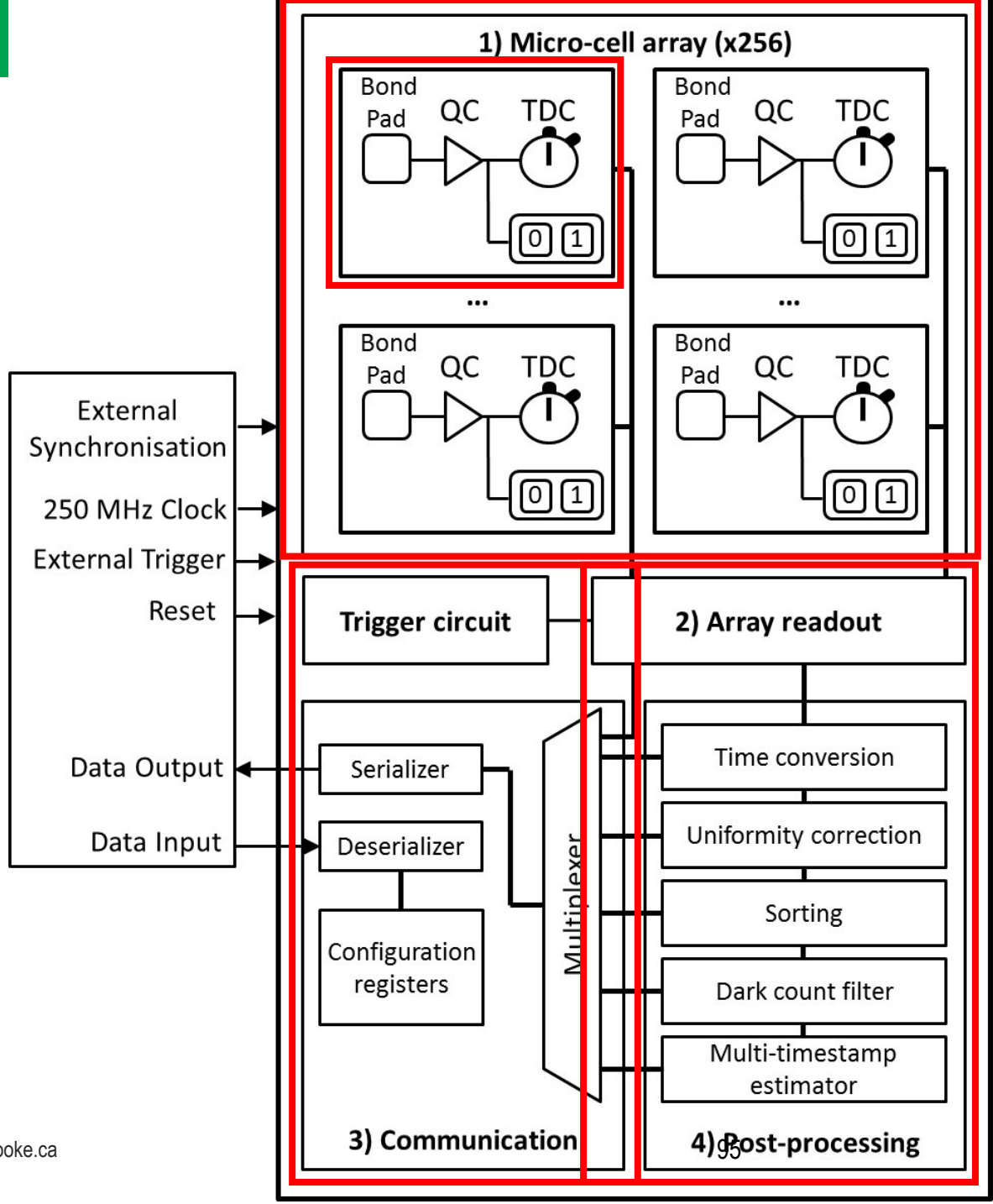
A PDC for PET

(and ToF-CT, and QKD, and wavefront sensing)

Overview of the First 65nm ASIC : PET

- TSMC 65 nm CMOS (GP)
- 16 × 16 pixels in 1.1 × 1.1 mm² (red box)
  Jitter: 18 ps RMS for 256 pixels





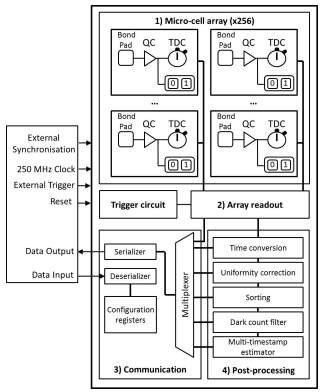
Nolet, Frédéric, et al. "A 256 pixelated SPAD readout ASIC with in-pixel TDC and embedded digital signal processing for uniformity and skew correction." NIMA, 949 (2020): 162891.

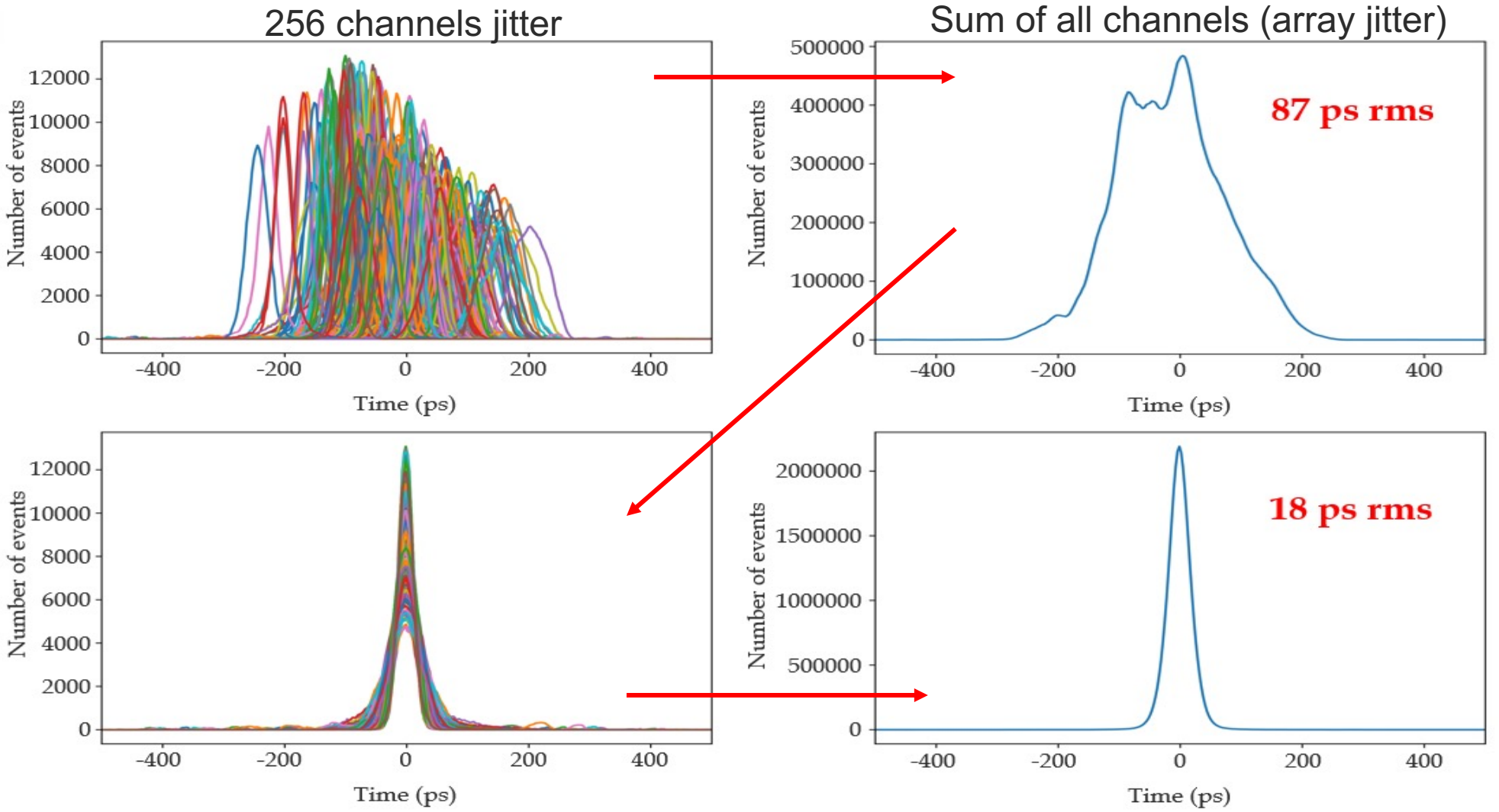
Lemaire, William, et al. "Embedded time of arrival estimation for digital silicon photomultipliers with in-pixel TDCs." NIMA, 959 (2020): 163538.

UNIVERSITÉ DE SHERBROOKE

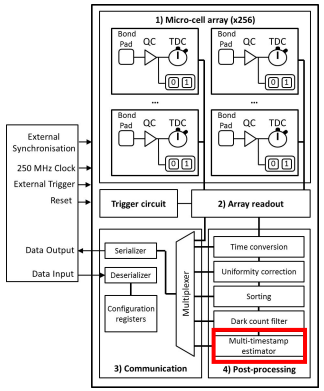
serge.charlebois@usherbrooke.ca

Embedded Digital Signal Processing Example: Uniformity Correction



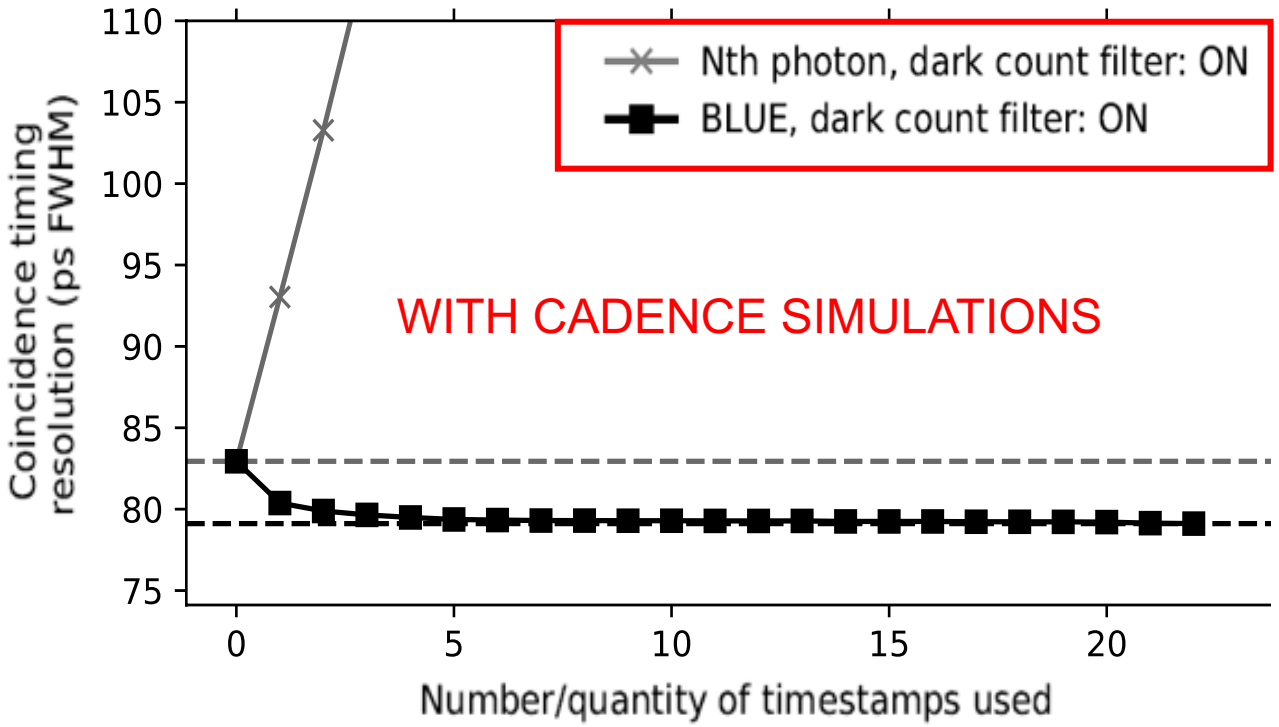


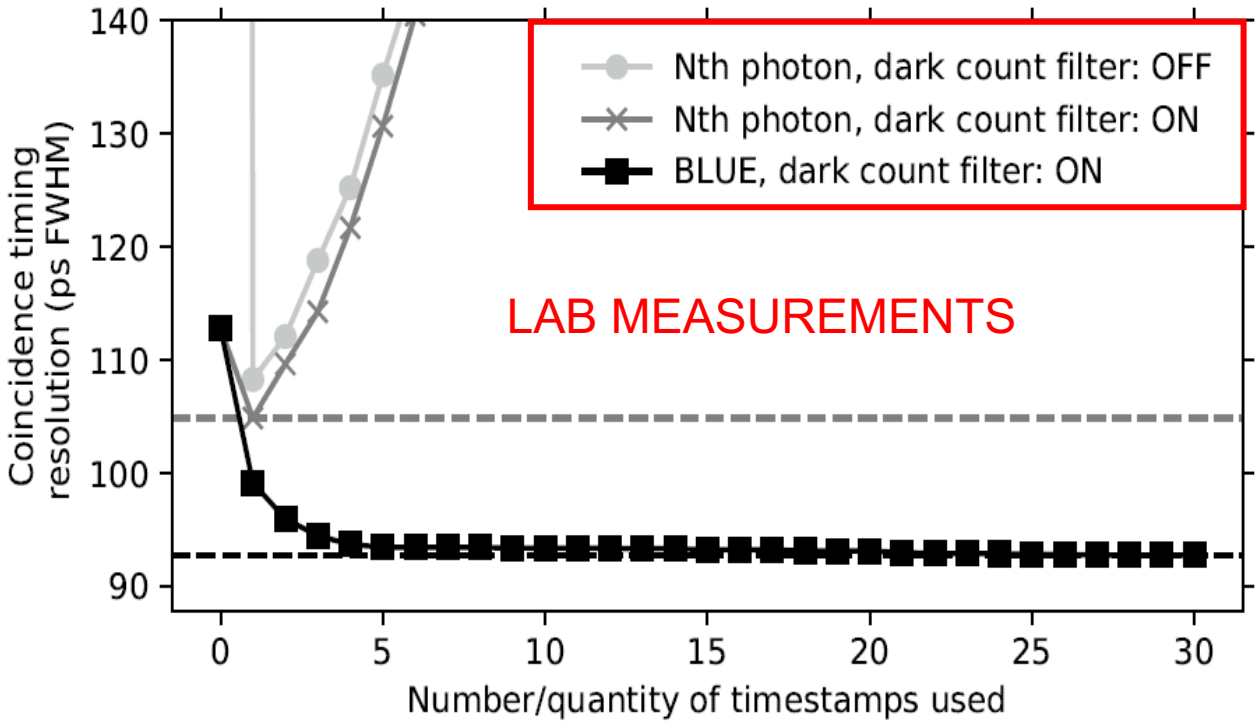
Best Linear Unbiased Estimator



Scintillator characteristic for Geant4 simulation

Material	LYSO
t_{rise} / t_{fall}	70 ps / 40 ns
Size	$1 \times 1 \times 3$ mm^3
Surface treatment	ESR reflector and optical grease
Single SPAD SPTR	35 ps
Array PDE	30%





PET: Energy Discrimination using Timestamps

JINST

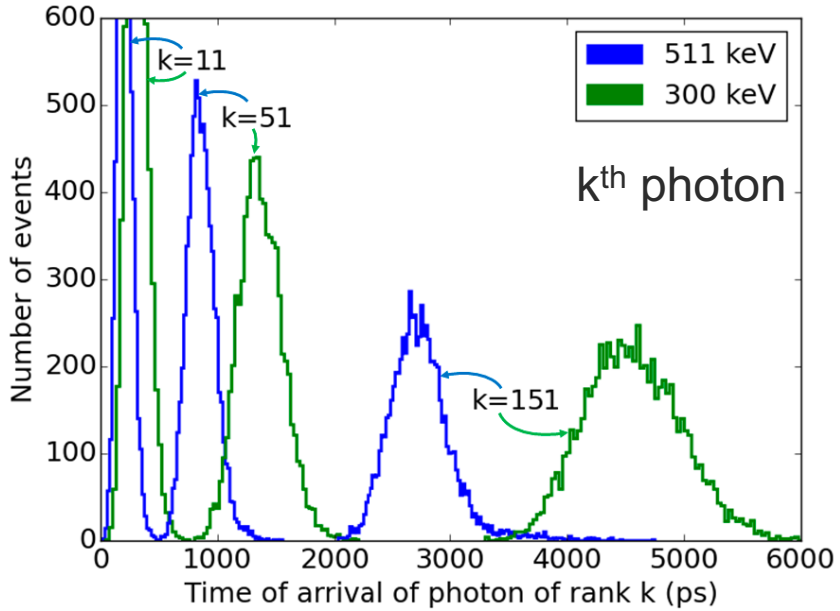
PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

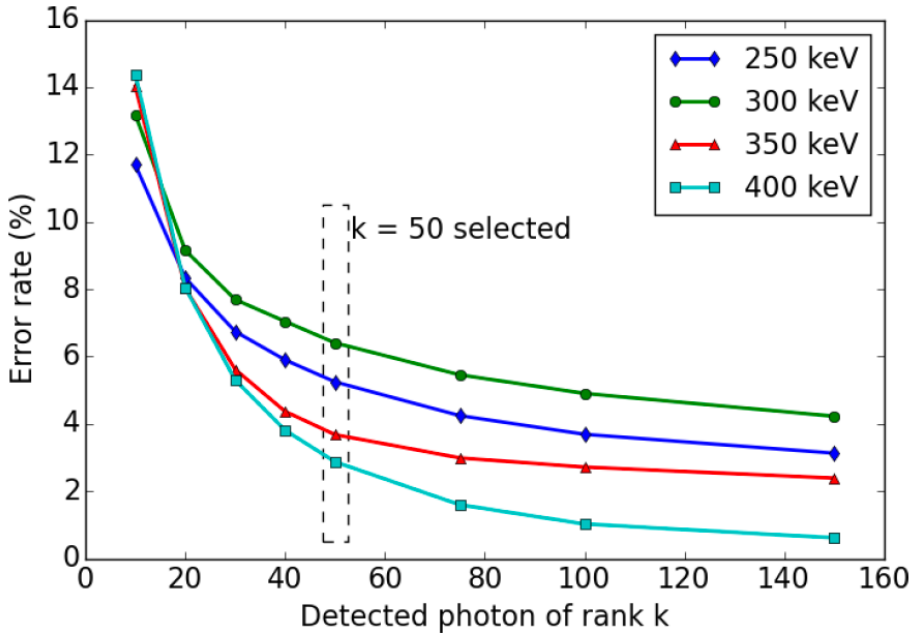
RECEIVED: *July 18, 2017*
REVISED: *October 30, 2017*
ACCEPTED: *January 2, 2018*
PUBLISHED: *January 15, 2018*

Energy discrimination for positron emission tomography using the time information of the first detected photons

A.C. Therrien,[a,1] W. Lemaire,[a] P. Lecoq,[b] R. Fontaine[a] and J.-F. Pratte[a]

- Use the first 5 ns timestamps at the beginning of the event
- The same data used previously with BLUE
- **Strategy based on timestamps**
- **Error rate < 3% for threshold at 400 keV**
  - Dark count rate up to ≤ 100 cps/μm²
  - Time-to-digital converter resolution up to 50 ps
  - PDE: 10 % to 70 %

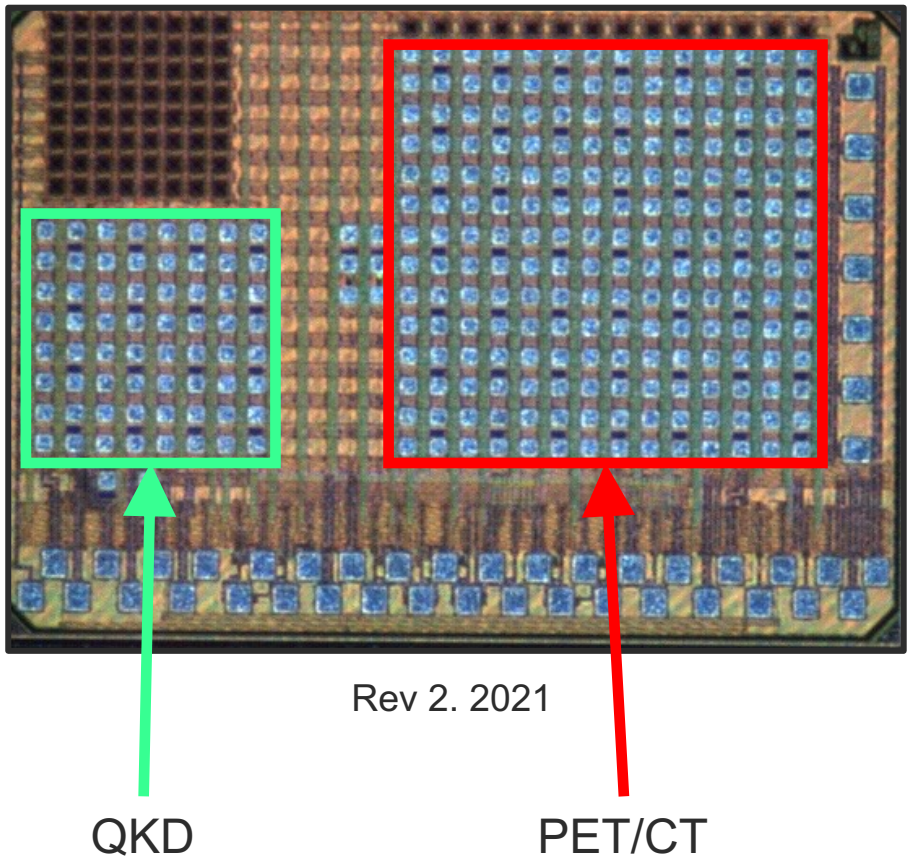


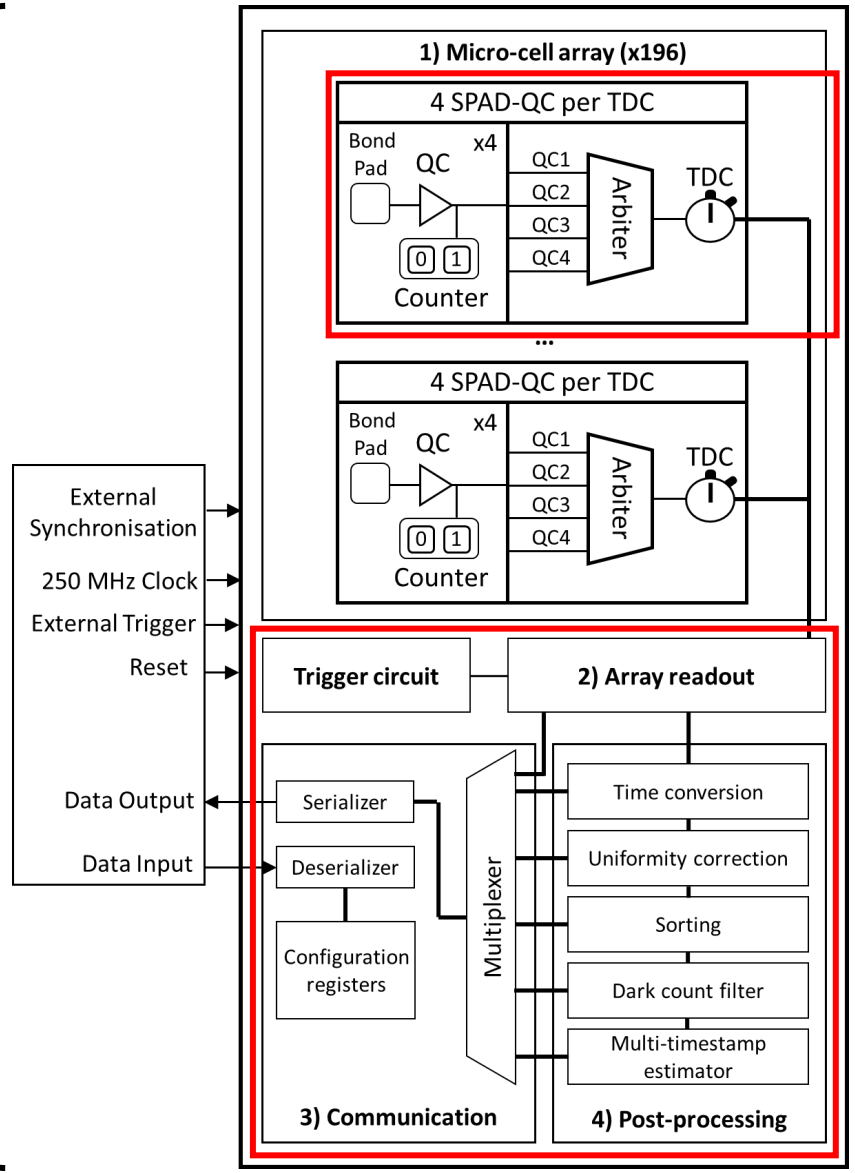


Overview of the Second 65nm ASIC: PET + CT + QKD

UDS

- TSMC 65 nm CMOS
- 16 × 16 pixels in 1.1 × 1.1 mm²





1 Sub-20 ps TDC for 4 SPADs

Advanced digital signal processing:

- Time windowing
- TDC code to time conversion
- Uniformity correction
- Timestamp sorting
- Dark count filtering
- BLUE

And for QKD

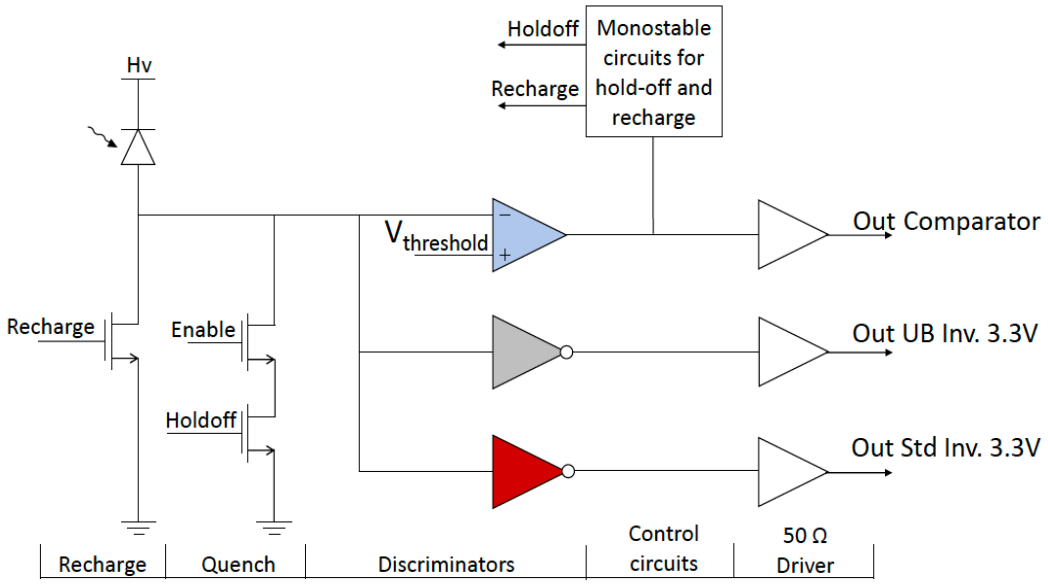
- Time categorization

serge.charlebois@usherbrooke.ca

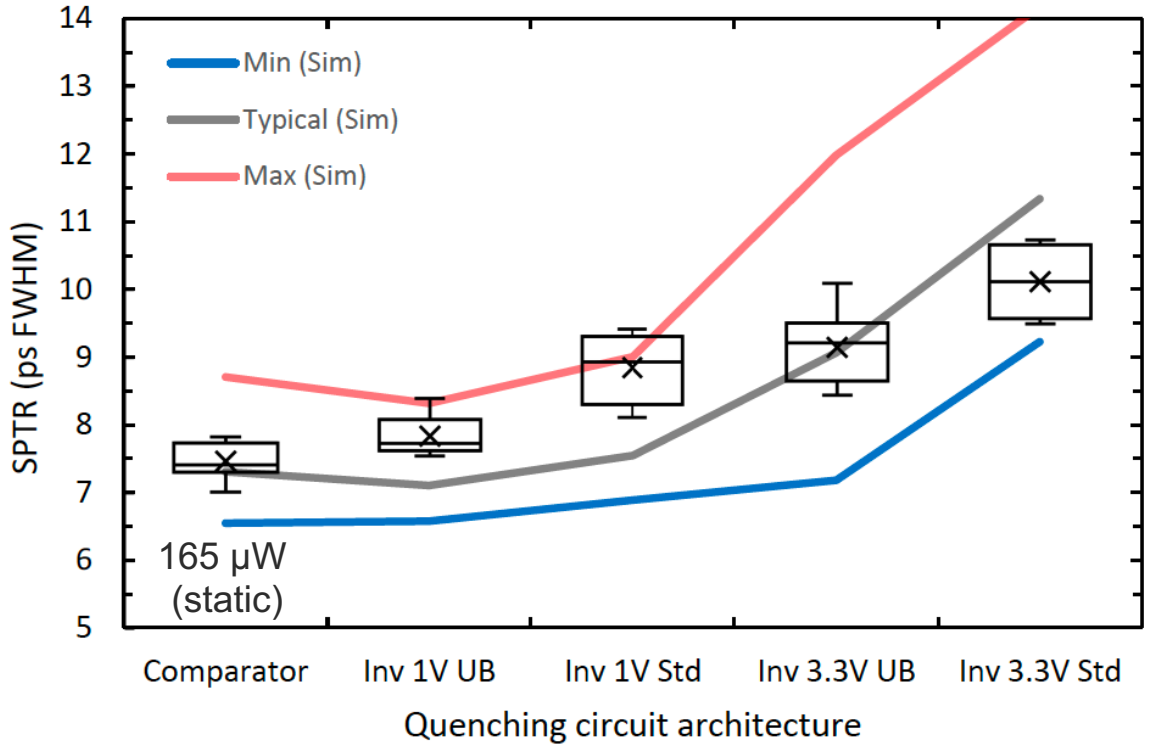
Quenching Circuit Discriminator Architecture Impact SPTR

UDS

- Exploring the impact of the discriminator design on the SPTR
  - TSMC 65 nm CMOS (general purpose)
- 6 designs
  - Also direct comparison between designs
  - Real SPAD signal
- All designs can provide < 10 ps SPTR (FWHM)



- Comparator (open-loop opamp)
- 1V unbalanced inverter 10:1
- 1V balanced inverter
- 3.3V unbalanced inverter 19:1
- 3.3V balanced inverter

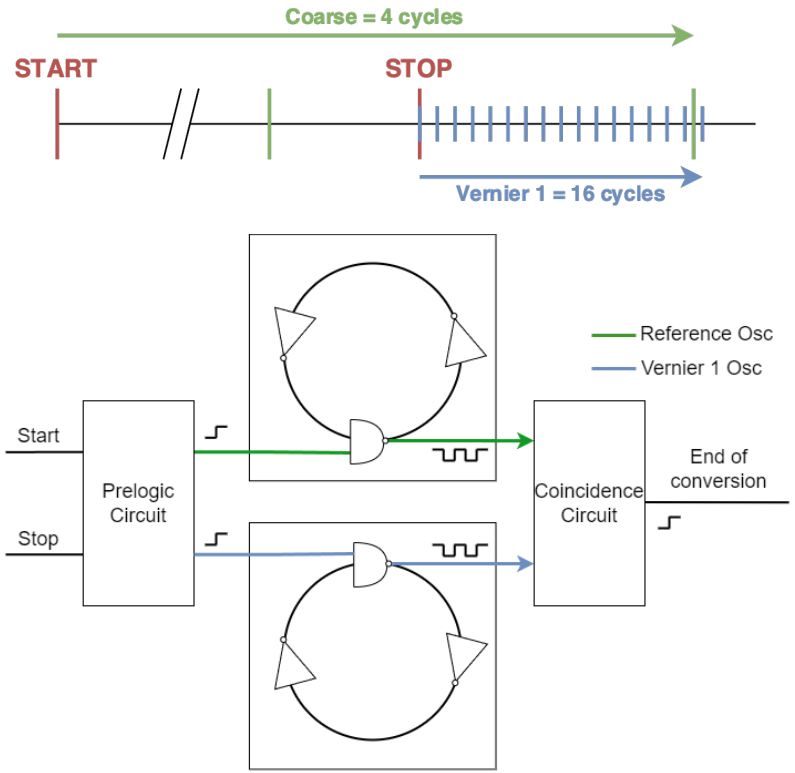


Nolet et al. Quenching Circuit Discriminator Architecture Impact on a Sub-10 ps FWHM Single-Photon Timing Resolution SPAD, Instruments 2023, 7, 16.

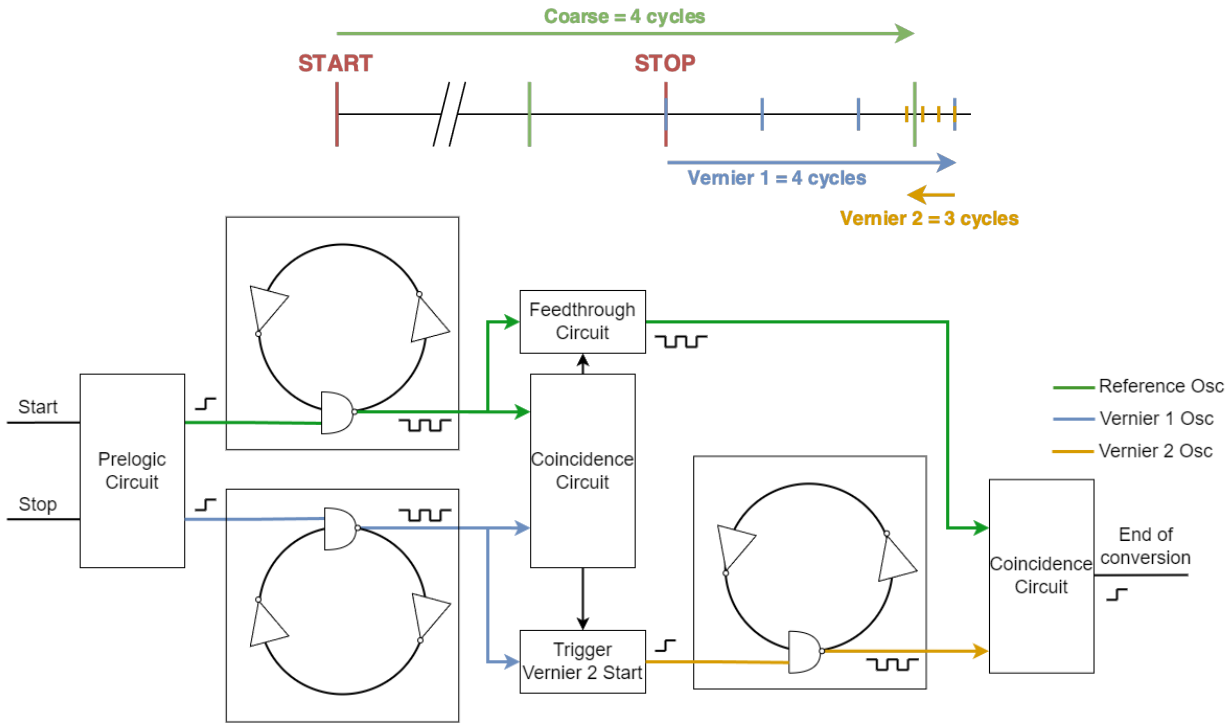
From single-vernier to multi-vernier TDC

- To reduce conversion time (lower number of cycles for a given time interval)
- While improving (or at least maintaining) resolution and precision (jitter)

Single vernier TDC



Multi-vernier TDC

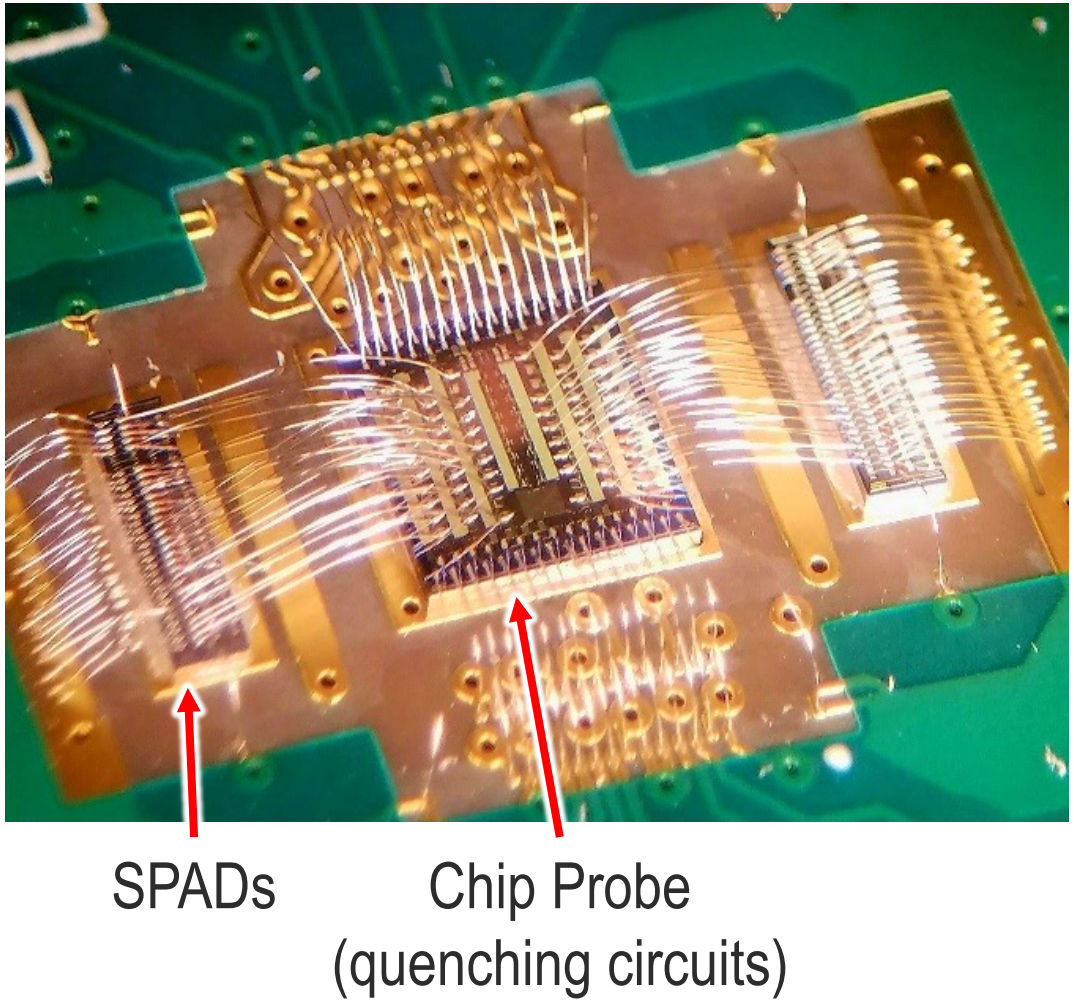


3D SPAD Characterization

Comparison with 2D SPAD

Detailed Characterization of SPAD Performances

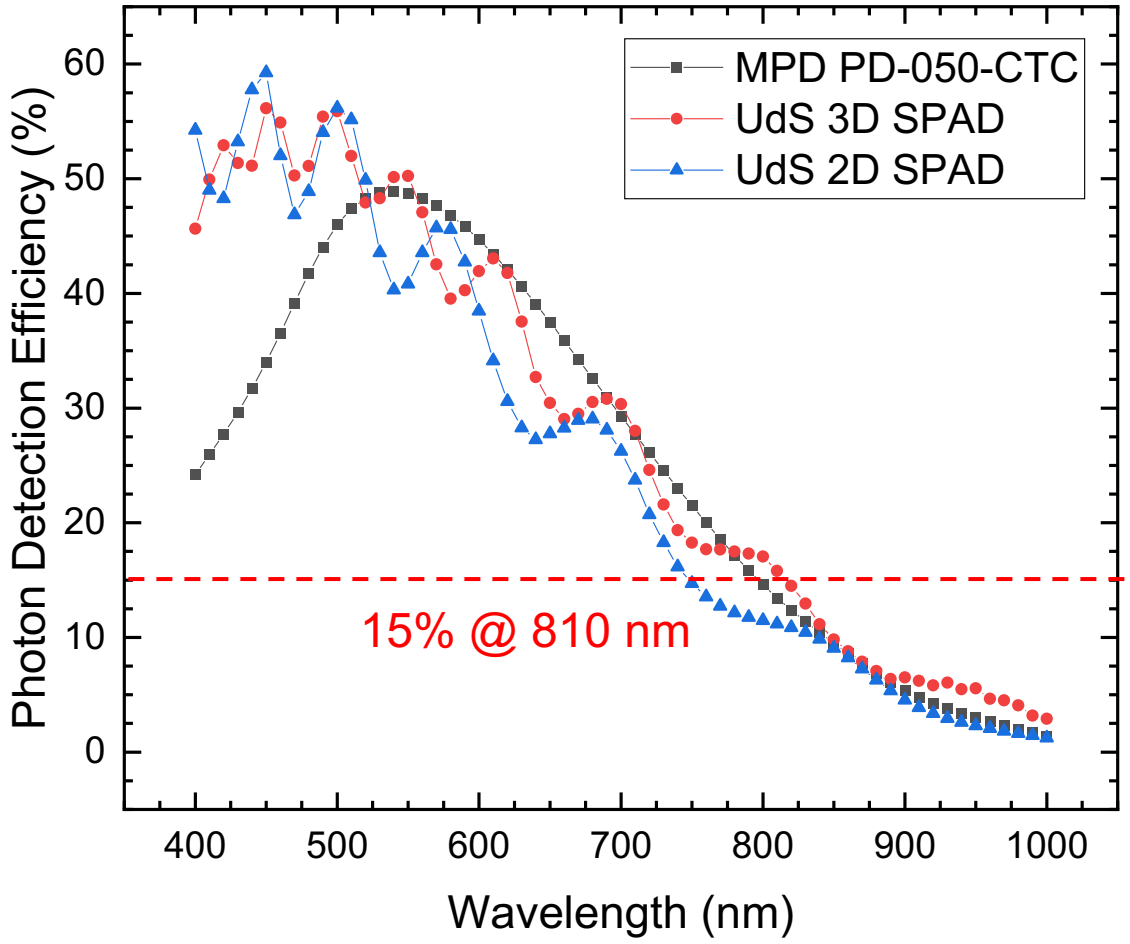
- We perform all relevant characterization in Geiger-mode (not through IV curves)
- Geiger-mode operation provided by the dedicated ASIC called “Chip Probe”
  - Quenches the SPAD (either at the Cathode or anode)
  - Can operate 4 SPADs at once while being connected to
- SPADs need to be diced and wirebonded to the Chip Probe
  - Tedious process



2D vs 3D Measurement: Photodetection Efficiency

UdS

- **Non-optimized** dielectric stack:
  - Nominal ~1 µm oxide layer
  - Next: optimize as application specific ARC
- **PDE peak** ~ 56-59% at 450 nm ~similar.
  - Difference is mostly due to SiO_2 thickness variation
- **PDE** > 15% ~wider range for 3D
  - In the red spectrum. Added thermal steps during the 3D integration process => widening of the depletion region => more red photons capture.



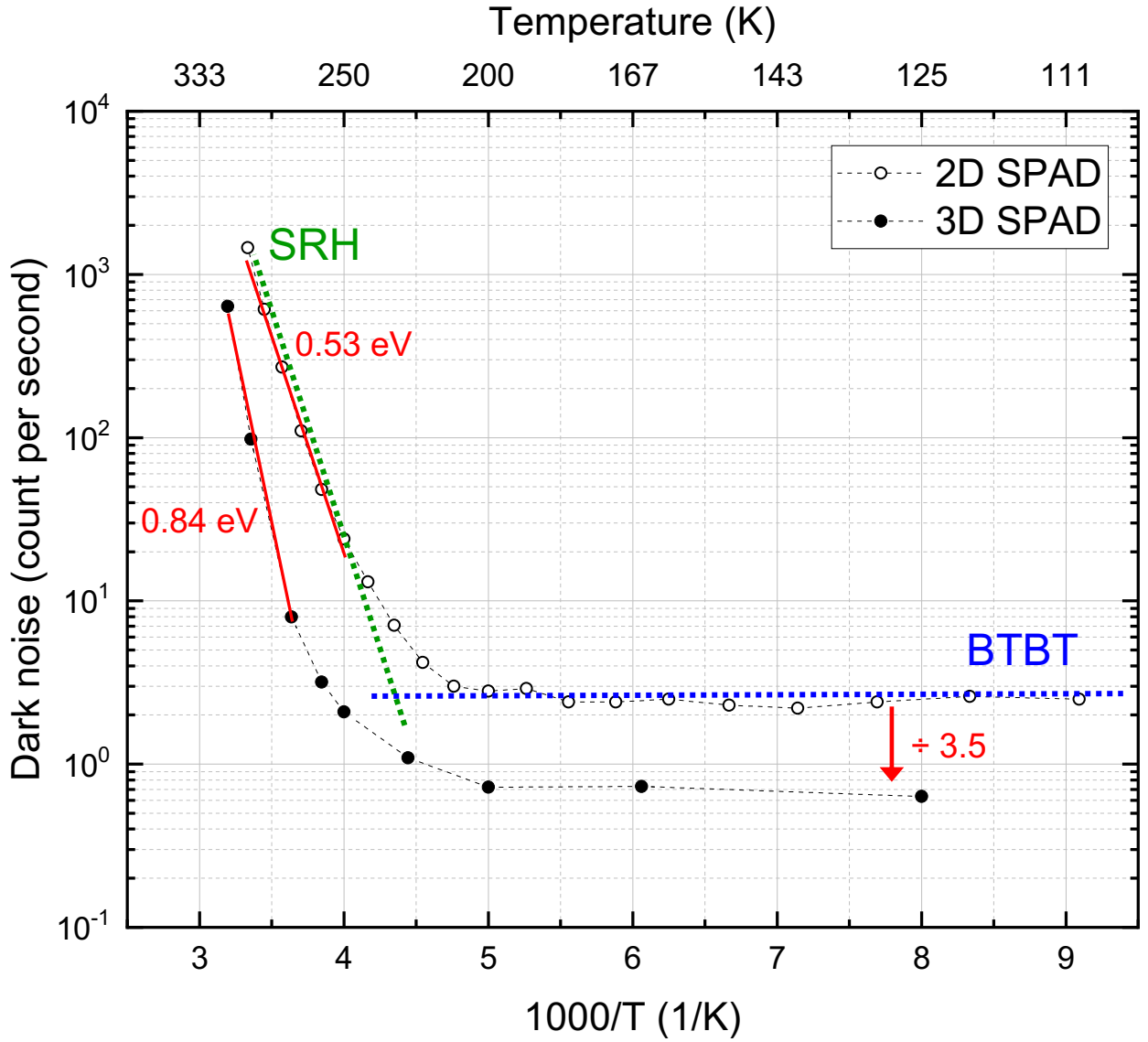
*all measurements done at 20°C, V_{ov} = 25%, t_{ho} = 545 ns, typical.

serge.charlebois@usherbrooke.ca

2D vs 3D Measurement: SPAD Noise

UDS

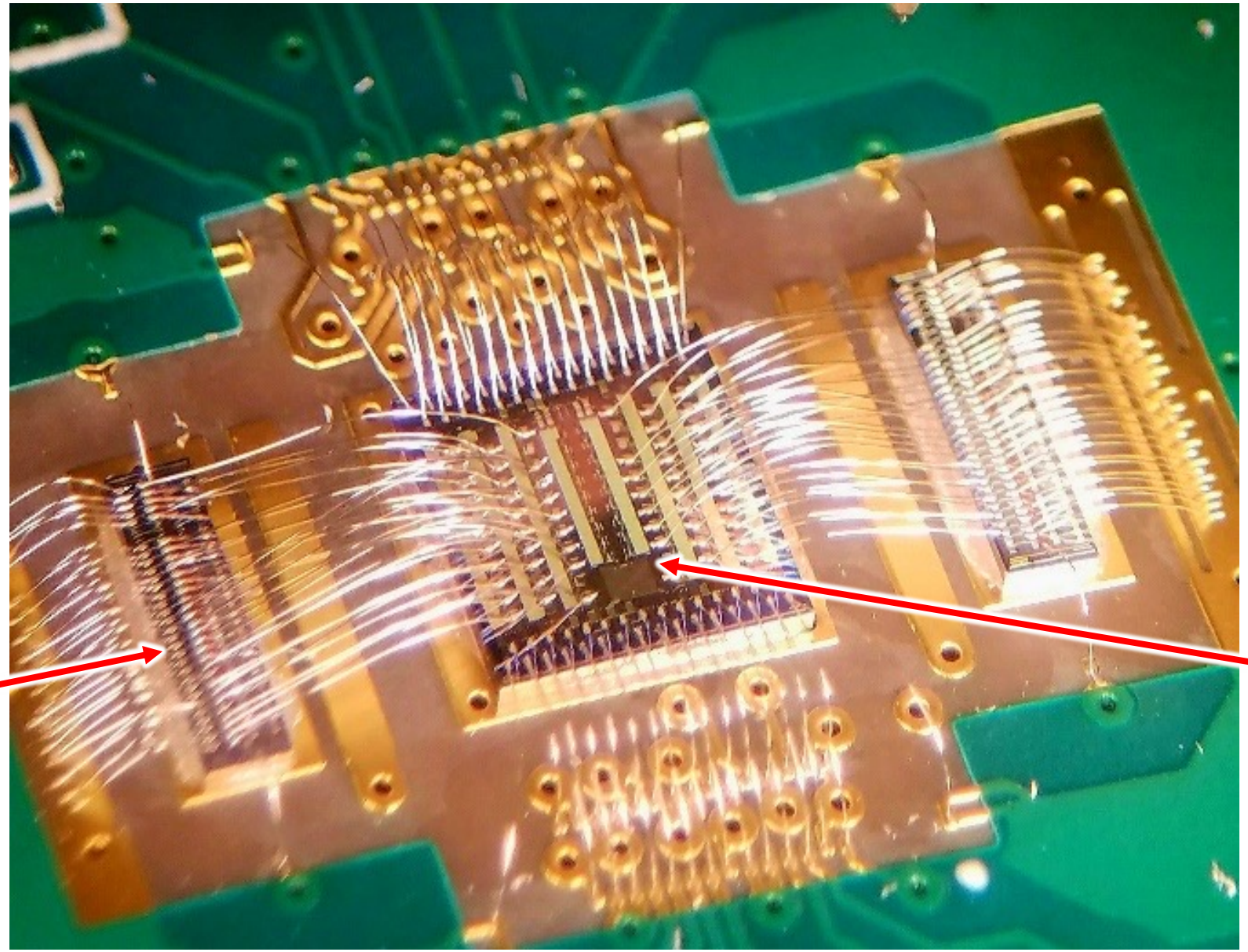
- Trap assisted Shockley-Read-Hall regime (SRH)
  - Slope increases toward gap value
  - Lower density of mid-gap traps
- Band to band tunneling regime (BTBT)
  - Increased breakdown voltage value
  - Lower electric field
- Improved noise performances
  - Added thermal steps during the 3D integration process => widening of the depletion region => lower E field



2D SPAD: V_{ov}=4V (18%) t_{ho}=250ns
3D SPAD: V_{ov}=6V (25%) t_{ho}=1µs

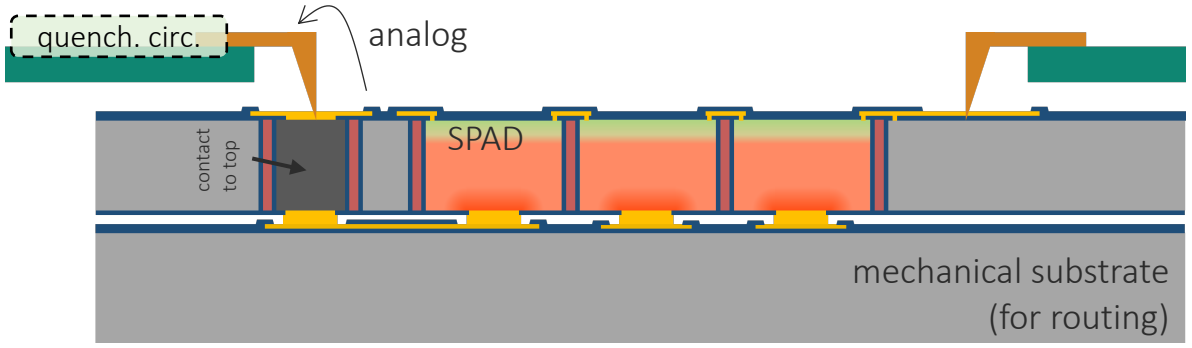
serge.charlebois@usherbrooke.ca

Detailed Characterization of SPAD Performances

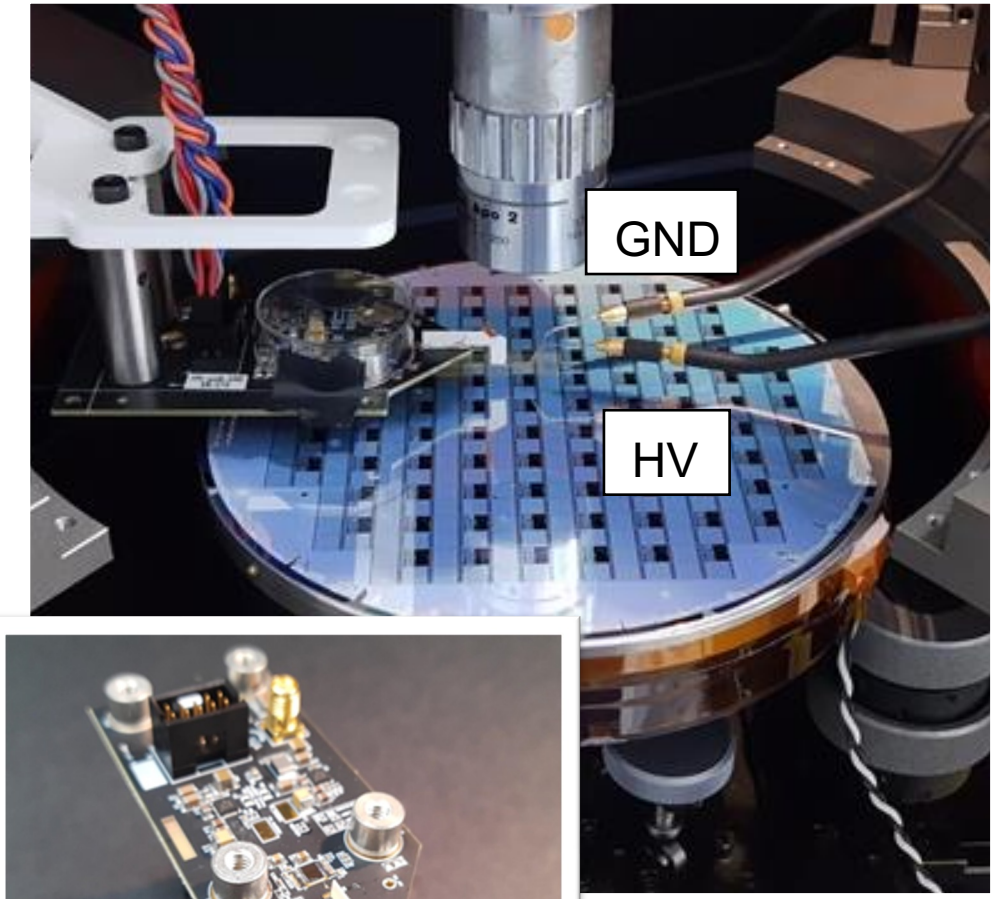


SPAD Wafer-Level Active Probing

- Active probe card with a single probe
  - Chip Probe ASIC on the probe card operates the SPADs in Geiger mode
  - Contact to SPAD through a blade-type needle
- Mesurements: V_{br}, DCR, afterpulsing, relative PDE
- For process monitoring, wafer uniformity, fast testing during R&D
- Cons: added parasitic capacitance => affects quenching/recharge time constants => SPAD behavior (dark noise, afterpulse, etc.)
- 16-channel probe card on the way, to be used also in foundry



Wafer Mapping on 94 single SPADs test sites



3. Parent, Samuel, et al. “Characterization and Monitoring Platform for Single-Photon Avalanche Diodes in the Development of a Photon-to-Digital Converter Technology.”, 2022 IEEE International Conference on Microelectronic Test Structures Proceedings (ICMTS). IEEE, 2022.

serge.charlebois@usherbrooke.ca

Wafer Uniformity Characterization (Geiger-mode)

UDS

- Breakdown voltage

			24.41	24.27	24.32	24.27	24.37			
		24.51	24.49	24.4	24.34	24.34	24.34	24.3	24.38	24.48
24.46	24.34	24.43	24.41	24.38	24.38	24.3	24.32	24.32	24.2	24.29
24.48	24.37	24.45	24.41	24.43	24.35	24.26	24.49	24.41	24.18	24.04
24.45	24.45	24.45	24.4	24.4	24.23	24.21	24.18	24.23	24.05	24.04
24.34	24.43	24.46	24.48	24.32	24.32	24.32	24.3	24.16	24.12	24.09
24.23	24.46	24.45	24.43	24.32	24.24	24.23	24.24	24.3	24.09	24.13
24.41	24.26	24.35	24.32	24.27	24.12	24.26	24.35	24.23	24.18	24.27
	24.38	24.41	24.26	24.16	24.16	23.93	24.26	24.16	24.21	
			24.35	24.23	24.16	23.9	24.26			

Avg.	24.3
Median	24.3
Min	23.9
Max	24.5
Std Dev	0.13 (0.5%)

Dispersion similar
to analog SiPM technologies

- Photodetection efficiency at 462 nm
(relative to median, OV=6 V (25%))

			-1%	7%	7%	-2%	-2%			
		-4%	4%	2%	6%	4%	-4%	-3%	-2%	8%
-2%	1%	4%	-3%	-1%	3%	3%	1%	2%	9%	4%
0%	-2%	1%	-4%	-5%	-2%	-1%	0%	-4%	-2%	5%
1%	-3%	4%	1%	-1%	-2%	3%	-2%	0%	1%	5%
-2%	-4%	1%	6%	4%	3%	1%	-5%	-2%	-4%	6%
0%	3%	-8%	-1%	3%	-4%	-3%	-5%	5%	0%	-2%
1%	-4%	7%	0%	-4%	-7%	-3%	-4%	1%	8%	-2%
	6%	-3%	0%	4%	4%	7%	-3%	6%	0%	
			7%	0%	-5%	3%	7%			

Avg.	0.5%
Median	0%
Min	-7.7%
Max	+8.9%
Std Dev	4%

Dispersion similar
to analog SiPM technologies (<5%)

serge.charlebois@usherbrooke.ca

Dark Noise Rate Wafer Uniformity Characterization (Geiger-mode)

UDS

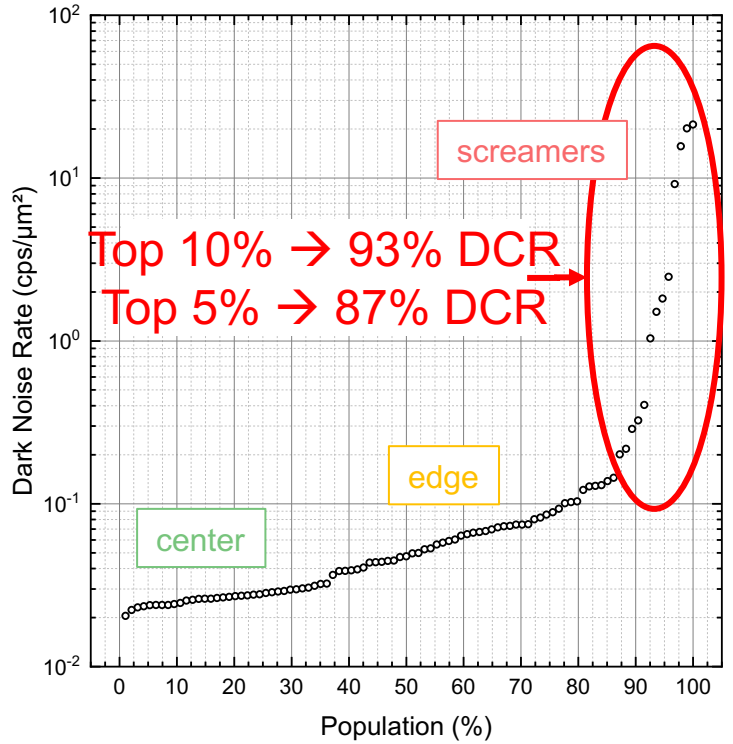
- Median DCR of ~0.05 cps/um2
- Outliers represent less than 10% of the population and are typical for SPAD (point defects) [1]
- Concentric distribution of the dark noise is caused by metal contacts misalignment during in-process issues (known solution underway).

Dark noise rate (cps/µm²)

			65E-3	56E-3	288E-3	41E-3	16E+0		
	80E-3	50E-3	39E-3	39E-3	31E-3	26E-3	21E+0	40E-3	47E-3
82E-3	66E-3	45E-3	2E+0	27E-3	27E-3	23E-3	26E-3	32E-3	53E-3	60E-3
73E-3	59E-3	9E+0	28E-3	24E-3	28E-3	23E-3	25E-3	30E-3	129E-3	72E-3
122E-3	50E-3	29E-3	24E-3	24E-3	30E-3	22E-3	27E-3	32E-3	58E-3	75E-3
2E+0	2E+0	44E-3	30E-3	26E-3	20E-3	24E-3	26E-3	29E-3	45E-3	74E-3
201E-3	68E-3	39E-3	27E-3	25E-3	24E-3	26E-3	27E-3	29E-3	48E-3	70E-3
217E-3	101E-3	324E-3	44E-3	20E+0	37E-3	28E-3	30E-3	44E-3	67E-3	93E-3
	130E-3	102E-3	1E+0	64E-3	73E-3	86E-3	53E-3	89E-3	144E-3	
			75E-3	138E-3	103E-3	405E-3	128E-3		

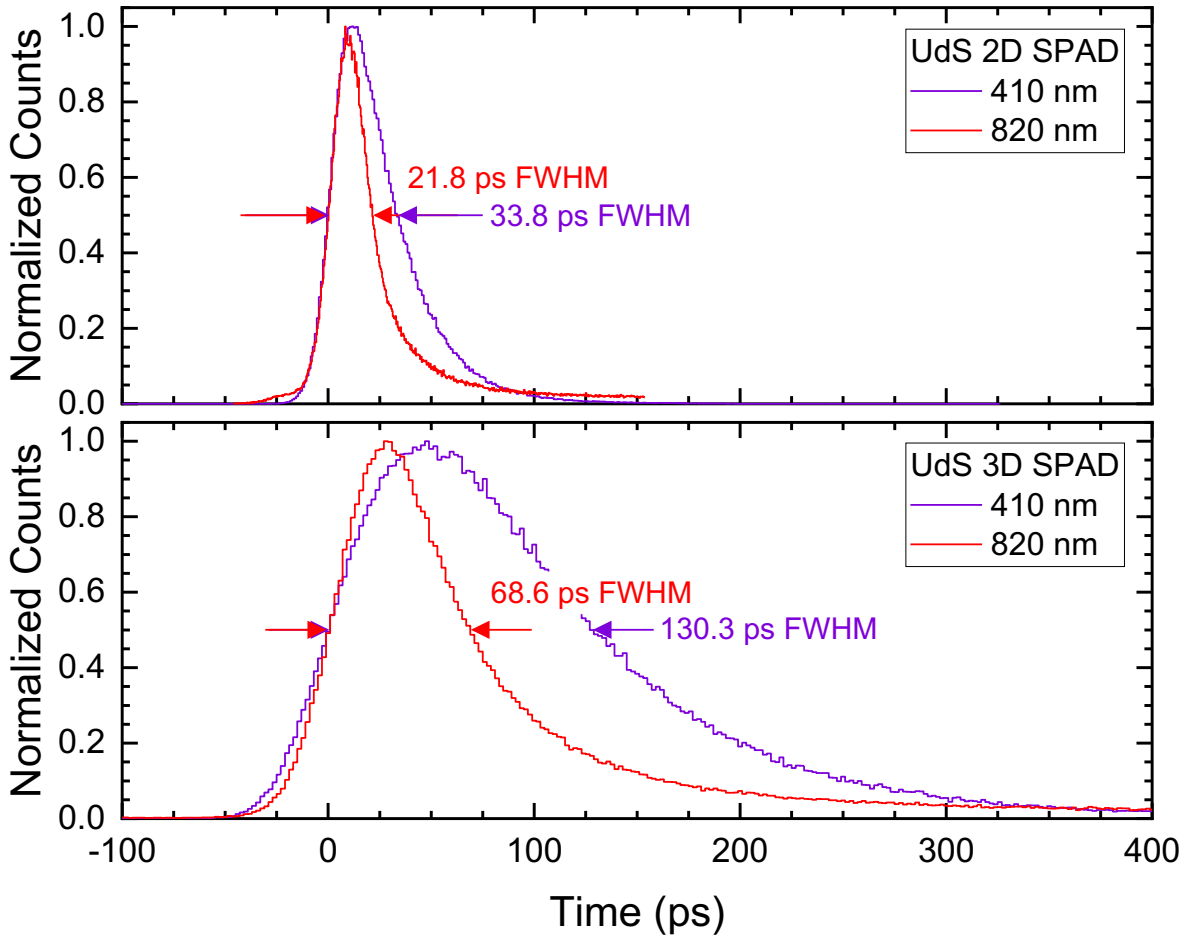
3D SPAD: V_{ov}=4.8V (20%) t_{ho} =1µs

Avg.	839E-3
Median	48.6E-3
Min	20.5E-3
Max	21.3E+0

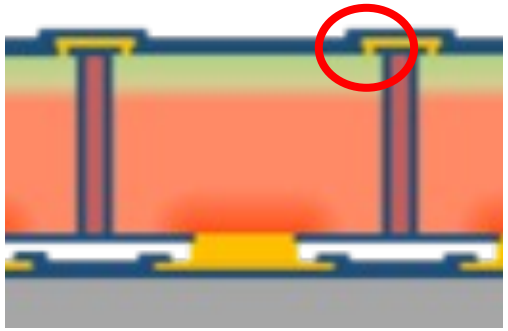


[1] Giudice et al., High-rate photon counting and picosecond timing with silicon-spad based compact detector modulesJournal of Modern Optics, 54(23):225–237, 2007

2D vs 3D Measurement: Single-Photon Timing Resolution



- The increased jitter of the 3D SPADs is linked to a flawed contact (non-ohmic and high valued)
  - Reduces the signal rising slope



- Process correction confirmed
  - New timing measurements to come fall 2023

Comparing 3D SPADs to their 2D Equivalent

UdS

	UdS 2D SPAD	UdS 3D SPAD	
Breakdown voltage (V)	typ. 22.1	typ. 24.3	✅
Dark Count Rate (cps/µm²)	typ. 0.78	0.05 (median @ RT) Lowered at cryogenics	✅ ✅
Photon Detection Efficiency peak (% at λ)	59 (450 nm)	56 (450 nm)	OK
Photon Detection Efficiency >15%	400 – 740 nm	400 – 810 nm	✅
Afterpulsing (%)	< 5	[10 – 15]	❌
Single-Photon Timing Resolution (ps FWHM at λ)	34 (410 nm) 22 (820 nm)	130 (410 nm) 69 (820 nm)	⚠️

*all measurements done at 20°C, V_{ov} = 25%, t_{ho} = 545 ns, typical.

- **V_{bd}:** increased by ~2 V
  - Added thermal processing during 3D bonding
  - More dopant diffusion
  - Lower breakdown field/voltage
- **DCR:** lowered by ×10
  - Lower peak E_{field} decreases the field-enhanced noise generation.
  - Reduces mid-gap state density.
  - Lower band-to-band tunneling
- **Afterpulsing:** increased at low T
  - But mitigation possible through configurable hold-off delay
- **SPTR:**
  - Contact issue being corrected

Starting dedicated optimization runs in 2024

serge.charlebois@usherbrooke.ca