BERKELEY LAB
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U.S. DEPARTMENT OF ENERGY
Office of Science

Introduction to Analog-to-Digital Converters

HEPIC Summer School

Carl Grace 6/21/2023

Lawrence Berkeley National Laboratory

Lawrence Berkeley National Laboratory

MOST DIVERSE US NATIONAL LABORATORY

Key Strengths

Physical Sciences, Computing, Biosciences, Earth and Energy Sciences, Materials, and Nanotechnology

EXCELLENCE & DIVERSITY

3500 employees

1000 students

1750 visiting researchers

NATIONAL USER FACILITIES

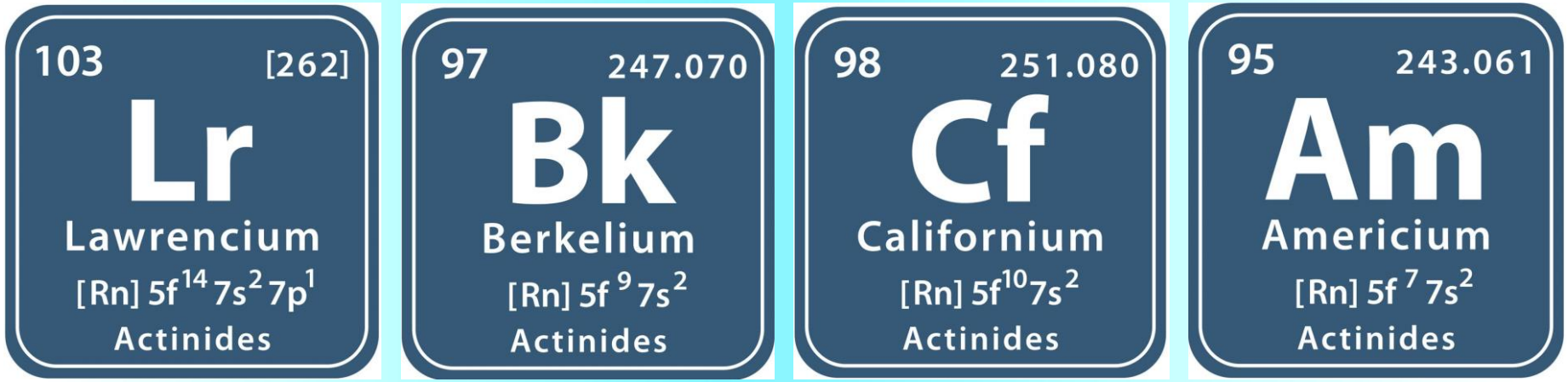
- Advanced Light Source
- National Energy Research Scientific Computing Center
- Energy Sciences Network
- Joint Genome Institute
- Molecular Foundry (including National Center for Electron Microscopy)

14 NOBEL PRIZES

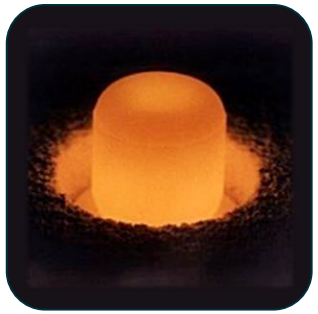
Most recent: 2020 Nobel Prize in Chemistry for co-discovery of CRISPR gene editing (Prof. Jennifer Doudna)

Fun Fact

LBNL may be the only workplace where you can **write your address in elements!**



All discovered by LBNL along with 12 other elements!



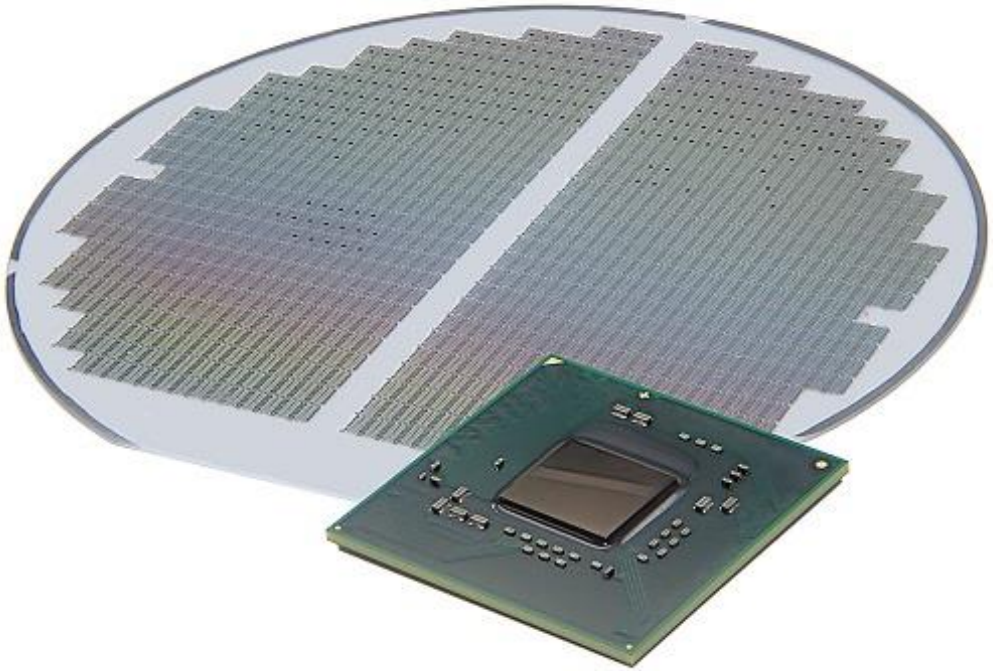
Plutonium discovered in 1940 at LBNL

Radiation hazard trefoil invented in 1946 at LBNL

Agenda

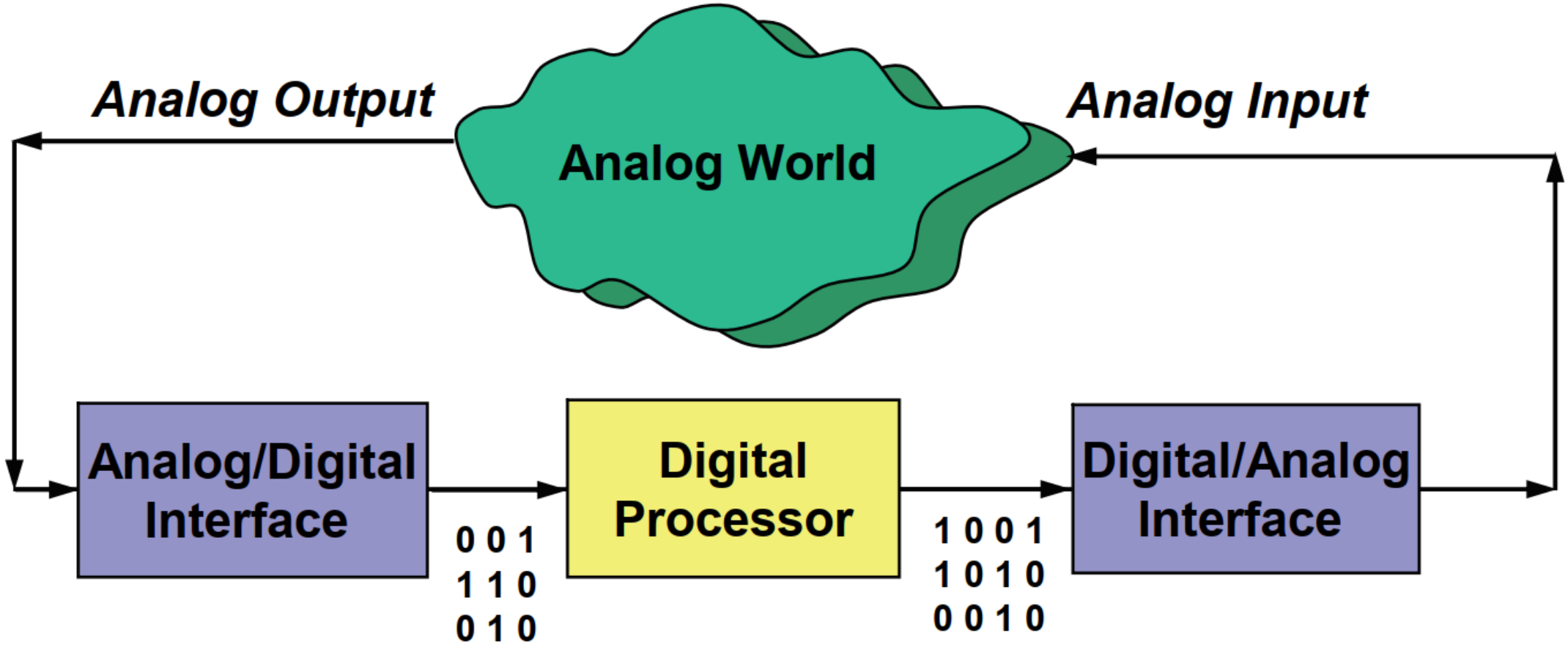
- ADC Overview
- ADC Specifications
- ADC Architectures
- ADCs for High-Energy Physics
- Design Study: Oversampling ADC

Focus will be on ADC architectures relevant to HEP



ADC Overview

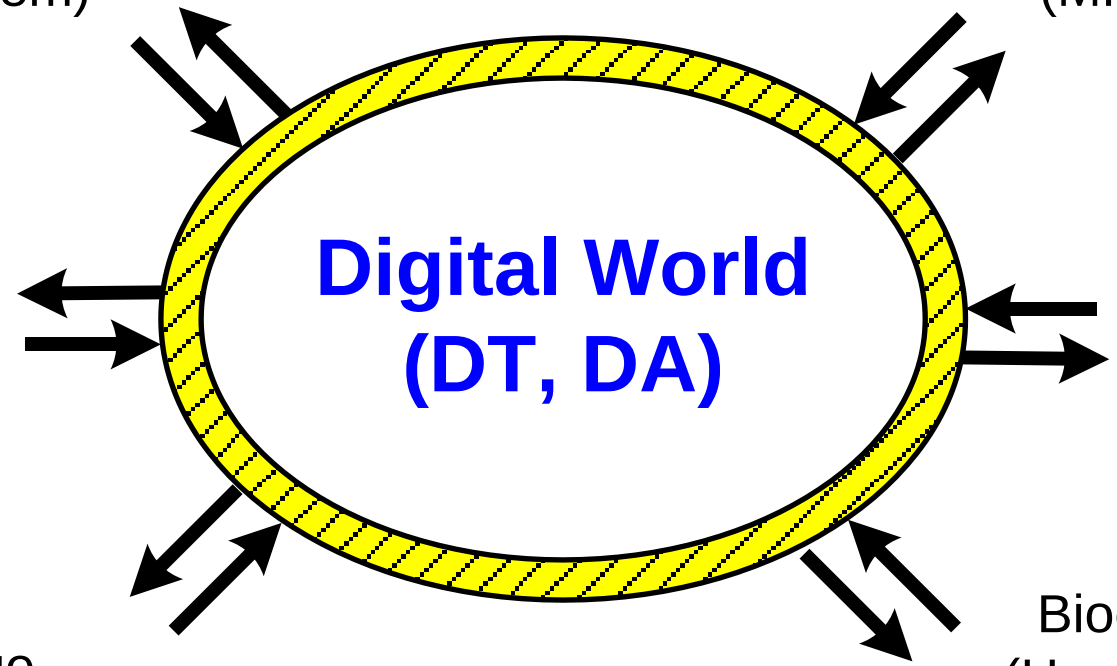
What are ADCs?



Analog-to-Digital Converters (ADCs) provide the link between the analog world and digital processing

In HEP, detector outputs are usually analog (e.g. charge pulses) and ADCs pace experimental improvements

ADC Applications



Phone Lines, Cables
(DSL, Cable Modem)

Audio
(MP3, Hearing Aid)

Video
(Dig. Camera, LCD TV,
TFT Display)

E&M Waves
(Cellphone, Radio,
GPS)

Mechanical Transducers
(Car/Airplane Sensors,
MEMS, Nanopore)

Digital Storage
(DVD, Hard Disk, Flash)

Biochemical Sensors
(Hazard detection, Drug
Delivery, Lab-on-a-Chip)

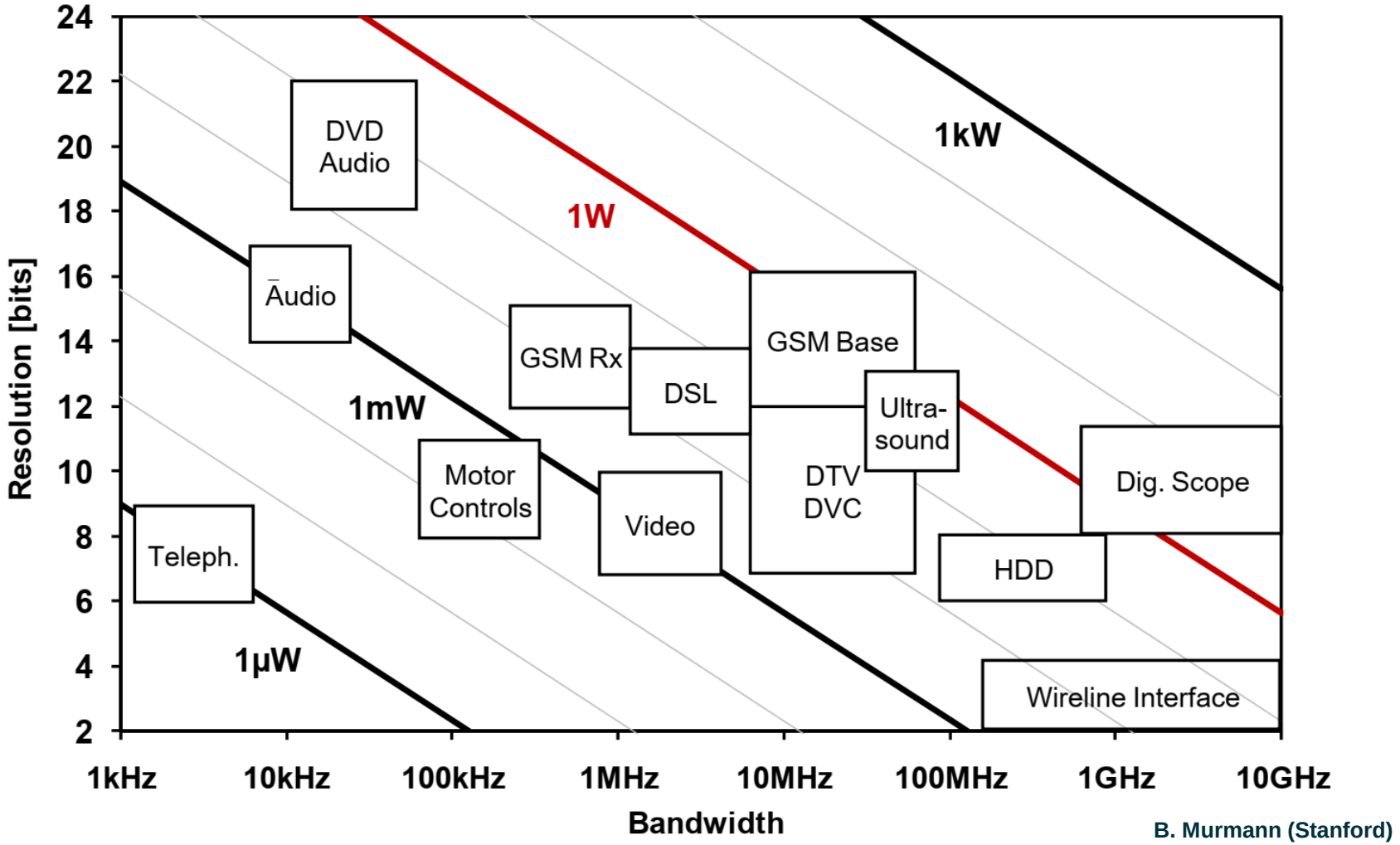
Paul Gray (UCB)

ADC Applications

Resolution: $\log_2$ of quantization levels

Sampling Rate: number of conversions/sec

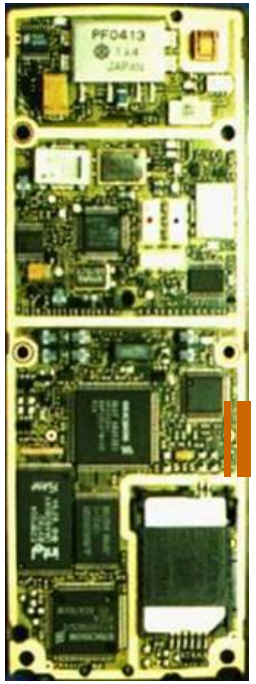
Bandwidth: Sampling Rate / 2 (stay tuned!)



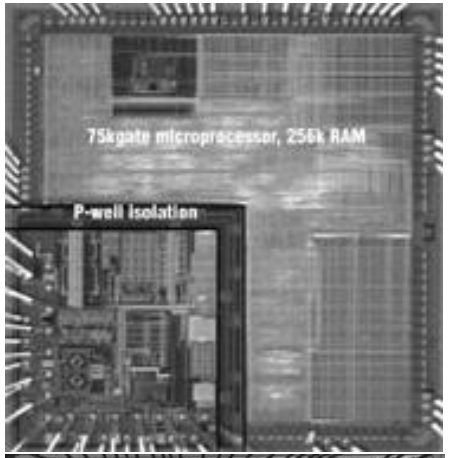
B. Murmann (Stanford)

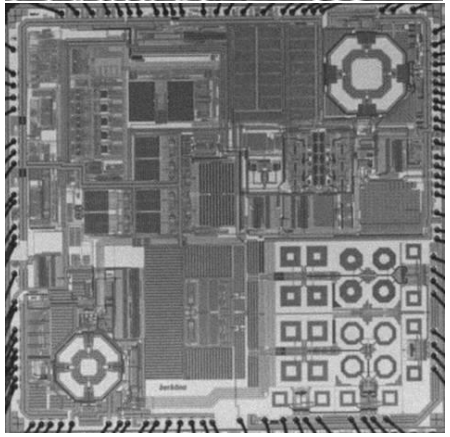
Huge application space → many complementary ADC techniques

ADC Applications (cellular phone example)



Ericsson CH388
(Hybrid, 1995)





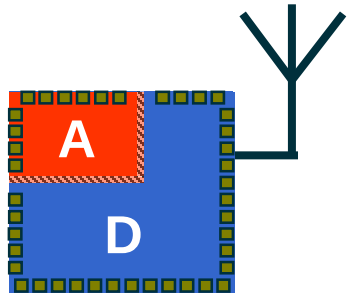
Past

Ericsson Bluetooth
(CMOS, 2001)

Berkäna GSM/GPRS
(CMOS, 2005)

Present

Future



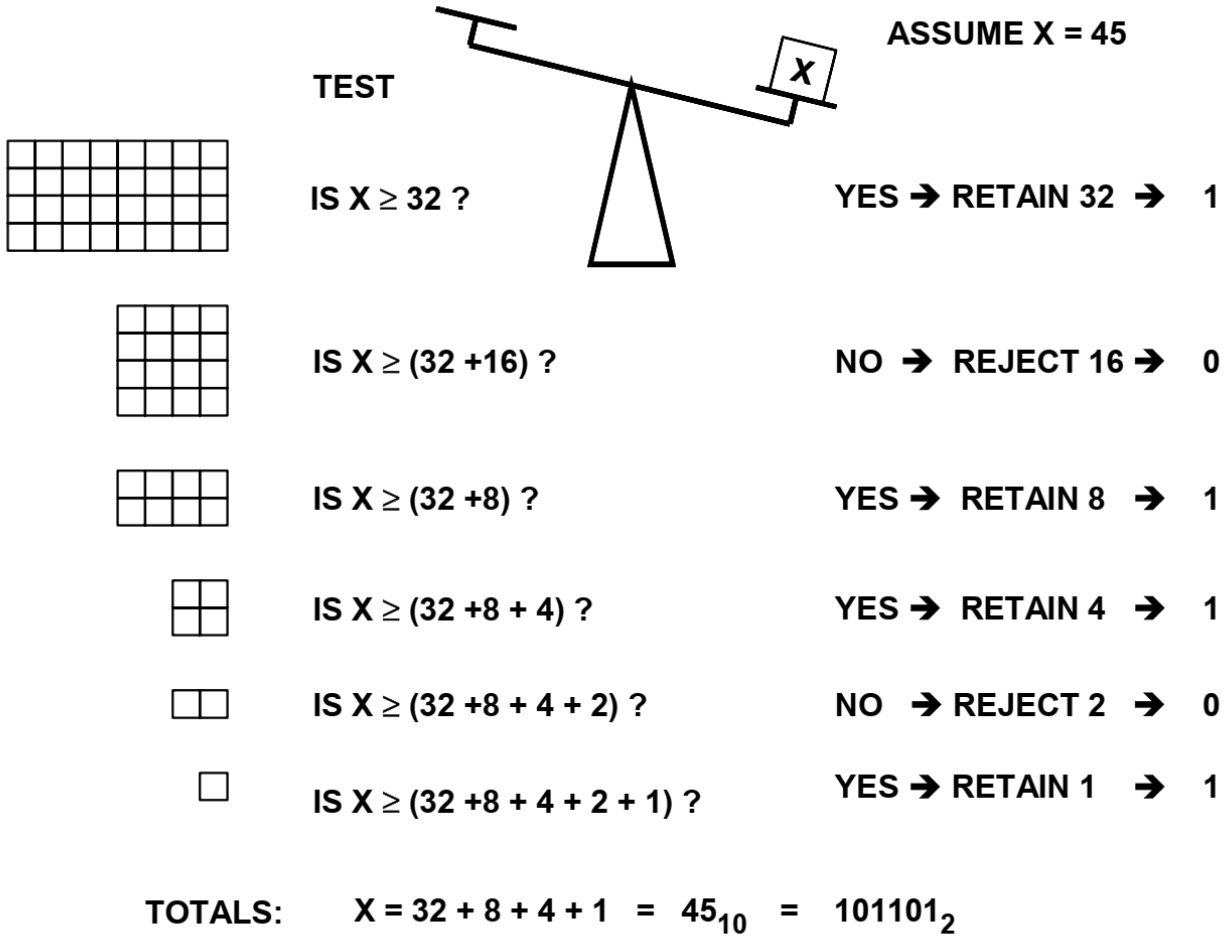
CMOS? or
something else?

Y. Chui (UTD)

What exactly is Analog-to-Digital Conversion?

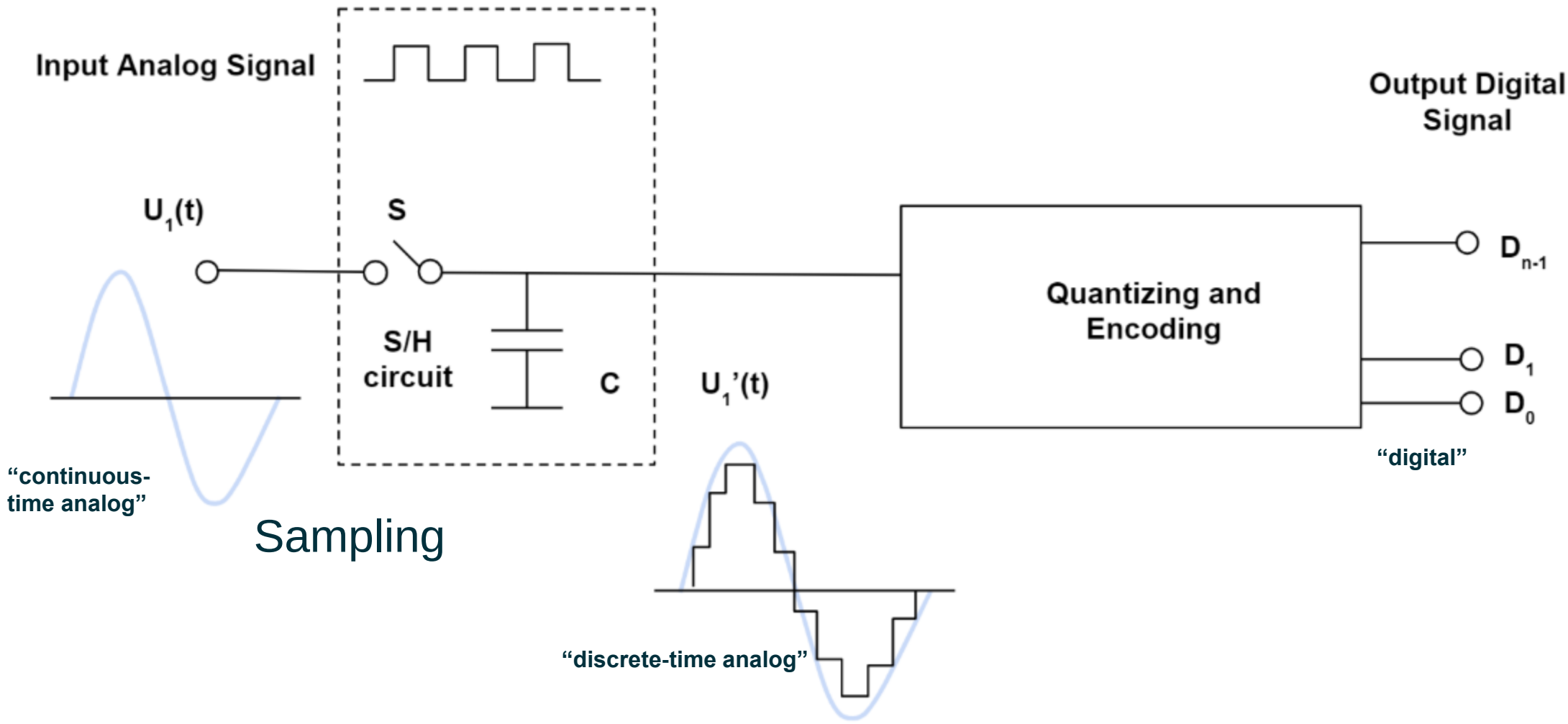
Analog-to-Digital conversion is essentially a ruler that can be used to measure an unknown quantity to some level of accuracy

This is an ancient algorithm to determine weights (for example in a metal assay). Today this algorithm is called Successive Approximation (and the leading ADC technique uses this algorithm still).



Analog Devices

Steps of Analog-to-Digital Conversion



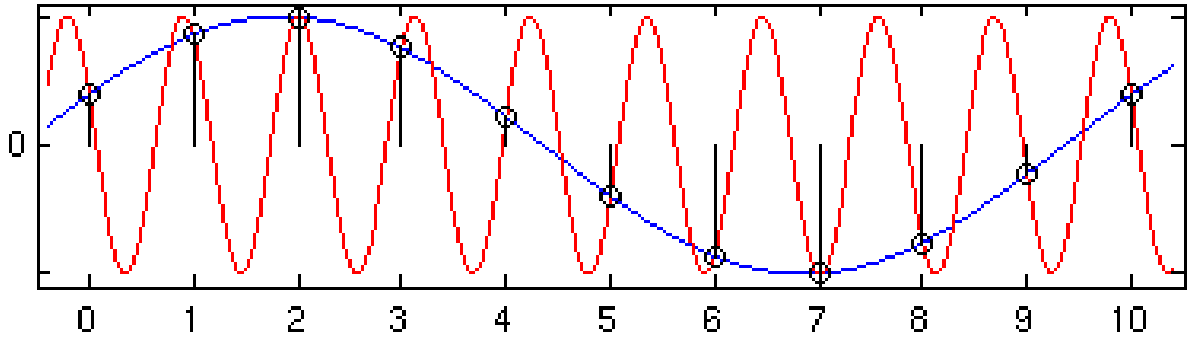
Sampling & Aliasing

How fast do you need to sample?

Shannon-Nyquist Theorem:

If a system uniformly samples an analog signal at a rate that exceeds the signal's highest frequency by at least a factor of two, the original analog signal can be perfectly recovered from the discrete values produced by sampling.

Aliasing

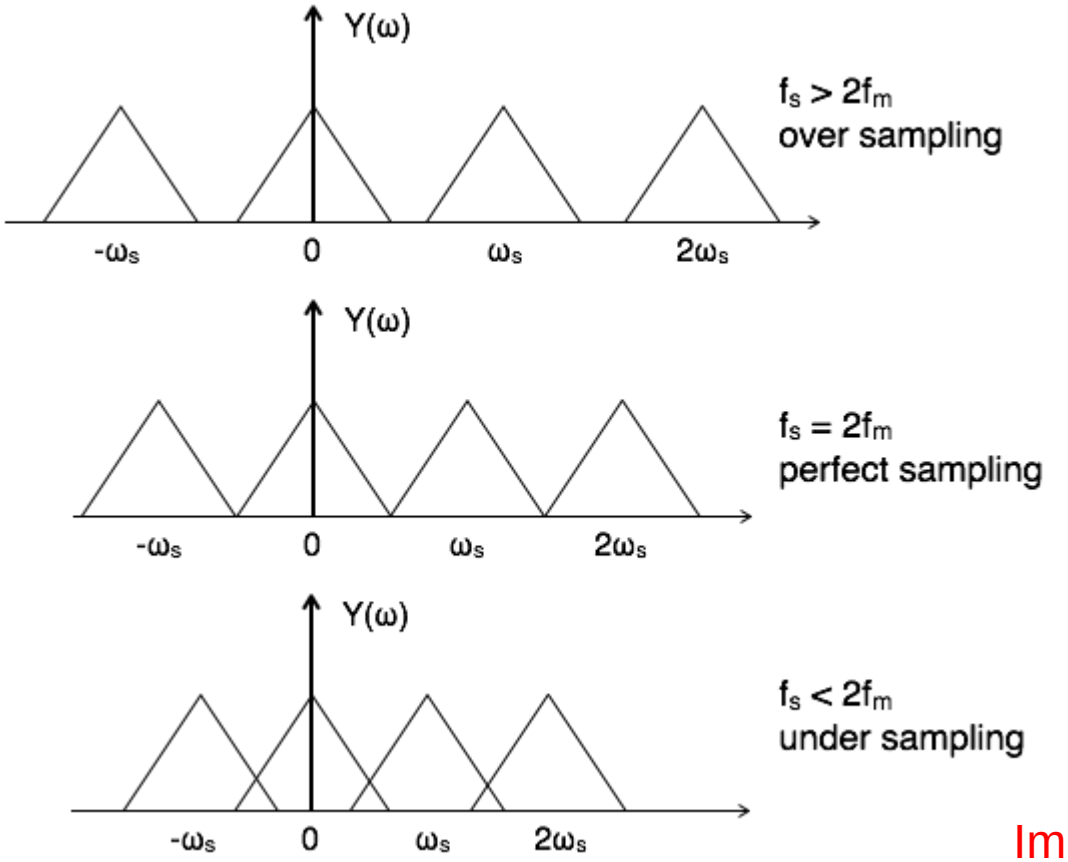


No aliasing if $f_{sample} > 2\ f_{max}$ where f_{max} is the maximum frequency in your input signal.

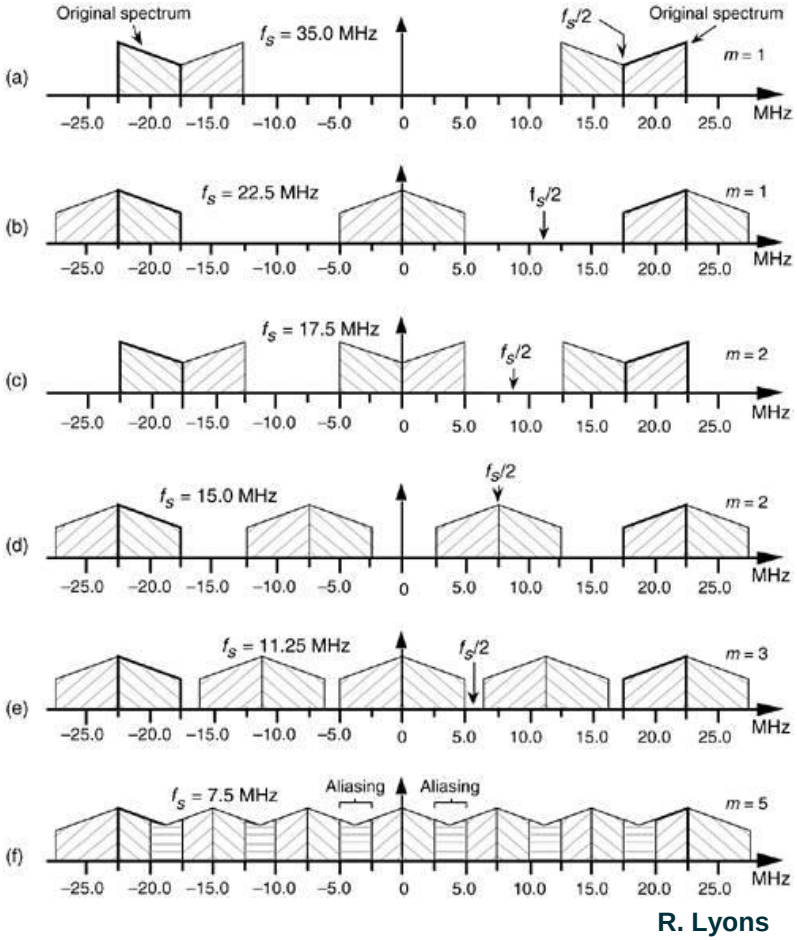
Did you sample the red curve? Or the blue curve?

Sampling & Aliasing

$$Y(\omega) = \frac{1}{T_S}\sum_{-\infty}^{\infty} X(\omega - n\omega_s)$$



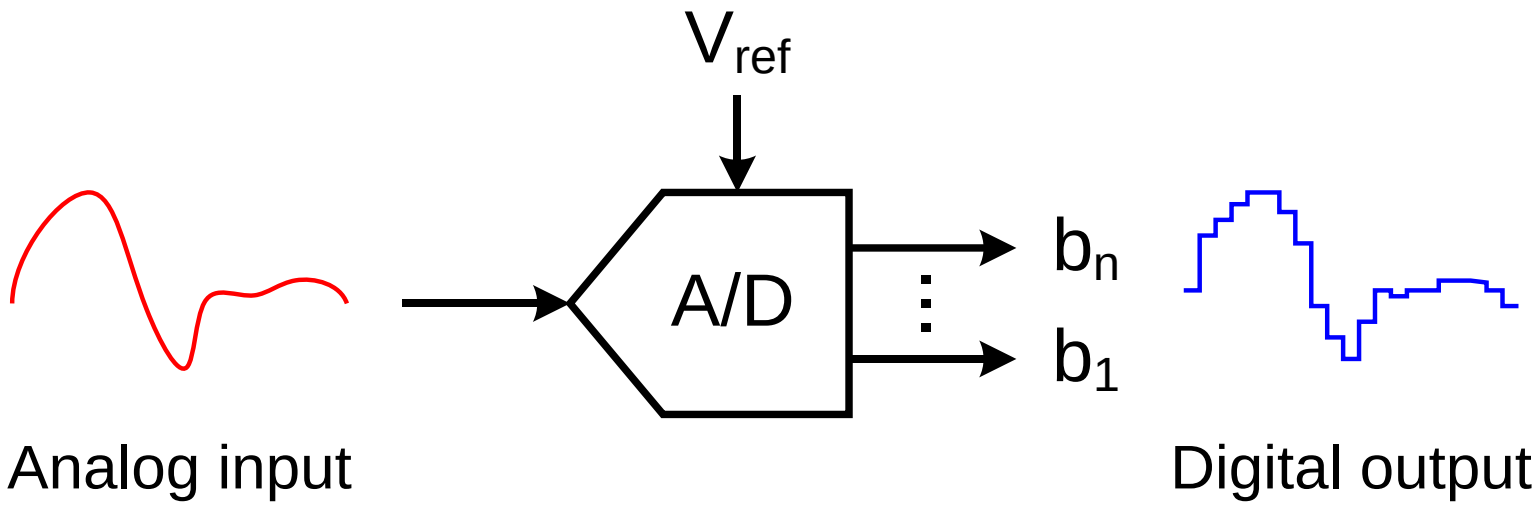
Sometimes aliasing is a *feature*. For example you can demodulate a bandpass signal “for free” using aliasing



R. Lyons

Important: sometimes you don’t care about aliasing. It depends on the application. But once your data is aliased, that’s it.

Quantization and Encoding



Y. Chui (UTD)

$$D_{out} = 2^n \frac{V_{in}}{V_{ref}}$$

Resolution: $\log_2$ of quantization levels

Sampling Rate: number of conversions/sec

Important! Every ADC has *three* inputs. The analog input, the reference, and the power supply.

ADC Specifications

Key ADC Specifications (there are many others…)

Performance Parameters:

- Sampling Rate
- Resolution
- Analog Bandwidth: Different from sampling rate! Can be more or less (e.g. subsampling applications)
- Power Dissipation
- Die Area

Static:

- Linearity
- Noise
- Offset (Typically don’t care, sometimes you do…)
- Gain Error (Typically don’t care)

Dynamic:

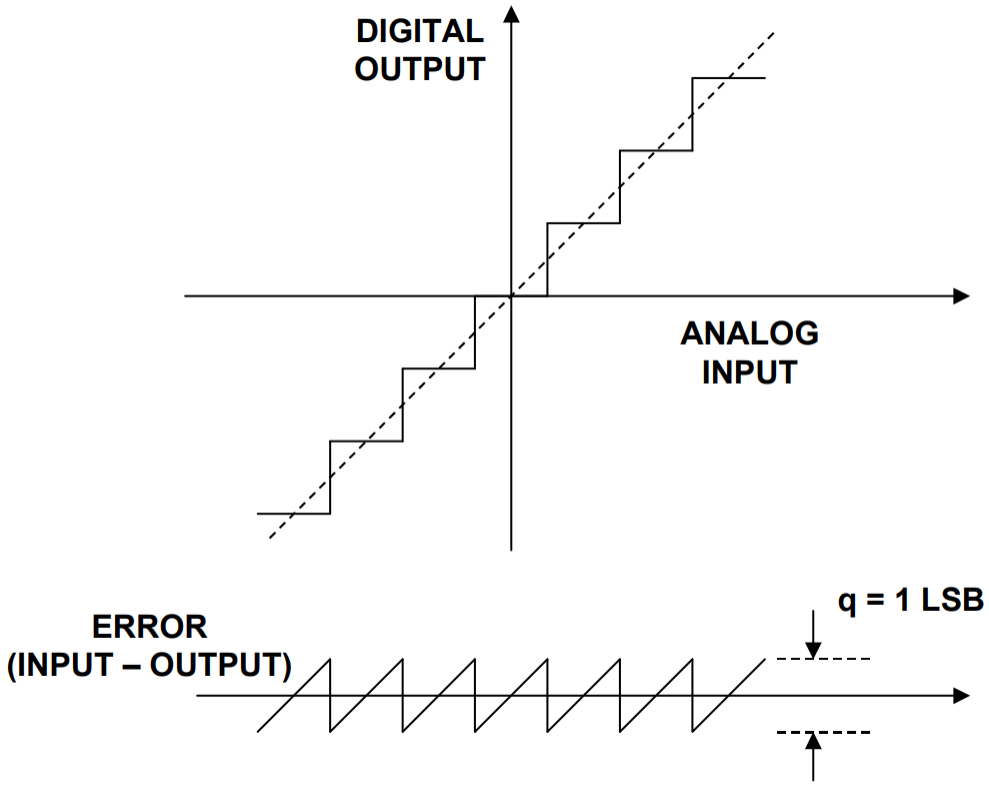
- Signal-to-Noise-Plus Distortion (SNDR)
- Spurious-Free Dynamic Range (SFDR)
- Total Harmonic Distortion (THD)
- Effective Number of Bits (ENOB)

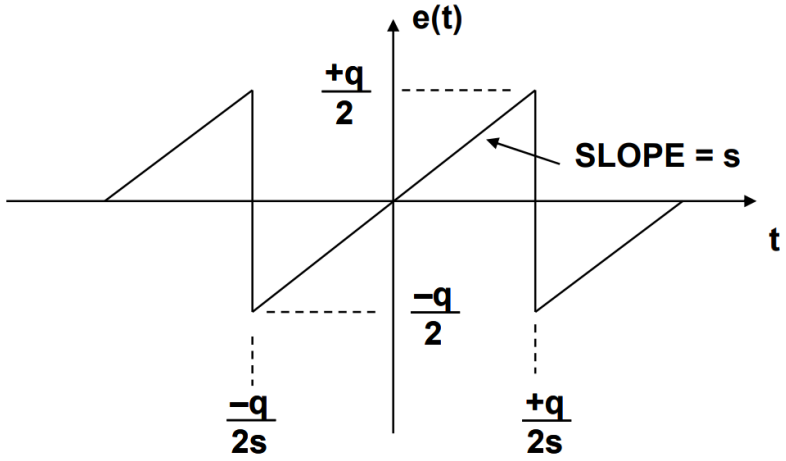
First commercial ADC. 11b, 50 kS/s
$8500 in 1954 ($96,000 today!)

ADC Noise - Quantization

Two main ADC noise sources: **quantization** noise, and thermal noise

Quantization: inherent uncertainty in mapping from continuous to discrete domain due to size of code





$$e(t) = st, -\frac{q}{2s} < t < \frac{q}{2s}$$

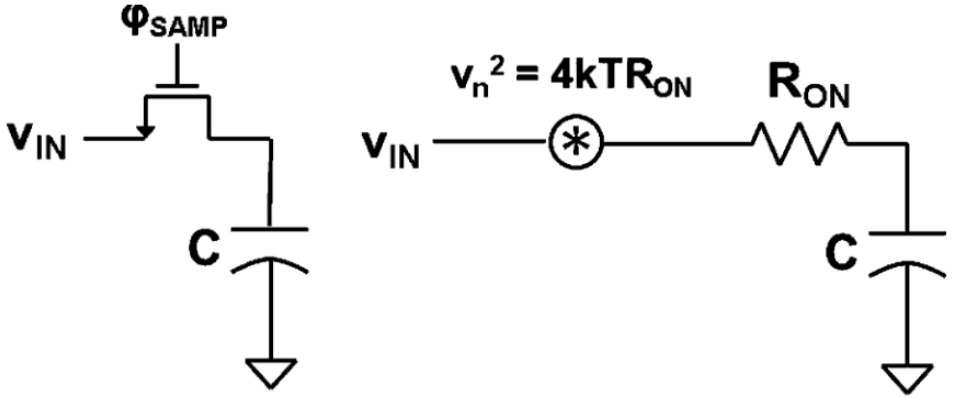
$$\overline{e^2(t)} = \frac{s}{q}\int_{-q/2s}^{q/2s} (st)^2\, dt = \frac{q^2}{12}$$

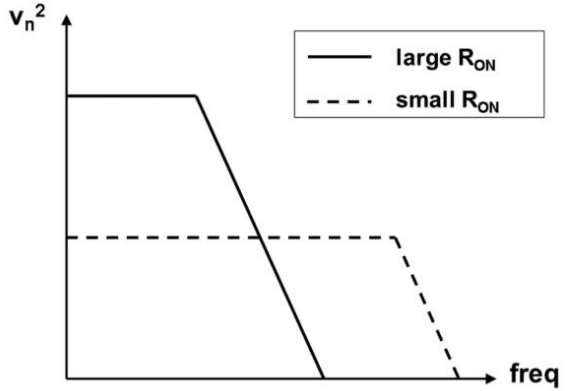
rms quantization noise = $\sqrt{\overline{e^2(t)}} = \frac{q}{\sqrt{12}}$

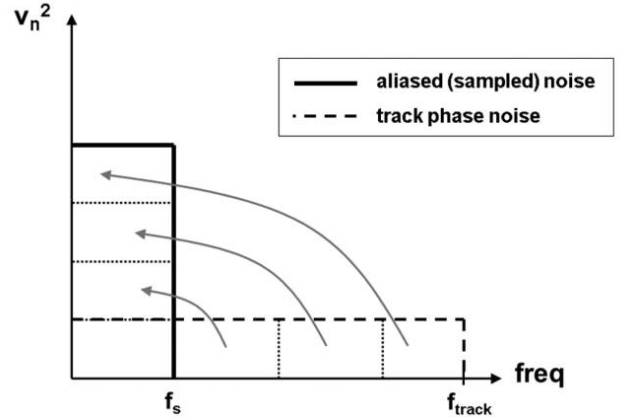
ADC Noise - Thermal

Two main ADC noise sources: quantization noise, and **thermal** noise

Thermal: noise generated by resistances in the circuit (rms level determined by capacitors when sampled)







$$\overline{v_n^2} = (4kTR_{ON}) \int_0^\infty \left| \frac{1}{1 + j2\pi f R_{ON} C} \right|^2 df = \frac{4kTR_{ON}}{4R_{ON}C} = \frac{kT}{C}$$

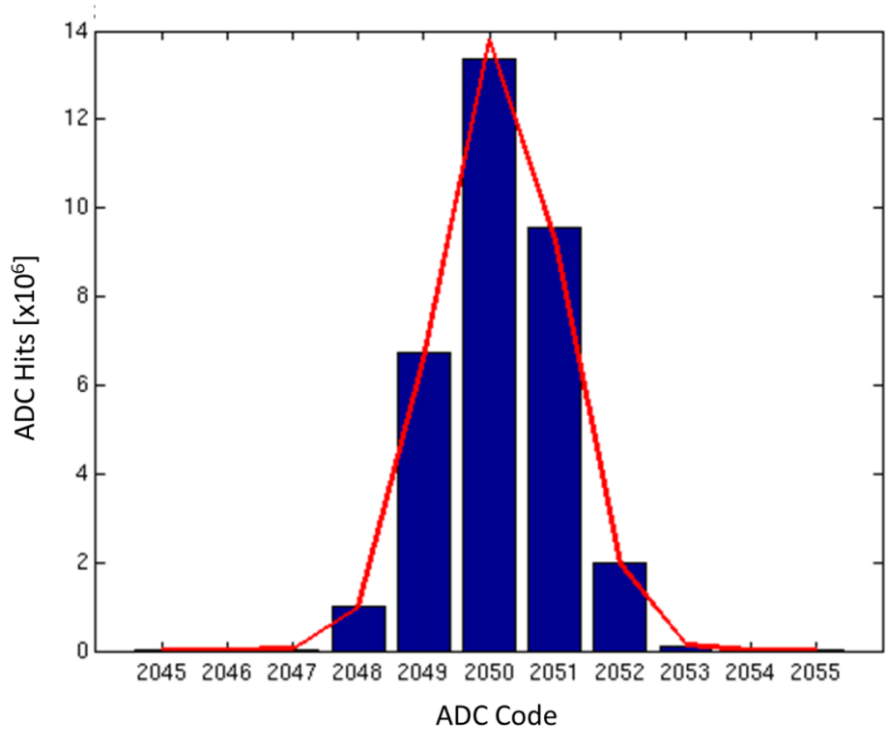
Thermal noise depends on sampling capacitance. Fundamental tradeoff between noise, speed, and power

Total rms noise = $\sqrt{\overline{e_n^2} + \overline{v_n^2}}$ Most efficient when they are equal

ADC Noise – example measurement

Idle Channel Test – disconnect (or connect to filtered DC value) and record some codes

By the Central Limit Theorem, we can expect the noise is Gaussian. If it isn't, that's a *clue*.



12-bit ADC

Width is about six codes, so
Rms noise about 0.9 LSB

(peak to peak = 6.6σ)

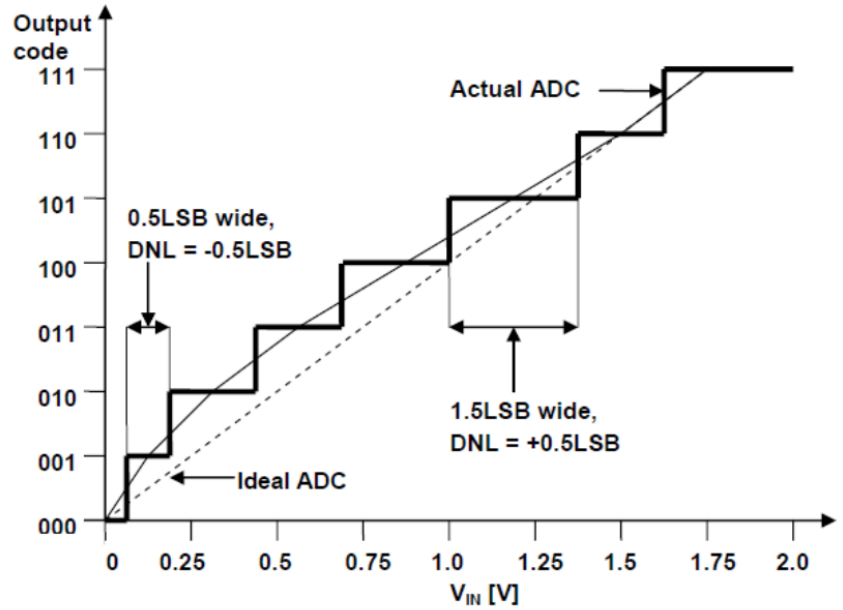
Offset: two LSBs

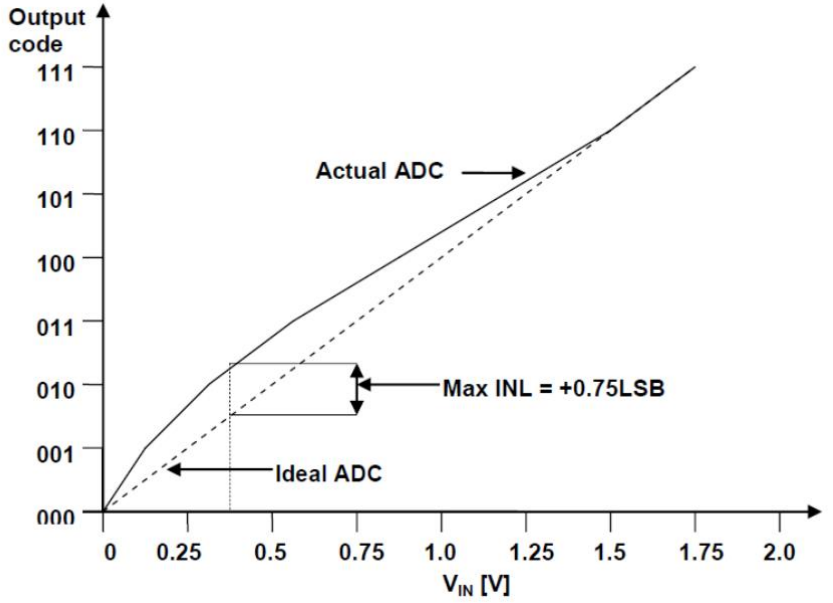
ADC Static Linearity

Often a key specification, and defines the accuracy of the ADC (as opposed to raw resolution)

Two main static linearity measurements: Differential Nonlinearity and Integral Nonlinearity

Simpler in practice than they seem.





$$DNL(i) = \frac{binwidth(i) - LSB}{LSB}$$

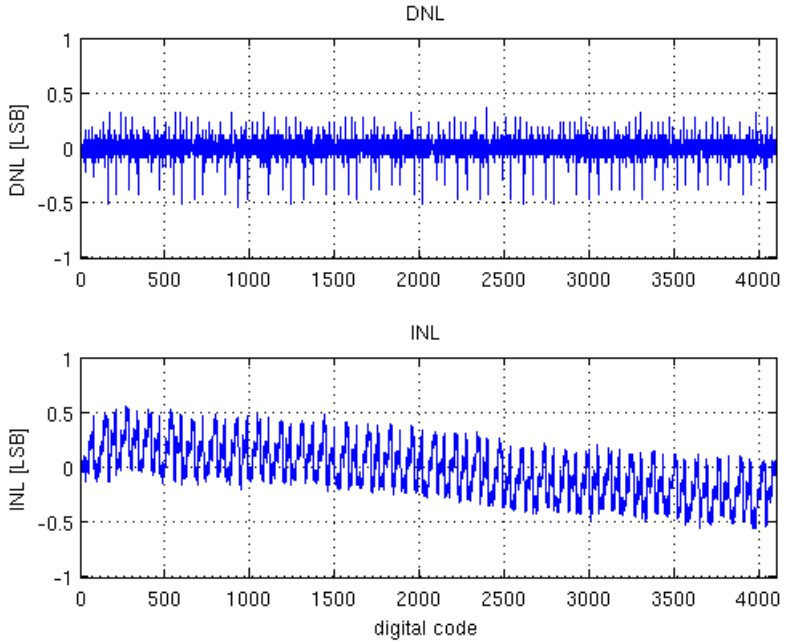
$$INL(i) = \sum_{n=0}^{i} DNL(n)$$

$$LSB = \frac{V_{FS}}{2^N}$$

Testing ADC Static Linearity

Knowing how to test an ADC is critical, because it:

1. informs your design choices
2. testing techniques can often be adapted to simulation



General approach:

1. apply test signal with known probability density function (PDF)
2. Create histogram of measured ADC codes
3. Map measured probability mass function to expected PDF
4. Interpret per-code deviations as DNL and sum DNL to get INL

Example:

Ramp Based Testing: Apply a ramp to ADC input. PDF is uniform (simple!)

DNL for each code is simply count for that code minus average count (simple!)

Don't need many codes - about 1/([DNL resolution] * number of codes). For 10b @ 0.01 LSB → 102400 counts

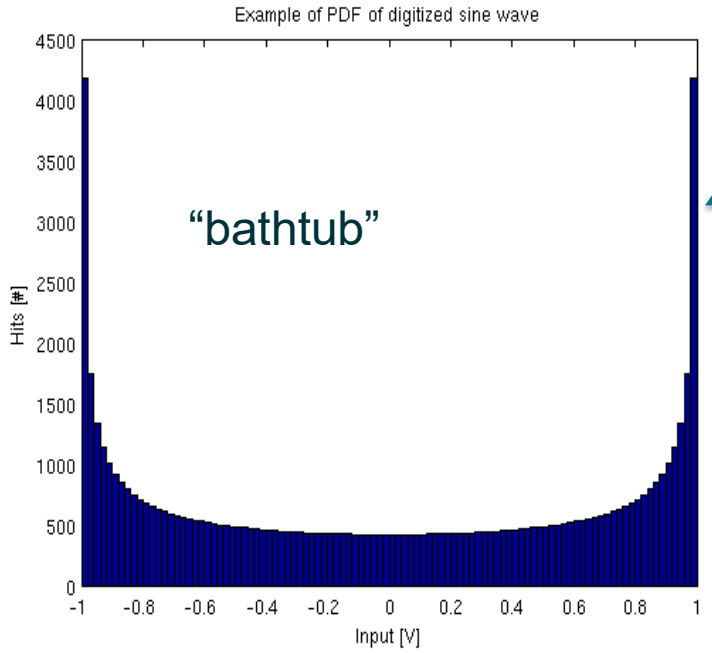
Catch: difficult to generate a linear ramp, and typically you want your test signal to be 10X more linear that ADC. Most commercial ramp generators aren't better than 0.1% linear (at best!)

Testing ADC Static Linearity

Solution sine-wave-based testing

It is much easier to generate a linear sine than ramp → can heavily filter

PDF of sine is more complicated than ramp



$$pdf(V) = \frac{1}{\pi\sqrt{A^2 - V^2}}$$

Number of samples needed: $$N_{samp} = \frac{\pi 2^{N-1} z_{\alpha/2}^2}{\beta^2}$$

α/2 = confidence level
β = desired DNL resolution
N = number of ADC codes

Many more samples needed.

ADC Dynamic Performance

SNDR: Captures both noise and nonlinearity into a single measure.

Assuming a full-scale sine wave input, SNDR is:

$$SNDR = \frac{2^N}{2\sqrt{2}\left(\frac{1+v_n}{\sqrt{12}} + \frac{DNL}{\sqrt{3}}\right)}$$

SFDR: Difference between input tone and highest harmonic.

Rule of thumb for estimating SFDR:

$$SFDR \approx \frac{2^B}{INL}$$

THD: Ratio of power of fundamental to sum of powers of all harmonics

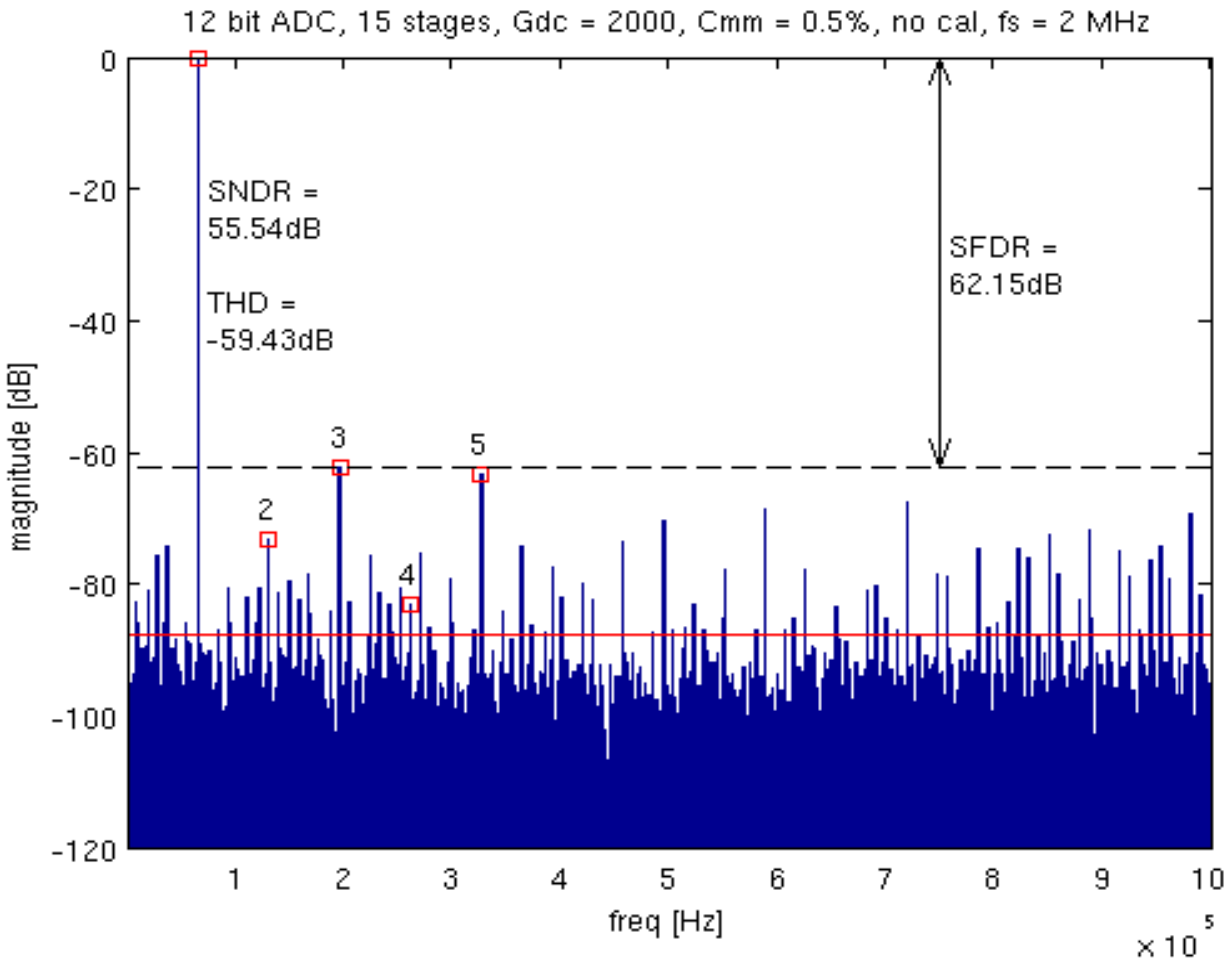
$$THD = \frac{\sum_{n=2}^{n} P_n}{P_1}$$

ENOB: Number of bits of ideal ADC that gives same SNDR as ADC under test.

When quantization = thermal, ENOB = N-1

$$ENOB = \frac{SNDR - 1.76 + 20\log_{10}\left(\frac{V_{FS}}{V_{input}}\right)}{6.02}$$

ADC Dynamic Performance – example plot



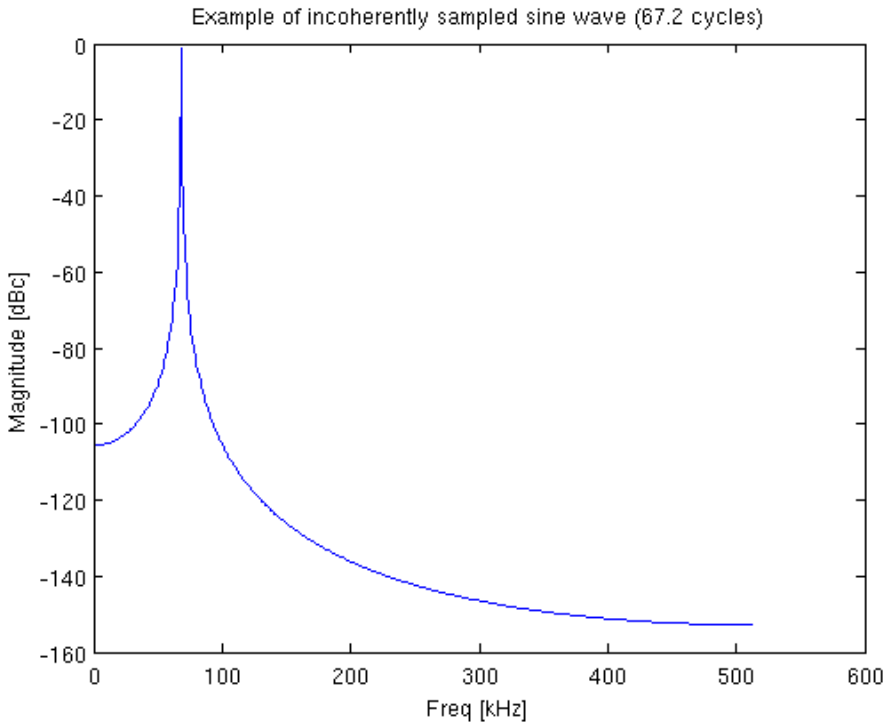
Here, ENOB = (55.54 – 1.76)/6.02 = 8.9 bits

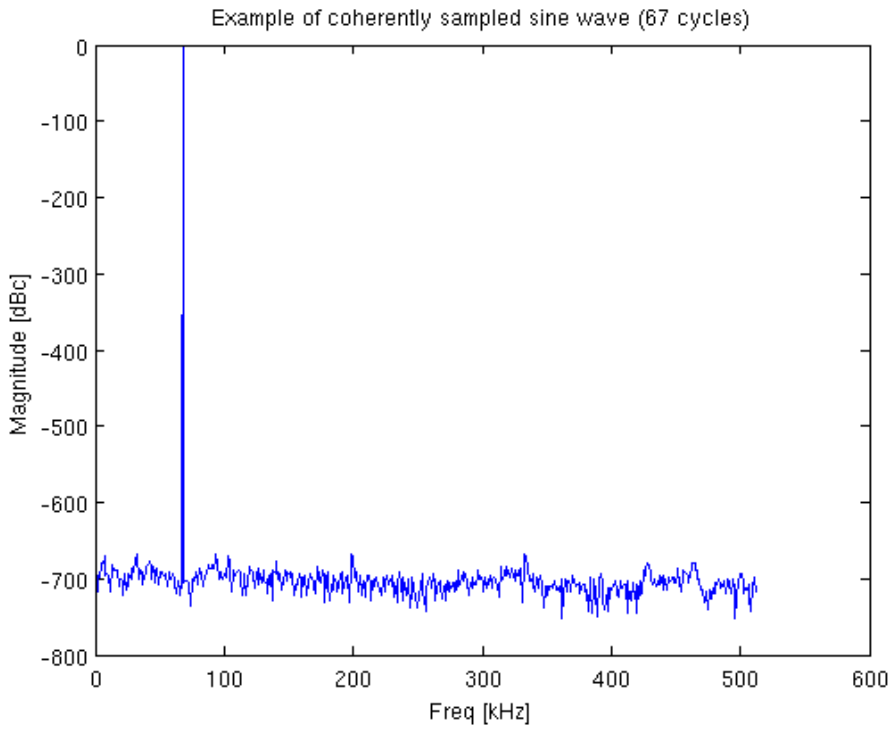
ADC Dynamic Performance – Coherent Sampling

General technique: apply pure sine wave to ADC and take FFT of resulting output codes

Vitally important that all power of input tone is in single FFT bin → Coherent Sampling

$$f_{in} = \frac{N_{cycles}}{N_{samples}} f_s$$





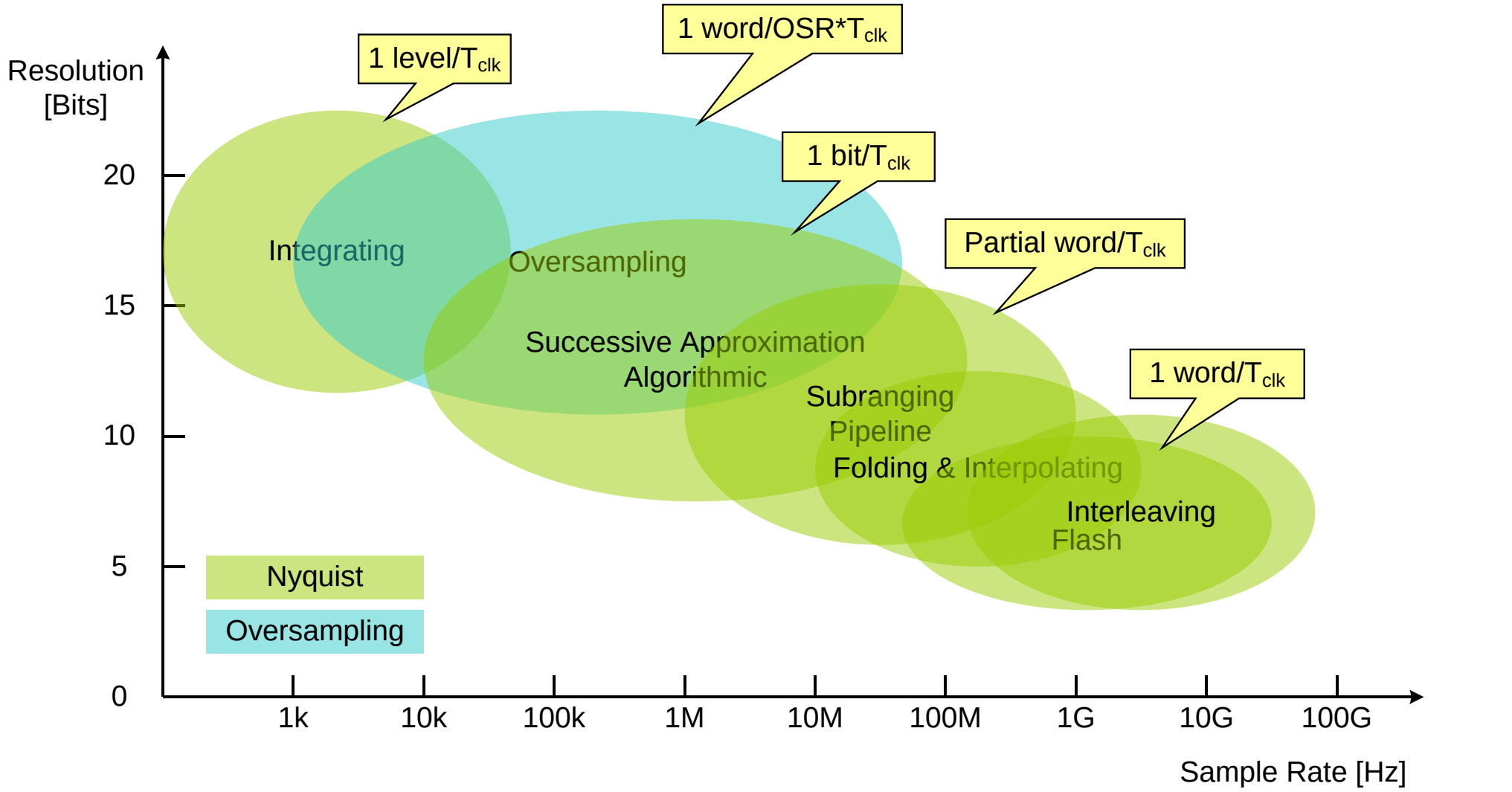
Tip: pick prime # of cycles

VERY useful for top-level simulation (and testing!) of ADCs

ADC Testing Takeaways

1. Make sure your reference & power are significantly more stable than your ADC
2. Make sure your test signal is significantly more linear than your ADC
3. Make sure your board and input have extremely low noise during noise tests
4. Make sure you use coherent sampling for dynamic testing
5. Make sure you lock both the signal generator and the ADC clock to the same time base

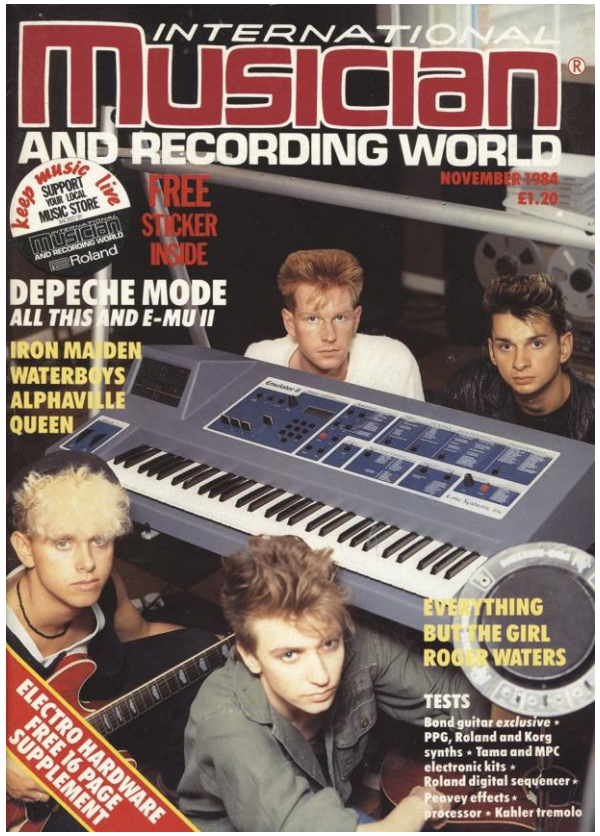
ADC Performance Space



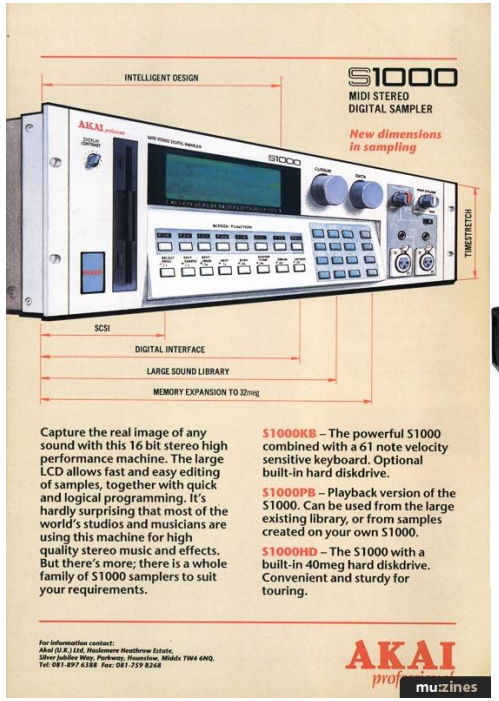
Y. Chiu (UTD)

Impact of ADCs (Digital Audio example)

Fairlight CMI
1979: $32000
($132k in 2023 $)
Stevie Wonder



E-mu Emulator II
1984: $8000
($23k in 2023 $)
Depeche Mode



Akai S-1000
1988: $2500
($6350 in 2023 $)
Everyone

Akai MPC-One
2023: $599

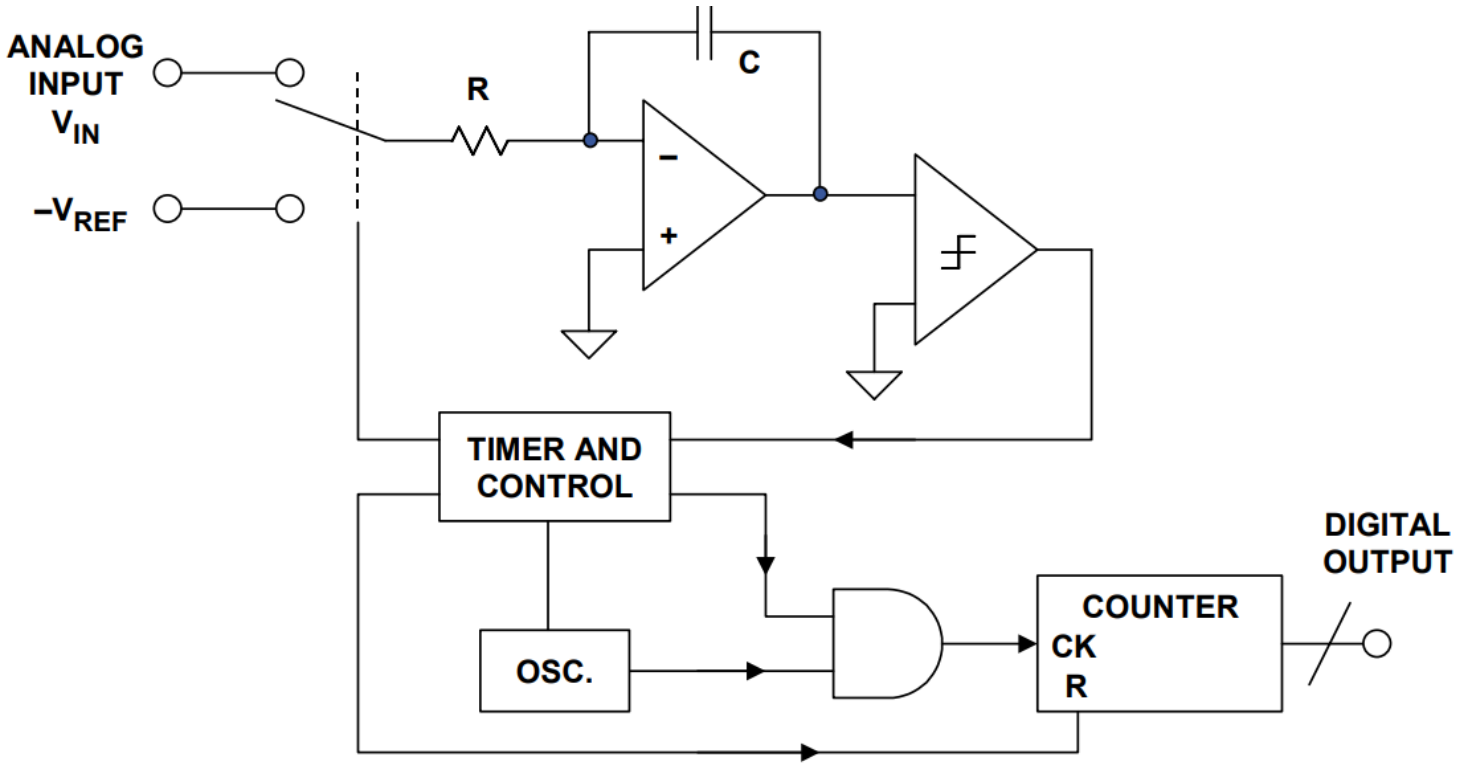
ADC Architectures

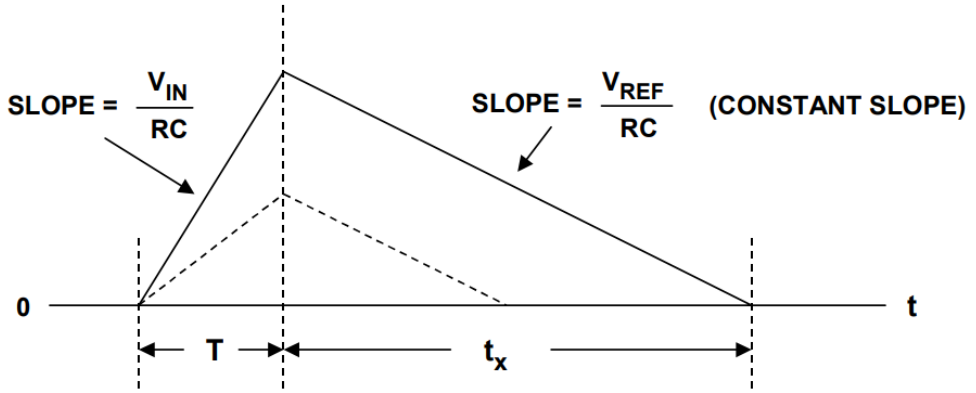
ADC Architectures

HEP Relevant ADC architectures from slowest to fastest. Note: Everything was invented by 1970.

1. Integrating (“Wilkinson”)
2. Sigma-Delta
3. Successive Approximation
4. Pipelined
5. Flash

Integrating ADC



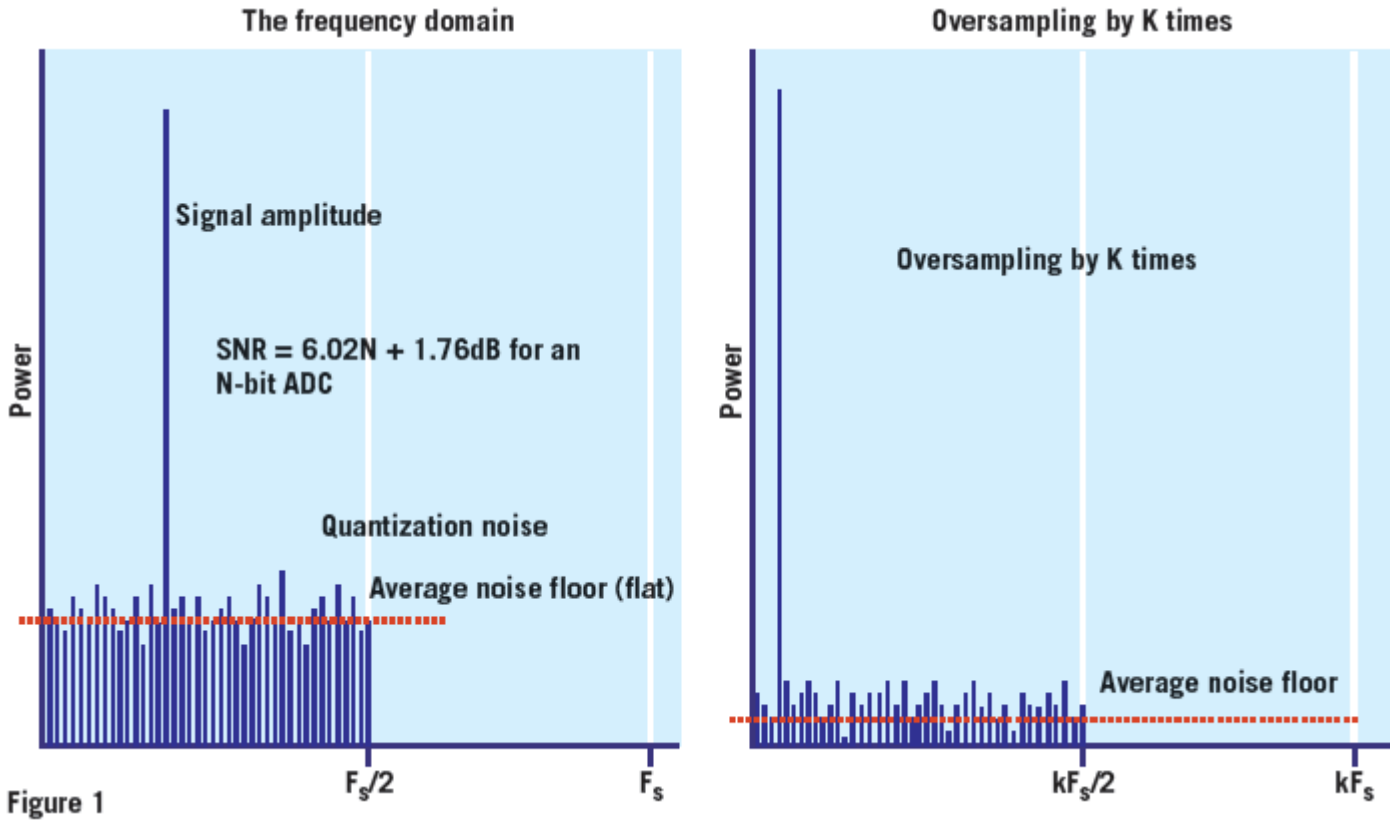


$$\frac{V_{IN}}{RC} T = \frac{V_{REF}}{RC} t_x$$

$$t_x = \frac{V_{IN}}{V_{REF}} T$$

Called “Dual Slope ADC” in industry. Remove R (direct charge readout) to make a Wilkinson

Oversampling



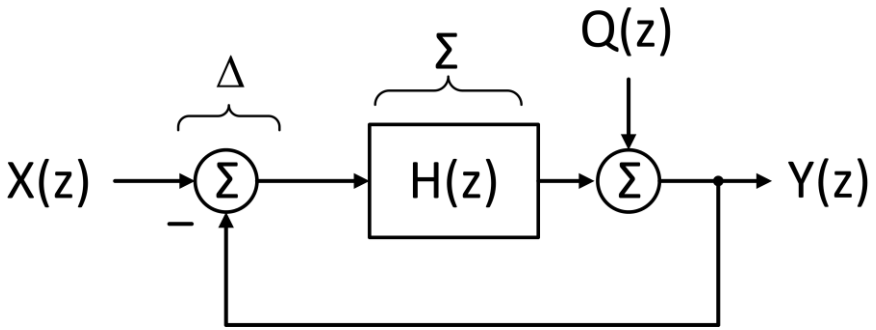
SNR increase:
3 dB / octave

Spread constant noise power over a larger bandwidth and then digitally filter → reduced quantization noise
Extend this by shaping the noise (pushing more of it to higher frequencies where it can be filtered)

Sigma-Delta ADC

Loop order is defined as number of poles in H(z)

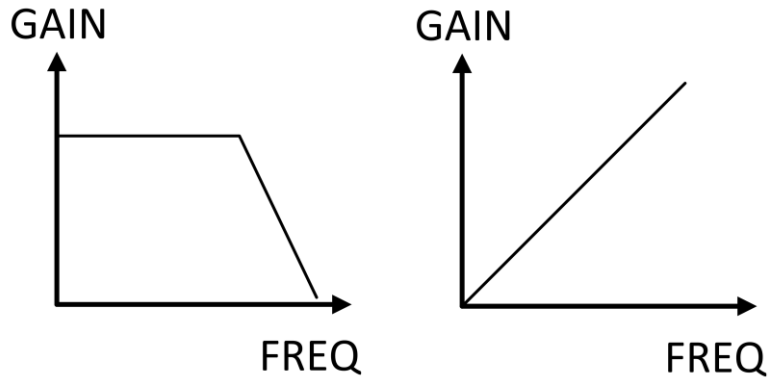
Idea: Don't just oversample, modulate the input to put more of the quantization noise power at higher frequencies

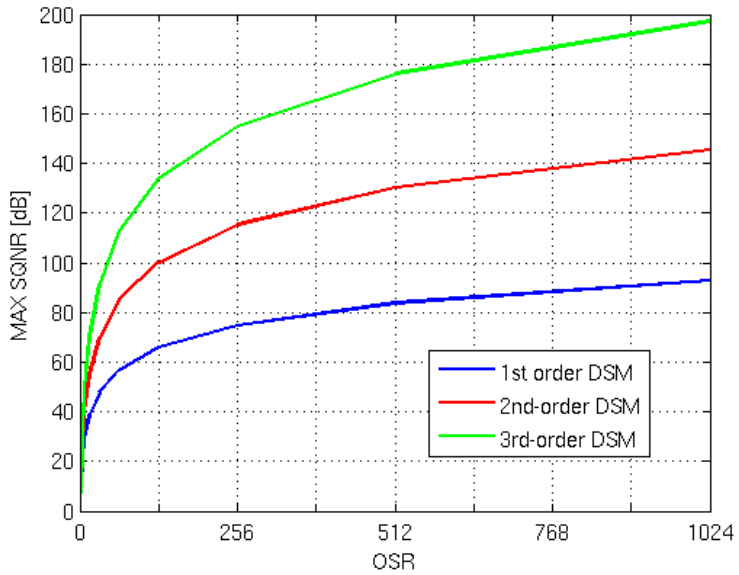


STF

NTF

$$Y(z) = \frac{H(z)}{1+H(z)} X(Z) + \frac{1}{1+H(z)} Q(Z)$$





Key Idea: signal sees low-pass filter, quantization noise sees high-pass filter.

$$SNQR\_improvement \approx 3(2L+1)\ dB$$

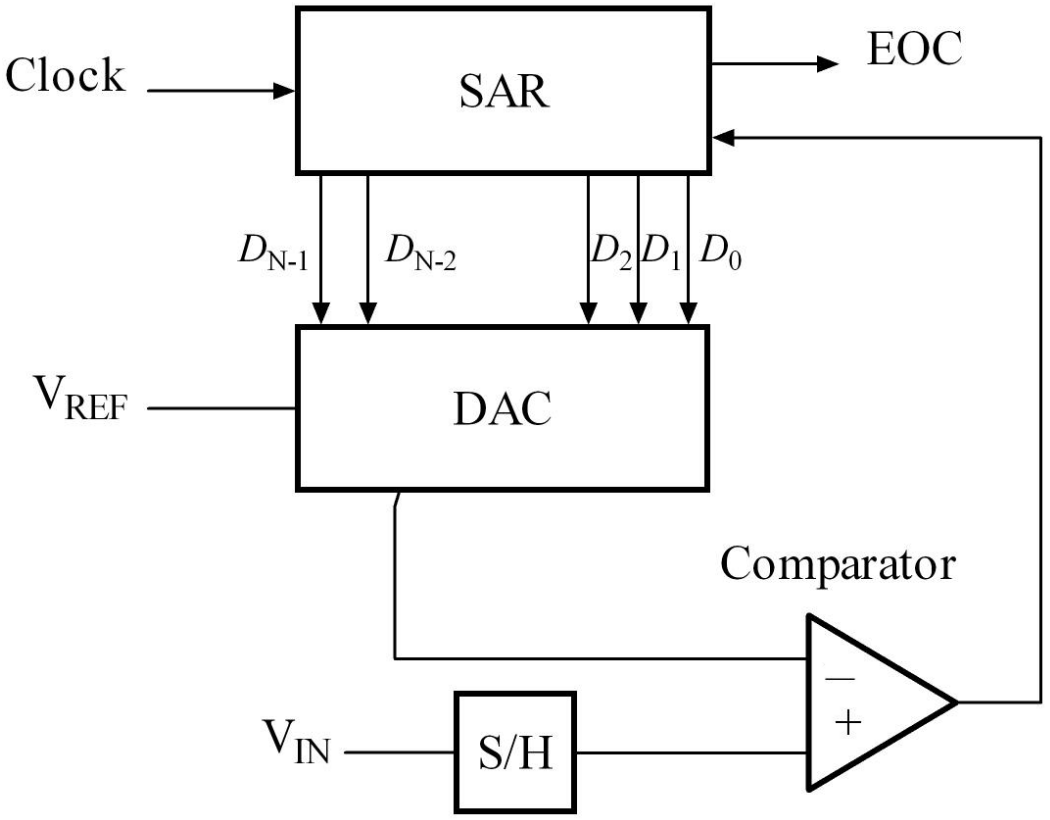
For L = 1, idle tones in output spectrum a problem and high OSR required

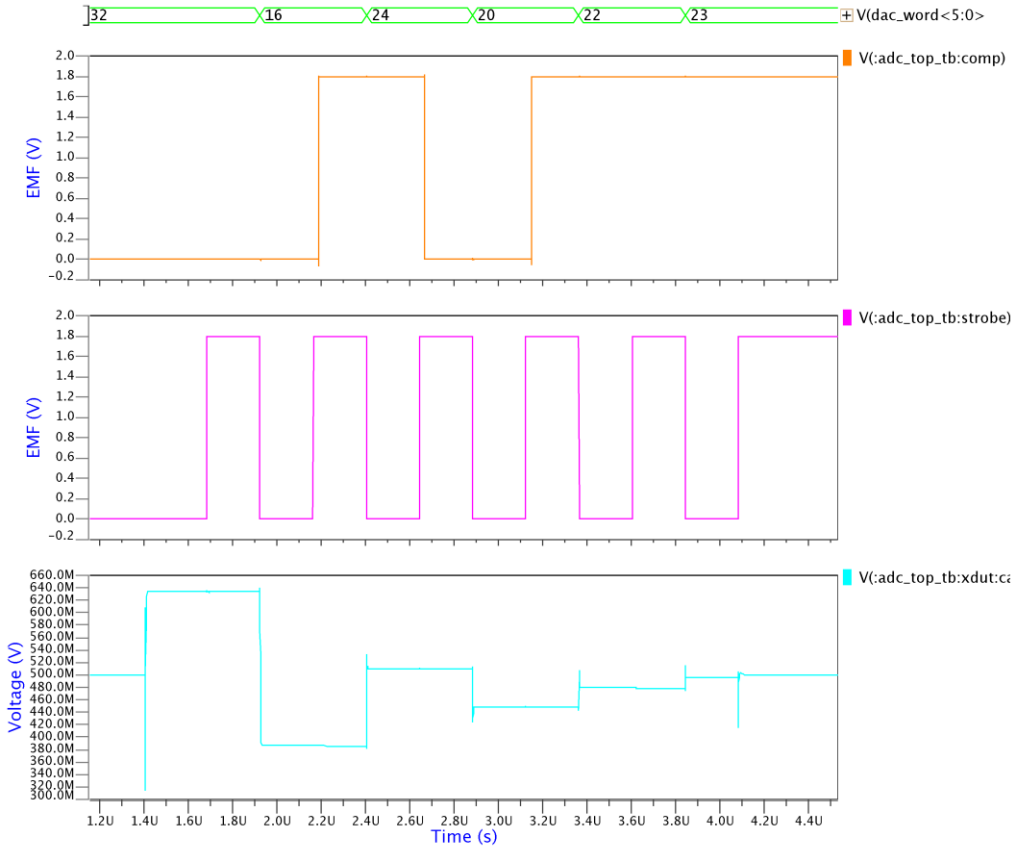
For L < 3, stability is assured → mitigates design risk

For L >= 3, low OSR possible (simplifying clocking design)

Successive Approximation (SAR) ADC

Simple 6-bit example





ADC output

Comparator output

ADC strobe

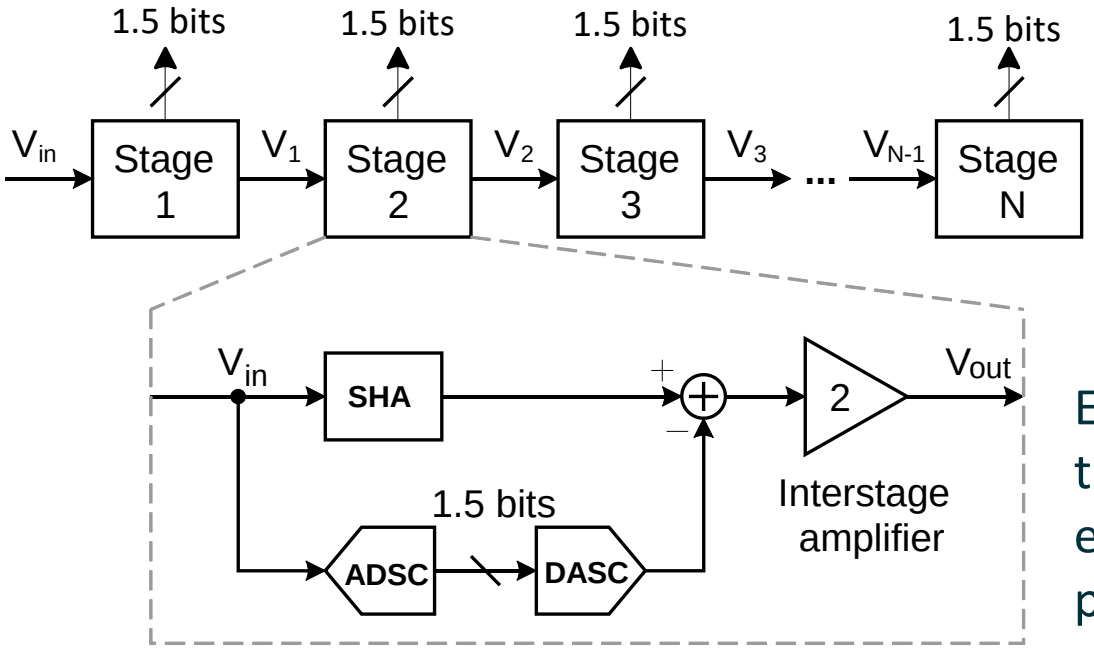
DAC output

Vin = 0.865 V, Vref = 1.5 V
Vcm = 0.5 V, → code = 23

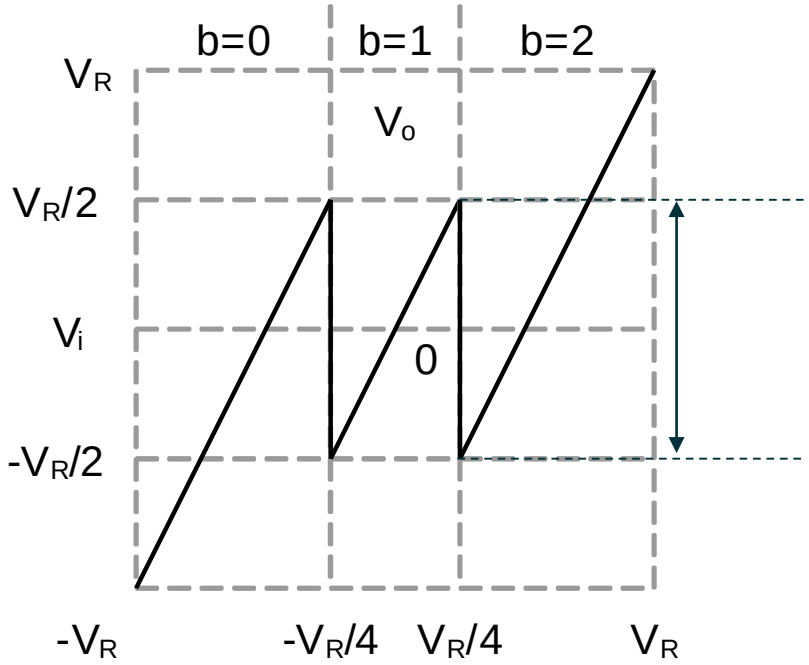
Directly implements binary search algorithm in hardware

Pipelined ADC

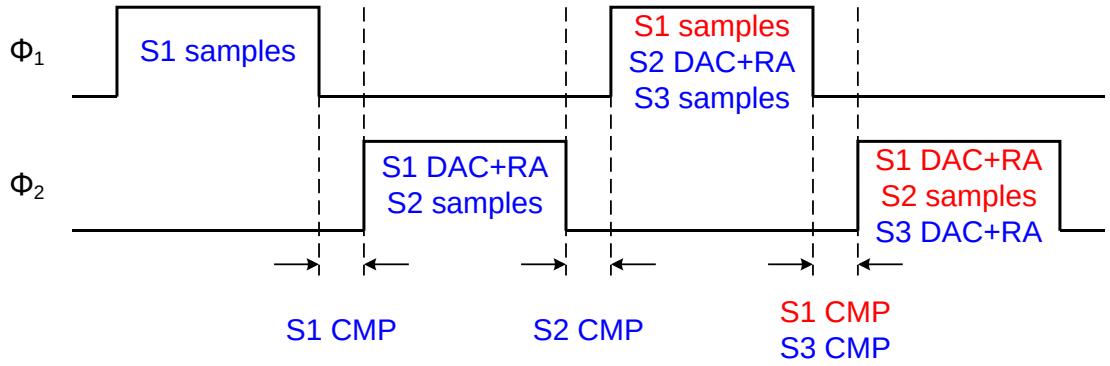
Multi-stage ADC, with each stage operating concurrently → high throughput



Each stage processes the quantization error (residue) of previous stage.



$$V_o = 2 \cdot V_i - (b-1) \cdot V_R$$



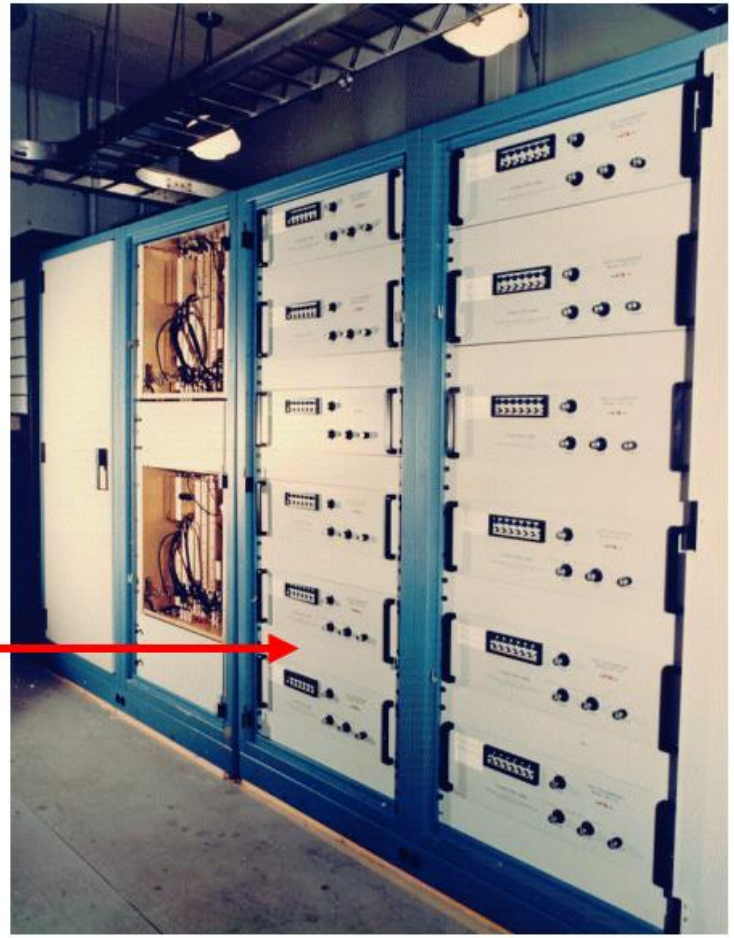
THE enabling technology for Pipelined ADCs

Pipelined ADC

19" RACK-MOUNTED, 150W, $10,000.00

$95k in 2023 dollars!

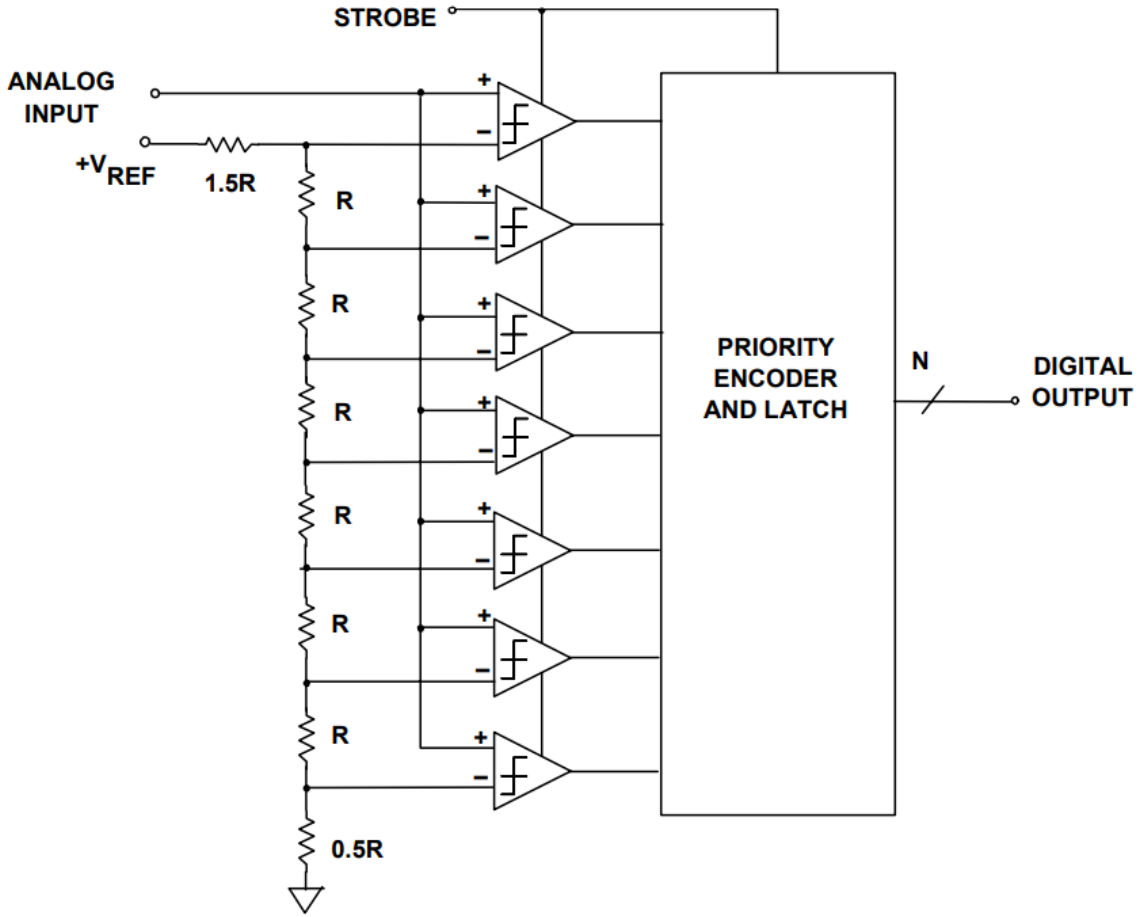
INSTALLATION OF 12 ADCs IN EXPERIMENTAL DIGITAL RADAR RECEIVER



8 bits, 10 MS/s (1966)

First high-speed Pipelined ADC (modular, not CMOS) by Computer Labs of North Carolina (later became Analog Devices High-Speed Converters Division, where I worked before LBNL).

Flash ADC

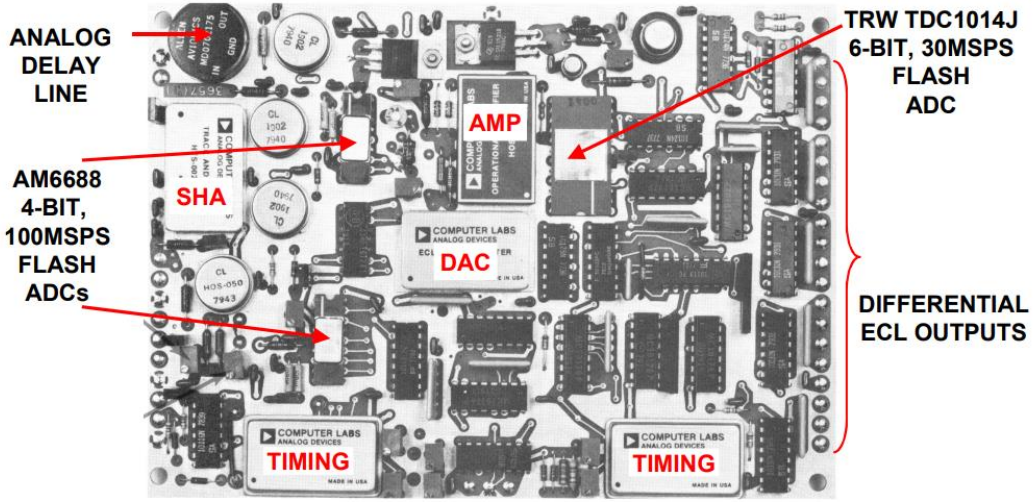


FAST.

Power Hungry.

Limited to about 8 bits.

Used as sub-ADCs in multi-stage ADCs



5" × 7" × 0.5", 21W, $3,500.00

10 bits, 20 MS/s (1979) $15k in 2023 dollars!

Flash ADC

TDC1007 TRW

Monolithic Video A/D Converter
8-bit, 20MSPS

The TDC1007 is an 8-bit fully parallel (flash) analog-to-digital converter, capable of digitizing an input signal at rates up to 20MSPS (MegaSamples Per Second). It will operate accurately without the use of an external sample-and-hold amplifier, with analog input signals having frequency components up to 7MHz.

A single CONVert (CONV) signal controls the conversion operation of the device which consists of 255 sampling comparators, encoding logic, and a latched output buffer register. The device will recover from a full-scale input step in 20ns. Control inputs are provided to format the output in binary, two's complement, or inverse data coding formats.

The TDC1007 is patented under U.S. Patent No. 3283170 with other patents pending.

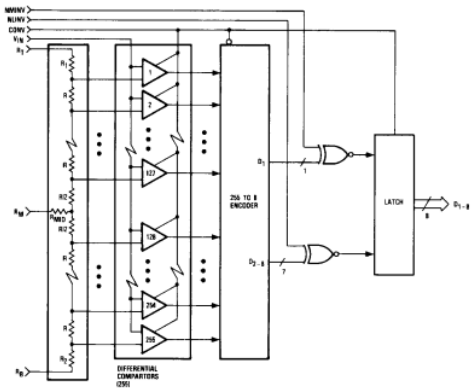
Features

- 8-Bit Resolution
- Conversion Rates Up to 20MSPS
- Sample-And-Hold Amplifier Not Required
- Bipolar Monolithic Construction
- TTL Compatible Inputs and Outputs
- Binary or Two's Complement Mode
- Differential Phase = 1.0 Degrees
- Differential Gain = 1.7%
- Evaluation Boards Available: TDC1007E1C or TDC1007P1C

Applications

- Video Systems 3x or 4x Subcarrier, NTSC or PAL
- Radar Systems
- High-Speed Multiplexed Data Acquisition
- Digital Signal Processing

Functional Block Diagram



TRW TDC1007 8-bit, 20 MS/s Flash ADC enabled new field of “digital video”

Won technical Emmy in 1989!

ADC designers are creative.

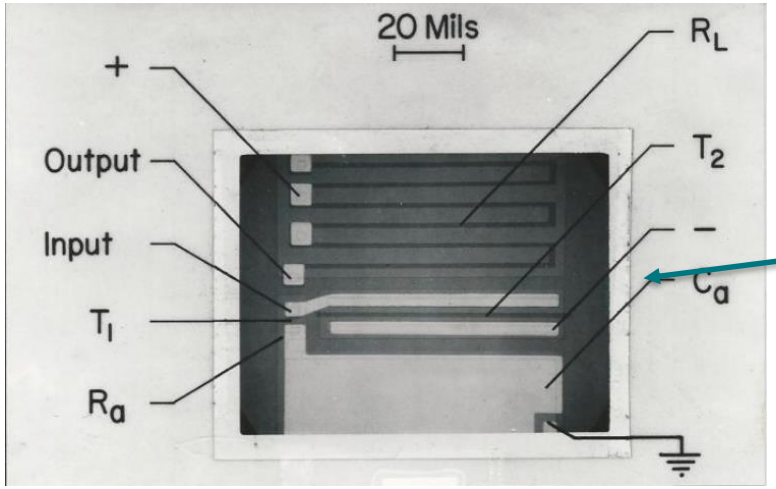
ADCs for High-Energy Physics

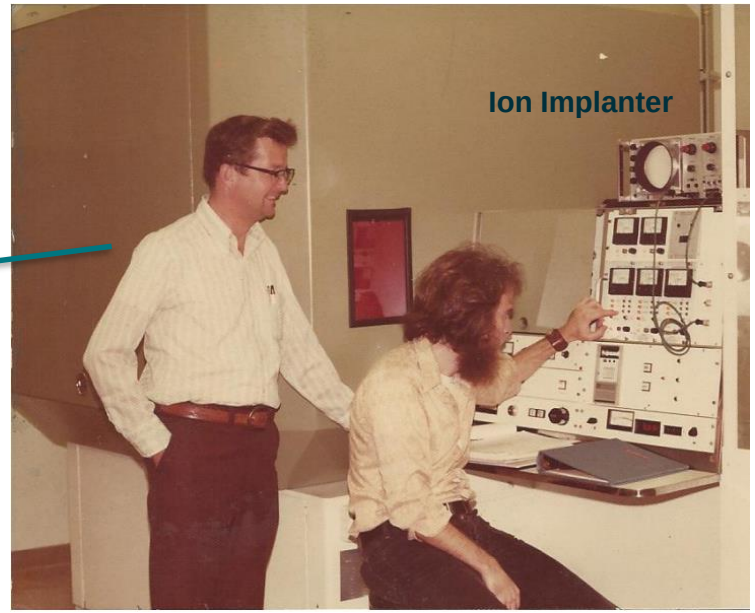
In the dark ages*…

IC Development at UC Berkeley

The Microlab was located on the 4th floor of Cory Hall, facing Hearst Avenue.

Hodges Flip-Flop (1963)





Ion Implanter

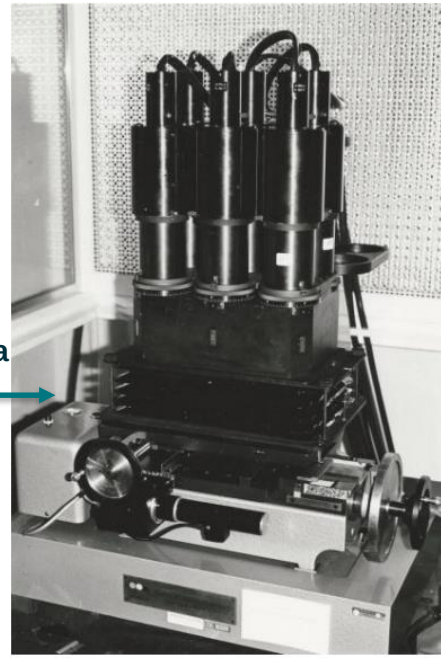
David Hodges William Black

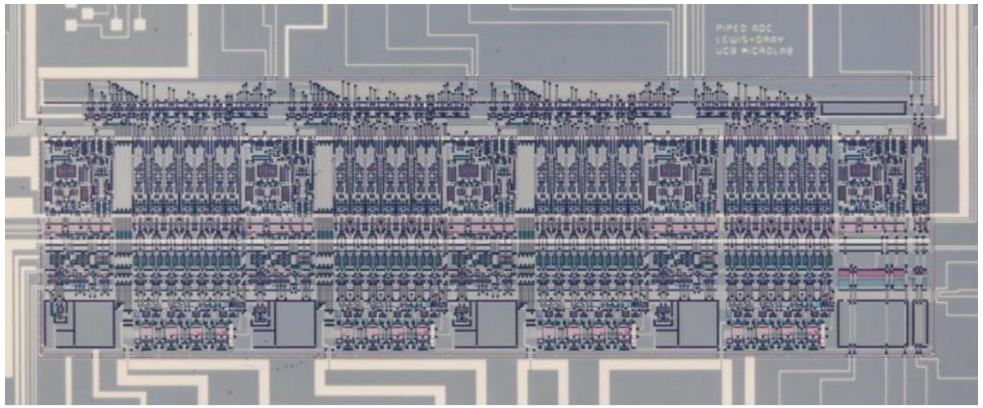
Paul Gray Paul McCreary

*1960s – 1970s

First all-MOS ADC (1975)!

Mask Camera





Stephen Lewis – First CMOS Pipelined ADC (1986)

The rise of the Custom ASIC

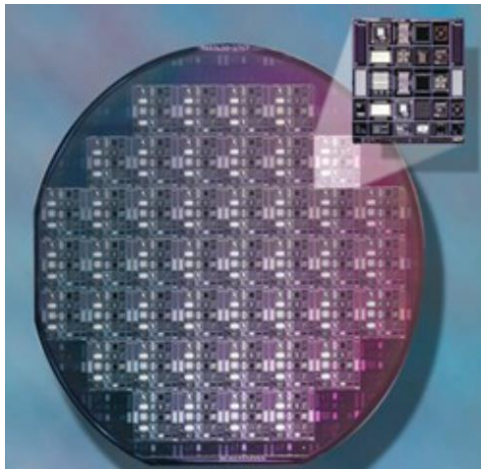
1960s : Only a few Universities made chips

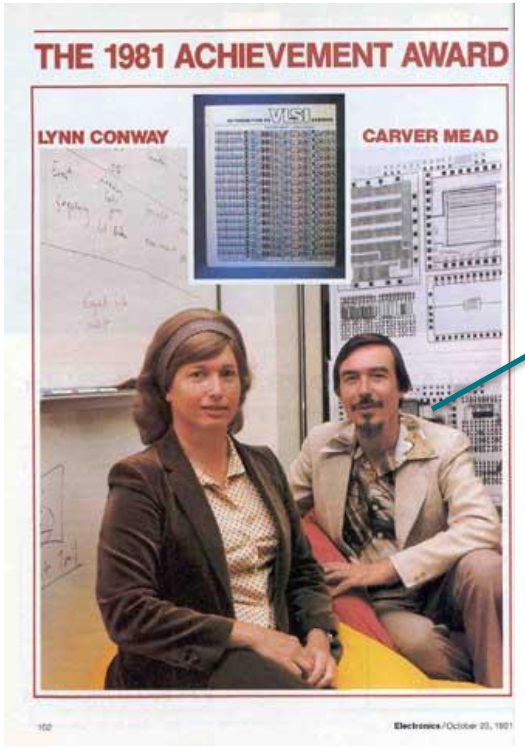
Late 70s : Technology for Multi-Project Wafers (Mead and Conway)

1981 : Founding of MOSIS with DARPA support

1987 : MOSIS commercialized (first large-scale eCommerce application on the Internet)

Also 1987 : TSMC founded (and Fabless Semi industry was born!)

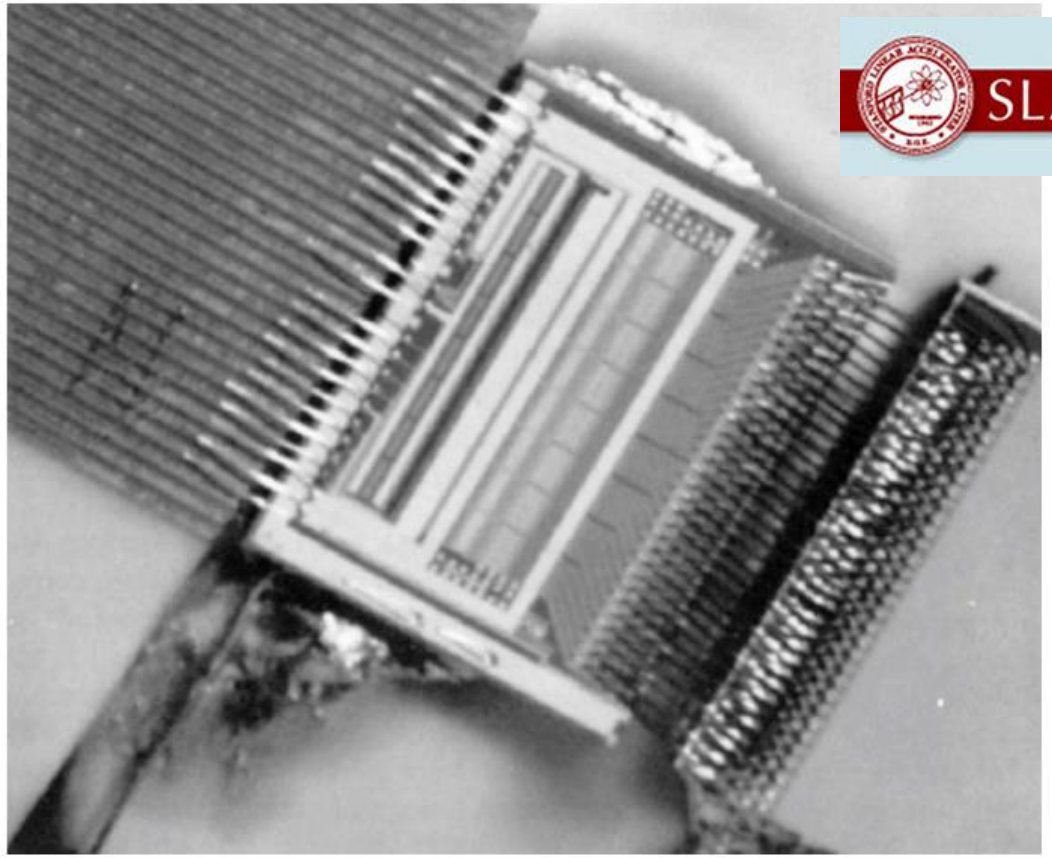




Trivia alert! The same DARPA program led to the development of the first hardware description language, VHDL.

First Physics ASICs

Microplex – first custom ASIC for Physics Research

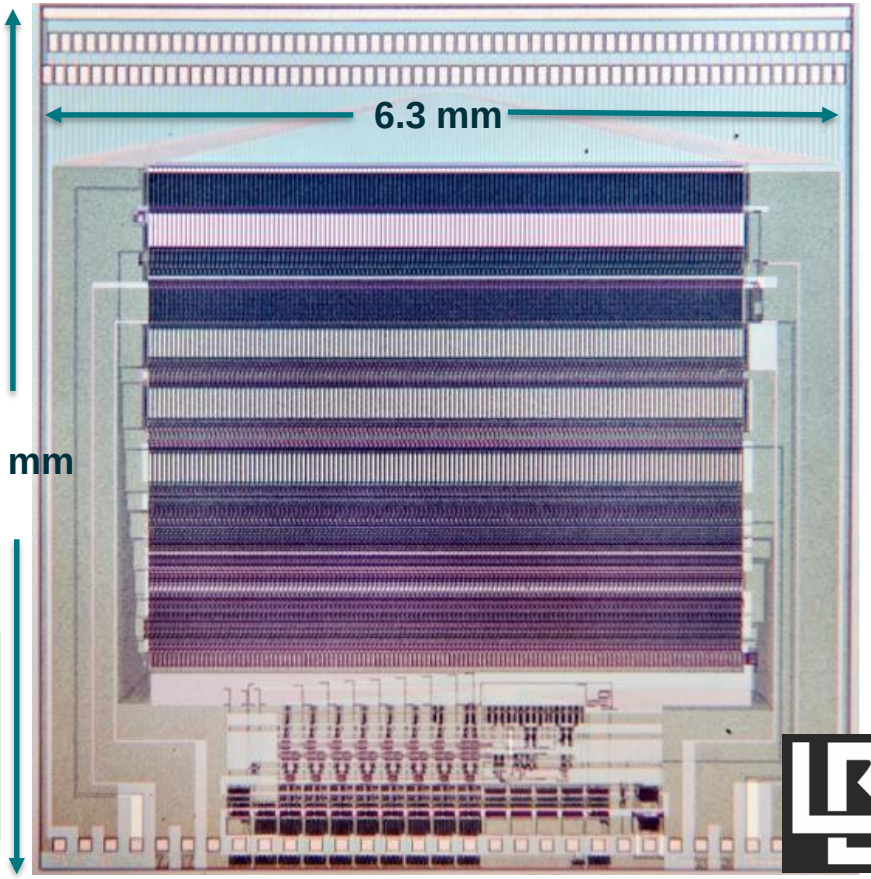


NMOS process (no P-channel devices) - SLAC - 1984

128 channels
3 mW / channel

Walker, Parker, Hyams, Shapiro, "Development of High Density Readout for Silicon Strip Detectors," NIM 226 (1984)

SVX – First CMOS ASIC for Physics Research



11,000 transistors

CDF experiment used 240 SVX chips → 30720 channels

Already at discrete limit

THE MOSIS SERVICE

CMOS process (with P-channel devices) - LBNL - 1987

128 channels
1.25 mW / channel

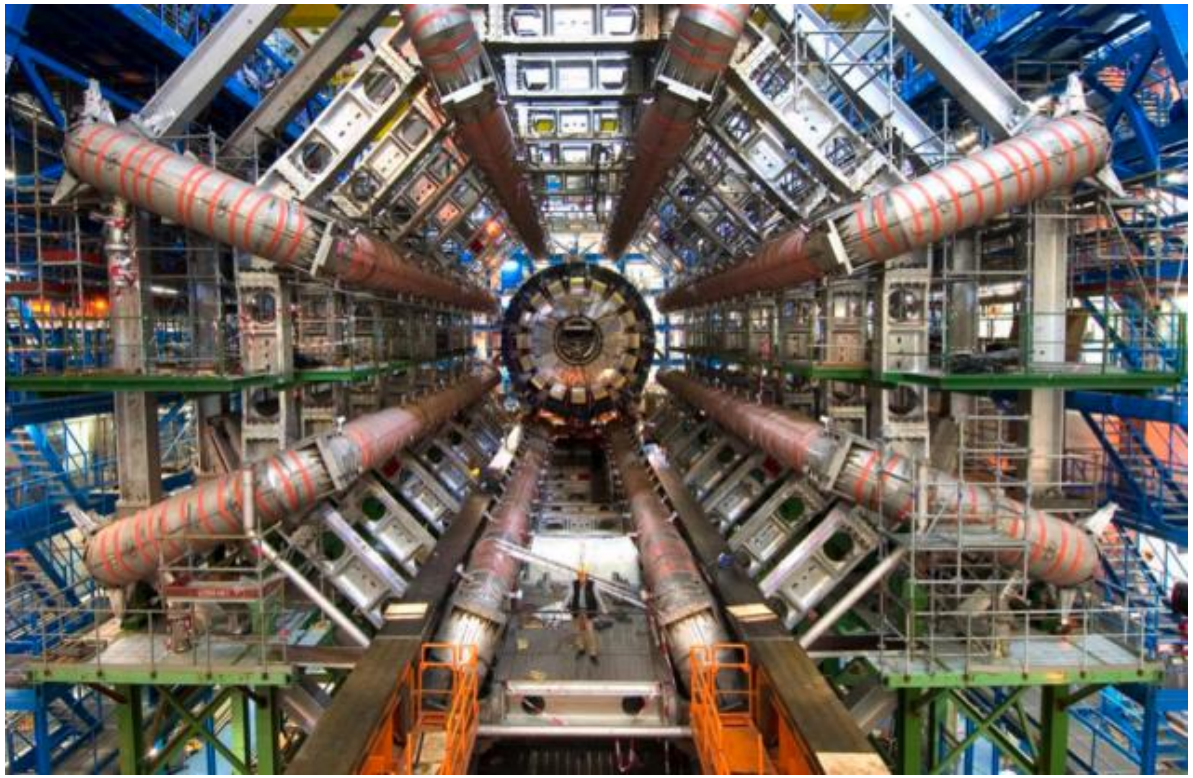
Kleinfelder, et al.; "A Flexible 128-Channel Silicon Strip Detector Instrumentation Integrated Circuit with Sparse Data Readout", TNS 35 (1988)

Technology soon advanced to make on-chip ADCs practical

Unique Challenges for HEP ADCs

Physics experiments often create extreme environments for their readout ASICs

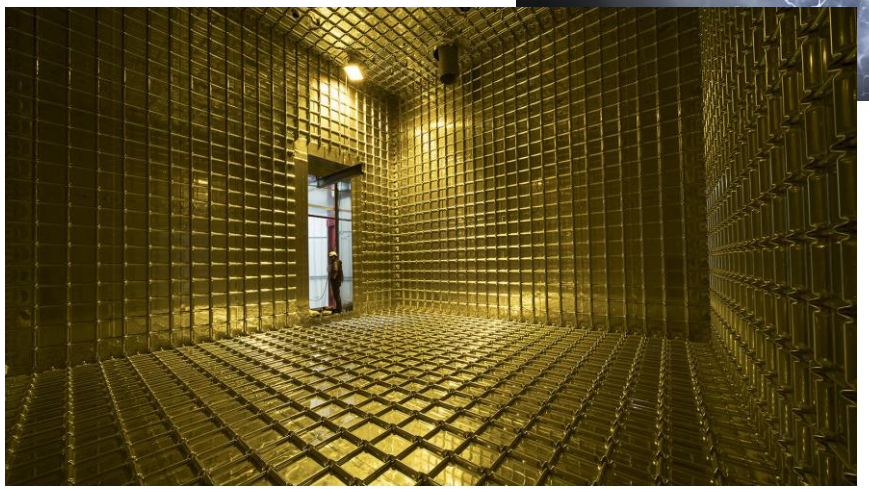
High Radiation



ATLAS Detector

Cold Temperature

Liquid Argon

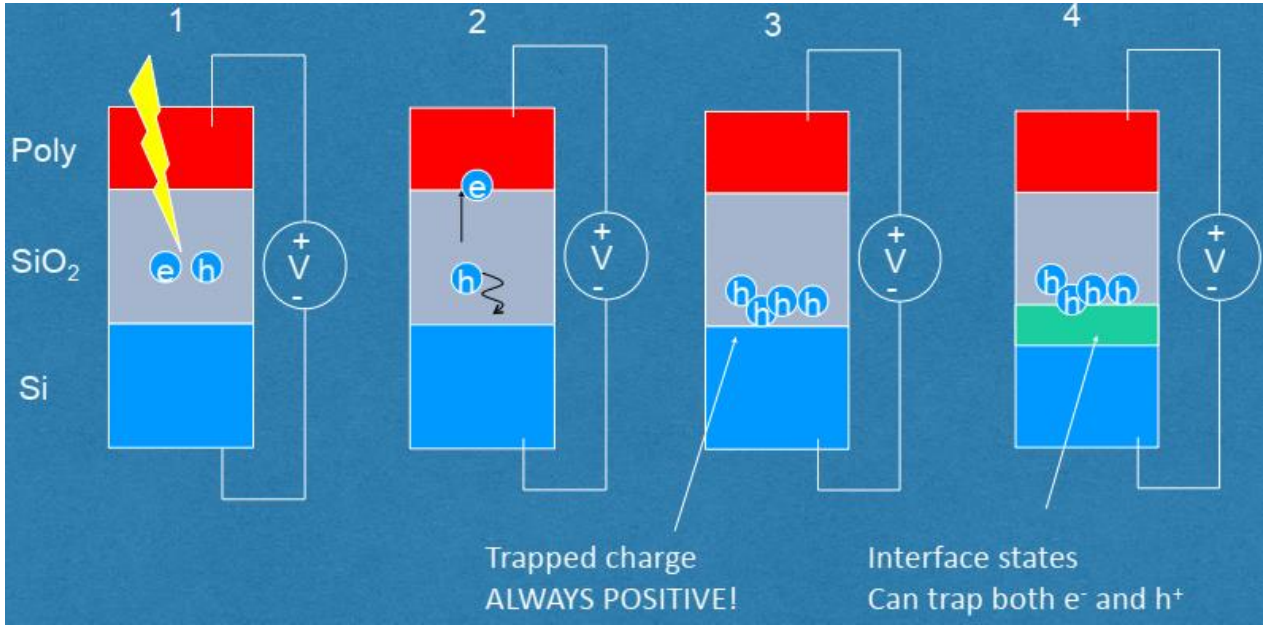


ProtoDUNE LAr TPC

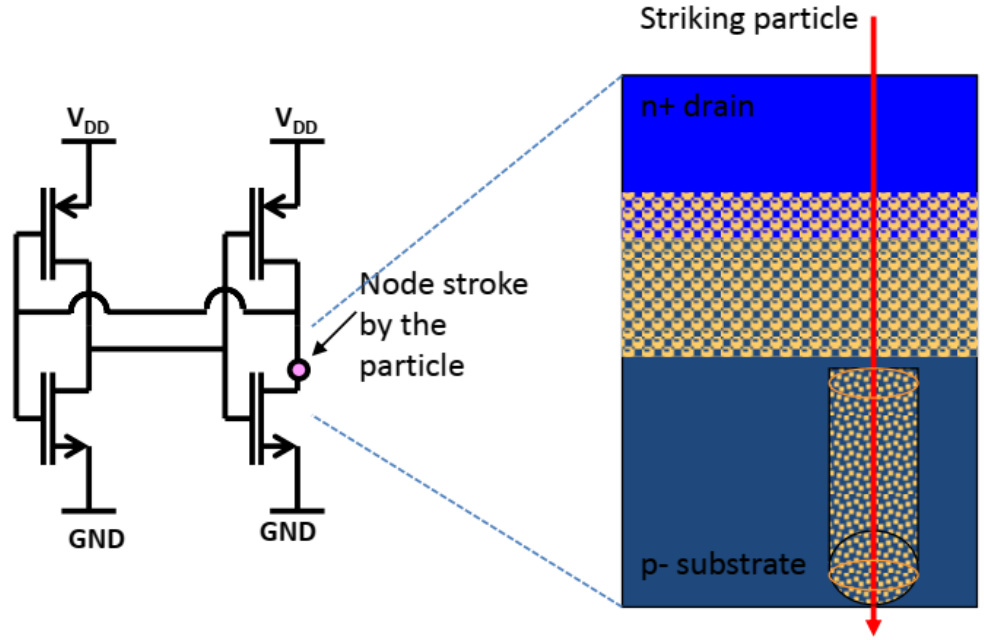
Unique Challenges for HEP Custom ADCs - Radiation

Two main types of radiation damage to integrated circuits that concern us (Single Event Latchup and Single Event Transients of less importance in HEP experiments)

Total Integrated Dose – structural damage to silicon structure that leads to failures

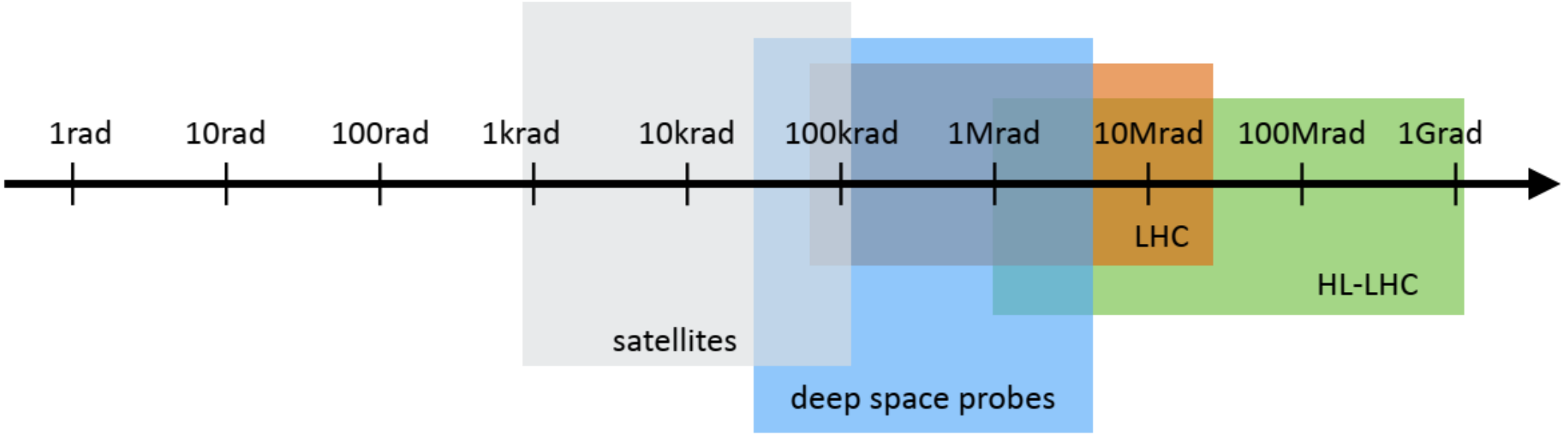


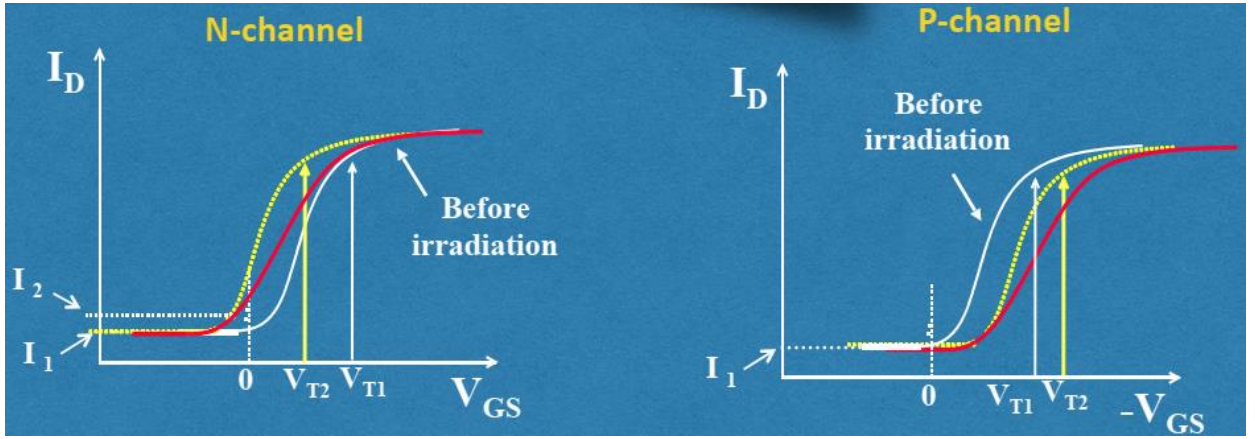
Single Event Upset – transient effects that could modify data or lead to incorrect data



Radiation -- Total Integrated Dose (TID)

Requirements for TID radiation tolerance for physics far exceed any commercial application



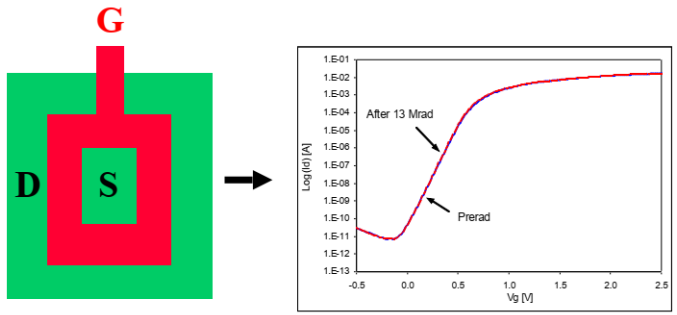


Radiation -- Total Integrated Dose (TID)

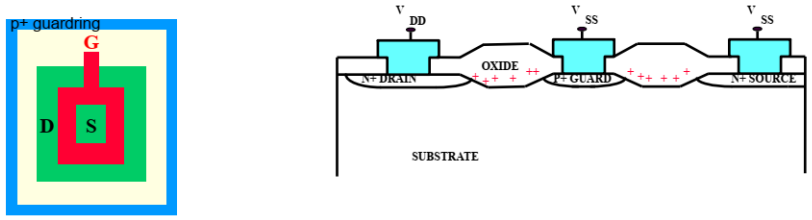
Key mitigations:

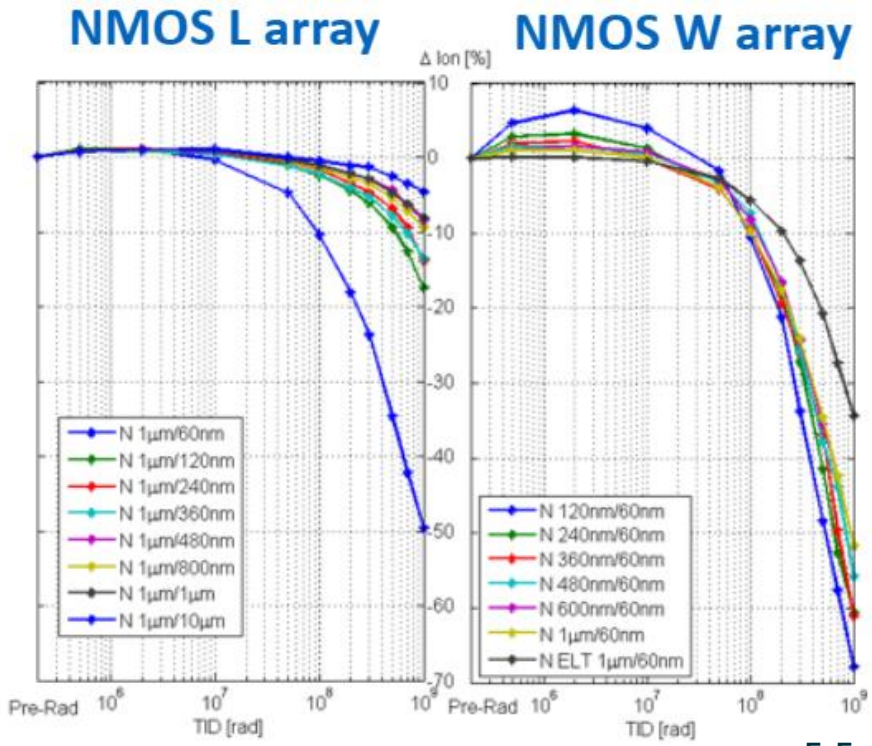
- use scaled technologies (Microplex and SVX only radiation tolerant to 10s of krad)
- “Hardness-By-Design” techniques (long devices / enclosed layout / guard rings / etc)
- Annealing

Source-Drain leakage is eliminated by the Enclosed Layout Transistor (ELT)…



Inter-diffusion leakage is eliminated by p+ guard rings…

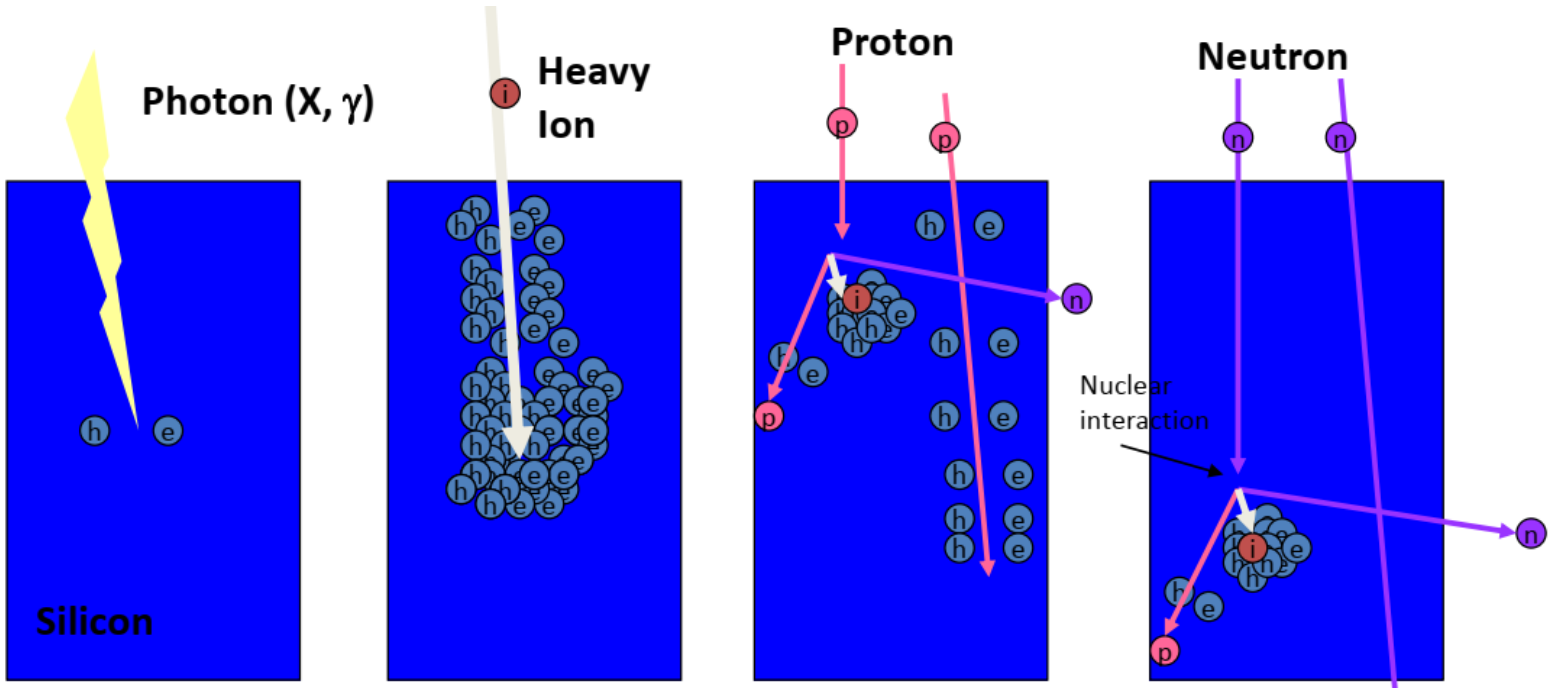




F. Faccio

Radiation – Single Event Effects (SEE)

Scaling devices makes ASICs more resilient to TID, but *less* resilient to SEE

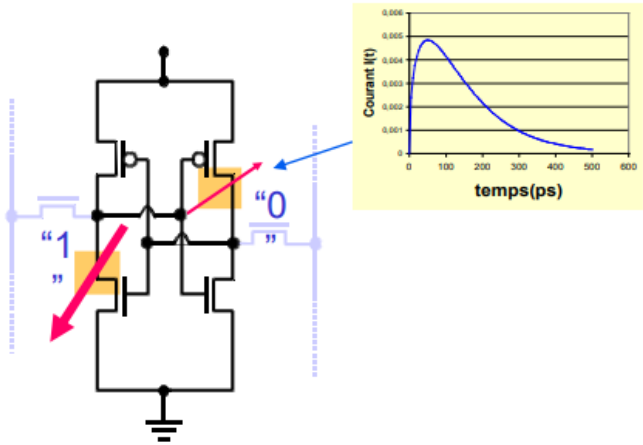


Small density of e-h pairs

Large density of e-h pairs

Small (proton) or no (neutron) density for direct ionization. Possible high density from Heavy Ion produced from nuclear interaction of the particle with Silicon nucleus.

C. Zamantzas



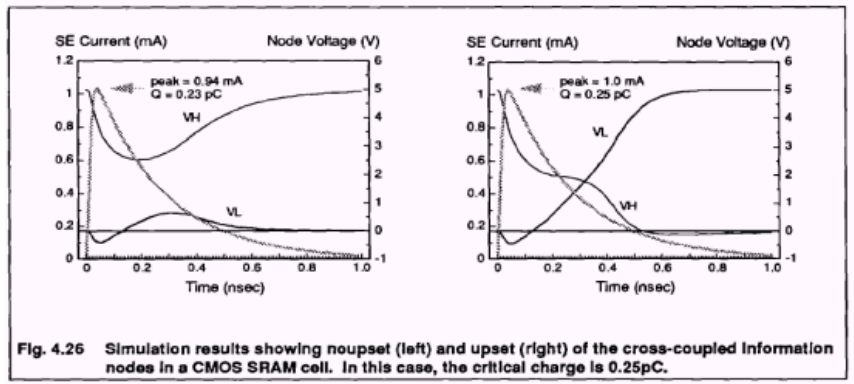
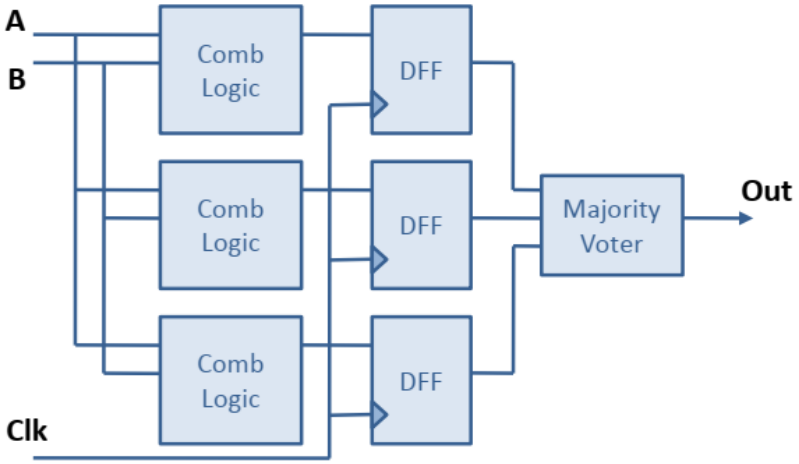


Fig. 4.26 Simulation results showing noupset (left) and upset (right) of the cross-coupled information nodes in a CMOS SRAM cell. In this case, the critical charge is 0.25pC.

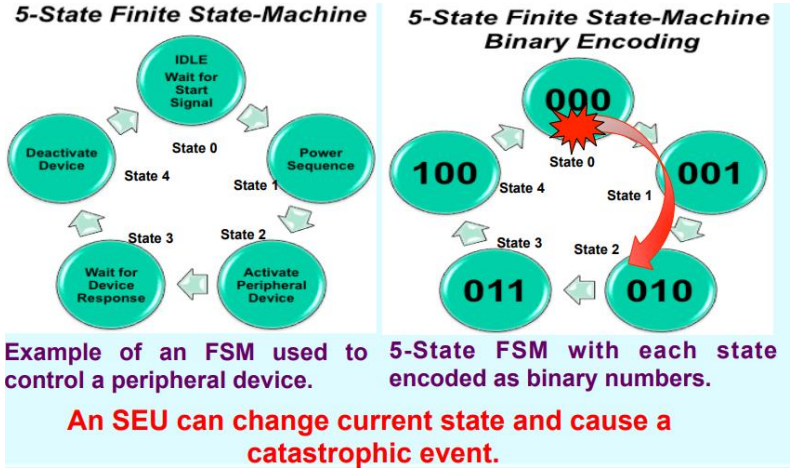
R. Gaillard

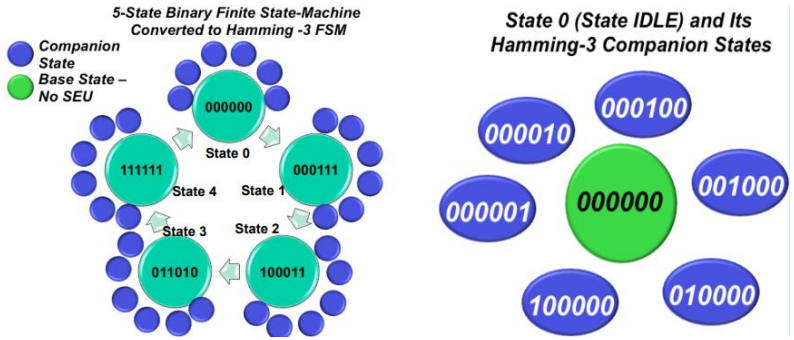
Radiation – Single Event Effects (SEE)

Key mitigations: Triple Modular Redundancy (TMR), Hamming encoding, continuous reconfiguration

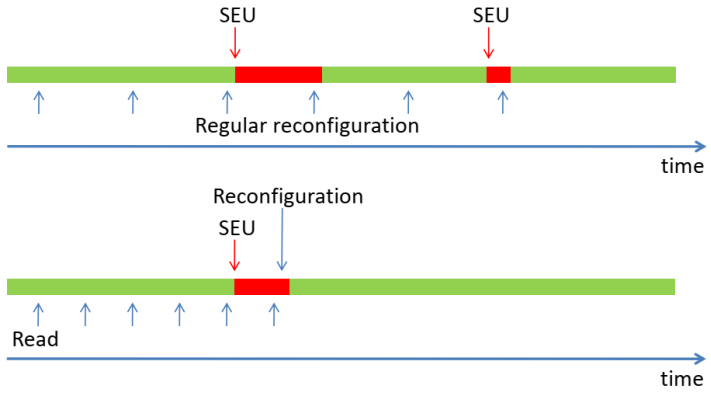


Triple Modular Redundancy (TMR)
- Device level? Circuit? Module?





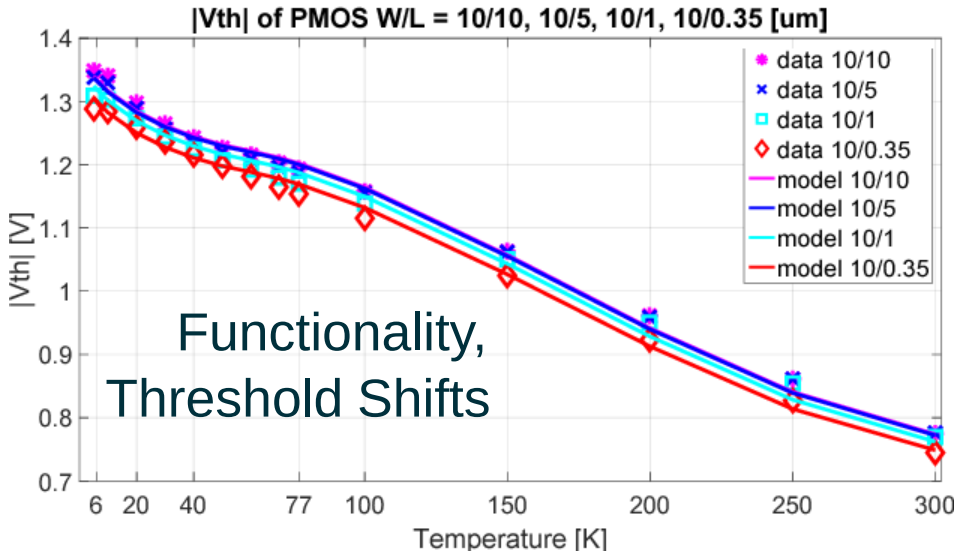
Hamming encoding

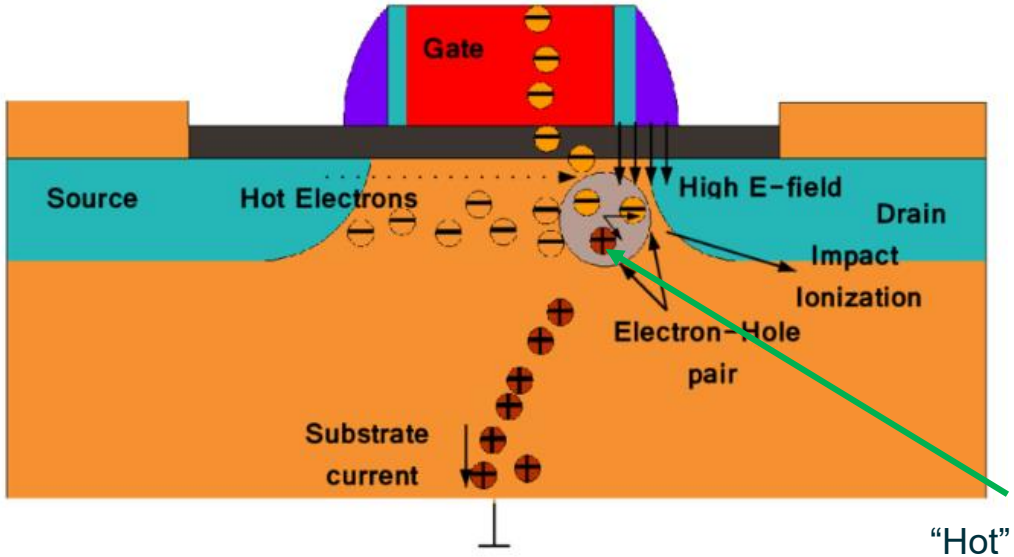


Continuous Reconfiguration

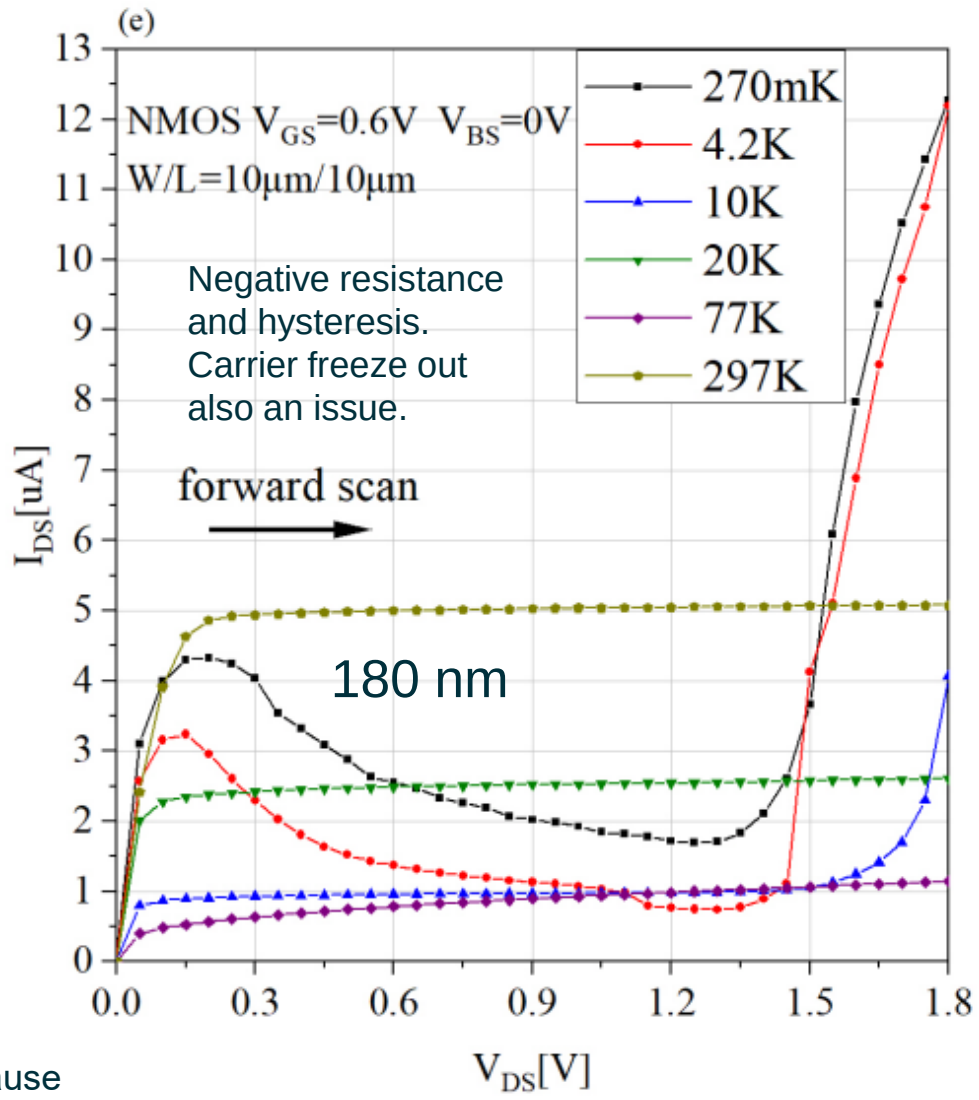
K. Berg

Cryogenic Operation





Reliability and biasing drift

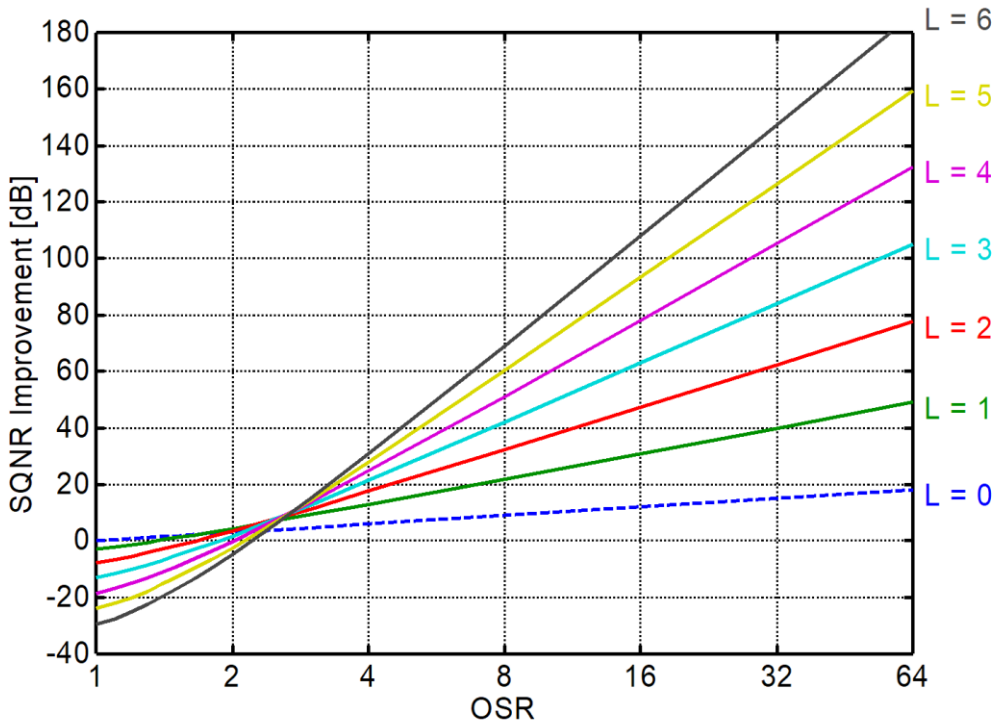


"Hot" carriers cause early device aging

Design Example

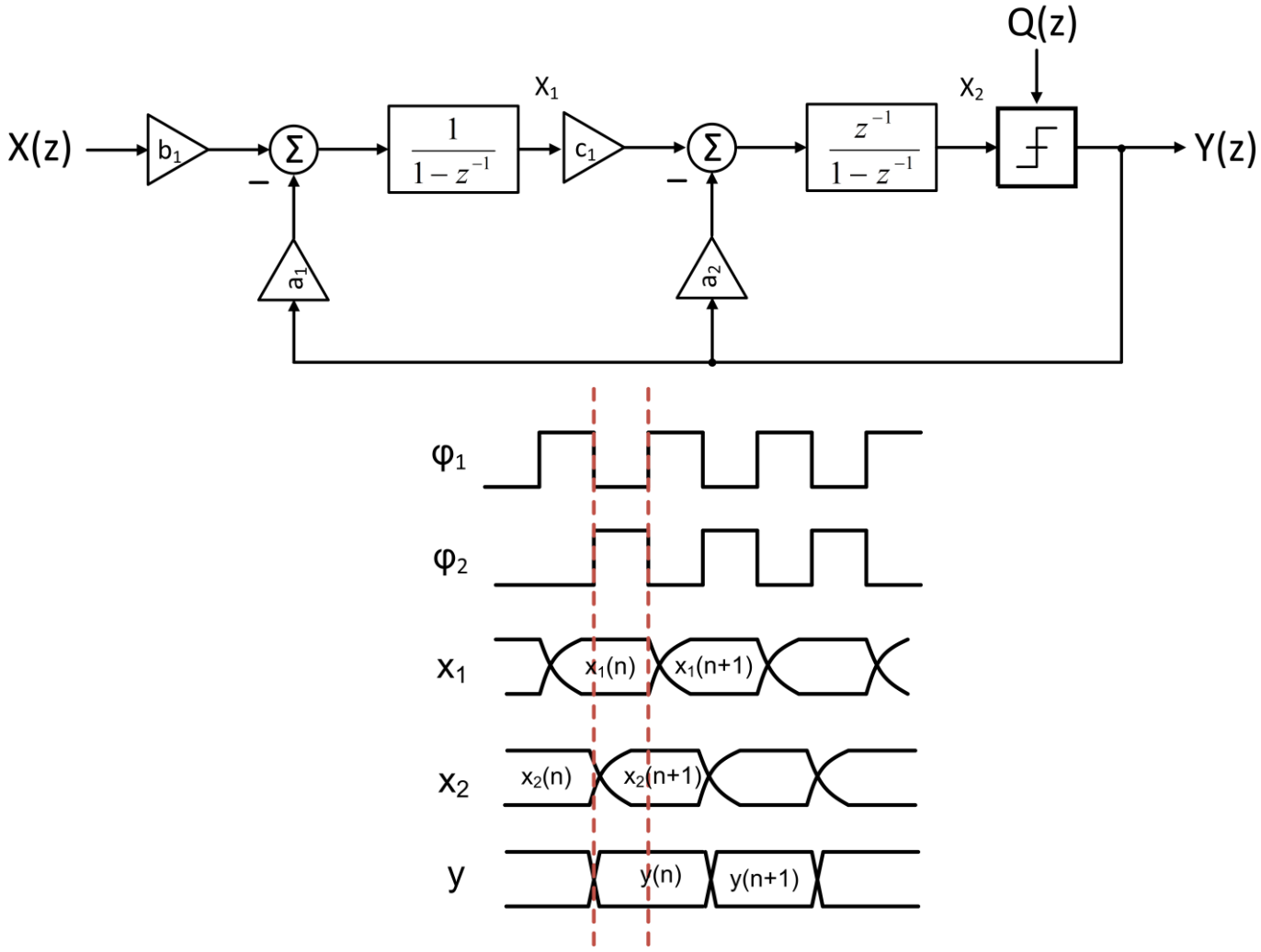
Design Example – Sigma-Delta ADC

Goal: 12b – 100 kHz ADC for power monitoring

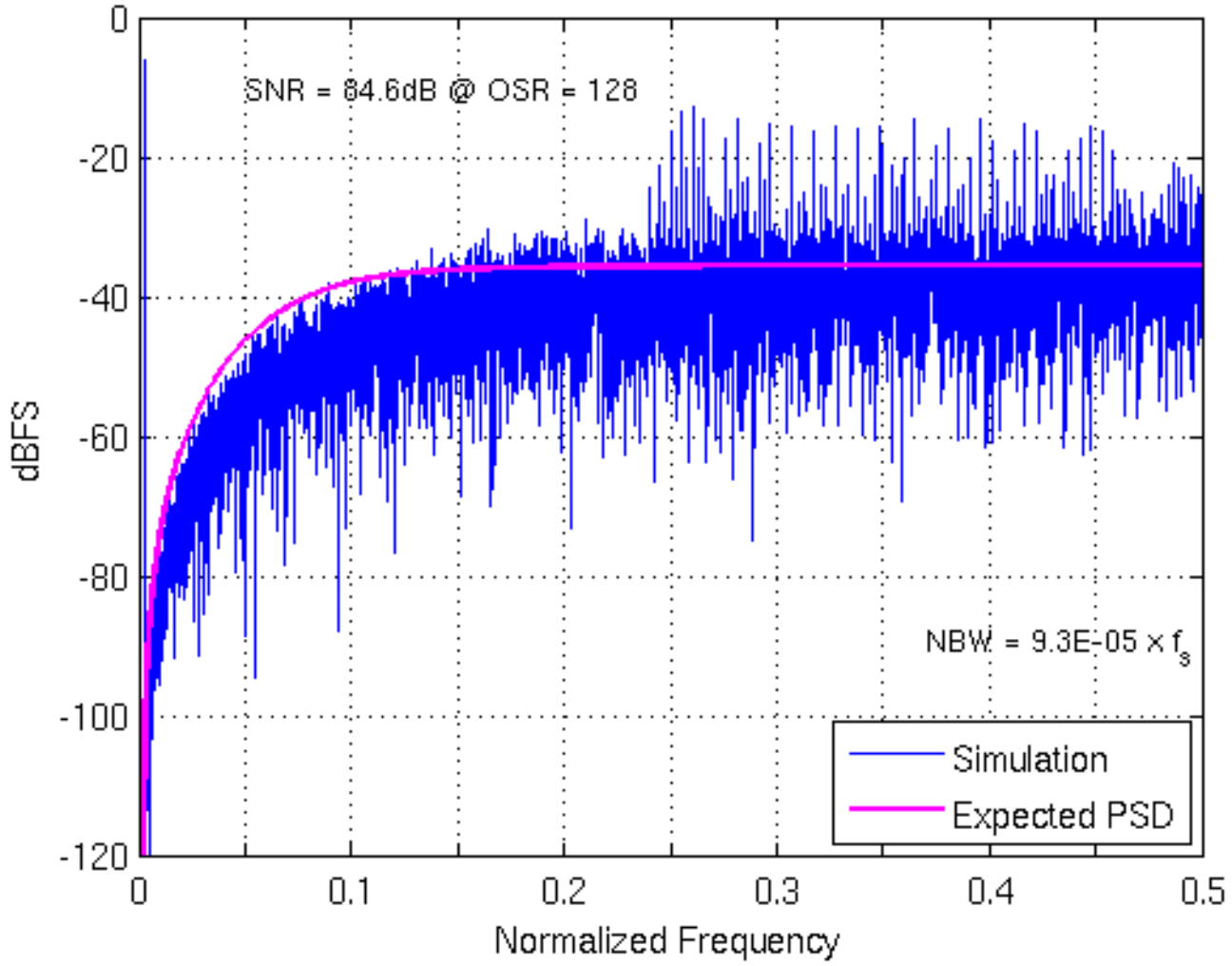


Doubling OSR improves
SQNR by (6L+3) dB
or L + 0.5 bits
Choose 2nd order modulator

Synthesize ADC transfer function in MATLAB or Python



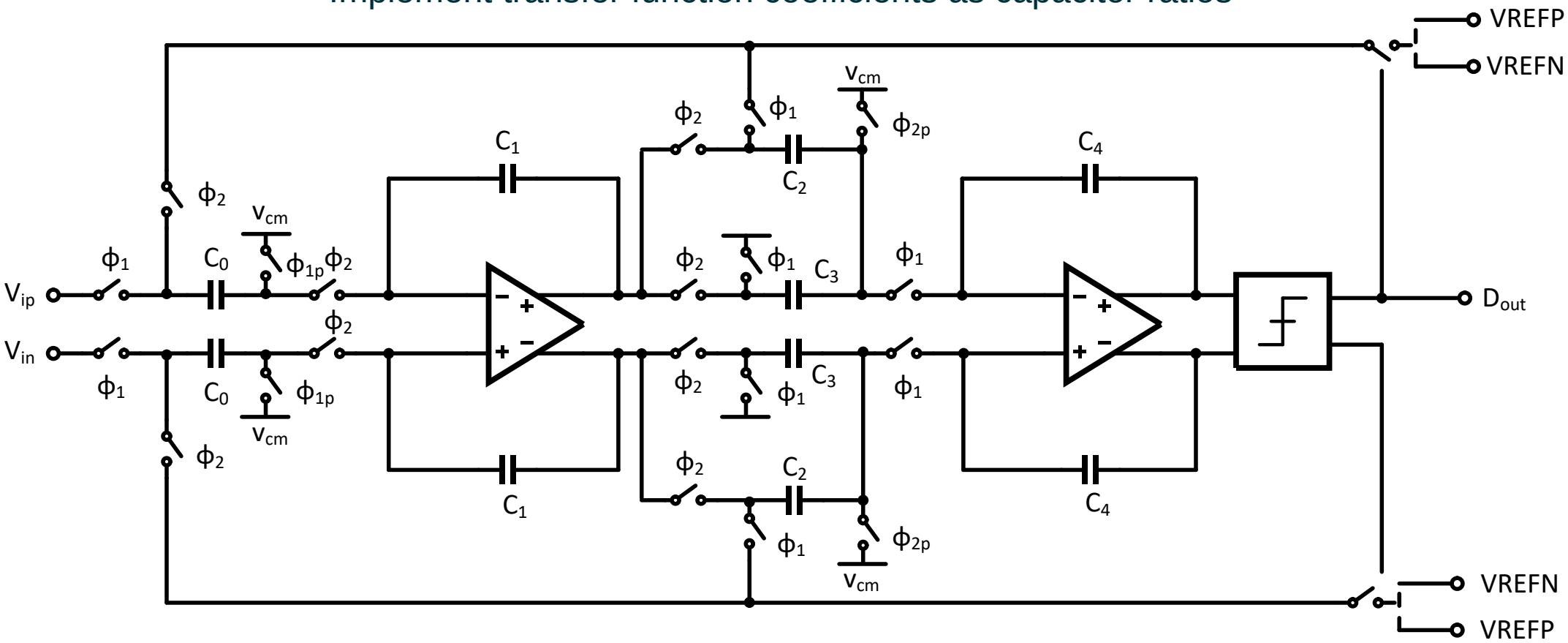
Design Example – Sigma-Delta ADC



Synthesized modulator close to ideal

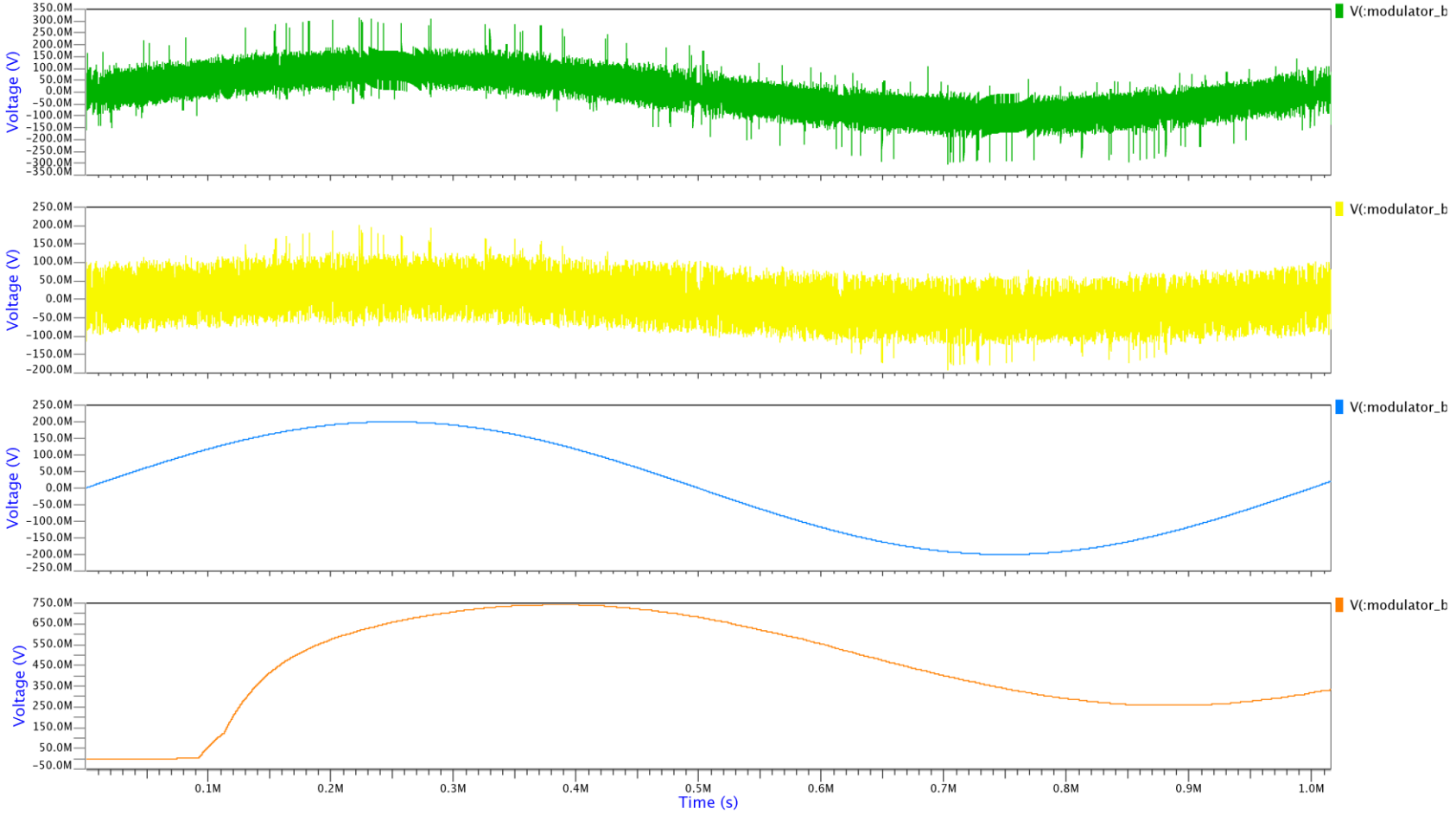
Design Example – Sigma-Delta ADC

Implement transfer function coefficients as capacitor ratios



Modulator Schematic

Design Example – Sigma-Delta ADC



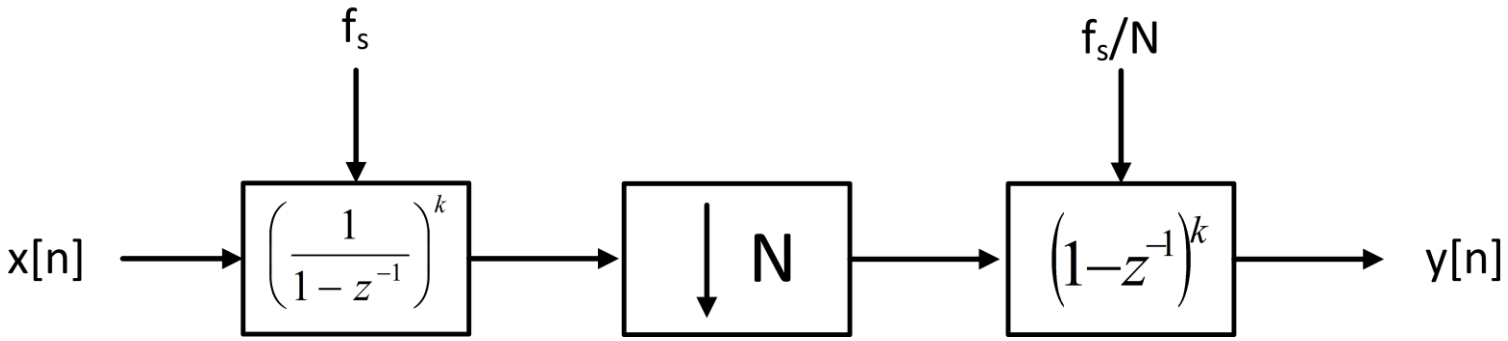
1st int

2nd int

Vinput

Digital out

Design Example – Sigma-Delta Digital Filter



Structure called Cascaded Integrator Comb (CIC) filter

For sinc³ filter: $$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^3$$

Filter implemented with Verilog HDL

C:\Users\CRGrace\Google Drive\LBNL work\projects\DUNE Cold ADC\Design Study\sinc3filter.v - Note...

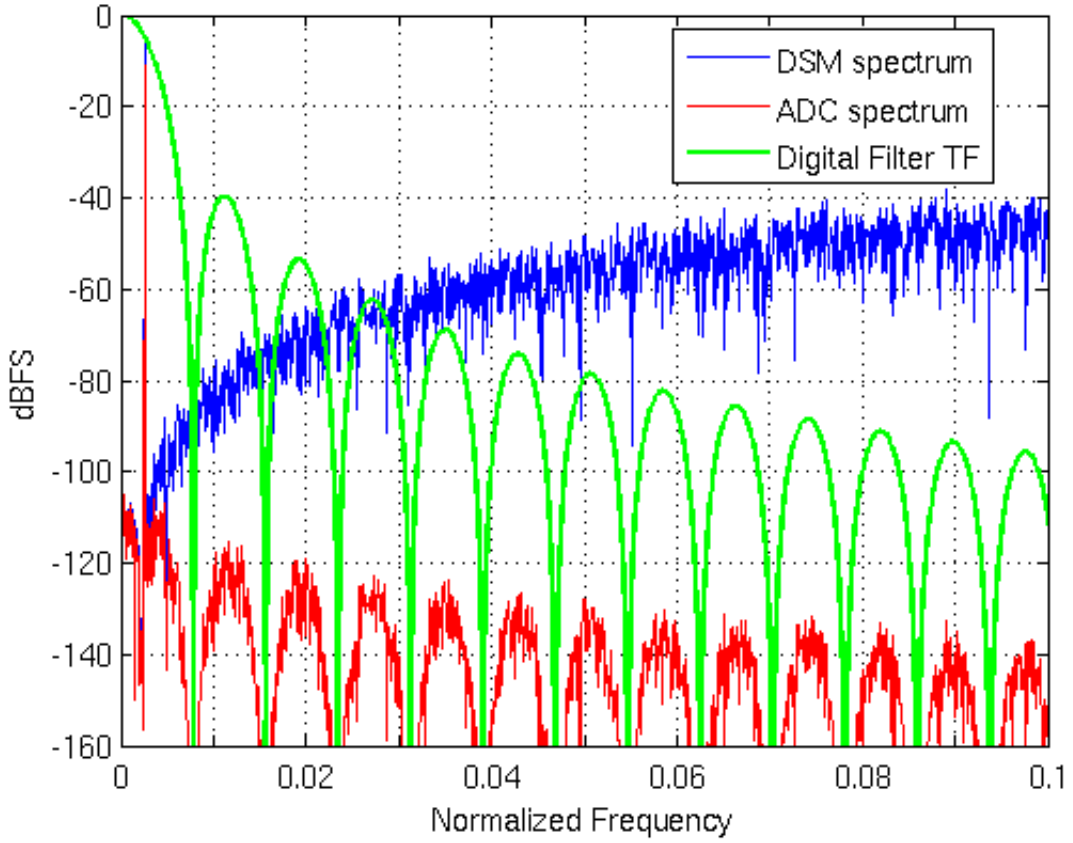
File Edit Search View Encoding Language Settings Macro Run Plugins Window ?

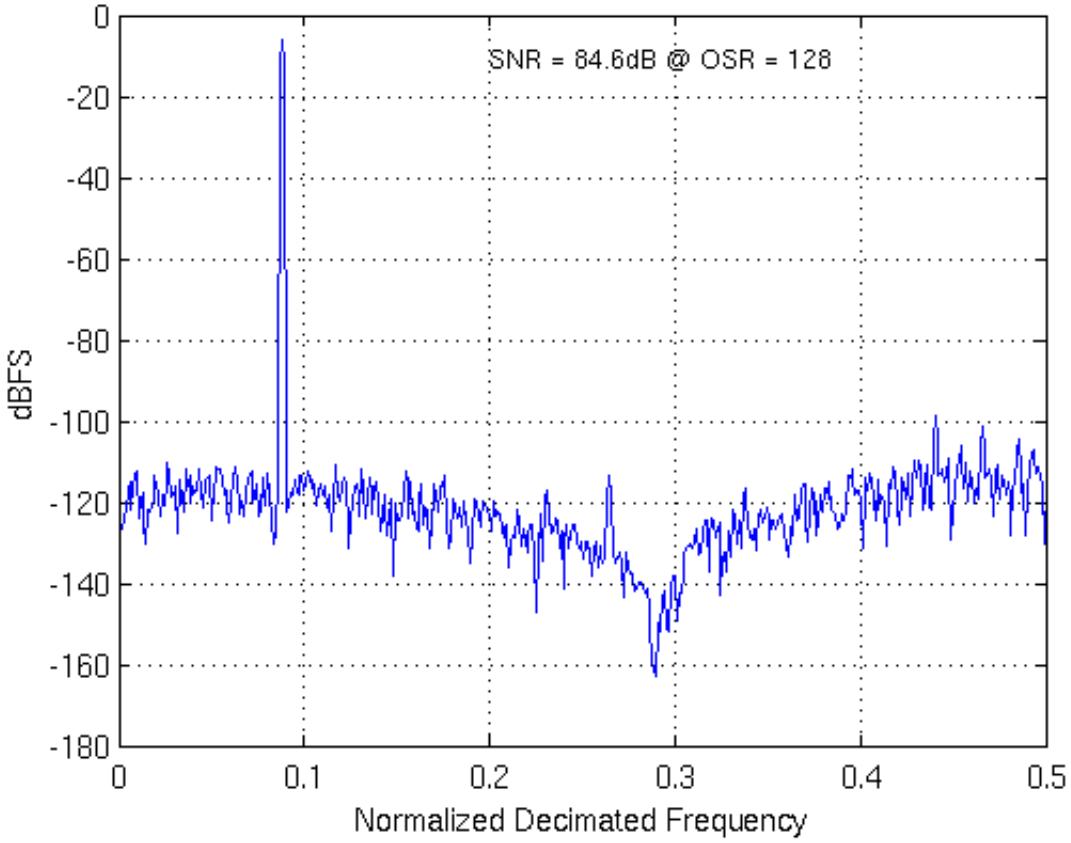
ila_1.cvs | octave_dc.m | adc_analysis.py | sinc3filter.v

```
25
26
27  /*Perform the Sinc3 ACTION*/
28  always @ (in_bit)
29    if(in_bit==0)
30      ip_data <= -1; /* change from a 0 to a -1 for 2's comp */
31    else
32      ip_data <= 1;
33
34  /*INTEGRATOR Perform the accumulation (IIR) at the speed of the modulator.
35  Z = one sample delay MCLKOUT = modulators conversion bit rate */
36
37  always @ (posedge clk or posedge reset)
38    if (reset) begin
39        /*initialize acc registers on reset*/
40      acc1 <= 0;
41      acc2 <= 0;
42      acc3 <= 0;
43    end else begin /*perform accumulation process*/
44      acc1 <= acc1 + ip_data;
45      acc2 <= acc2 + acc1;
46      acc3 <= acc3 + acc2;
47    end
48
49  /*DECIMATION STAGE (MCLKOUT/ WORD_CLK) */
50  always @ (negedge clk or posedge reset)
51    if (reset)
52      word_count <= 0;
53    else
54      word_count <= word_count + 1;
55
56  always @ (word_count) word_clk <= word_count[6];
57
58  /* DIFFERENTIATOR  Perform the comb filtering (FIR) at a lower speed.
59  WORD_CLK = output word rate */
60
61  always @ (posedge word_clk or posedge reset)
62    if(reset) begin
63      acc3_d2 <= 0;
64      diff1_d <= 0;
65      diff2_d <= 0;
66      diff1 <= 0;
```

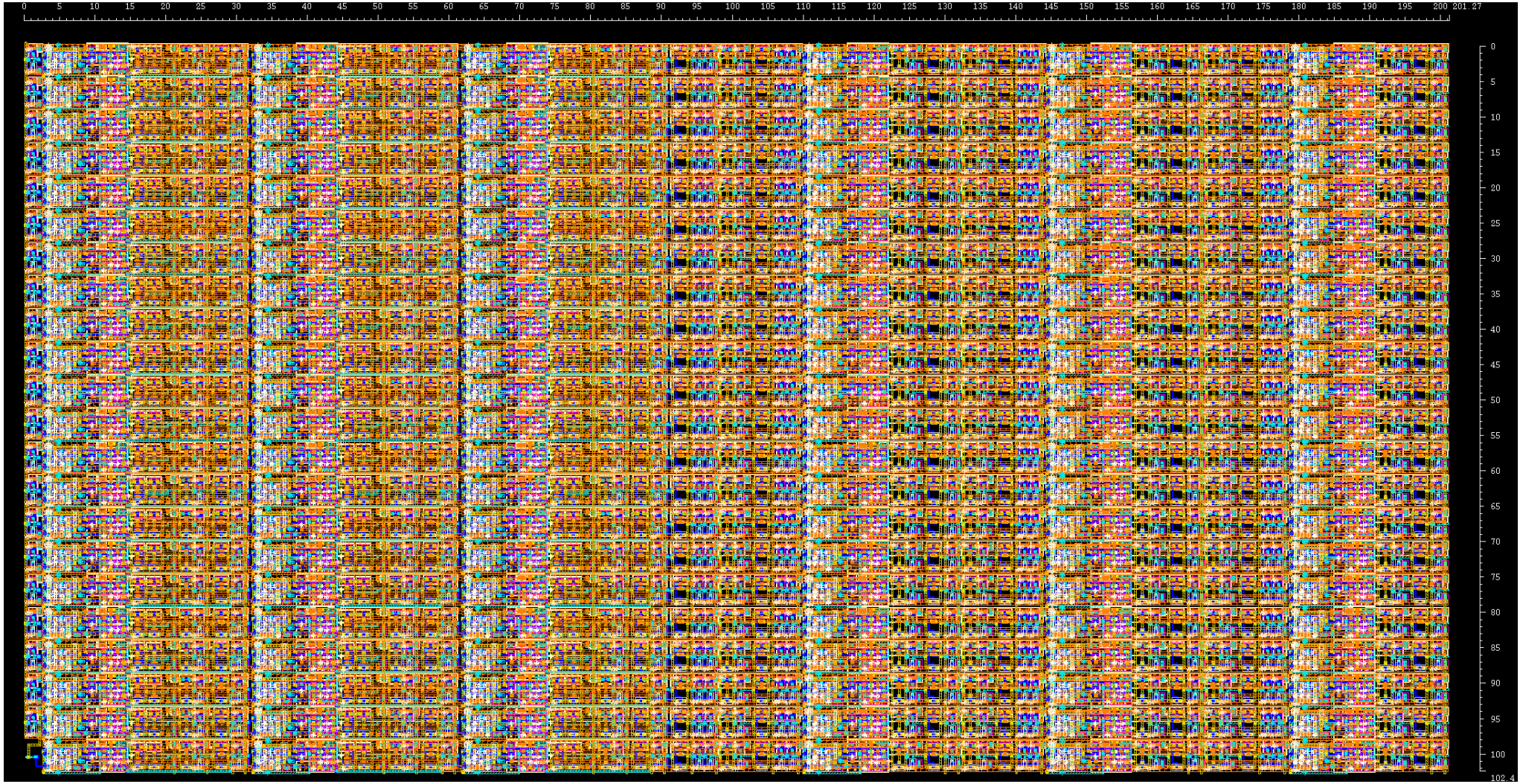
length : 2342 lines : 96 Ln : 1 Col : 1 Sel : 0 | 0 UNIX ANSI INS

Design Example – Sigma-Delta ADC





Design Example – Sigma-Delta ADC filter layout

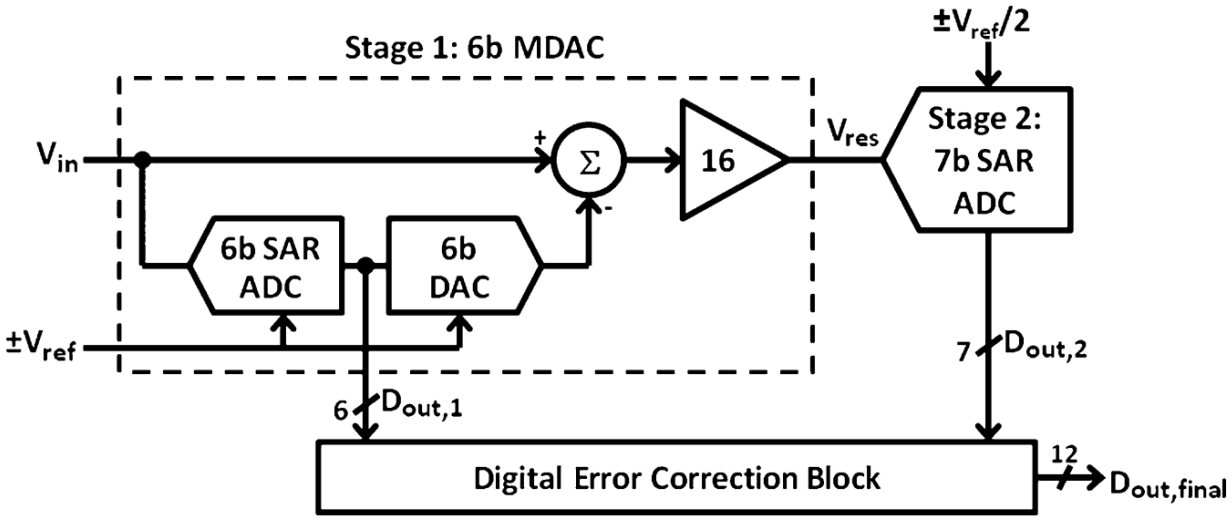


What's Next?

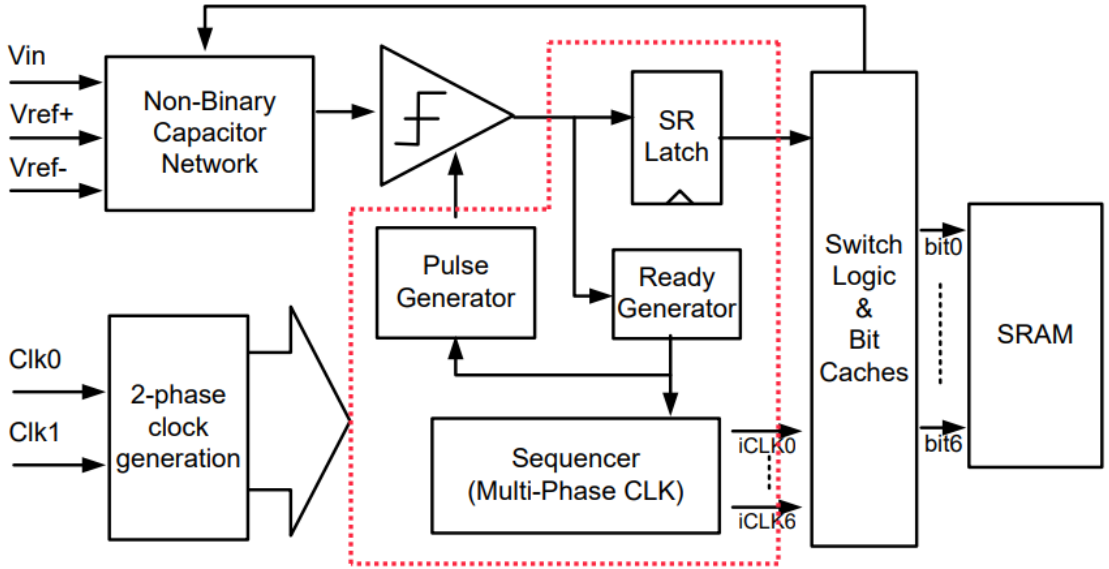
Architectures that harness the unique capabilities of scaled CMOS to improve efficiency

Examples

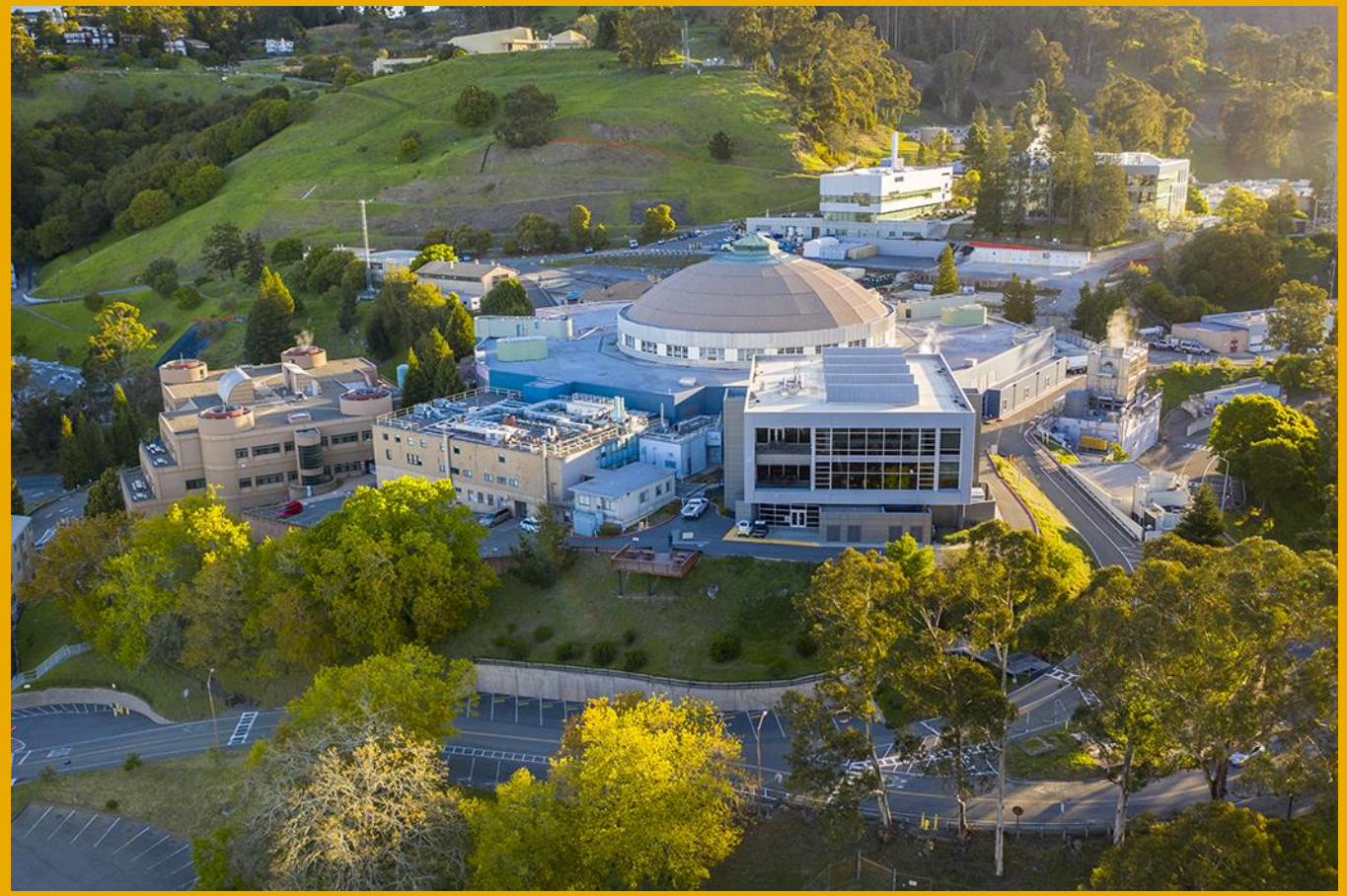
Pipelined SAR



Asynchronous SAR



Thank You



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