Silicon and CMOS HEP Sensors

HEPIC Summer Week 2023

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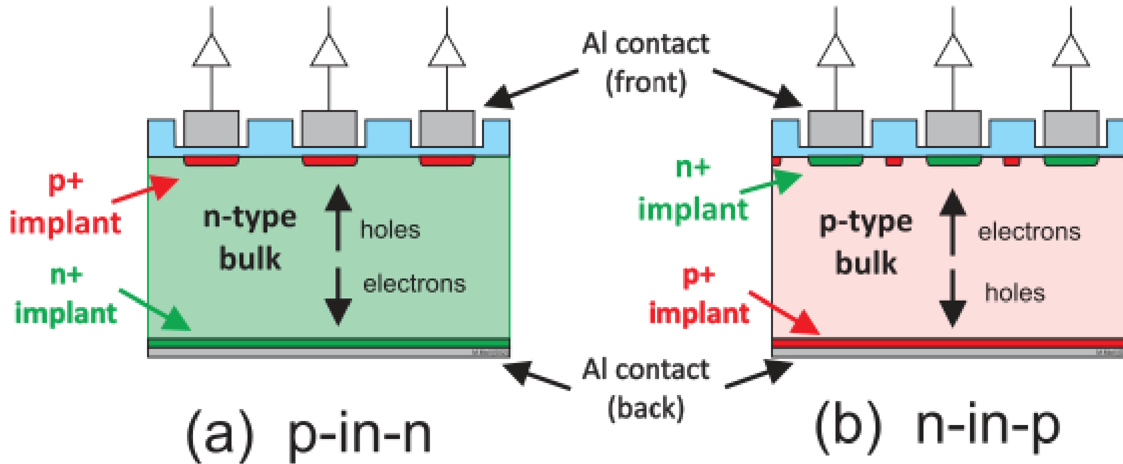
Silicon Sensor: Basic PIN Diode

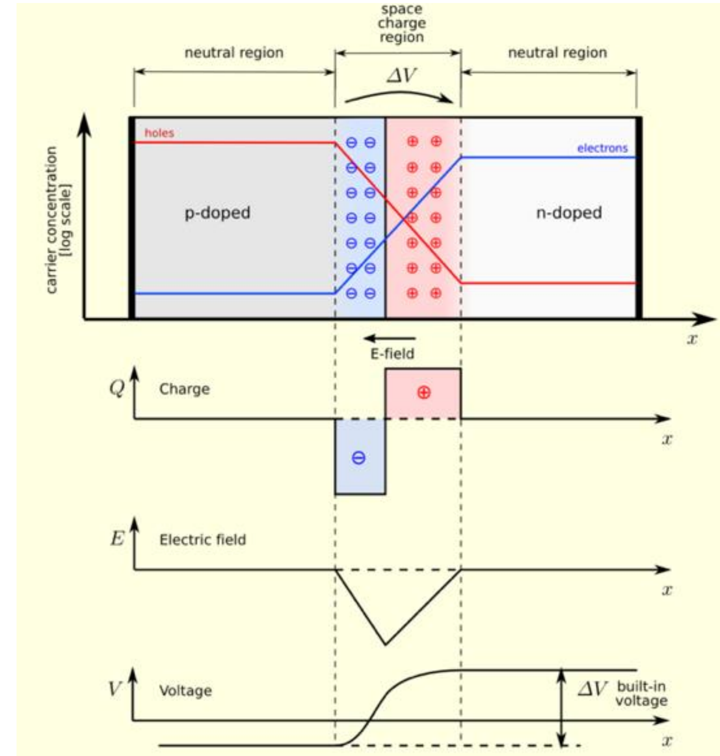


- The "I" is for intrinsic bulk, but in fact its high resistivity, or low doping concentration
- Basic device is built on silicon wafers with double-sided processing (though patterning may be only on one side
- Hole/electron pairs are created in the bulk region by ionizing radiation either holes or electrons are read-out depending on configuration

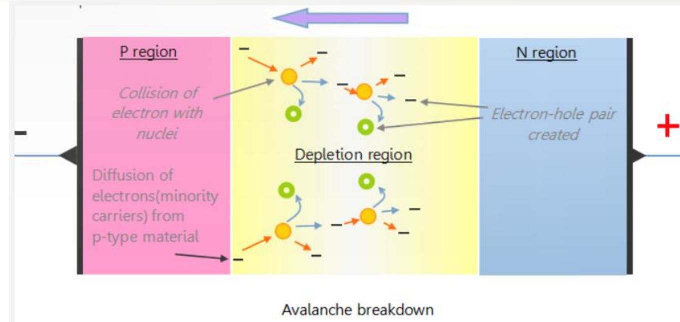
Importance of the Depletion Region depth

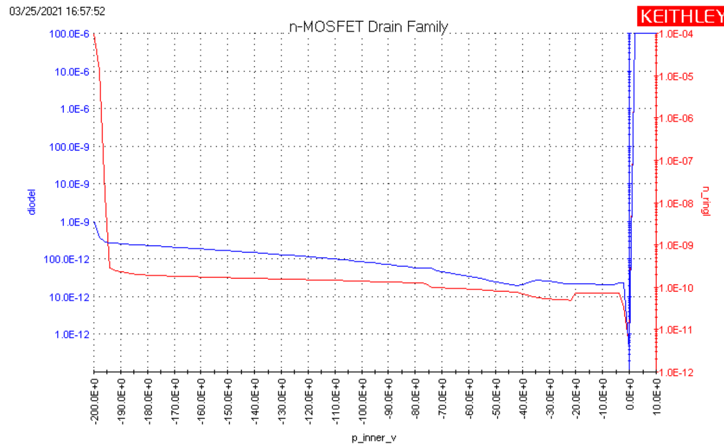
PN Diode Sensor basics

- Holes diffuse from p-doped side, electrons diffuse from n-doped side
- Depletion region, also called space charge region: p-side depleted of holes, n-side depleted of electrons creates electric field, results drift/diffusion balance
- Diode *depletion region width* inversely proportional to *doping of lower-doping concentration side*, proportional to resistivity
- Depletion width increased by reverse bias
- Commercial CMOS -> low resistivity /highly doped substrate
    - Latch-up
    - Cost/availability
- Special high-resistivity silicon used for sensors
- **Drift field is only present in depletion region**
    - ***Electron/hole pairs created in the drift region will separate can generate signal***
    - ***Electron/hole pairs generated n the neutral region will recombine***



Avalanche Breakdown: Limit to applied bias





- If electric field is high enough, carriers passing through the region create additional carriers through "impact ionization"
- Breakdown field in silicon is around 3E5 V/cm, but the actual effect depends on combination of field and distance
- The impact ionization coefficients α electrons and holes are strongly dependent on electric field:

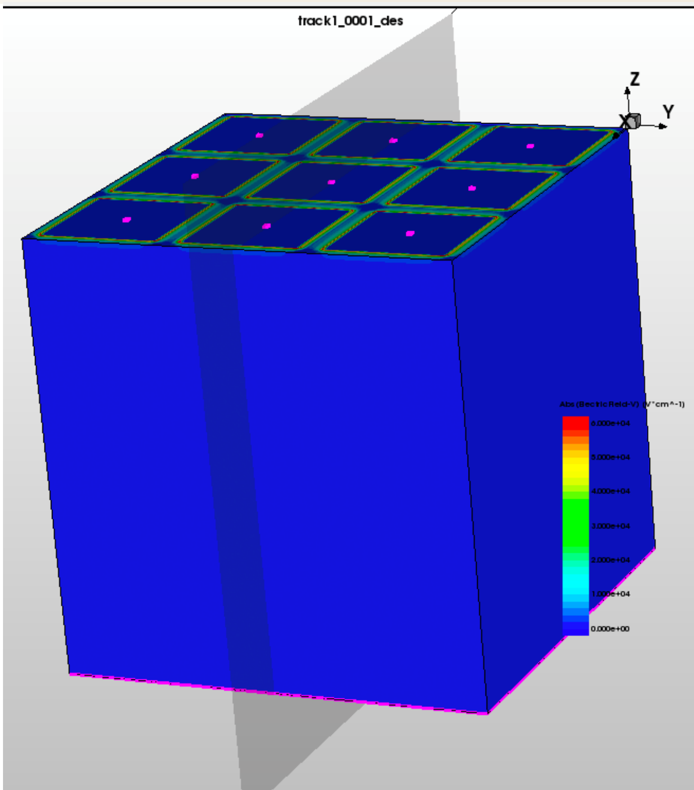
$$\alpha_{e,h} \sim \exp(-\text{const}/E)$$

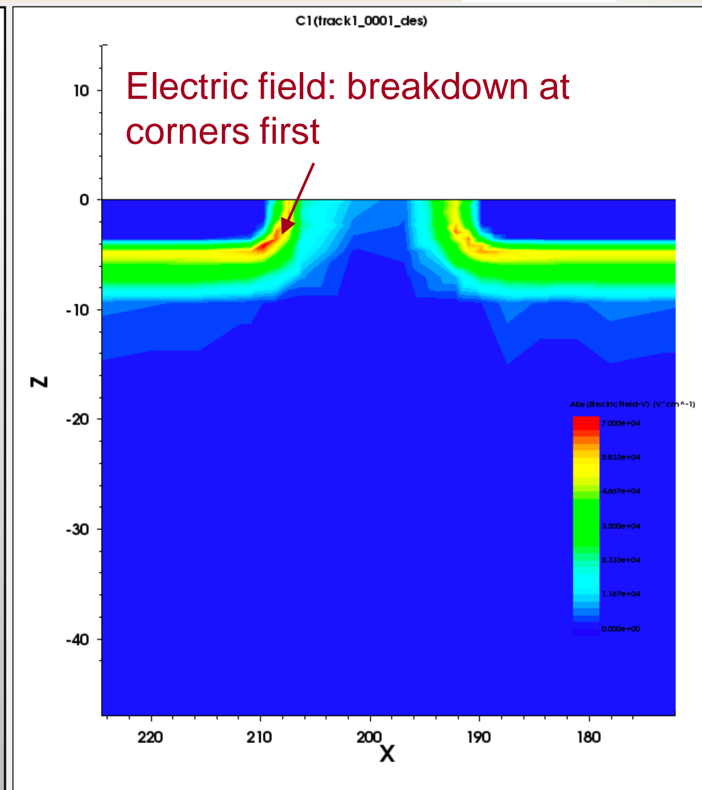
- The Ionization integral for electrons/holes is the integral of $\alpha_{e,h}$ across the depletion region. In silicon is α_e is higher.
- Multiplication

$$M = 1/(1 - \text{ionization integral})$$

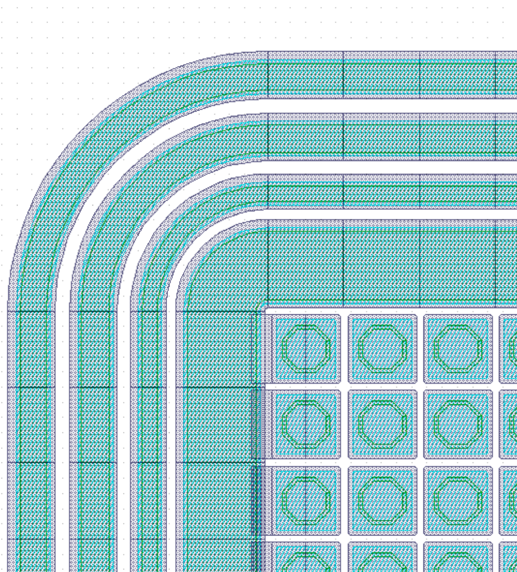
- Avalanche breakdown, or runaway breakdown occurs when the ionization integral = 1

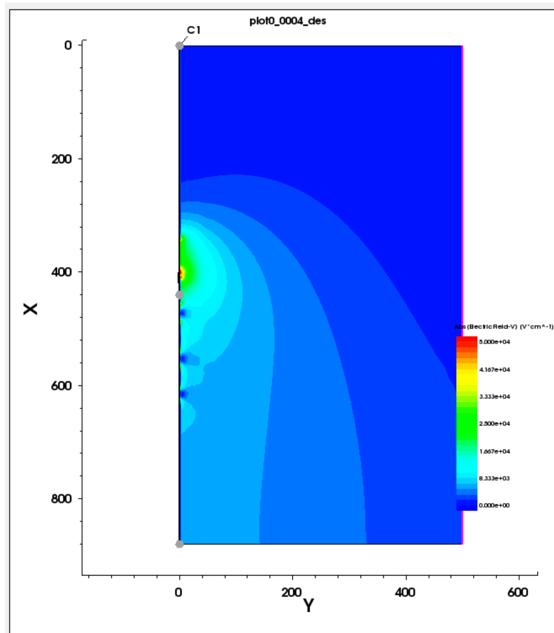
Problem: performance limited by avalanche breakdown at the edge of the diffusion region

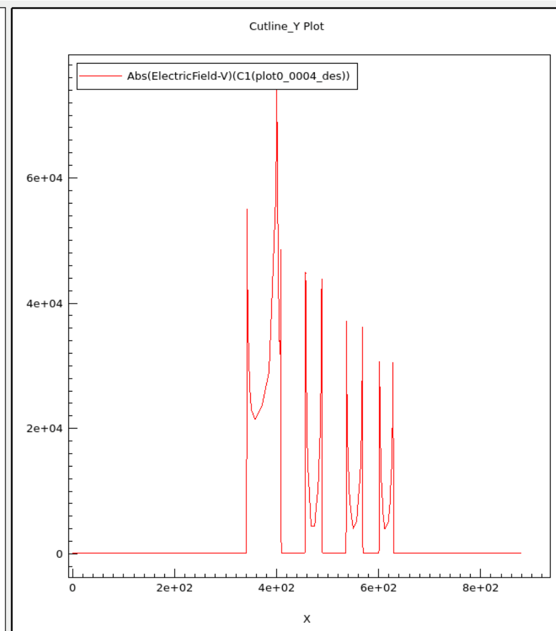




HV Termination termination structure: floating rings







Simulation of high resistivity vs. low resistivity substrate: Electric Field

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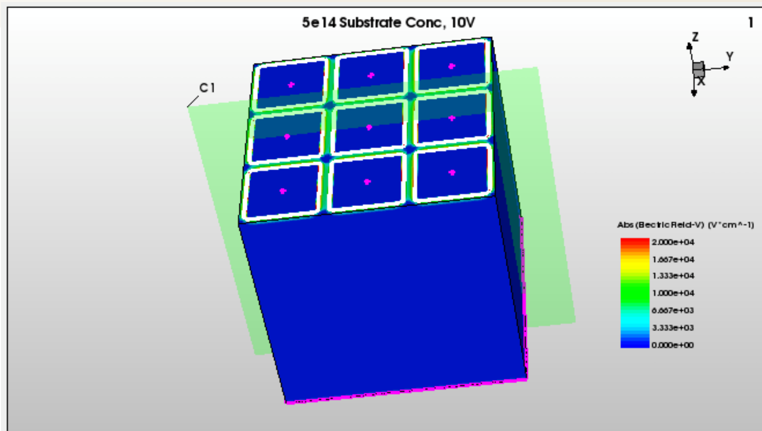
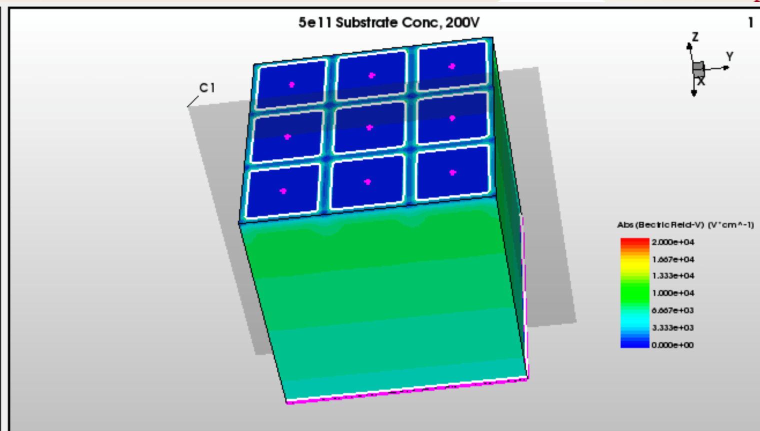
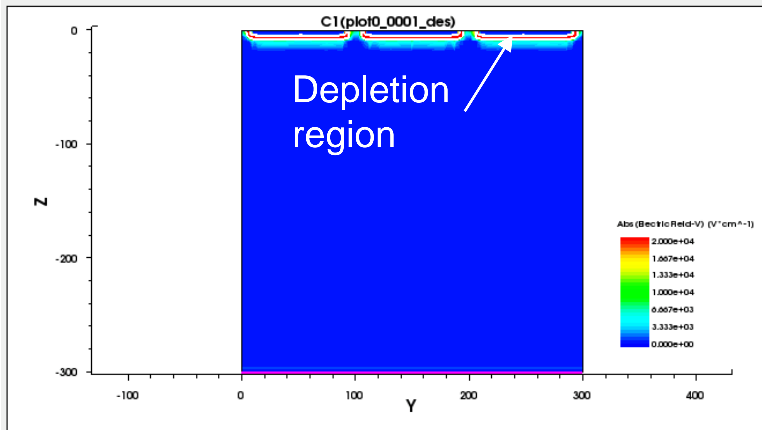
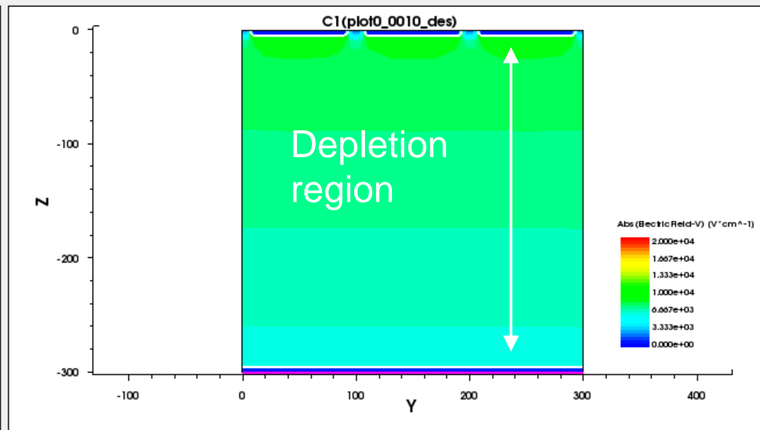
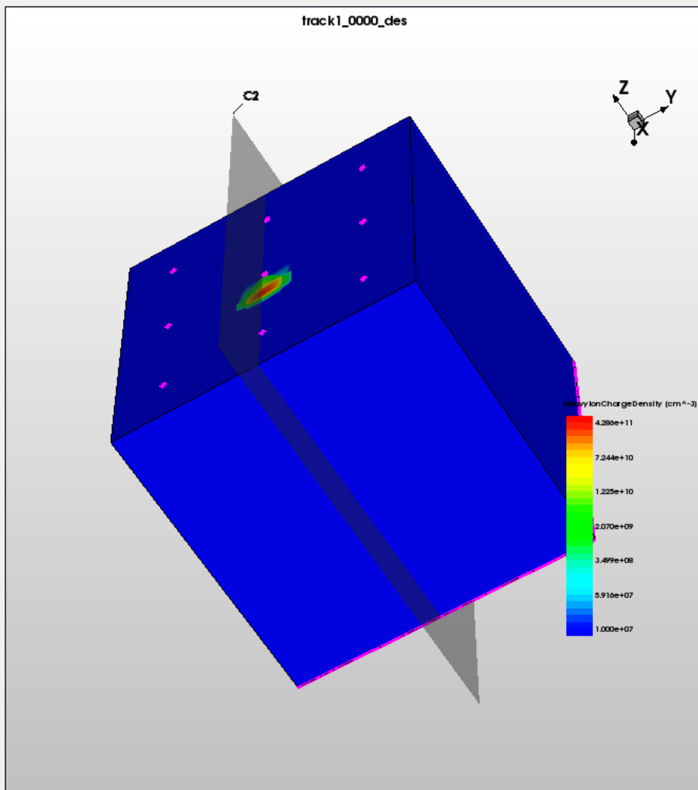


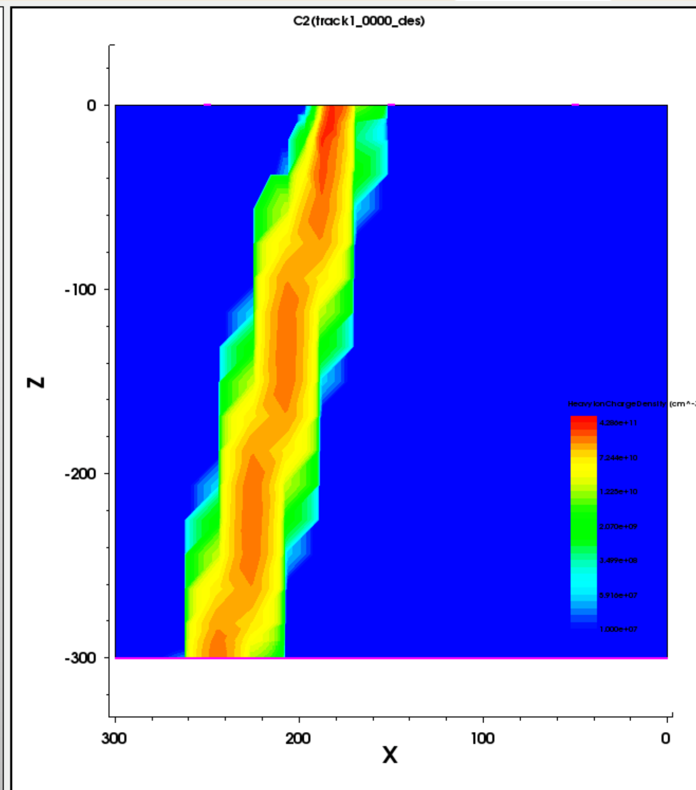






MIP (minimum ionizing particle) simulation – hole/electron pair generation





Simulations of MIP read-out signal in high-resistivity vs low resistivity bulk

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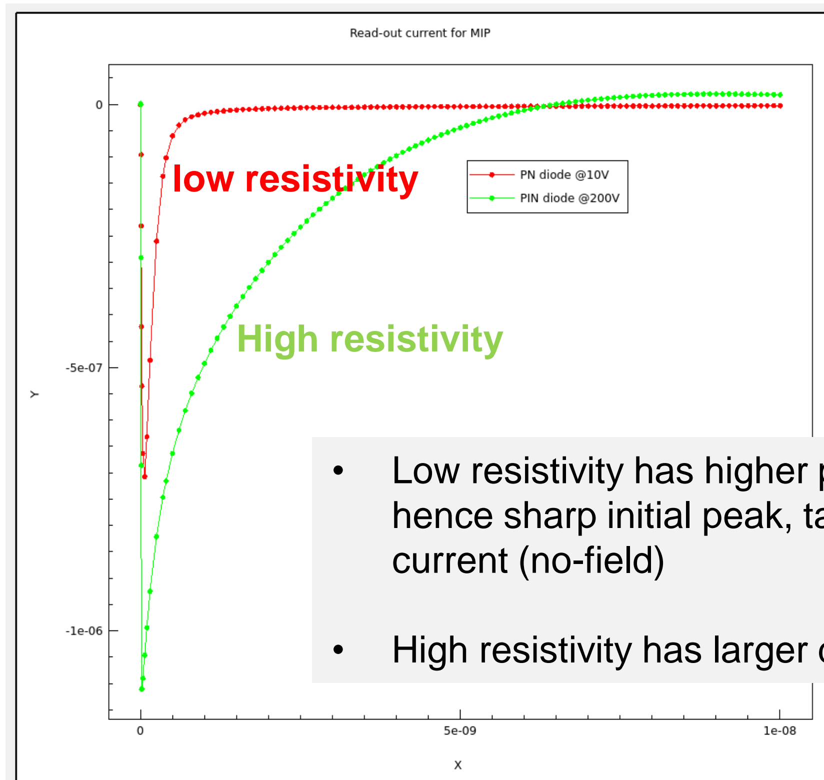

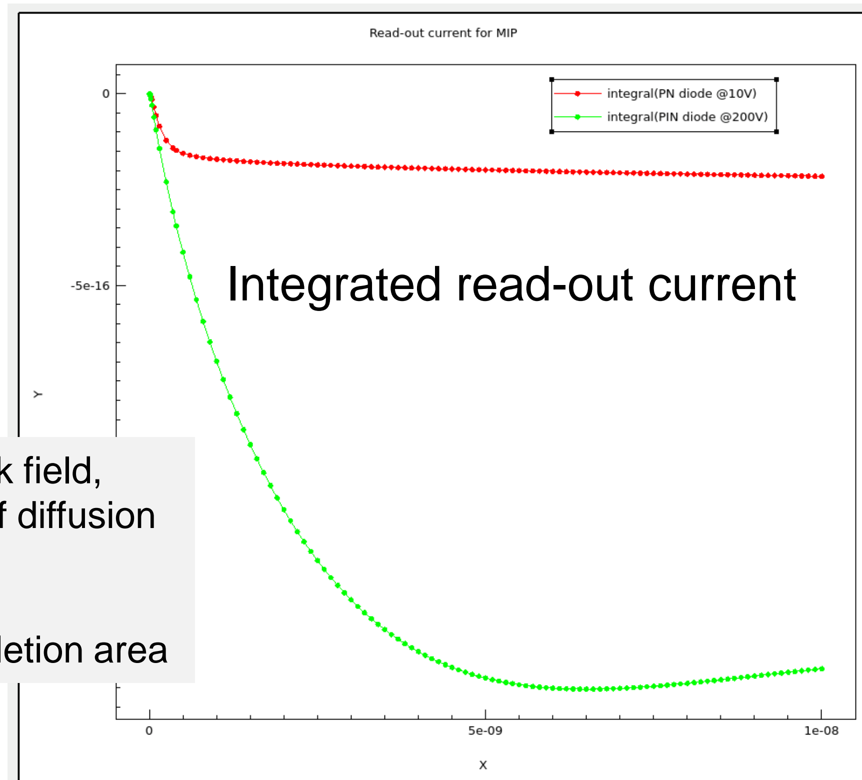

- Low resistivity has higher peak field, hence sharp initial peak, tail of diffusion current (no-field)
- High resistivity has larger depletion area

Leakage current or Dark Current

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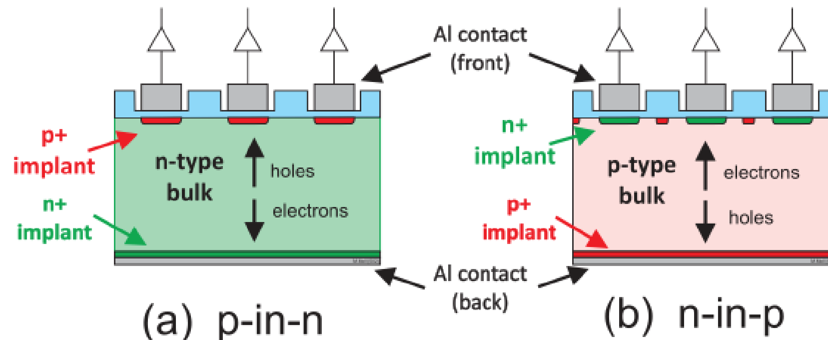
- Leakage current, or dark current, degrades signal-to-noise
- In equilibrium, SRH generation = recombination and

  $p*n = n_i^2$
- In the depletion region, p = n = 0, and generation results in leakage current:

  $I = volume_{depletion} * q * n_i / \tau$
- n_i is proportional to temperature, so cooling can help
- τ (carrier lifetime) depends on silicon quality and processing history

Surface Charge at the oxide-silicon interface

- At the silicon oxide interface, there is always a positive charge, or q_{ss}, due to dangling bonds in the silicon
- It ranges from $1E10/cm^2$ to $1E11/cm^2$ depending on oxidation process
- Electrons are attracted to the surface, creating an “n” type layer at the surface
- ”p-spray” implant may be required (n-in-p)
- Electric fields at the surface may be increased by q_{ss} or p-spray or both



Surface Leakage

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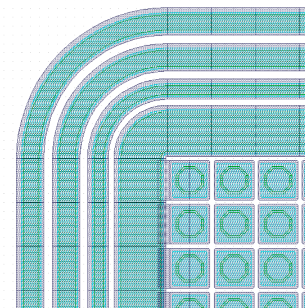
- Large surface currents can be generated at the silicon surface
  - Worst case is when the depletion region “touches” the interface, or is less than diffusion length
- The ”surface recombination velocity”, which determines the current density per area, is very strongly dependent on processing
  - Worst case is an un-passivated saw-cut, may need a biased guard ring around array to collect current
  - Best case is a polished surface with a high-quality oxide, but still want to minimize depleted surface



Strip vs Pixels: Trade-offs

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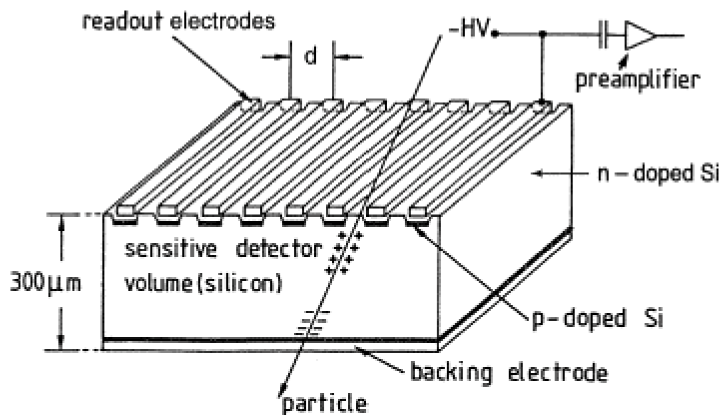
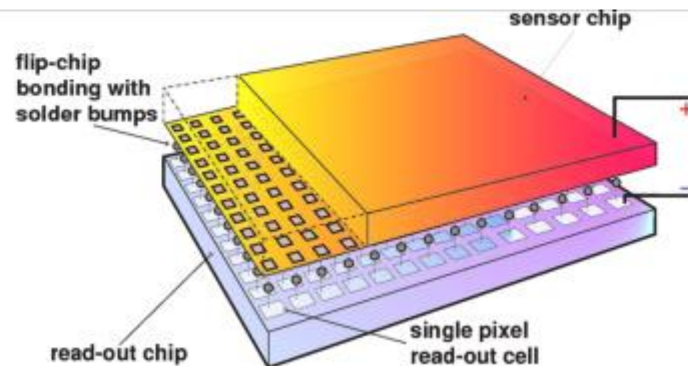
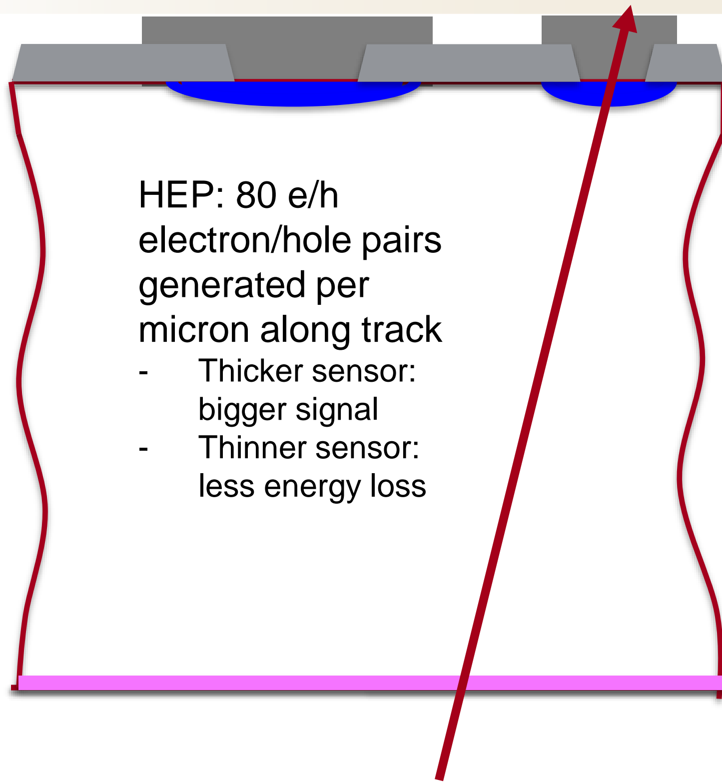
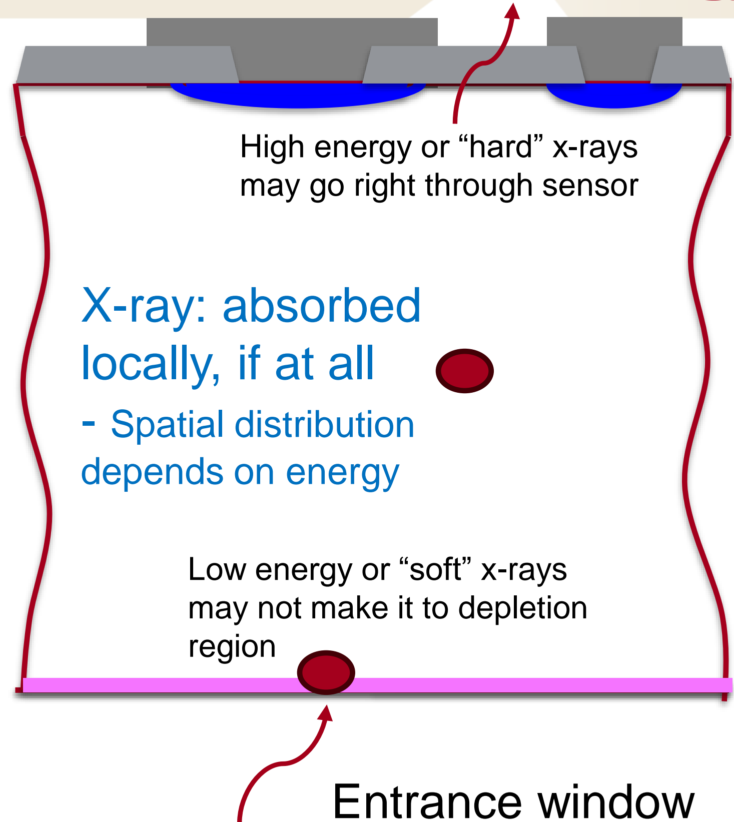
- Spatial resolution
- Capacitance (signal to noise)
- Read-out configuration/packaging





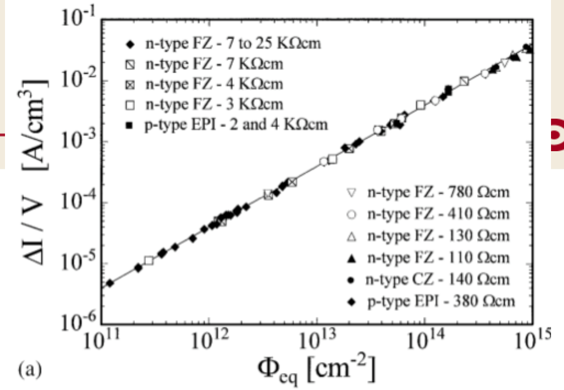
HEP vs X-ray

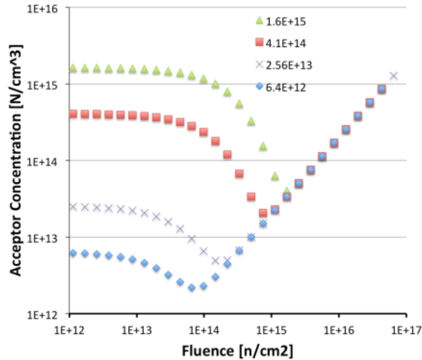


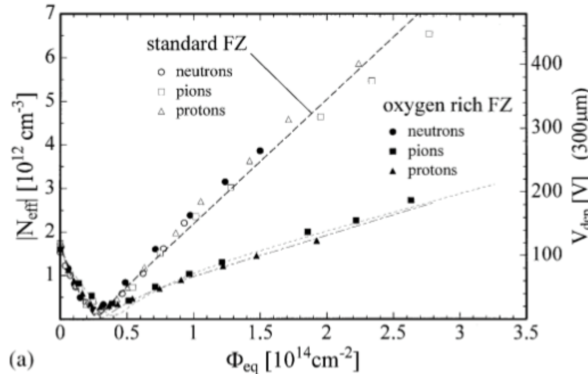


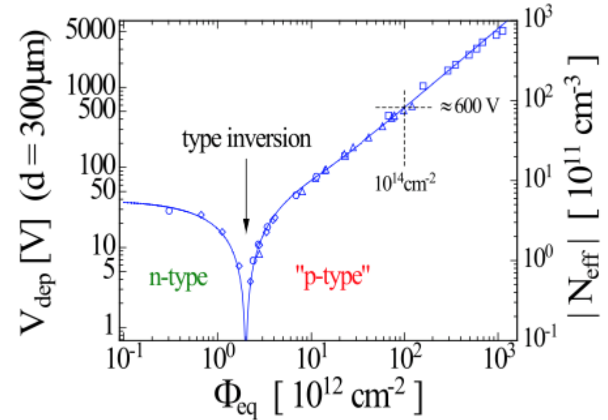
Radiation Damage in Silicon Sensor

- Type change/type inversion
- Leakage increase (signal to noise) decrease)
- Charge trapping due to radiation induced defects: “double peak” E-field effect





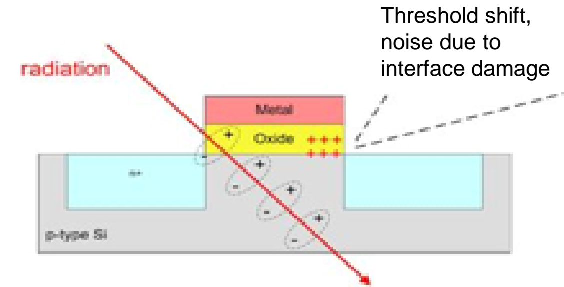


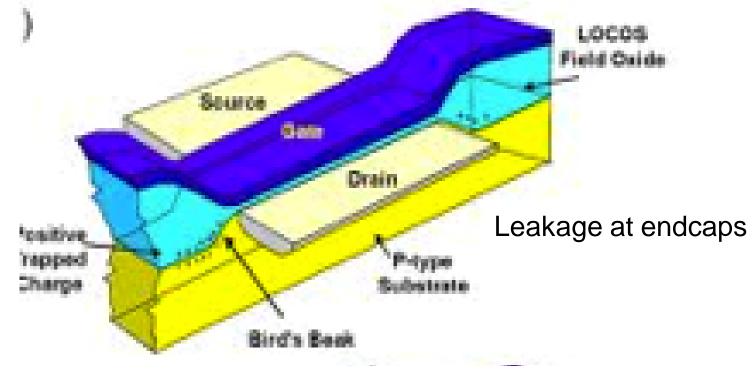


ig. 7. Effective doping concentration (depletion voltage) as a function of article fluence for a standard FZ n-type silicon detector. Data were measured rectly after exposure and are taken from [42].

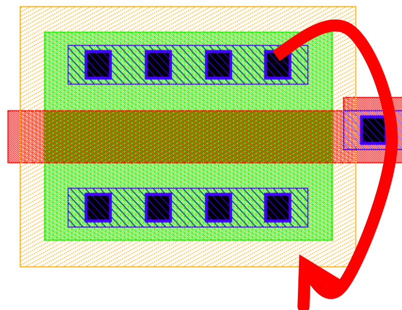
Radiation Damage in CMOS

- Electron-hole pairs generated in oxide; holes get stuck at oxide-silicon interface
- Trapped charge is exponentially dependent on (oxide thickness)$^{-1}$, so more advanced CMOS technology better
- But field oxide is thicker, so leakage at transistor endcaps is problem



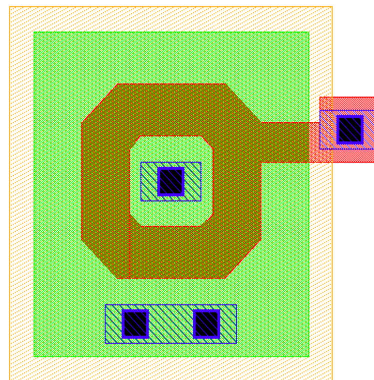


Fixes for Endcap leakage problem

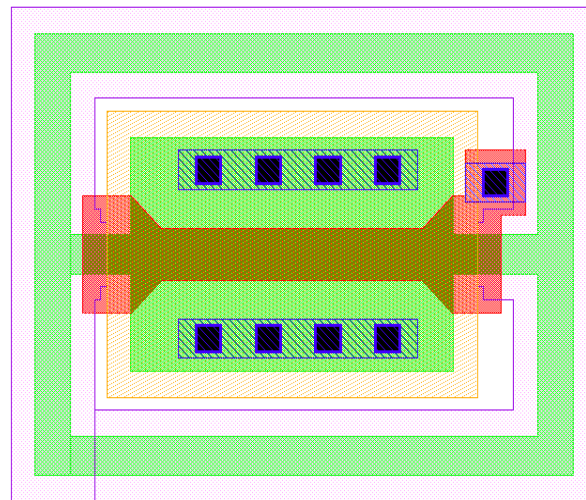


Regular transistor

Leaks when STI/field inverts



Annular transistor:
No path over STI/field



H-gate transistor:
Leakage path over STI/field is blocked by P-implant

radhard design in CMOS image sensors: **Caeleste**

Sensor Design: what to worry about?

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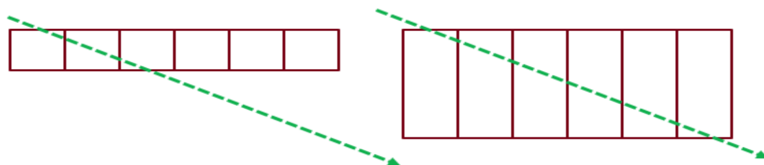
- Depletion region width important for signal magnitude
- Avalanche breakdown due to high fields can limit performance
- Dark current (bulk)
- Surface charge
- Surface generation
- Radiation damage

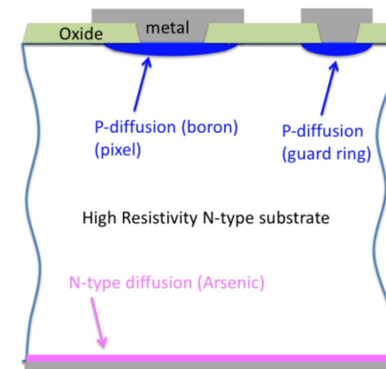
In the following slides, some different sensor architectures

Sensors for HEP: Thin sensors desired

ATLAS/CMS high luminosity upgrades requires thinned sensors (100μm–150μm) compared to traditional Silicon thickness (300μm–500μm)

- improved radiation hardness – lower voltage for full depletion
- reduced material mass
- lower occupancy for large angle tracks





- We cannot process thin wafers in semiconductor processing equipment
- Why not thin sensors *after* processing?
  - Fully depleted high-resistivity sensors require backside diode implant (why?)
    - Backside process: ion implantation followed high temperature anneal to activate
  - If backside process done after frontside is completed, required backside anneal would damage frontside
- Solutions:
  - silicon on Insulator (SOI) wafers, expensive, complex
  - SLAC innovation: microwave annealing (MWA)

3D Sensor History

- Enabled by development of high-aspect silicon etch technology
- De-couples sensor thickness from depletion voltage
- Radiation hardness advantage over planar sensors in the presence of bulk radiation damage
- 3D sensors make up ¼ of ATLAS IBL

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ELSEVIER

Nuclear Instruments and Methods in Physics Research A 395 (1997) 328–343

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH
Section A

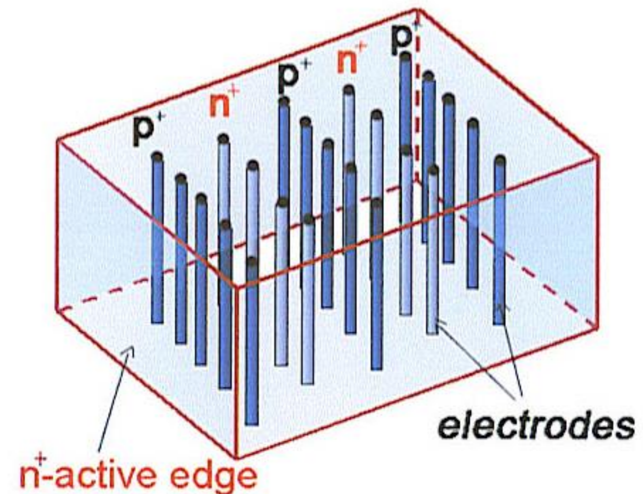
3D – A proposed new architecture for solid-state radiation detectors[1]

S.I. Parker[a,*], C.J. Kenney[a], J. Segal[b]

[a] University of Hawaii, Honolulu, USA
[b] Integrated Circuits Laboratory, Stanford University, Stanford, USA

Abstract

A proposed new architecture for solid-state radiation detectors using a three-dimensional array of electrodes that penetrate into the detector bulk is described. Proposed fabrication steps are listed. Collection distances and calculated collection times are about one order of magnitude less than those of planar technology strip and pixel detectors with electrodes confined to the detector surface, and depletion voltages are about two orders of magnitude lower. Maximum substrate thickness, often an important consideration for X-ray and gamma-ray detection, is constrained by the electrode length rather than by material purity or depletion-depth limitations due to voltage breakdown. Maximum drift distance should no longer be a significant limitation for GaAs detectors fabricated with this technology, and collection times could be much less than one nanosecond. The ability of silicon detectors to operate in the presence of the severe bulk radiation damage expected at high-intensity colliders should also be greatly increased.



Pros and cons od 3D compared to planar sensors

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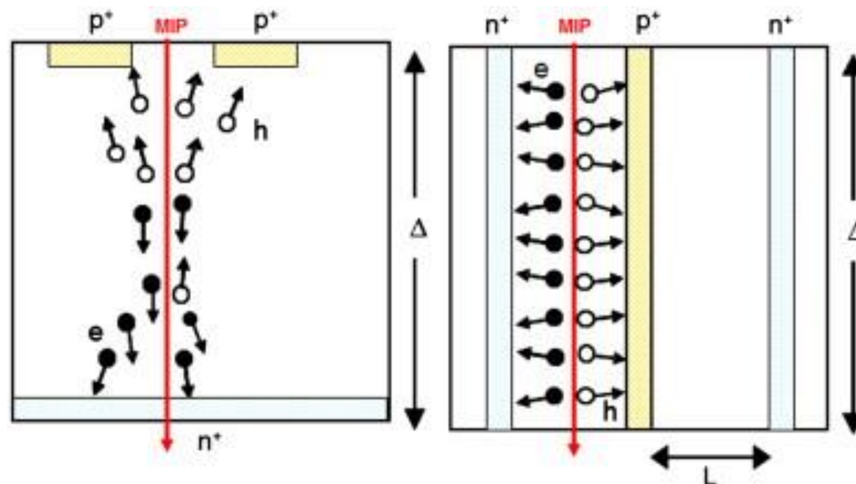
Pros

- De-couple depletion voltage and electric field from sensor thickness
    - Lower depletion voltage
    - Faster read-out
    - Radiation hardness

Cons

- Process complexity and yield
- Test complexity
- More difficult to scale pixel size
- Higher capacitance



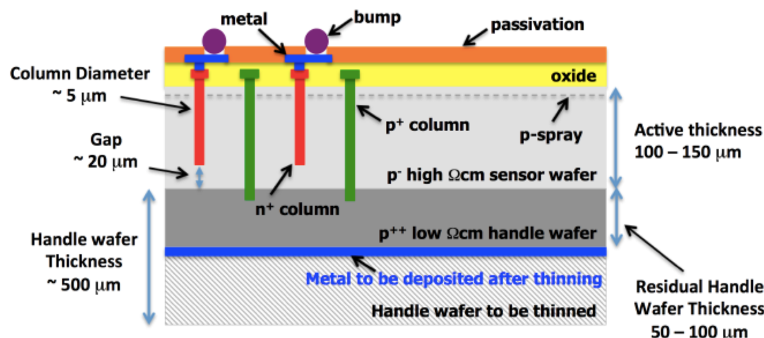
Schematic cross-sections of (left) planar sensor, and (right) 3D sensor, emphasizing the decoupling of active thickness (*Δ*) and collection distance (*L*) in 3D sensors.

* Cinzia Da Via , et al **3D silicon sensors: Design, large area production and quality assurance for the ATLAS IBL pixel detector upgrade, NIM Voume 694 2012 321-330**

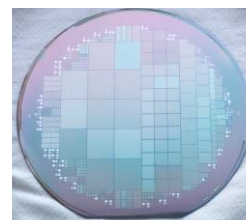
FBK 3D Technology

Single-sided, small-pitch thin 3D for HL-LHC

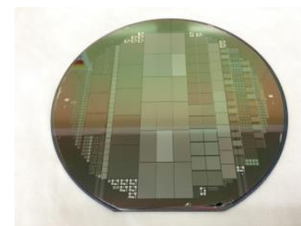
G.-F. Dalla Betta et al., NIMA 824 (2016) 386&388; DMS Sultan et al., JINST 12 (2017) C01022



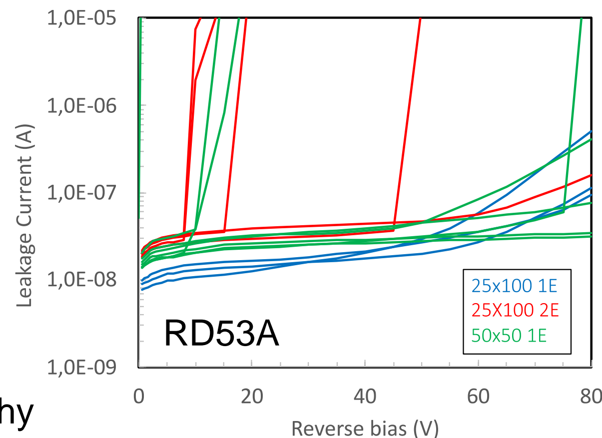
1st batch (2015): FEI4 and PSI46



2nd batch (2017): including RD53A



- Thin active layer (130 um) SiSi DWB wafers
- Different small-pitch pixel layouts
  - 50x50 1E, 25x100 1E: good results
  - 25x100 2E: critical (very dense layout)
- Irradiated RD53A modules under test
- 3rd batch being fabricated with stepper lithography



CNM 3D Technology

- SOI process with backside p-implant
- Wet etch to selectively remove backside in active region

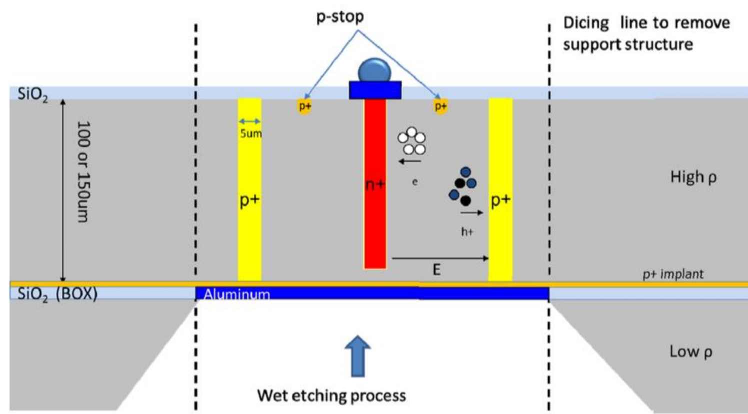
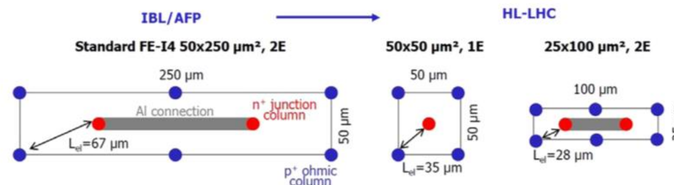


Fig. 1. Scheme for a 3D-SS detector.



3D-Si single sided sensors for the innermost layer of the ATLAS pixel upgrade

G. Pellegrini *, M. Manna, D. Quirion

Centro Nacional de Microelectrónica, IMB-CNM-CSIC, Barcelona, Spain

Active Edge for 3D and Planar Sensors

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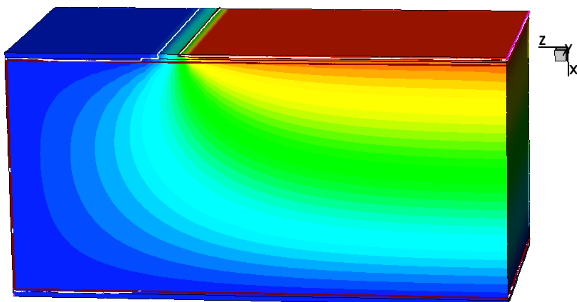
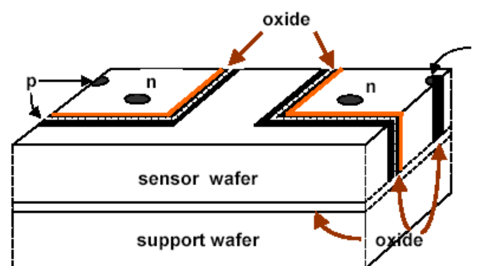
- Active Edge is an edge electrode located at the perimeter of the whole device
- Using the 3D electrode process but for the full edge of the device, eliminates large dead regions. (guard rings)
- Tiling these sensors together will produce large seamless detector area

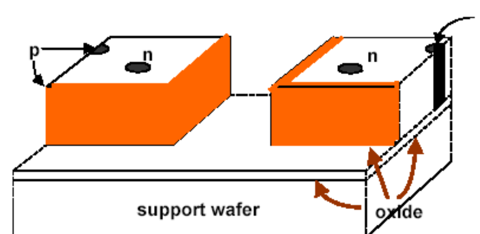
Tixel Active Edge: Electrostatic Potential



NO SAWING NECESSARY !

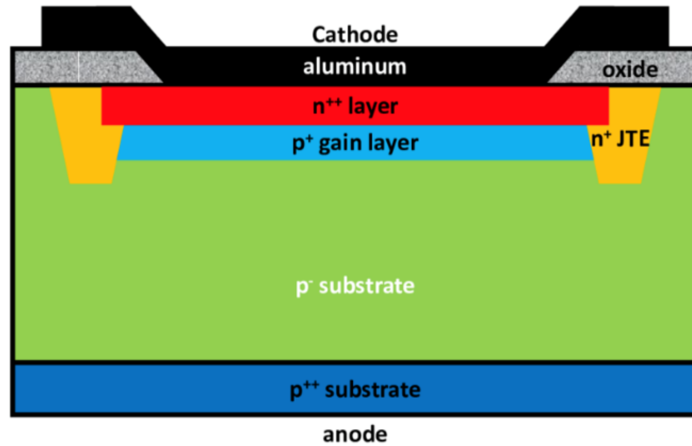
- **No chips or cracks**
- **Arbitrary edge shapes**





1. etch border trenches
2. diffuse in dopant
3. grow protective oxide cover
4. fill trench with poly
5. vertical, directed etch (to dotted lines)
6. turn off sidewall protection step
7. isotropic etch to oxide stop
8. additional steps are not included on this slide (and note, bonding oxide to support wafer not colored)
9. n and p electrodes can be reversed

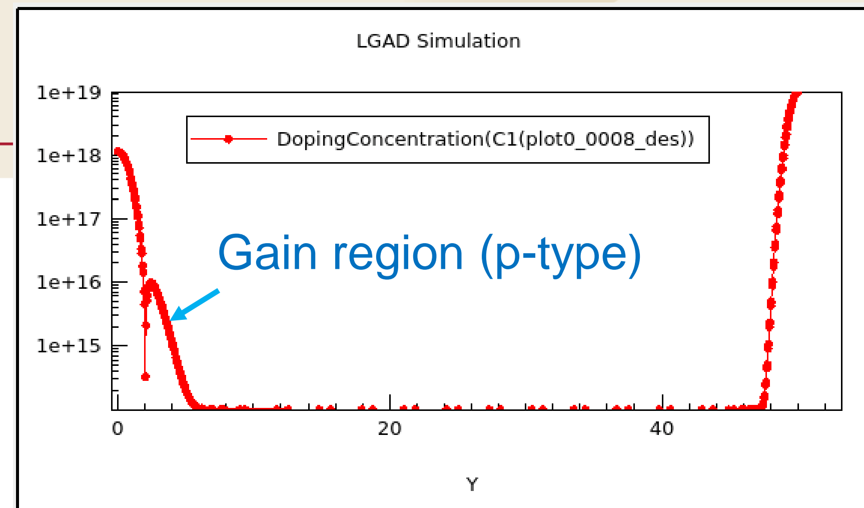
LGAD – Low gain avalanche detector

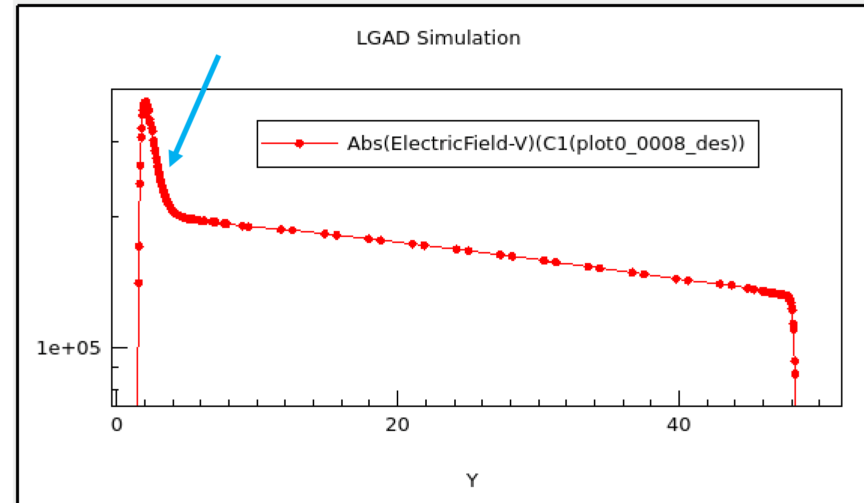


Compare to avalanche photo-diode without the LG
What is the difference? Positive feedback needs quenching, also lose info

Also note termination issue

Acceptor Delta Model (Nicolo)
Vary concentration of *shallow* acceptor traps.





Radiation Damage in LGADs

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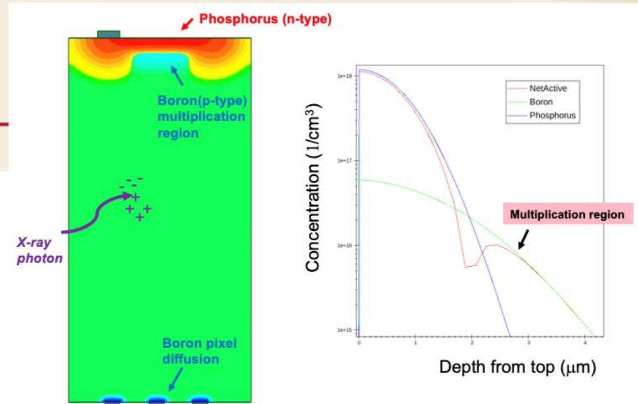
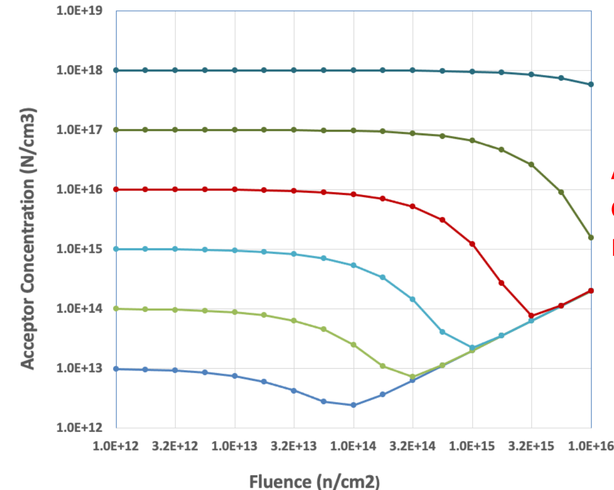
- Acceptor removal occurs after exposure to hadron radiation
- Effective boron dose is reduced
- Reduced boron dose leads to reduced LGAD gain
- Approaches to fix problem
  - Increase boron dose
  - Replace boron with Gallium
  - Co-implant boron with carbon
- These approaches provide some improvement, but not enough
- Its challenging to adequately increase boron peak with conventional processing techniques: need approximately 10^{18} cm $^{-3}$

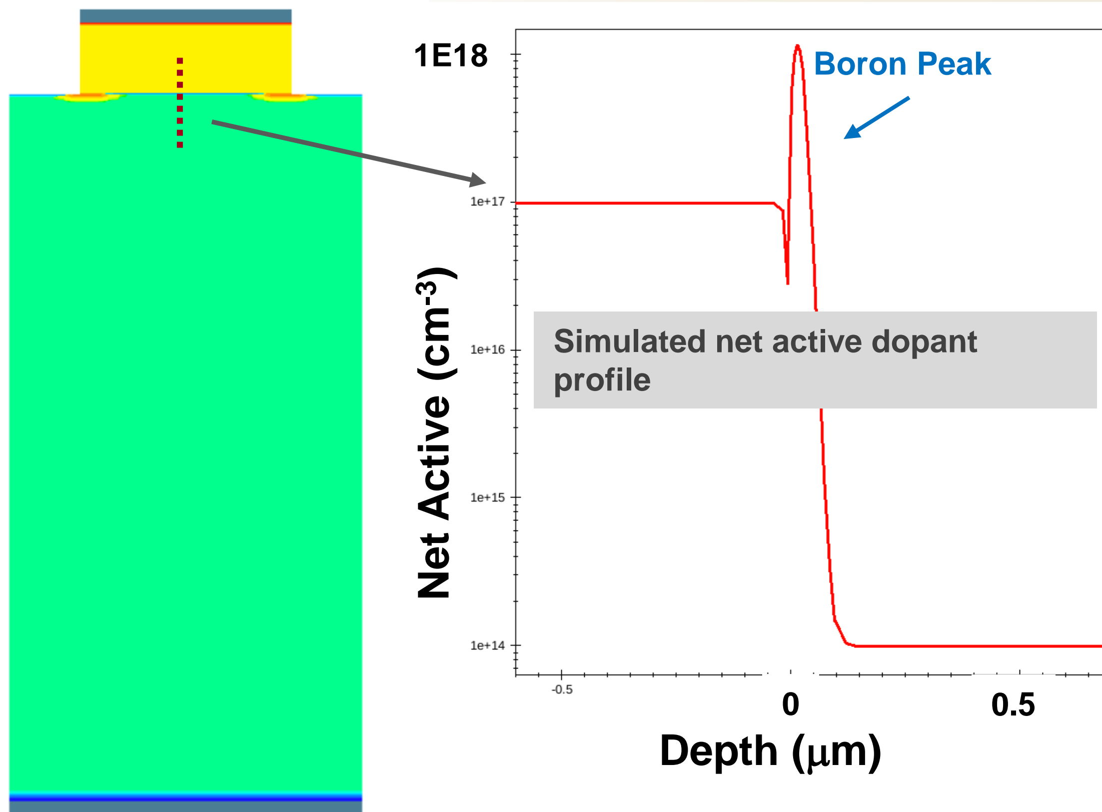




Acceptor levels decrease with radiation *

* Model from M. Ferrero et al, “Radiation resistant LGAD design”, Nuclear Instruments and Methods A 919 (2019) 16-26

Our Proposed Rad-hard LGAD Device



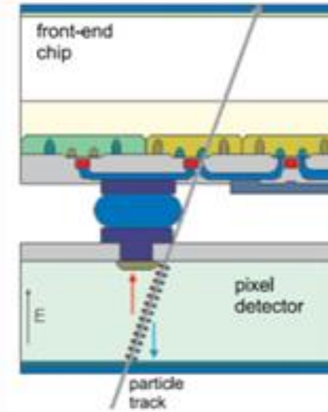
Needs two developments to enable super-sharp profile

1) Low temp wafer-to-wafer bonding
   - Low temp epitaxial deposition could also work
2) Low temp annealing (mwa)

What is a monolithic CMOS sensor?

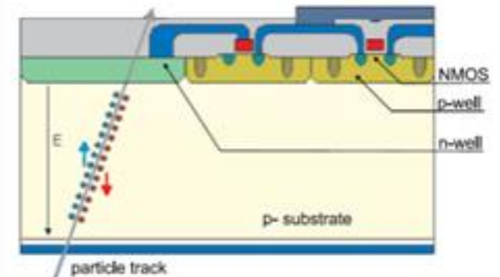
- CMOS sensor combines the circuitry and sensor in one monolithic substrate
- Hybrid detectors have distinct sensor, bump interconnect, and circuit chip
- Advantages of CMOS for HEP:
  - Lower capacitance, less noise
  - Cheaper, potentially better yield
  - Take advantage of higher volume foundry process (potentially)
  - Less material
  - Pixel size, resolution.
- Disadvantage of CMOS:
  - harder to optimize sensor and CMOS at the same time
  - Availability of process/foundry

Hybrid Pixel Detectors



Could be planar sensor or 3D

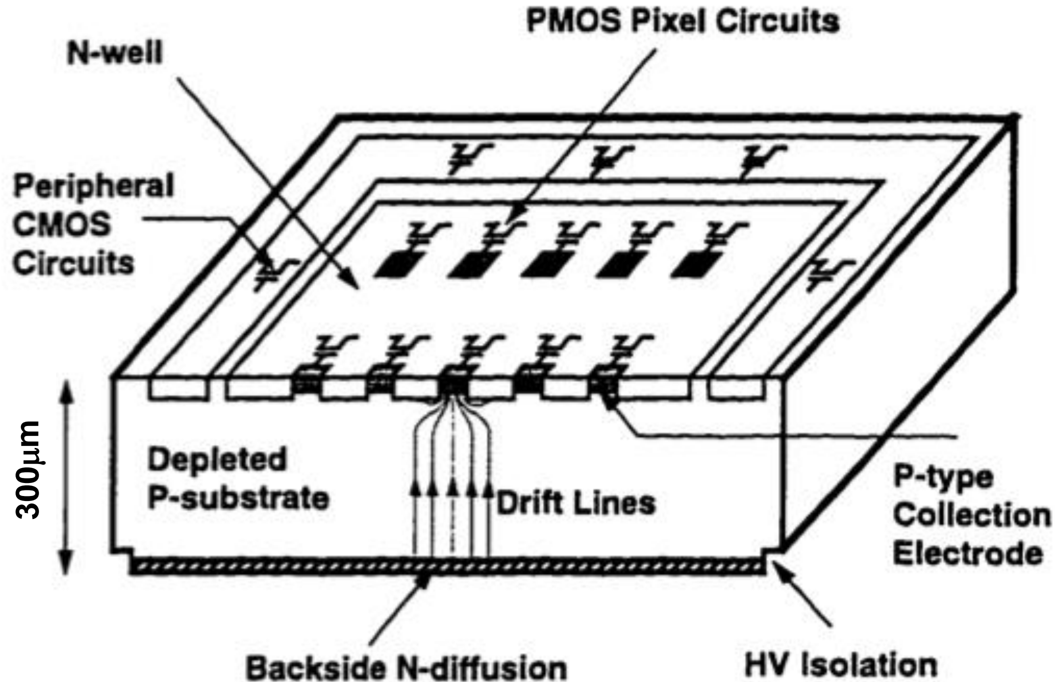
Depleted Monolithic Pixels



Monolithic Full-Depletion Sensor with Integrated CMOS

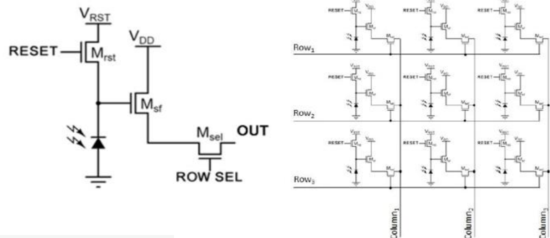
SLAC

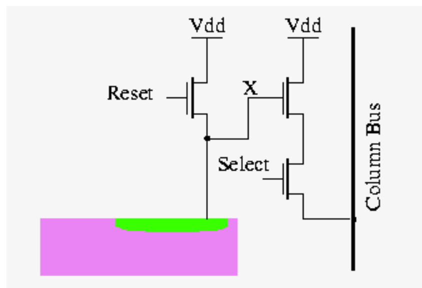
- Fully depleted substrate (high resistivity
- 300 μm thick active volume
- Processed at SNF in 1990's by W. Snoeys (gen 1) and J. Segal (gen 2)
- Hard to do production at SNF…



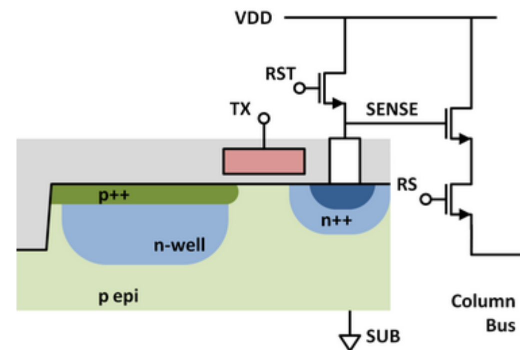
CMOS Sensors for Optical Imaging

SLAC





3T architecture

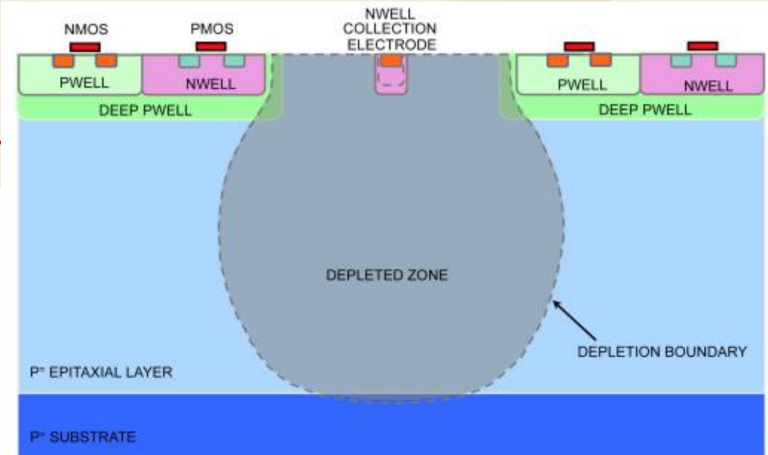


4T architecture: Pinned photo-diode used in most cameras today

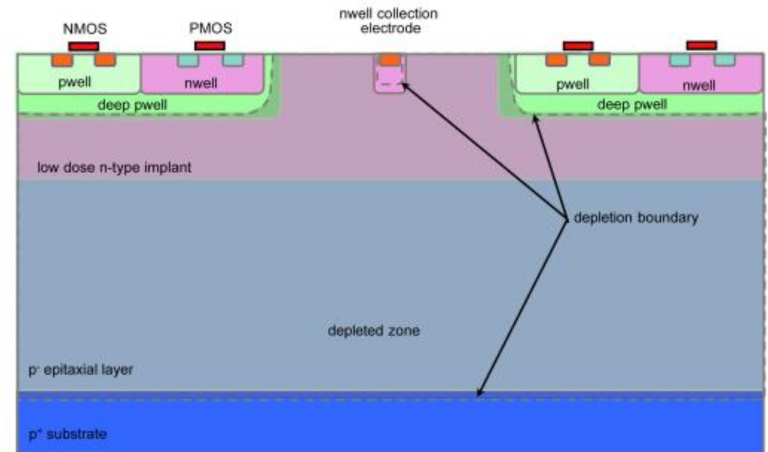
- Manufactured in high volume
- Could be used for HEP, but depletion region is < 1μm

Foundry CMOS

- Foundries reluctant to work with high resistivity wafers, or wafers unavailable in desired size
- High resistivity epitaxial layer is sometimes compromise solution



(a)

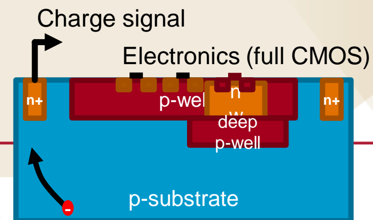


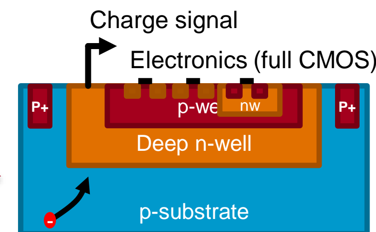
(b)

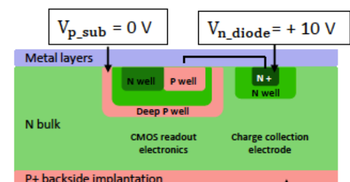
"Standard" (drift/diffusion) and "modified" (mostly drift) Tower 0.18um CMOS imaging process
From W. Snoeys "Monolithic CMOS sensors for high energy physics"

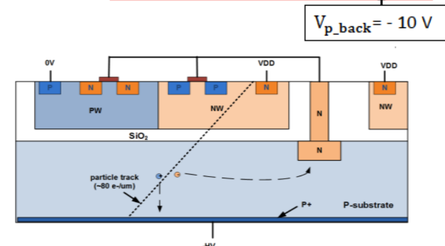
New Wave of Interest in CMOS Sensors (Slide from 2014)

- Deep N-well MAPS (diffusion mode collection, particle tracking): ST130, IBM65, GF130
- Deep P-well MAPS (improved fill factor over Deep N-well): TJ180
- HVCMOS (drift mode, partially depleted, particle tracking): AMS H35, AMS H18, GF130, GF55(proposed)
- DMAPS (drift mode, fully depleted, X-ray and NIR, also particle tracking): ESPROS (50um), Sensor Creation/ON Silicon (up to 500um)
- SOI w/fully depleted bulk: Oki
- Pinned Photodiode (X-ray): TJ180, TJ high end, LF150, LF110 (many others used for optical imaging)
- 3D Technology w/TSV: Tezzaron, GF, LF

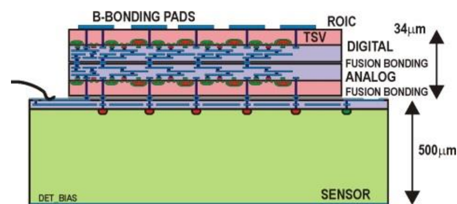




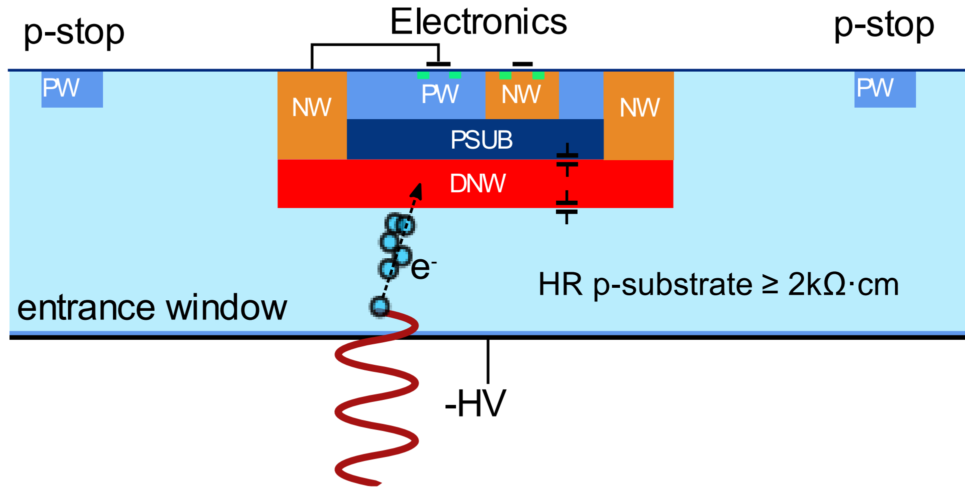


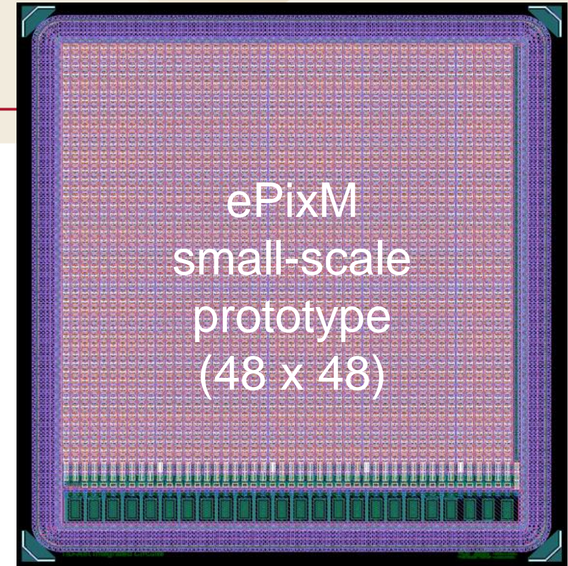


SOI developments: partially depleted (shown here), also double SOI



SLAC Soft X-ray detector (Lfoundry)





- HV applied on backside: full-depletion, charge collected by drift
- Electronics sits in deep n-well (DNW), which also acts as collection node
- Additional deep p implant (PSUB) isolates NW (PMOS transistors) from DNW
- P-stop around pixels, guard rings at chip periphery
- Wafers thinned to 300um (could be thicker with ~10Kohm-cm material) and back-processed with microwave anneal
- Not clear if Lfoundry will continue to support