Potential and Limits of MAPS for Large Area Sensors with Nanosecond Timing

Alexandre Habib¹, James E. Brau², Martin Breidenbach¹, Lorenzo Rota¹, Caterina Vernieri¹, Angelo Dragone¹

¹ SLAC National Accelerator Laboratory, 2575 Sand Hill Road, Menlo Park, CA 94025, USA
² Department of Physics, University of Oregon, Eugene, OR 97403, USA

*Correspondence: alexhab@slac.Stanford.edu

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Presentation Outline

• State of the Art
• Potential of MAPS
• Limits of MAPS
  • Power
  • Timing
• SLAC Development: NAPA_p1
• Conclusion
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<td>Hexagonal</td>
<td>0.077 – 0.02</td>
<td>40 - 2700</td>
</tr>
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</table>


[8] S. Zambito et al 2023 *JINST* 18 P03047 [DOI 10.1088/1748-0221/18/03/P03047](https://doi.org/10.1088/1748-0221/18/03/P03047)

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Potential of MAPS

In Monolithic Active Pixel Sensors (MAPS), the sensor is integrated in the same wafer as readout electronics. This translates into many advantages:

- **Small pixel** (down to ~ 10 µm) → High Granularity
- **Small sensor capacitance** (few fF) → better performance for lower power consumption than hybrid detectors
- **Low material budget** → The wafer can be thinned (<100 µm)
- **Fast production** → no bump bonding necessary
- **Relatively cheap solution**, using commercial CMOS imaging technologies
- **Possibility of large stitched sensor** → up to 30 cm x 10 cm
Example of Application: Digital E-Calorimeter for ILC

GEANT4 simulations of Transverse distribution of two 10 GeV showers separated by one cm

Pixel amplitudes (analog) in the ILC 13 mm² TDR pixel design

Clusters in the first 5.4 radiation lengths in the new SiD digital MAPS of 2500 µm² pixel

Energy Resolution for gamma showers

For different cluster configurations

It is shown with simulations that the design of the digital MAPS applied to the ECal exceeds the physics performance required for the linear collider as specified in the ILC TDR

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Limit of MAPS on power

- **Power lower limits are determined by:**
  - What is the lowest signal to be detected? (minimum SNR)
  - How fast? (Maximum Bandwidth)
- As demonstrated in [1], for most commonly used front-ends, we can prove that:
  \[
  \frac{\text{Signal}}{\text{Noise}} \propto \frac{Q_{\text{in}}}{C_{\text{sensor}}} \sqrt{gm} \Rightarrow \frac{\text{Signal}}{\text{Noise}} \propto m\sqrt{\text{Power}} \text{ with } 2 \leq m \leq 4
  \]
- For a fixed sensor thickness, the total input charge \( Q_{\text{in}} \) is governed by physics (\(~ 50 - 80 \text{ e-h/\(\mu\)m})
- The transconductance \( gm \propto I_{\text{bias}} \) or \( gm \propto \sqrt{I_{\text{bias}}} \) depending on the inversion mode of the input MOS
- We can conclude the sensor capacitance \( C_{\text{sensor}} \) is a key factor
- **Power** \( \propto \left(\frac{\text{SNR}}{Q_{\text{in}}/C_{\text{sensor}}}\right)^m \) and for a constant SNR and \( Q_{\text{in}} \) \( \Rightarrow \) \( \text{Power} \propto (C_{\text{sensor}})^m \text{ with } 2 \leq m \leq 4 \)

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CERN developments on Tower Semiconductor 180 nm and 65 nm demonstrated that it is possible to achieve \( C_{\text{sensor}} \) as low as 2-3 fF/pixel

Power Distribution in a Large Stitched Sensor

Power upper limits are:

- Power density to allow gas cooling \( \Rightarrow < 20 \text{ mW/cm}^2 \)
- Voltage drop across a large matrix
  - if we’re powering from 2 sides, with a pitch of 25 \( \mu \text{m} \), we would have a maximum column length of 2000 pixels (5 cm)
  - Voltage drop \( \propto N_{\text{pixels}}^{2} \)

Estimation of Voltage drop with a pixel pitch of 25 \( \mu \text{m} \), pixel current of 600 nA and pixel resistance of 300 m\( \Omega \)

Possible solutions:
- Decrease pixel current
- Increase pixel pitch
- Supply over-voltage with in-pixel regulation
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Timing limits with MAPS ➔ Complete detection chain

\[ \sigma_{Total}^2 = \sigma_{TOA}^2 + \sigma_{FE}^2 + \sigma_{Timewalk}^2 + \sigma_{TDC}^2 \]

\[ \sigma_{Timewalk}^2 = \sigma_{Amplitude}^2 \times \left[ \frac{d(TOA)}{d(V)} \right]^2 \]

\[ \sigma_{Amplitude}^2 = \sigma_{Landau}^2 + \sigma_{charge\_sharing}^2 \]

\[ \sigma_{Total}^2 = \sigma_{TOA}^2 + \sigma_{FE}^2 + (\sigma_{Landau}^2 + \sigma_{charge\_sharing}^2) \times \left[ \frac{d(TOA)}{d(V)} \right]^2 + \sigma_{TDC}^2 \]
Limits on Time of Arrival Jitter ($\sigma_{\text{TOA}}$)

While the smaller pitch leads to a shorter drift distance, it also leads to more charge sharing and a larger cluster size, resulting in a deteriorated time resolution for the seed pixel.

Beam tests from [2] (Tower 65 nm), time residuals after time walk correction for 10 µm (a) and 20 µm (b) pixel pitch

While the smaller pitch leads to a shorter drift distance, it also leads to more charge sharing and a larger cluster size, resulting in a deteriorated time resolution for the seed pixel.

Limits on Electronic Jitter ($\sigma_{FE}$)

$$\sigma_{FE} = \frac{\text{Noise}}{dV/dt}$$

and Noise \( \propto \frac{1}{\sqrt{\text{gm}}} \) if bandwidth is fixed by a shaper, otherwise thermal noise is independent from gm

and \( \frac{dV}{dt} \propto \text{gm} \) and \( \text{gm} \propto (\text{Power})^{1/n} \) with \( 1 \leq n \leq 2 \)

$$\Rightarrow \sigma_{FE} \propto \frac{1}{(\text{Power})^{1/n}} \text{ with } 1 \leq n \leq 2 \text{ (case with no shaper)}$$
Limit on TimeWalk ($\sigma_{\text{Timewalk}}$)

$$\sigma_{\text{Timewalk}}^2 = \sigma_{\text{Amplitude}}^2 \times \left[ \frac{d(\text{TOA})}{d(V)} \right]^2$$

$$\sigma_{\text{Amplitude}}^2 = \sigma_{\text{Landau}}^2 + \sigma_{\text{charge-sharing}}^2$$

- The term $\frac{d(\text{TOA})}{d(V)}$ depends on the comparator characteristics. It can be 'ideally' zero for a constant fraction discriminator. (Not easily feasible in a small pixel)
- Most developments correct for TimeWalk offline. If not corrected, TimeWalk is typically a dominant term for time resolution

Ref: Fuyue Wang, Su Dong, Benjamin Nachman, Maurice Garcia-Sciveres, Qi Zeng, The impact of incorporating shell-corrections to energy loss in silicon, Nuclear Instruments and Methods in Physics Research Section A, Volume 899, 2018
https://doi.org/10.1016/j.nima.2018.04.061

Reference:
https://doi.org/10.48550/arXiv.2212.08621
Limits on TDC ($\sigma_{TDC}$)

- TDC can be made with a Ring Oscillator in pixel
- Simulations of a 15-stage Ring Oscillator show very good timing resolution < 1 ps-rms.
- The main noise will be the quantization noise = $\frac{\text{Period}}{\sqrt{12}}$
- For a $\sigma_{\text{quantization}}$ < 150 ps-rms, we need a period of 520 ps $\Rightarrow$ Ring Oscillator frequency of $\sim$ 2 GHz
- This could become a digital challenge if the occupancy is high
- In e+e- tracker we can expect an occupancy $\sim$ 100 hits/cm$^2$ (in a bunch train). For a pixel pitch of 25 µm that would be 1 hit every 160 pixels, so that’s a sufficiently low occupancy compatible with such a solution.

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Example of Ring Oscillator based TDC
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NAPA_p1: NA
nosecond PI
xel for large A
rea sensors – P
rototype 1

- Design in Tower Semiconductor 65 nm imaging technology, capitalizing on the CERN WP1.2 efforts over a decade of sensor optimization.
- The prototype design submitted with a total area 5 mm x 5 mm and a pixel of 25 µm \( \times \) 25 µm, to serve as a baseline for sensor and pixel performance.

Pixel key elements

- Charge Sensitive Amplifier (CSA) with a synchronous reset, which can be powered down during inactive time
- A comparator with auto-zero technique, removing the need for per-pixel threshold calibration

Layout of MAPS SLAC prototype for WP1.2 shared submission
Simulation of Jitter and ENC as a Function of $C_{\text{sensor}}$

- **Jitter < 1 ns-rms** for $C_{\text{sensor}} < 10$ fF
- **ENC < 25 e-rms**

These simulations are with a pixel current of 600 nA $\Rightarrow \langle \text{Power density} \rangle = 115$ mW/cm$^2$ x duty cycle

For e+e- machines such as ILC and C$^3$, duty cycle is expected < 1%
Simulation Results: Jitter and Time Walk

From theory we expect: $\sigma_{FE} \propto \frac{1}{(\text{Power})^n}$ with $1 \leq n \leq 2$

Here fitted with $n = 1$

Jitter < 400 ps-rms with power of 720 nW/pixel and Cdet of 2 fF

Time walk for MIP → MIP/4 = 16 ns

Not negligible and must be corrected
Timing Limits for NAPA-p1

\[ \sigma_{Total}^2 = \sigma_{TOA}^2 + \sigma_{FE}^2 + \sigma_{Timewalk}^2 + \sigma_{TDC}^2 \]

- \( \sigma_{TOA} < 150 \text{ ps-rms} \)
  - For small optimized pixels

- \( \sigma_{FE} < 400 \text{ ps-rms for } < 1 \mu\text{W/pixel} \)

- \( \sigma_{Timewalk} = 16 \text{ ns} \)
  - Can be corrected if we measure the ToT inside the pixel

- \( \sigma_{TDC} < 150 \text{ ps-rms} \)
  - Limited by quantization noise

Assuming time walk is fully corrected \( \Rightarrow \sigma_{Total} \approx 500 \text{ ps-rms} \) with reasonable pixel power consumption, going lower will cost increasingly more power, not compatible with large area sensors.

Accounting for residual time walk after correction, and other non-idealities, it is reasonable to aim for 1 ns-rms time resolution.

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SLAC
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Conclusion

• MAPS has great a potential to fit the future e+e- colliders requirements (vertex, tracker, calorimeter)

• It is possible to achieve very low sensor capacitance of 2-3 fF in Tower Semiconduction 65nm technology, improving power efficiency by at least 2 order of magnitude with respect to hybrid detectors.

• Improving timing requires optimization of all the elements of the detection chain. Time walk can be dominant if not corrected.

• Simulations of NAPA_p1 show that it is possible to achieve a time resolution ~ 1 ns-rms with reasonably low power consumption of 115 mW/cm² × Duty Cycle. For e+e- machines duty cycles are typically < 1%

• NAPA-p1 characterization is planned for this summer. Results should be available soon.

Thank You For Your Attention!
Backup
According to Shockley-Ramo Theorem, the induced signal in a sensor electrode is:

\[ i(t) = Q \cdot \ddot{v} \cdot E_w \]

- Total charge generated: \( Q \propto d \)
- Carrier velocity: \( \ddot{v} = \mu \ddot{E} \) if \( |v| < v_{sat} \)
- Weighting Field

Depends on sensor geometry:

\[ E_w \propto \frac{1}{d} \]

The induced current peaks instantaneously as the charges are created in the depletion region. However, the integrated charge peak will depend on the current signal form, and thus on sensor geometry and weighting field form.

How low can we go on $C_{\text{sensor}}$?

- CERN has been working on Tower Semiconductor imaging technology (180 nm and 65 nm) for a decade, trying to optimize the sensor performance [1][2]
- The standard imaging process offer a balloon shape depletion region around the sensor electrode. Small $C_{\text{sensor}}$ but Epitaxial layer not fully depleted
- Adding lightly doped N-layer allows the full depletion of the epitaxial layer while maintaining low $C_{\text{sensor}}$
- Adding an N-gap or extra deep P-well in the pixel corners allow for faster charge collection and higher efficiency
- $\Rightarrow$ It has been proven that we can achieve high efficiency with a $C_{\text{sensor}} \sim 2 - 3 \text{ fF}$

$Power \propto (C_{\text{sensor}})^m$ with $2 \leq m \leq 4$

ALPIDE is the first MAPS to be used in a big HEP experiment. It was designed for ALICE ITS2, with Pb-Pb collisions up to 100 kHz so it does not have fast timing constraints.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Pixel dimension</th>
<th>Pix shape</th>
<th>Rise time</th>
<th>Time res.</th>
<th>Consumption</th>
<th>P. Density</th>
<th>ENC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tower 180 nm</td>
<td>29.24x 26.88 µm²</td>
<td>~square</td>
<td>2 us</td>
<td>&lt; 2 us</td>
<td>40 nW/pixel</td>
<td>40 mW/cm²</td>
<td>3.9 e-rms</td>
</tr>
</tbody>
</table>

- Very low power consumption
- Low sensor capacitance (2-3 fF)
- Epitaxial layer not entirely depleted. Collection by drift + diffusion
- → cannot achieve fast signal detection

References:
FastPix

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<thead>
<tr>
<th>Technology</th>
<th>Pixel pitch</th>
<th>Pix shape</th>
<th>Rise time</th>
<th>Time res.</th>
<th>Consumption</th>
<th>P. Density</th>
<th>ENC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tower 180 nm</td>
<td>8.6 µm – 20 µm</td>
<td>Hexagonal</td>
<td>1-2 ns</td>
<td>~130 ps-rms</td>
<td>18 µA in pixel</td>
<td>&gt;1500 mW/cm²</td>
<td>11 e-rms</td>
</tr>
</tbody>
</table>

Designed for fast response
Smaller pixels and large consumption are needed

Process Modifications

References:
• Time over Threshold (ToT) is measured for time walk correction (50 ns Vs 6 ns)
• Good detection efficiency up to $10^{15}$ 1MeV $n_{eq}/cm^2$

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<tr>
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<th>Pixel pitch</th>
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<th>Consumption</th>
<th>P. Density</th>
<th>ENC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tower 65 nm</td>
<td>15 µm</td>
<td>square</td>
<td>≈ 1us</td>
<td>6.3 ns-rms</td>
<td>210 nA/pixel</td>
<td>112 mW/cm²</td>
<td>2-6 e- rms</td>
</tr>
</tbody>
</table>

**Reference:**
Cactus

<table>
<thead>
<tr>
<th>Technologie</th>
<th>Pixel size</th>
<th>Pix shape</th>
<th>Rise time</th>
<th>Time res</th>
<th>Consumption</th>
<th>P. Density</th>
<th>ENC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lfoundry 150nmn</td>
<td>1x1 mm²</td>
<td>Square</td>
<td>1 ns</td>
<td>100 - 500 ps-rms</td>
<td>800 µA/pixel</td>
<td>145 mW/cm²</td>
<td>300 e-rms</td>
</tr>
<tr>
<td></td>
<td>1x0.5 mm²</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Up to 300 V on 200 µm thickness of high resistivity substrate (2 kΩ .cm)
- Input diode capacitance is more than an order of magnitude larger than expected (15 pF vs 1 pF)
- Signal is much lower than expected, probably due to parasitics. A second iteration was submitted

Reference:
- Y. Degerli et al 2020 JINST 15 P06011 DOI 10.1088/1748-0221/15/06/P06011
**Min-Cactus**

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<thead>
<tr>
<th>Technology</th>
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<th>Pix shape</th>
<th>Rise time</th>
<th>Time res</th>
<th>Power Density</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lfoundry 150 nm</td>
<td>1x0.5 mm²</td>
<td>Rectangle</td>
<td>1 ns</td>
<td>88 ps-rms (timewalk corrected)</td>
<td>300 mW/cm²</td>
</tr>
</tbody>
</table>

**Reference:**
Monolith Project - SiGe BiCMOS

<table>
<thead>
<tr>
<th>Technology</th>
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<th>Pix shape</th>
<th>Time res</th>
<th>Consumption</th>
<th>Power Density</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiGe 130nm IHP</td>
<td>100 µm</td>
<td>Hexagonal</td>
<td>77 – 20 ps-rms (timewalk corrected)</td>
<td>0.7 – 2.3 uA/pixel</td>
<td>40 – 2700 mW/cm²</td>
</tr>
</tbody>
</table>

- SiGe HBT very high $f_T$ (hundreds of GHz) → excellent performance
- High-resistivity (220 Ω⋅cm) substrate, about 130 µm thickness
- Hexagonal pixels integrated as triple wells, pixel capacitance of 80 fF
- Possibility of adding a gain layer (~60 for a MIP)

References:
- S. Zambito et al 2023 JINST 18 P03047 DOI 10.1088/1748-0221/18/03/P03047
- L. Paolozzi “A Picosecond Avalanche Detector in SiGe BiCMOS’ ULITIMA Conference 2023
Duty Cycle for e+e- machines

ILC Timing Structure

![Image of ILC Timing Structure]

Duty Cycle = 0.48%

C³ Timing Structure

![Image of C³ Timing Structure]

Duty Cycle = 0.03%

For NAPA_p1 <Power density> = 115 mW/cm² x duty cycle << 20 mW/cm²

⇒ Compatible with gas cooling if we use power pulsing

⇒ As for voltage drop, the pixel works up to a Vdrop of 300 mV

Ref: 2110.15800.pdf (arxiv.org)