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Potential and Limits of MAPS for Large Area Sensors with Nanosecond Timing

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SLAC NATIONAL ACCELERATOR LABORATORY

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Presentation Outline

- State of the Art
- Potential of MAPS
- Limits of MAPS
  - Power
  - Timing
- SLAC Development: NAPA_p1
- Conclusion

State of the Art

Chip name	Technology	Pixel pitch [µm]	Pixel shape	Time resolution [ns]	Power Density [mW/cm^2]
ALPIDE [1][2]	Tower 180 nm	28	Square	< 2000	40
FastPix [3][4]	Tower 180 nm	10 - 20	Hexagonal	0.122 – 0.135	>1500
DPTS[5]	Tower 65 nm	15	Square	6.3	112
Cactus [6]	LF 150 nm	1000	Square	0.1-0.5	145
MiniCactus [7]	LF 150 nm	1000	Square	0.088	300
Monolith [8][9]	IHP SiGe 130 nm	100	Hexagonal	0.077 – 0.02	40 - 2700

[1] Gianluca Aglieri Rinella, "The ALPIDE pixel sensor chip for the upgrade of the ALICE Inner Tracking System, Nuclear Instruments and Methods in Physics Research, Volume 845,2017, https://doi.org/10.1016/j.nima.2016.05.016

[2] M. Mager, "ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITS upgrade", Nuclear Instruments and Methods in Physics Research, Volume 824, 2016, https://doi.org/10.1016/j.nima.2015.09.057

[3] T. Kugathasan *et al.,* "Monolithic CMOS sensors for sub-nanosecond timing", Nuclear Instruments and Methods in Physics Research, Volume 979, 2020, https://doi.org/10.1016/j.nima.2020.164461.

[4] J. Braach et al., "Performance of the FASTPIX Sub-Nanosecond CMOS Pixel Sensor Demonstrator", *Instruments* 2022, *6*(1), 13; https://doi.org/10.3390/instruments6010013

[5] G.A. Rinella *et al.* "Digital Pixel Test Structures implemented in a 65 nm CMOS process" https://doi.org/10.48550/arXiv.2212.08621

[6] Y. Degerli *et al* 2020 *JINST* **15** P06011 **DOI** 10.1088/1748-0221/15/06/P06011

[7] Y. Degerli *et al., "*MiniCACTUS: Sub-100 ps timing with depleted MAPS", Nuclear Instruments and Methods in Physics Research, Volume 1039, 2022, https://doi.org/10.1016/j.nima.2022.167022.

[8] S. Zambito *et al* 2023 *JINST* **18** P03047**DOI** 10.1088/1748-0221/18/03/P03047

[9] L. Paolozzi "A Picosecond Avalanche Detector in SiGe BiCMOS' ULITIMA Conference 2023

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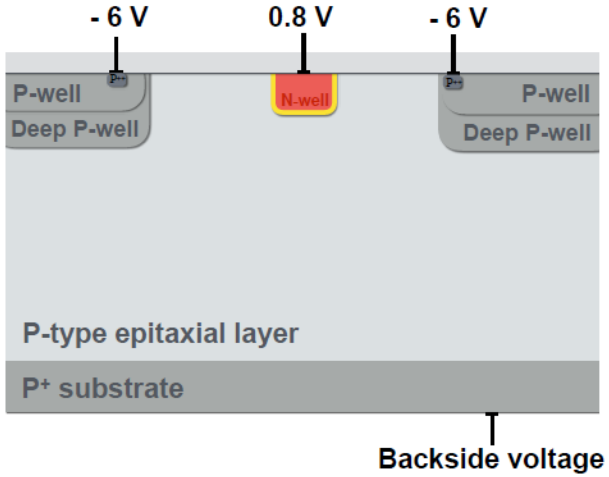
Potential of MAPS

In Monolithic Active Pixel Sensors (MAPS), the sensor is integrated in the same wafer as readout electronics. This translates into many advantages:

- **Small pixel** (down to ~ 10 µm) → High Granularity
- **Small sensor capacitance** (few fF)→ better performance for lower power consumption than hybrid detectors
- **Low material budget** →The wafer can be thinned (<100 µm)
- **Fast production** → no bump bonding necessary
- **Relatively cheap solution**, using commercial CMOS imaging technologies
- Possibility of **large stitched sensor** → up to 30 cm x 10 cm



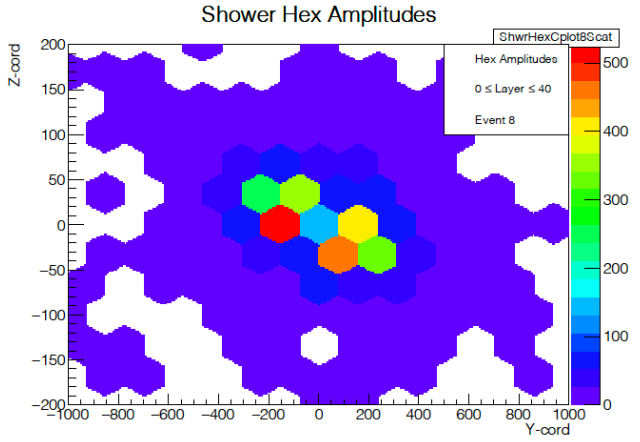
IN MAPS the sensor is integrated in the same monolithic wafer as the readout electronics

Large Area, Bent, Stitched Sensor, in the framework of R&D for ALICE ITS3

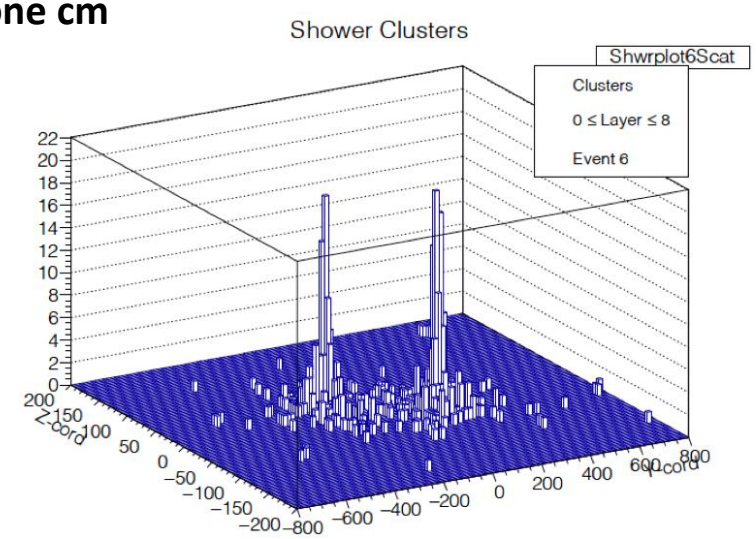
From: Magnus Mager (CERN) | bent MAPS *ITS3* | C3 R&D | 17.05.2022

Example of Application : Digital E-Calorimeter for ILC

GEANT4 simulations of Transverse distribution of two 10 GeV showers separated by one cm

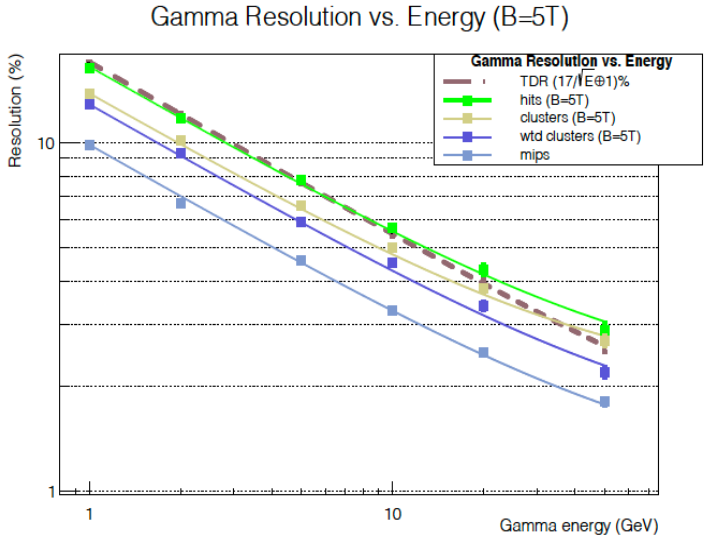


Pixel amplitudes (analog) in the ILC 13 mm^2 TDR pixel design



Clusters in the first 5.4 radiation lengths in the new SiD digital MAPS of 2500 μm^2 pixel

Energy Resolution for gamma showers



For different cluster configurations

It is shown with simulations that the design of the digital MAPS applied to the ECal exceeds the physics performance required for the linear collider as specified in the ILC TDR

Ref: Brau JE, Breidenbach M, Habib A, Rota L, Vernieri C. The SiD Digital ECal Based on Monolithic Active Pixel Sensors. *Instruments*. 2022; 6(4):51. https://doi.org/10.3390/instruments6040051

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Limit of MAPS on power

- **Power lower limits are determined by:**
  - What is **the lowest signal** to be detected? (minimum SNR)
  - How **fast**? (Maximum Bandwidth)
- As demonstrated in [1], for most commonly used front-ends, we can prove that:

$$\frac{Signal}{Noise} \propto \frac{Q_{in}}{C_{sensor}}\sqrt{gm} \rightarrow \frac{Signal}{Noise} \propto \sqrt[m]{Power} \; with \; 2 \leq m \leq 4$$

- For a fixed sensor thickness, the total input charge Q_{in} is governed by physics (~ 50 – 80 e-h/µm)
- The transconductance $gm \propto Ibias$ or $gm \propto \sqrt{I_{bias}}$ depending on the inversion mode of the input MOS
- We can conclude the sensor capacitance C_{sensor} is a key factor ➔
- $\boldsymbol{Power} \propto \left(\frac{SNR}{Q_{in}/C_{sensor}}\right)^{m}$ and for a constant SNR and Q_{in} ➔ $\boldsymbol{Power \propto (C_{sensor})^{m} \; with \; 2 \leq m \leq 4}$

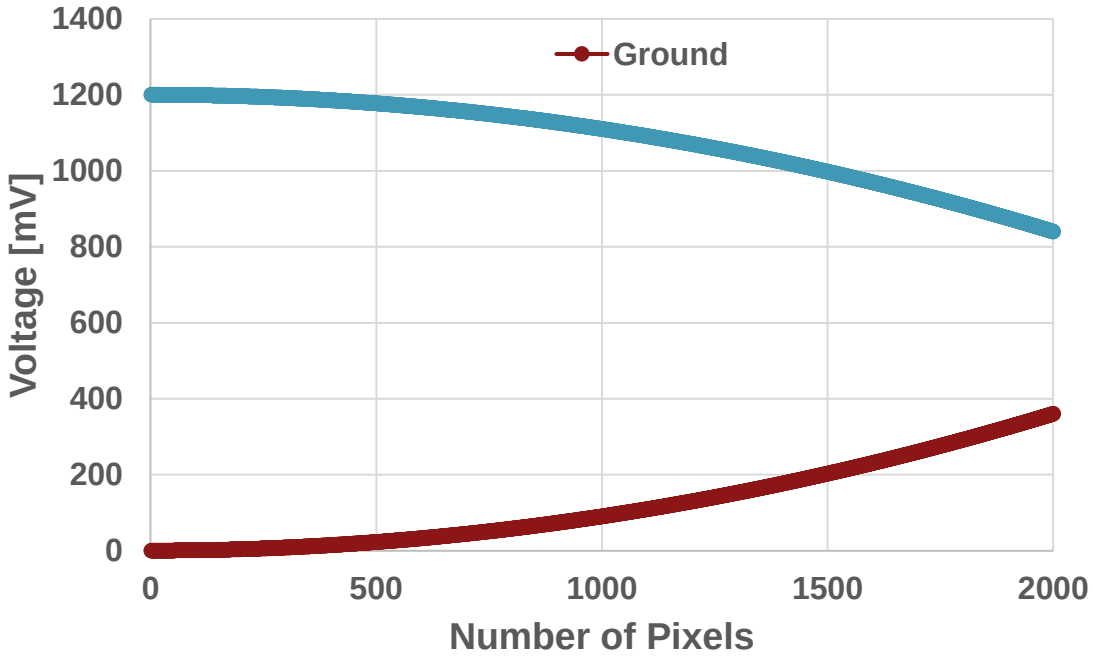
CERN developments on Tower Semiconductor 180 nm and 65 nm demonstrated that it is possible to achieve C_{sensor} a low as 2-3 fF/pixel

[1] W. Snoeys, *Monolithic Pixel Detectors for High Energy Physics,* Nuclear Instruments and Methods in Physics Research A 731 (2013) 125–130

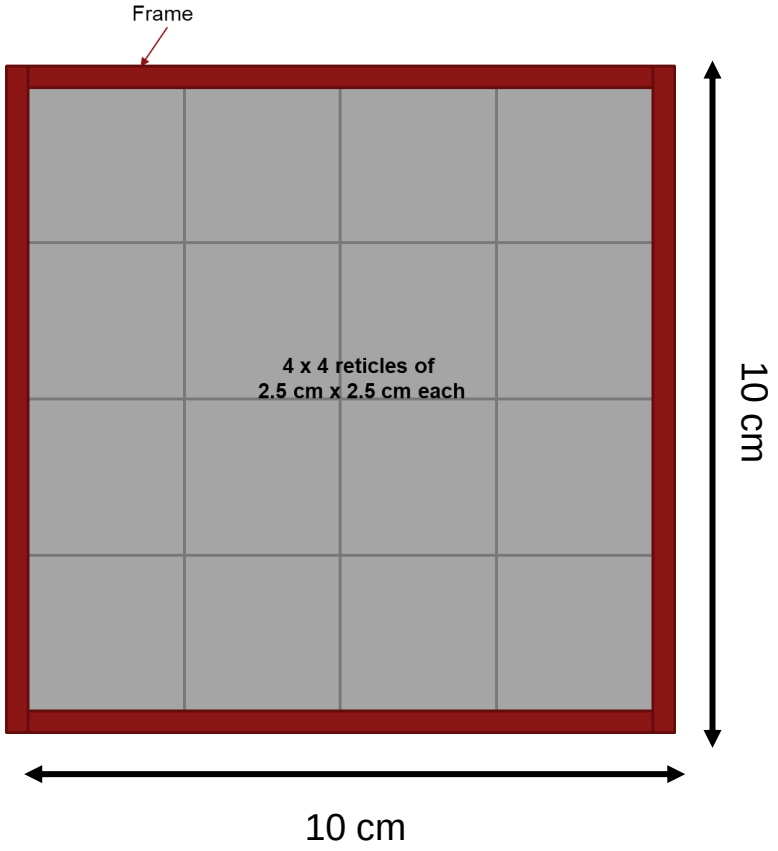
Power Distribution in a Large Stitched Sensor

Power <u>upper limits</u> are:

- Power density to allow gas cooling ➔ < 20 mW/cm^2
- Voltage drop across a large matrix
  - if we're powering from 2 sides, with a pitch of 25 µm, we would have a maximum column length of 2000 pixels (5 cm)
  - Voltage drop ∝ N_{pixels}^2



Estimation of Voltage drop with a pixel pitch of 25 µm, pixel current of 600 nA and pixel resistance of 300 mΩ



Possible solutions:

- Decrease pixel current
- Increase pixel pitch
- Supply over-voltage with in-pixel regulation

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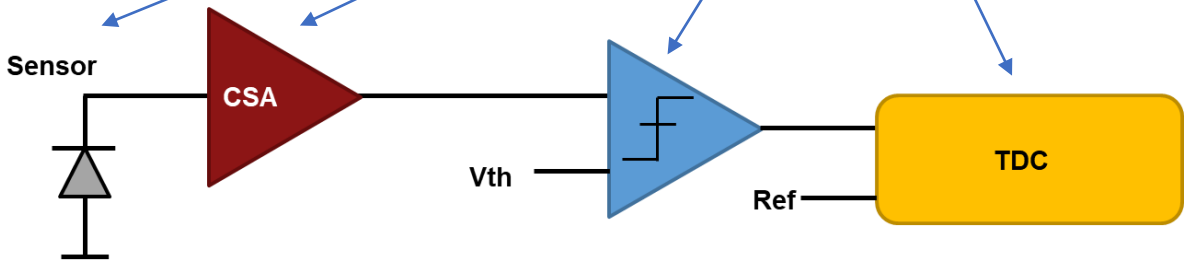
Timing limits with MAPS ➔ Complete detection chain

$$\sigma^2_{Total} = \sigma^2_{TOA} + \sigma^2_{FE} + \sigma^2_{Timewalk} + \sigma^2_{TDC}$$



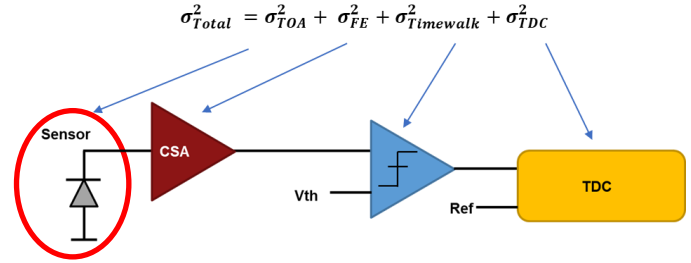
$$\sigma^2_{Timewalk} = \sigma^2_{Amplitude} \times \left[\frac{\mathrm{d(TOA)}}{\mathrm{d(V)}}\right]^2$$

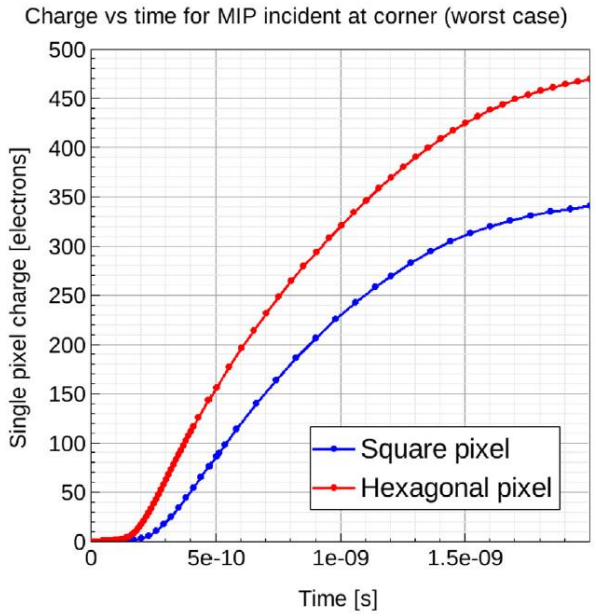
$$\sigma^2_{Amplitude} = \sigma^2_{Landau} + \sigma^2_{charge\_sharing}$$

$$\sigma^2_{Total} = \sigma^2_{TOA} + \sigma^2_{FE} + (\sigma^2_{Landau} + \sigma^2_{charge\_sharing}) \times \left[\frac{\mathrm{d(TOA)}}{\mathrm{d(V)}}\right]^2 + \sigma^2_{TDC}$$

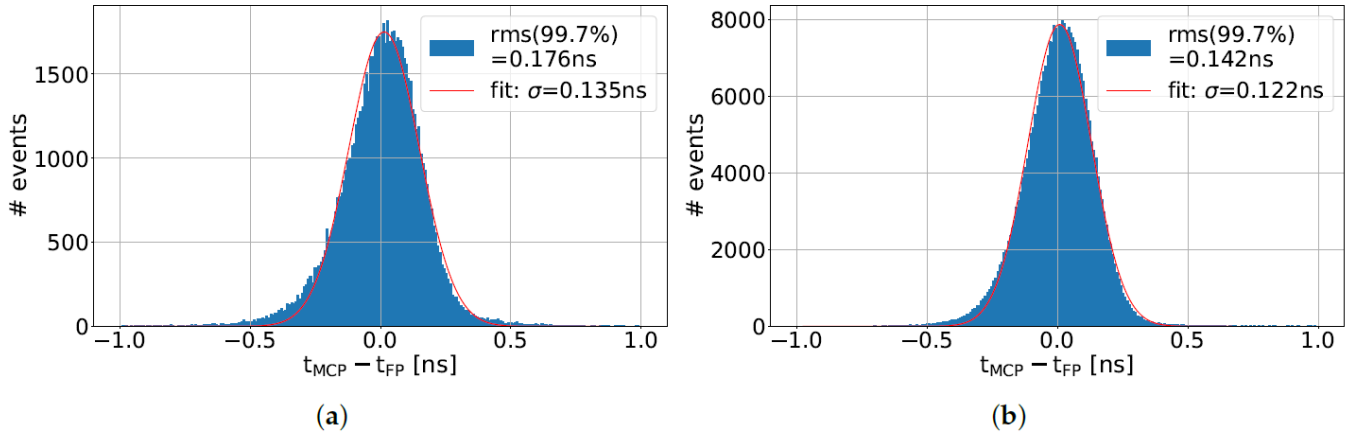
Limits on Time of Arrival Jitter (σ_{TOA})

$$\sigma^2_{Total} = \sigma^2_{TOA} + \sigma^2_{FE} + \sigma^2_{Timewalk} + \sigma^2_{TDC}$$





TCAD simulation from [1] (Tower 180 nm), for MIP incident on pixel corner, pixel pitch of 10 µm,



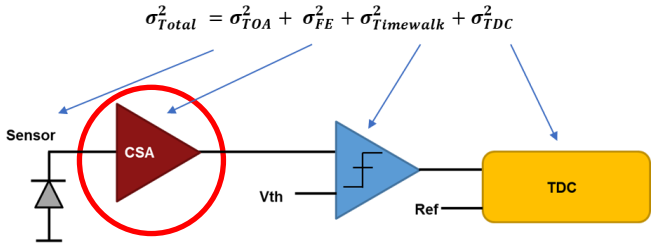
Beam tests from [2] (Tower 65 nm), time residuals after time walk correction for 10 µm (a) and 20 µm (b) pixel pitch

While the smaller pitch leads to a shorter drift distance, it also leads to more charge sharing and a larger cluster size, resulting in a deteriorated time resolution for the seed pixel.

➔ **For Tower Semi 65 nm we can estimate $\sigma_{TOA} < 150$ ps-rms**

[1] T. Kugathasan *et al.,* "Monolithic CMOS sensors for sub-nanosecond timing", Nuclear Instruments and Methods in Physics Research, Volume 979, 2020, https://doi.org/10.1016/j.nima.2020.164461.
[2] J. Braach et al., "Performance of the FASTPIX Sub-Nanosecond CMOS Pixel Sensor Demonstrator", *Instruments* 2022, *6*(1), 13; https://doi.org/10.3390/instruments6010013

Limits on Electronic Jitter (σ_{FE})



$$\sigma_{FE} = \frac{\text{Noise}}{dV/dt}$$

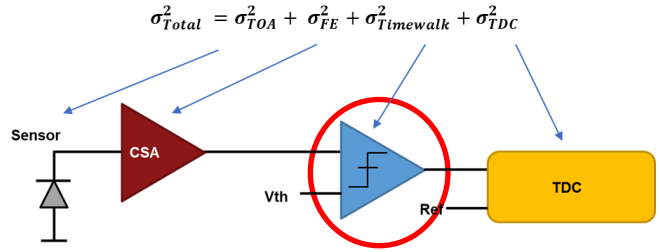
and Noise $\propto \frac{1}{\sqrt{gm}}$ if bandwidth is fixed by a shaper, otherwise thermal noise is independent from gm

and $\frac{dV}{dt} \propto gm$ and $gm \propto (\text{Power})^{1/n}$ with $1 \leq n \leq 2$

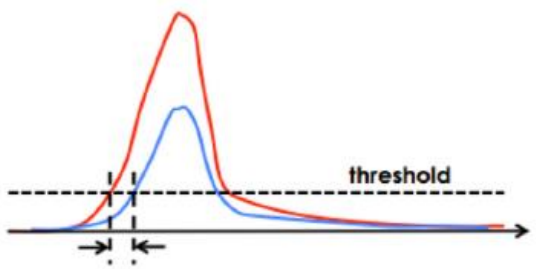
➔ $\boldsymbol{\sigma_{FE} \propto \frac{1}{(\text{Power})^{\frac{1}{n}}}}$ **with $1 \leq n \leq 2$ (case with no shaper)**

Limit on TimeWalk ($\sigma_{Timewalk}$)

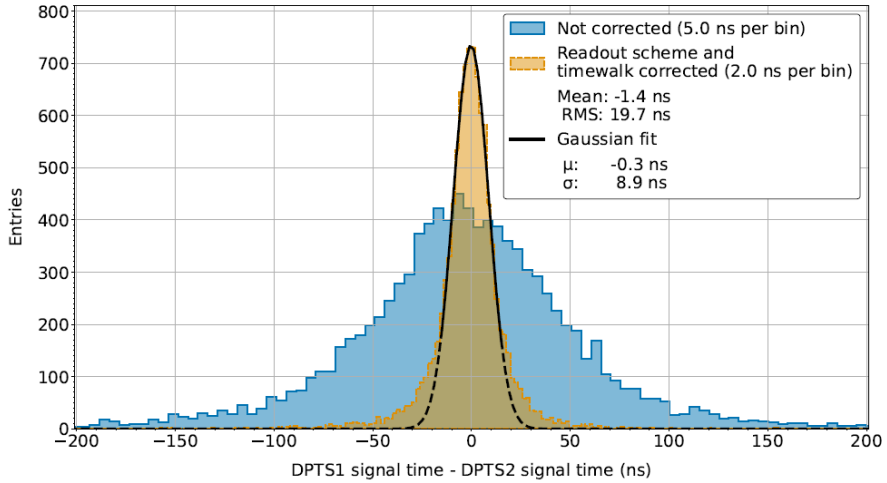
$$\sigma^2_{Timewalk} = \sigma^2_{Amplitude} \times \left[\frac{d(TOA)}{d(V)}\right]^2 \qquad \sigma^2_{Amplitude} = \sigma^2_{Landau} + \sigma^2_{charge\_sharing}$$



- The term $\frac{d(TOA)}{d(V)}$ depends on the comparator characteristics. It can be 'ideally' zero for a constant fraction discriminator. (Not easily feasible in a small pixel)
- Most developments correct for TimeWalk offline. If not corrected, TimeWalk is typically a dominant term for time resolution

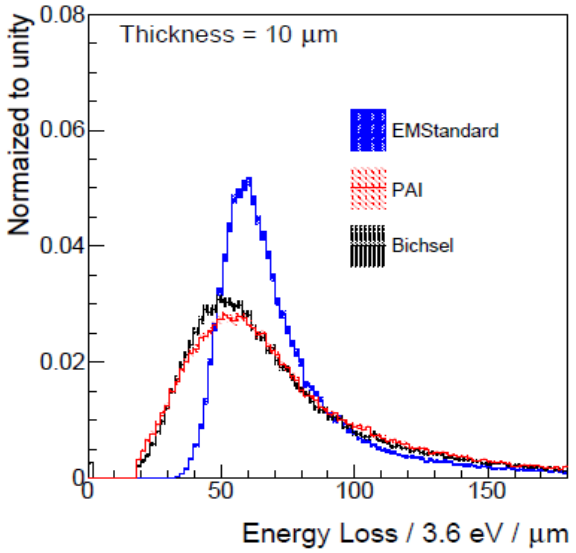


Time Walk



DPTS[1] time resolution with and without time walk correction

Landau Fluctuations

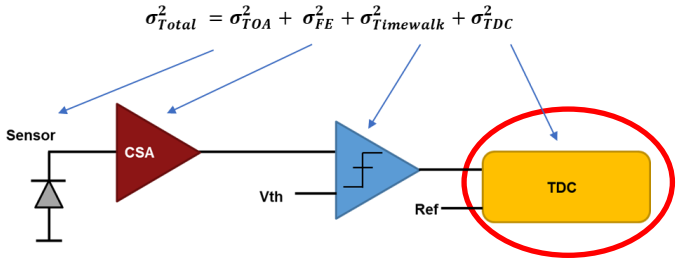


Ref: Fuyue Wang, Su Dong, Benjamin Nachman, Maurice Garcia-Sciveres, Qi Zeng, *The impact of incorporating shell-corrections to energy loss in silicon*, Nuclear Instruments and Methods in Physics Research Section A, Volume 899, 2018
https://doi.org/10.1016/j.nima.2018.04.061

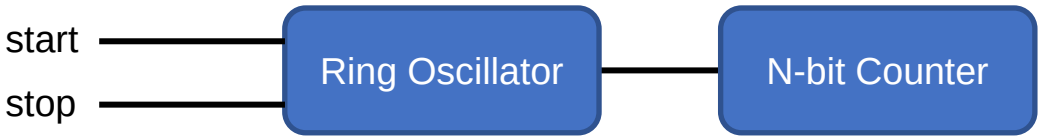
Reference:
[1] G.A. Rinella *et al.* "Digital Pixel Test Structures implemented in a 65 nm CMOS process"
https://doi.org/10.48550/arXiv.2212.08621

SLAC

Limits on TDC (σ_{TDC})



- TDC can be made with a Ring Oscillator in pixel
- Simulations of a 15-stage Ring Oscillator show very good timing resolution < 1 ps-rms.
- The main noise will be the quantization noise = $\frac{Period}{\sqrt{12}}$
- For a $\sigma_{quantization}$< 150 ps-rms, we need a period of 520 ps ➔ Ring Oscillator frequency of ~ 2 GHz
- This could become a digital challenge if the occupancy is high
- In e+e- tracker we can expect an occupancy ~ 100 hits/cm^2 (in a bunch train). For a pixel pitch of 25 µm that would be 1 hit every 160 pixels, so that's a sufficiently low occupancy compatible with such a solution.



Example of Ring Oscillator based TDC

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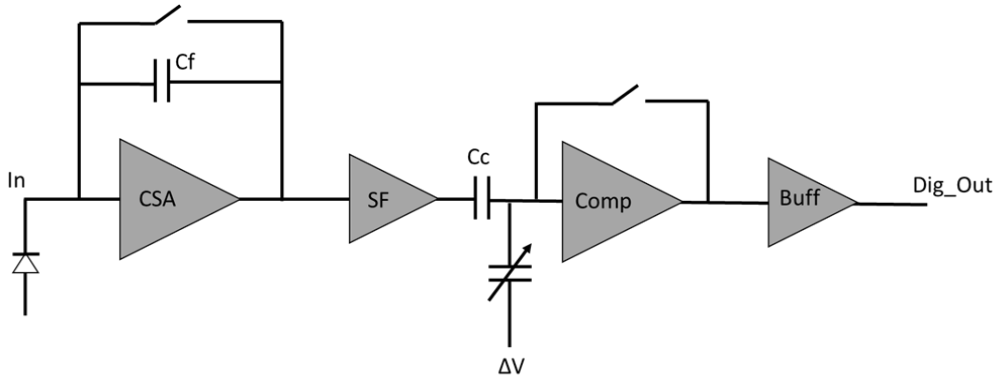
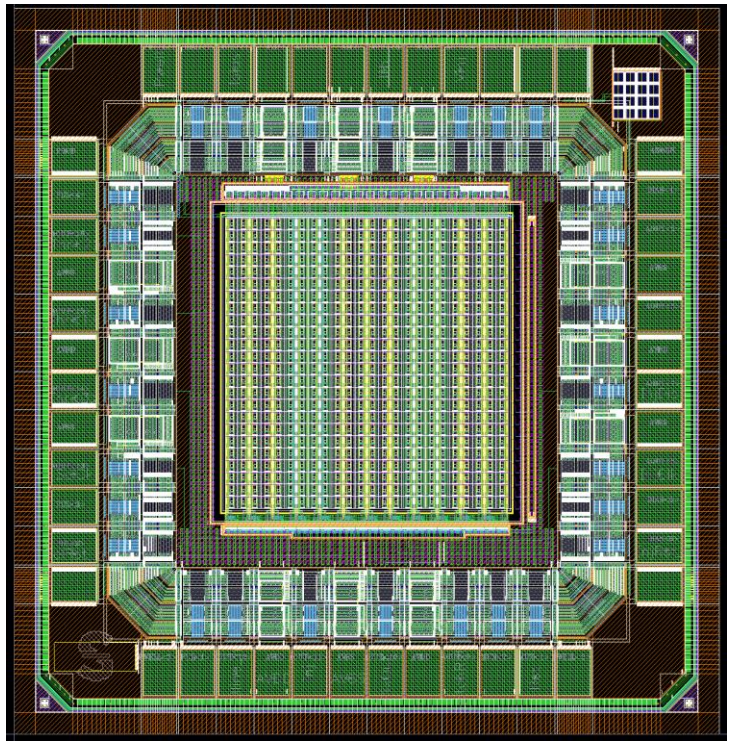
NAPA_p1: **NA**nosecond **P**ixel for large **A**rea sensors – **P**rototype **1**

- Design in Tower Semiconductor 65 nm imaging technology, capitalizing on the CERN WP1.2 efforts over a decade of sensor optimization.
- The prototype design submitted with a total area 5 mm x 5 mm and a pixel of 25 µm × 25 µm, to serve as a baseline for sensor and pixel performance.



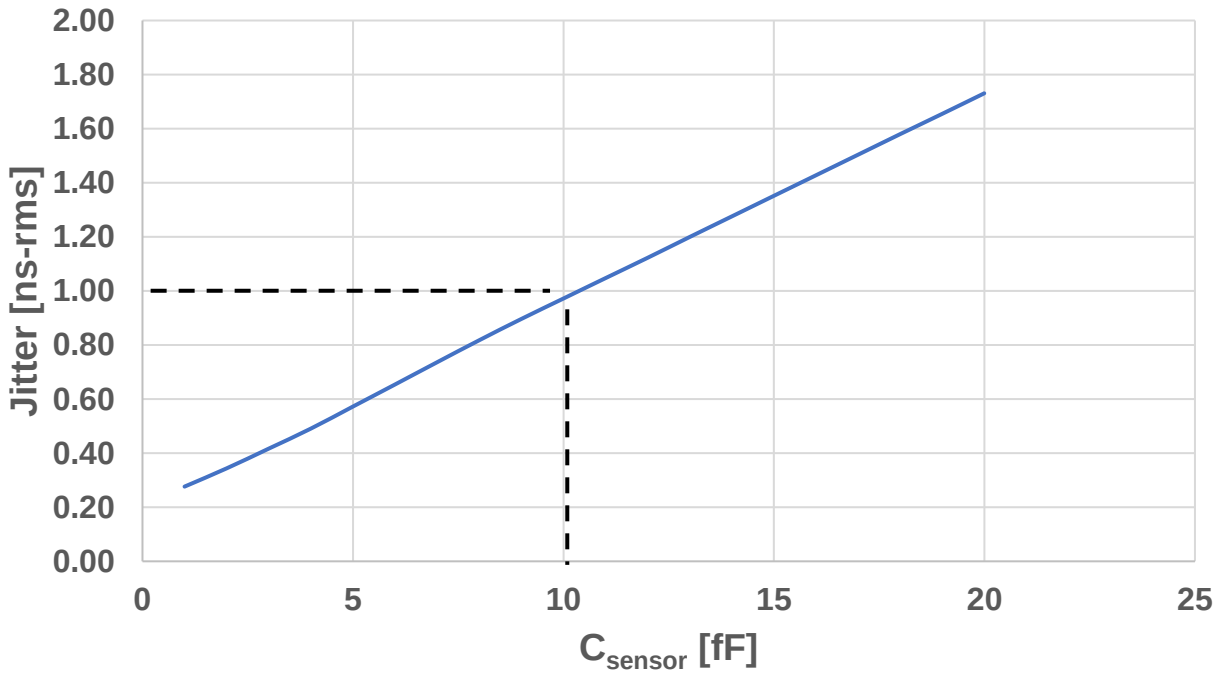


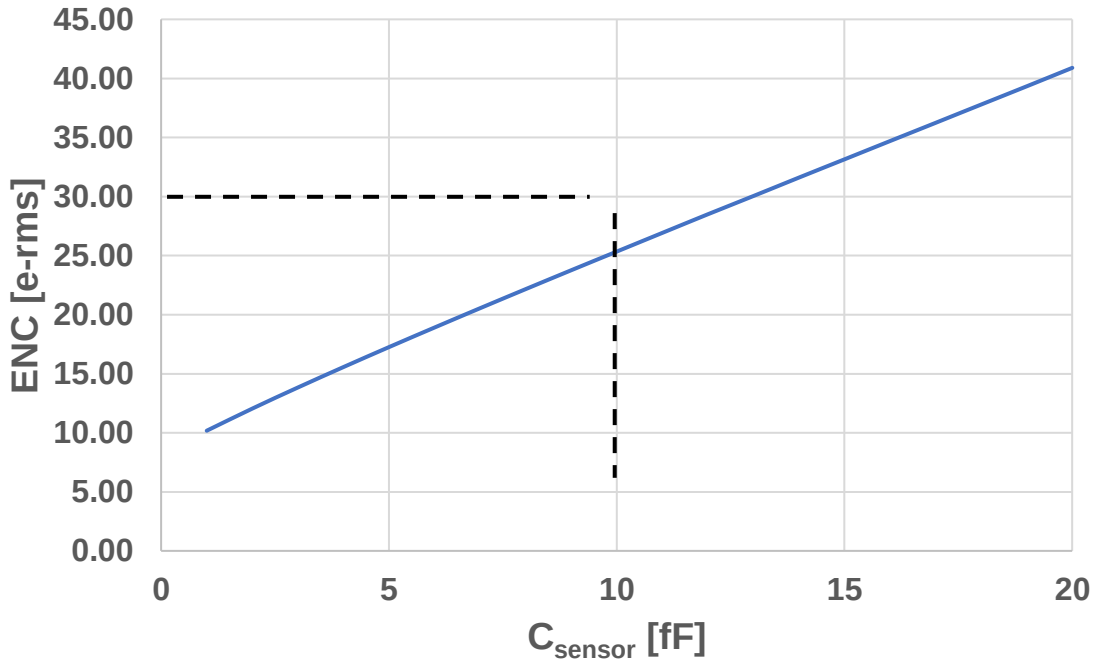
Layout of MAPS SLAC prototype for WP1.2 shared submission

Pixel key elements

- Charge Sensitive Amplifier (CSA) with a synchronous reset, which can be powered down during inactive time
- A comparator with auto-zero technique, removing the need for per-pixel threshold calibration

Simulation of Jitter and ENC as a Function of C_{sensor}





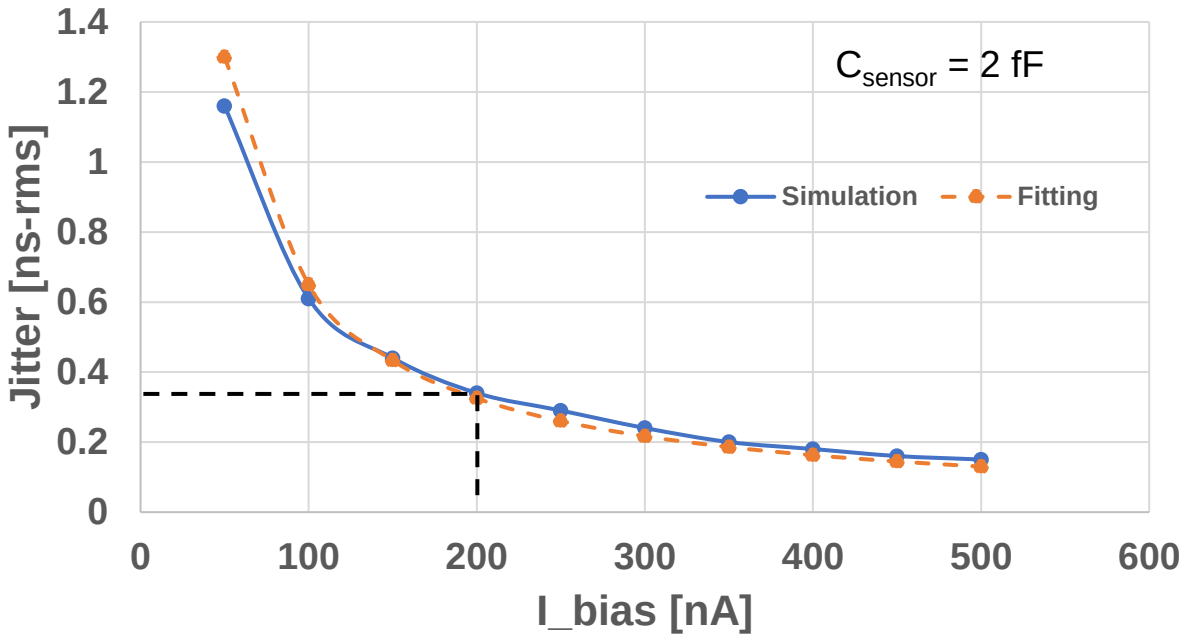
jitter < 1 ns-rms for C_{sensor} < 10 fF

ENC < 25 e-rms

These simulations are with a pixel current of 600 nA ➔ <Power density> = 115 mW/cm^2 x duty cycle
For e+e- machines such as ILC and C^3, duty cycle is expected < 1%

Simulation Results : Jitter and Time Walk

Jitter

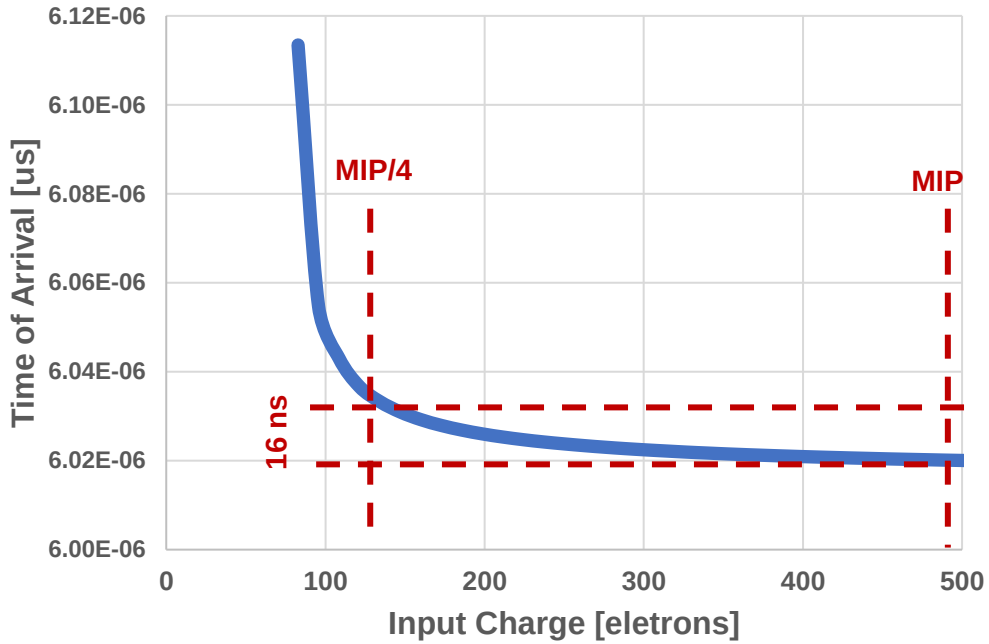


From theory we expect : $\sigma_{FE} \propto \frac{1}{(\text{Power})^{\frac{1}{n}}}$ with $1 \leq n \leq 2$

Here fitted with n = 1

Jitter < 400 ps-rms with power of 720 nW/pixel and Cdet of 2 fF

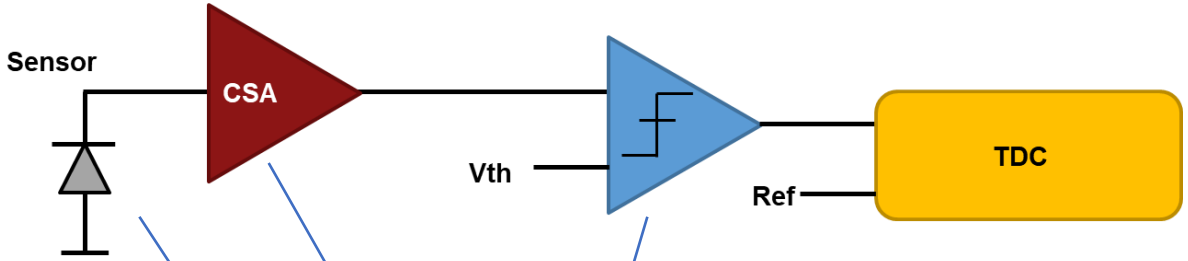
Time Walk



Time walk for MIP → MIP/4 = 16 ns

Not negligeable and must be corrected

Timing Limits for NAPA-p1



$$\sigma^2_{Total} = \sigma^2_{TOA} + \sigma^2_{FE} + \sigma^2_{Timewalk} + \sigma^2_{TDC}$$

σ_{TOA} < 150 ps-rms
For small optimized pixels

σ_{FE} < 400 ps-rms for < 1 µW/pixel

$\sigma_{Timewalk}$ =16 ns
Can be corrected if we measure the ToT inside the pixel

σ_{TDC} < 150 ps-rms
Limited by quantization noise

Assuming time walk is fully corrected ➔σ_{Total}~500 ps-rms with reasonable pixel power consumption, going lower will cost increasingly more power, not compatible with large area sensors
Accounting for residual time Walk after correction, and other non-idealities, it is reasonable to aim for 1 ns-rms time resolution

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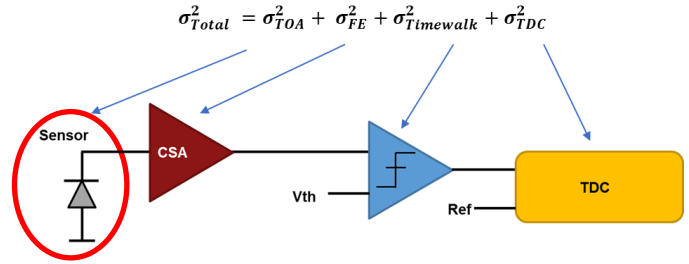
Conclusion

- **MAPS has great a potential to fit the future e+e- colliders requirements (vertex, tracker, calorimeter)**
- **It is possible to achieve very low sensor capacitance of 2-3 fF in Tower Semiconduction 65nm technology, improving power efficiency by at least 2 order of magnitude with respect to hybrid detectors.**
- **Improving timing requires optimization of all the elements of the detection chain. Time walk can be dominant if not corrected.**
- **Simulations of NAPA_p1 show that it is possible to achieve a time resolution ~ 1 ns-rms with reasonably low power consumption of 115 mW/cm^2 × Duty Cycle. For e+e- machines duty cycles are typically < 1%**
- **NAPA-p1 characterization is planned for this summer. Results should be available soon.**

Thank You For Your Attention!

Backup

Signal Formation



According to Shockley-Ramo Theorem, the induced signal in a sensor electrode is:

$$i(t) = Q.\vec{v}.\overrightarrow{E_w}$$

- Total charge generated → $Q \propto d$
- Carrier velocity → $\vec{v} = \mu.\vec{E}$ if $|v| < v_{sat}$
- Weighting Field → Depends on sensor geometry $\overrightarrow{E_w} \propto \frac{1}{d}$

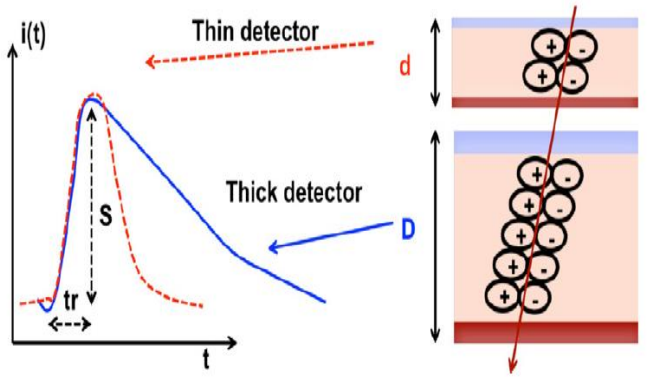


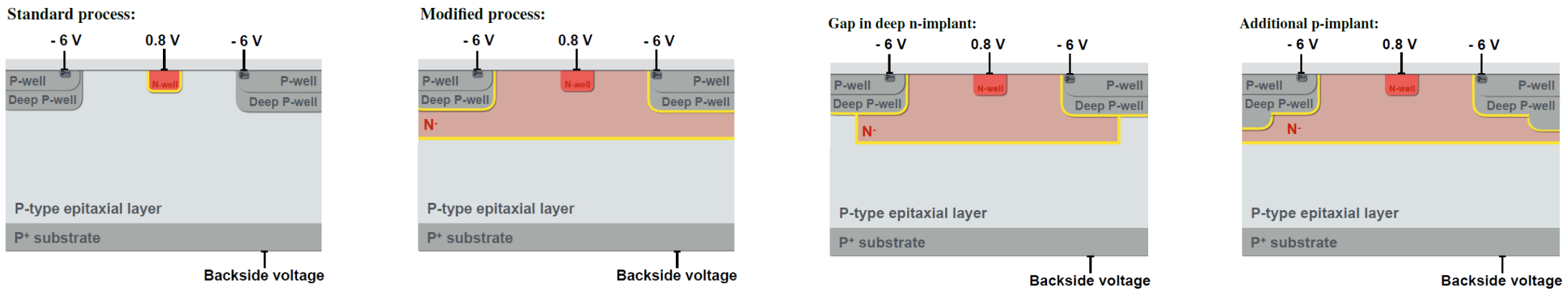
Figure from [1]

The induced current peaks instantaneously as the charges are created in the depletion region. However, the integrated charge peak will depend on the current signal form, and thus on sensor geometry and weighting field form

[1] N. Cartiglia *et al*., "4D tracking: present status and perspectives", Nuclear Instruments and Methods in Physics Volume 1040, 2022, https://doi.org/10.1016/j.nima.2022.167228

How low can we go on C_{sensor}?

$$Power \propto (C_{sensor})^m \ with\ 2 \leq m \leq 4$$



- CERN has been working on Tower Semiconductor imaging technology (180 nm and 65 nm) for a decade, trying to optimize the sensor performance [1] [2]
- The standard imaging process offer a balloon shape depletion region around the sensor electrode. Small C_{sensor} but Epitaxial layer not fully depleted
- Adding lightly doped N-layer allows the full depletion of the epitaxial layer while maintaining low C_{sensor}
- Adding an N-gap or extra deep P-well in the pixel corners allow for faster charge collection and higher efficiency
- ➔ It has been proven that we can achieve high efficiency with a C_{sensor}~2 – 3 fF

[1] M. van Rijnbach et al., *Radiation hardness and timing performance in MALTA monolithic pixel sensors in TowerJazz 180 nm*, 2022 *JINST* C04034
[2] M. Munker et al., *Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance,*2019 *JINST* 14C05013

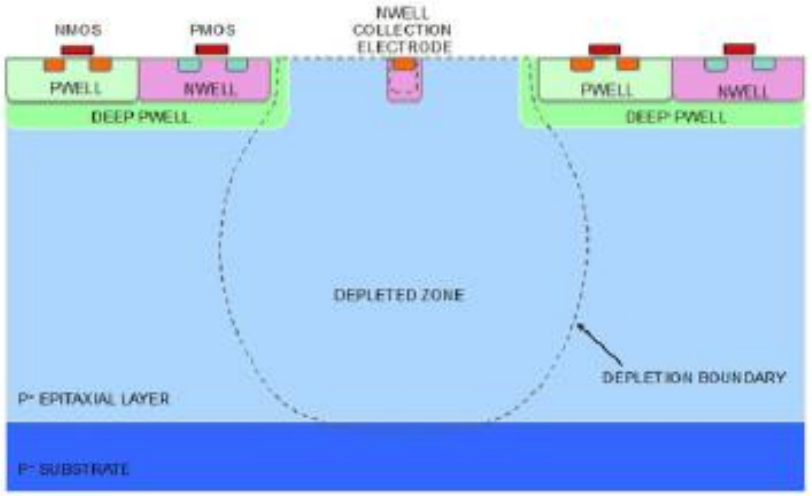
ALPIDE

Technology	Pixel dimension	Pix shape	Rise time	Time res.	Consumption	P. Density	ENC
Tower 180 nm	29.24x 26.88 μm^2	~square	2 us	< 2 us	40 nW/pixel	40 mW/cm^2	3.9 e-rms

ALPIDE is the first MAPS to be used in a big HEP experiment.

It was designed for ALICE ITS2, with Pb-Pb collisions up to 100 kHz so it does not have fast timing constraints

- **Very low power consumption**
- **Low sensor capacitance (2-3 fF)**
- **Epitaxial layer not entirely depleted. Collection by drift + diffusion**
- **→ cannot achieve fast signal detection**



References:

- Gianluca Aglieri Rinella, “The ALPIDE pixel sensor chip for the upgrade of the ALICE Inner Tracking System, Nuclear Instruments and Methods in Physics Research, Volume 845,2017, https://doi.org/10.1016/j.nima.2016.05.016
- M. Mager, “ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITS upgrade”, Nuclear Instruments and Methods in Physics Research, Volume 824, 2016, https://doi.org/10.1016/j.nima.2015.09.057

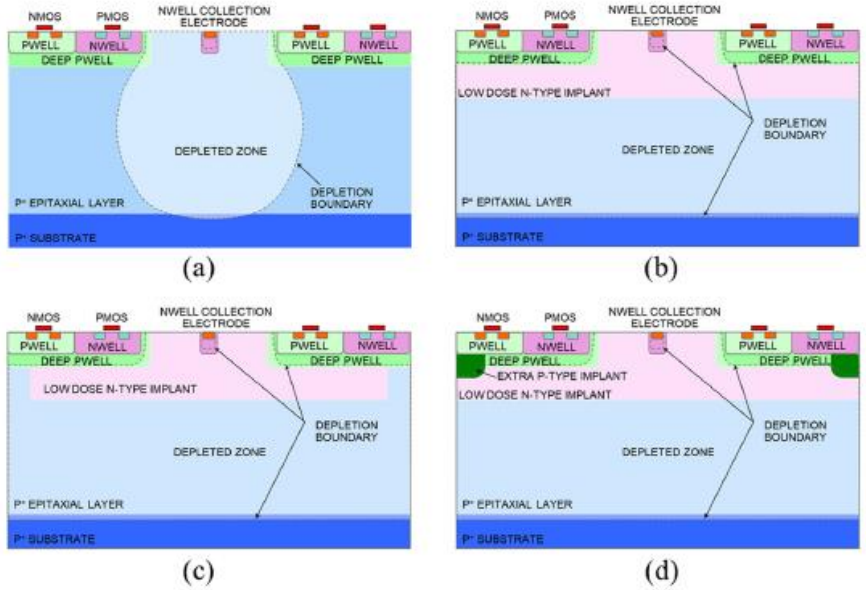
FastPix

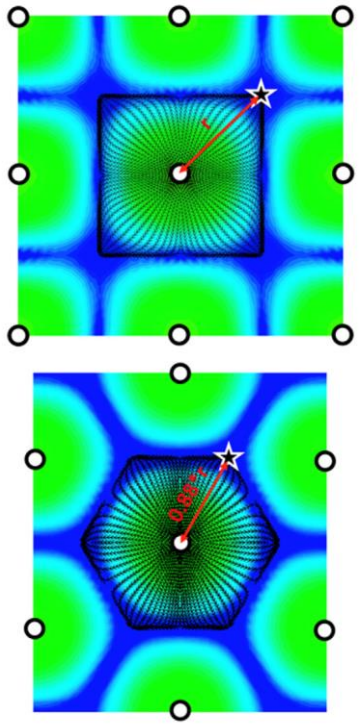
Technology	Pixel pitch	Pix shape	Rise time	Time res.	Consumption	P. Density	ENC
Tower 180 nm	8.6 µm – 20 µm	Hexagonal	1-2 ns	~130 ps-rms	18 µA in pixel	>1500 mW/cm^2	11 e-rms

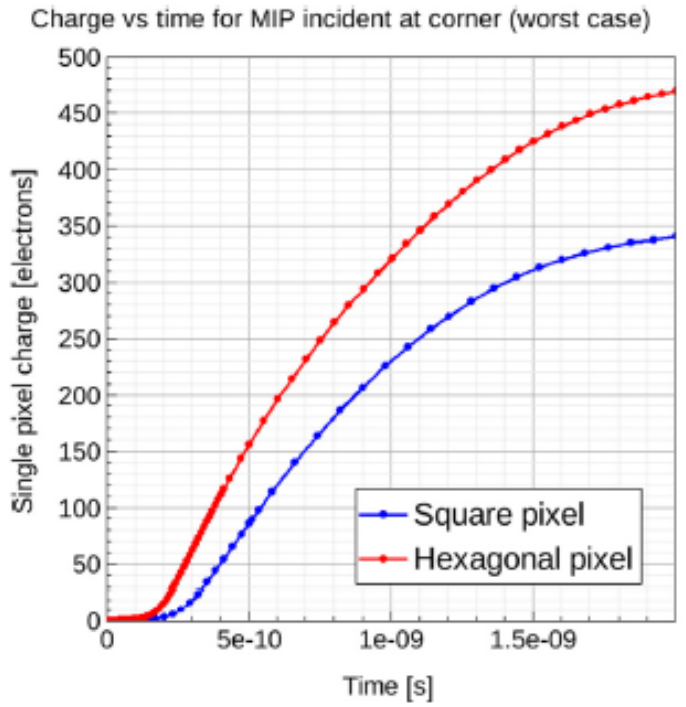
Designed for fast response

→Smaller pixels and large consumption are needed

Process Modifications







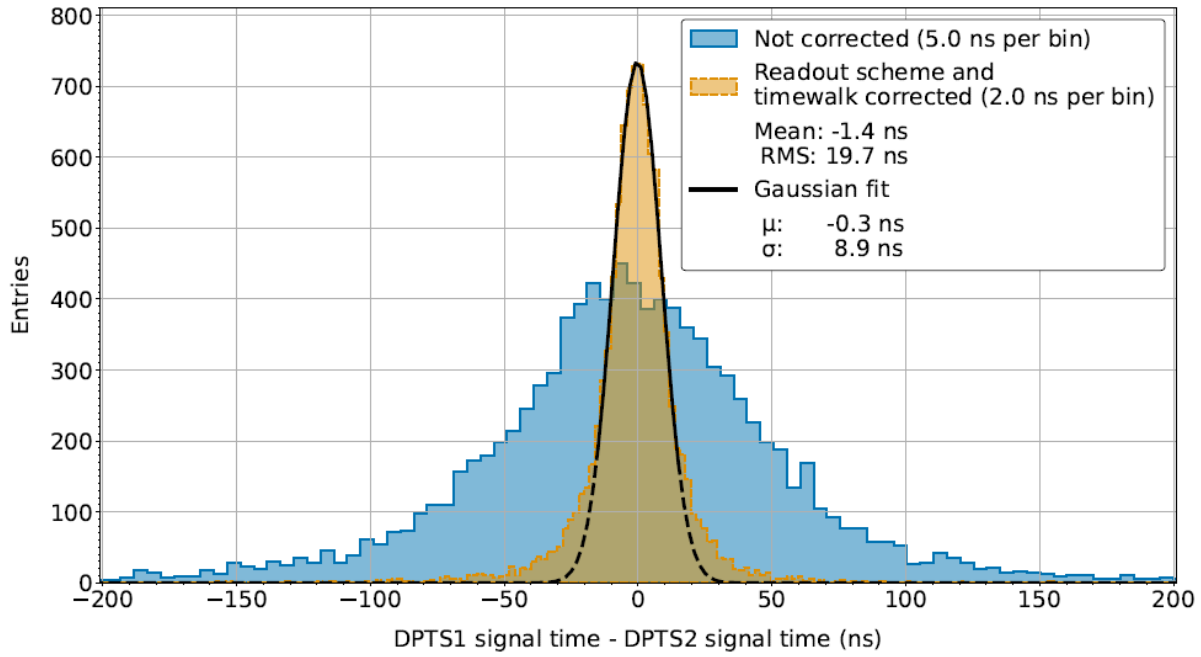
References:

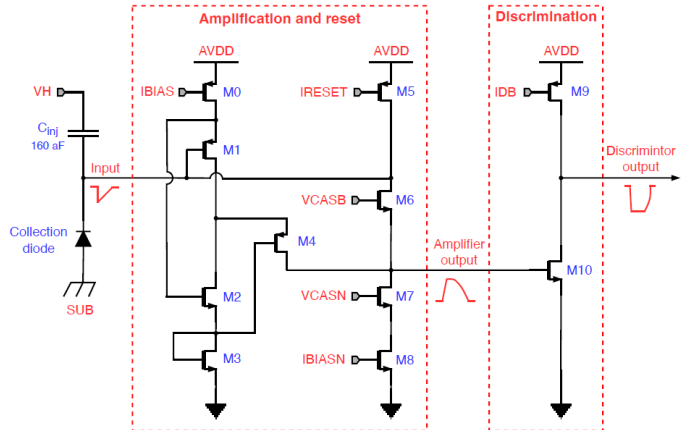
- T. Kugathasan *et al.,* "Monolithic CMOS sensors for sub-nanosecond timing", Nuclear Instruments and Methods in Physics Research, Volume 979, 2020, https://doi.org/10.1016/j.nima.2020.164461.
- J. Braach et al., "Performance of the FASTPIX Sub-Nanosecond CMOS Pixel Sensor Demonstrator", *Instruments* 2022, *6*(1), 13; https://doi.org/10.3390/instruments6010013

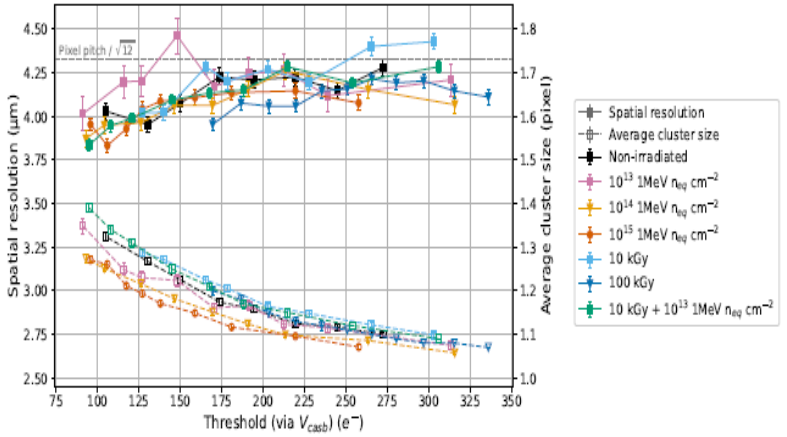
DPTS

Technology	Pixel pitch	Pix shape	Rise time	Time res.	Consumption	P. Density	ENC
Tower 65 nm	15 µm	square	≈ 1us	6.3 ns-rms	210 nA/pixel	112 mW/cm^2	2-6 e- rms

- Time over Threshold (ToT) is measured for for time walk correction (50 ns Vs 6 ns)
- Good detection efficiency up to 10^{15} 1MeV n_{eq}/cm^2





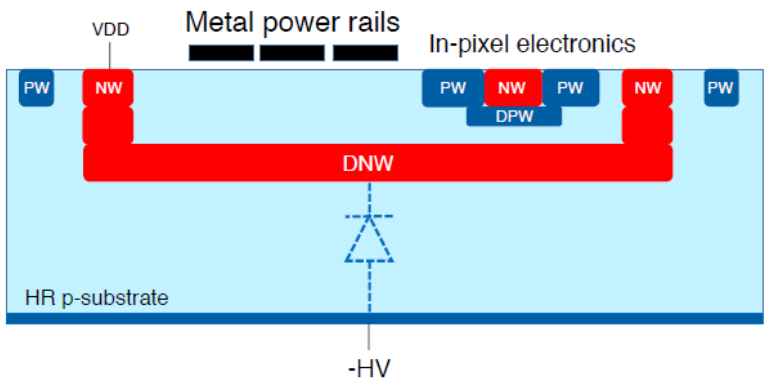


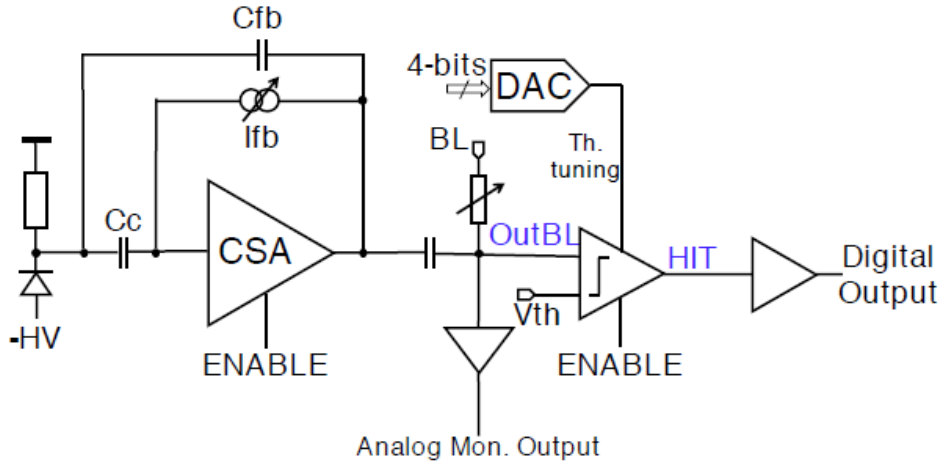
Reference:
G.A. Rinella *et al.* "Digital Pixel Test Structures implemented in a 65 nm CMOS process" https://doi.org/10.48550/arXiv.2212.08621

Cactus

Technologie	Pixel size	Pix shape	Rise time	Time res	Consumption	P. Density	ENC
Lfoundry 150nmn	1x1 mm2 1x0.5 mm2	Square	1 ns	100 - 500 ps-rms	800 µA/pixel	145 mW/cm^2	300 e-rms

- Up to 300 V on 200 µm thickness of high resistivity substrate (2 kΩ .cm)
- Input diode capacitance is more than an order of magnitude larger than expected (15 pF vs 1 pF)
- Signal is much lower than expected, probably due to parasitics. A second iteration was submitted

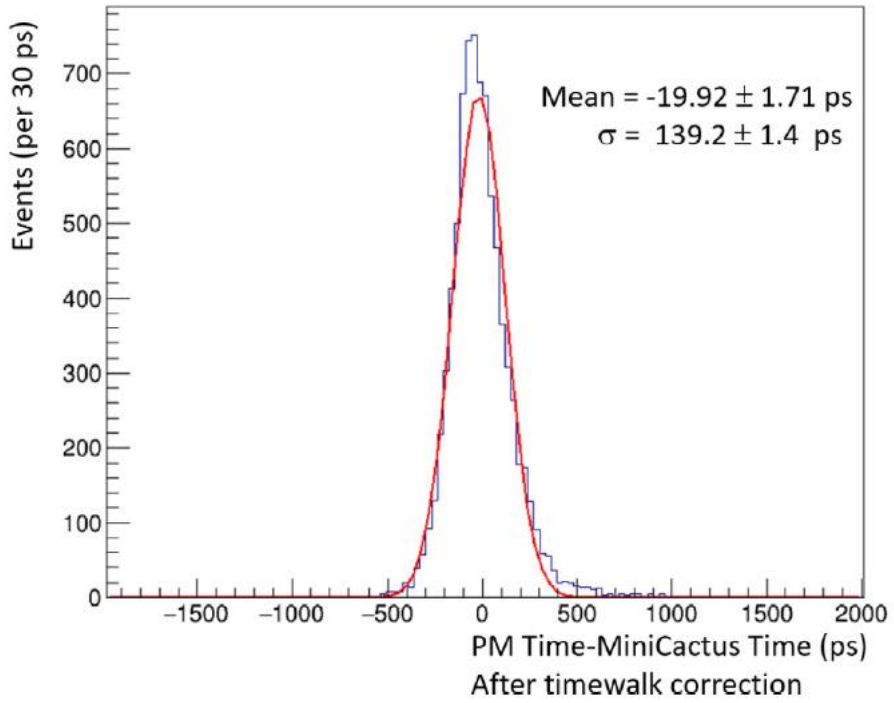


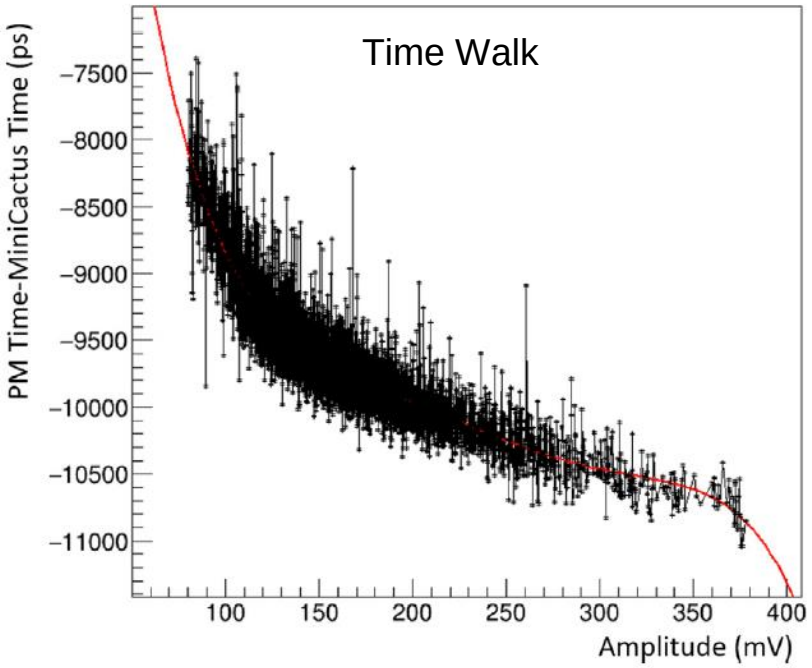


Reference:
- Y. Degerli *et al* 2020 *JINST* **15** P06011 **DOI** 10.1088/1748-0221/15/06/P06011

Min-Cactus

Technology	Pixel size	Pix shape	Rise time	Time res	Power Density
Lfoundry 150 nmn	1x0.5 mm2	Rectangle	1 ns	88 ps-rms (timewalk corrected)	300 mW/cm^2



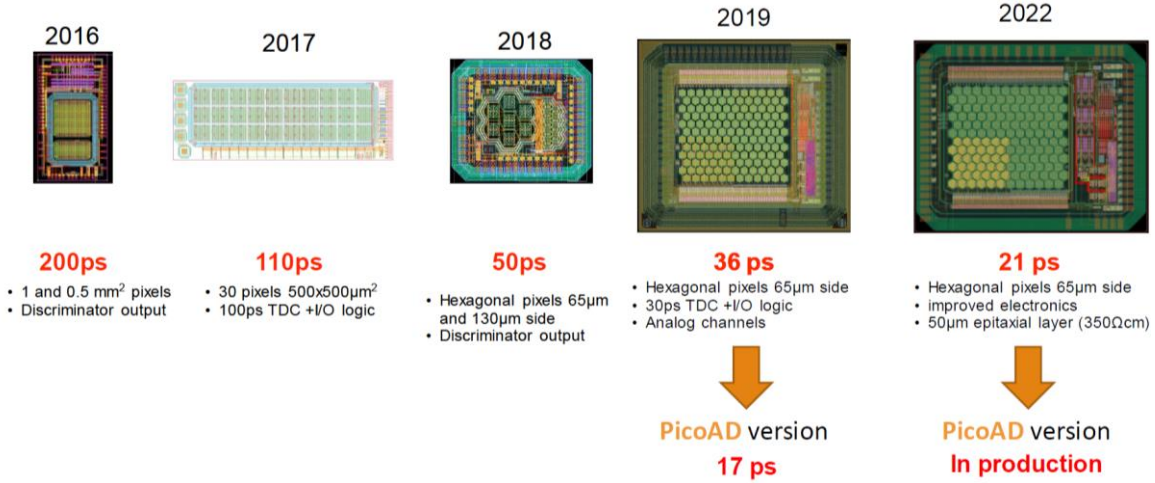


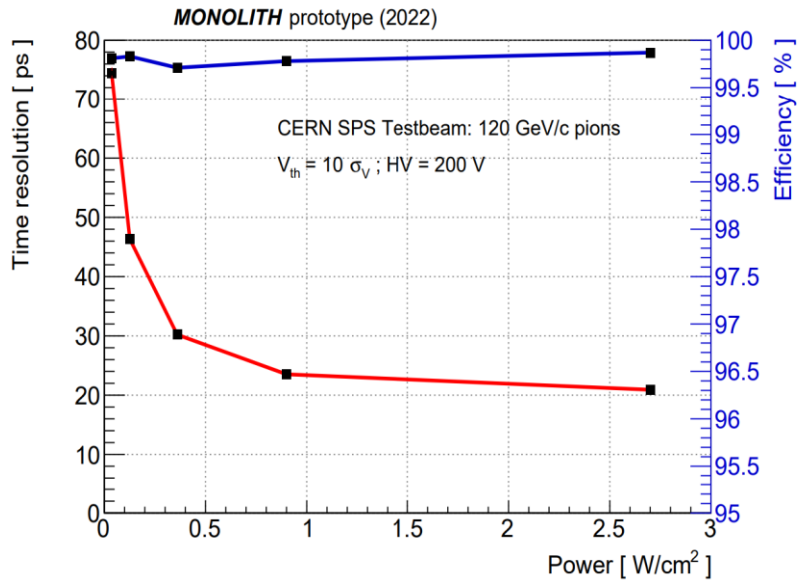
Reference:
Y. Degerli *et al., "*MiniCACTUS: Sub-100 ps timing with depleted MAPS", Nuclear Instruments and Methods in Physics Research, Volume 1039, 2022, https://doi.org/10.1016/j.nima.2022.167022.

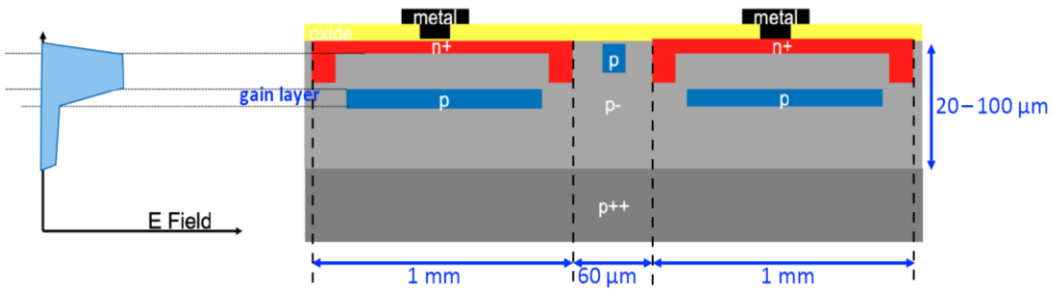
Monolith Project- SiGe BiCMOS

Technology	Pixel pitch	Pix shape	Time res	Consumption	Power Density
SiGe 130nm IHP	100 µm	Hexagonal (65 µm side)	77 – 20 ps-rms (timewalk corrected)	0.7 – 2.3 uA/pixel	40 – 2700 mW/cm^2

- SiGe HBT very high f_T(hundreds of GHz) → excellent performance
- High-resistivity (220 Ω·cm) substrate, about 130 µm thickness
- Hexagonal pixels integrated as triple wells, pixel capacitance of 80 fF
- Possibility of adding a gain layer (~60 for a MIP)



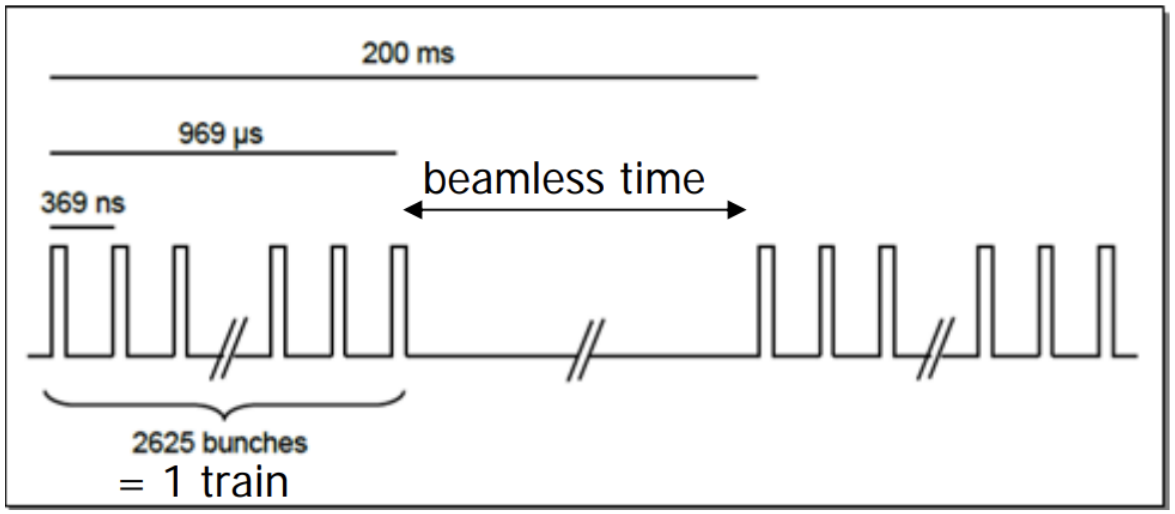




References:
- S. Zambito *et al* 2023 *JINST* **18** P03047**DOI** 10.1088/1748-0221/18/03/P03047
- L. Paolozzi "A Picosecond Avalanche Detector in SiGe BiCMOS' ULITIMA Conference 2023

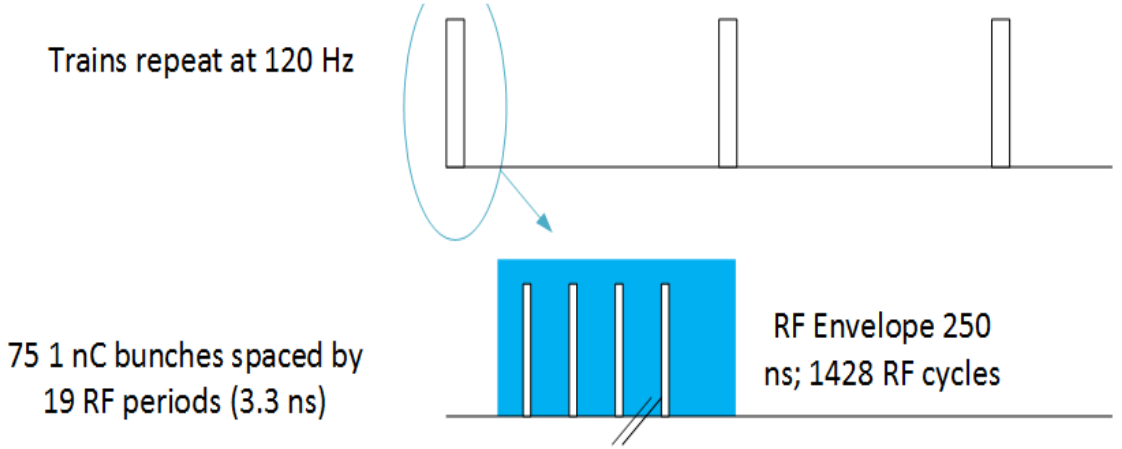
Duty Cycle for e+e- machines

ILC Timing Structure



Duty Cycle = 0.48%

C^3 Timing Structure



Duty Cycle = 0.03 %

For NAPA_p1 <Power density> = 115 mW/cm² x duty cycle << 20 mW/cm²

➔ Compatible with gas cooling <u>if we use power pulsing</u>

➔ As for voltage drop, the pixel works up to a Vdrop of 300 mV

Ref: 2110.15800.pdf (arxiv.org)