LCWS2023
INTERNATIONAL WORKSHOP ON LINEAR COLLIDERS

Commissioning and noise study of the ultra-thin chip-on-board PCB for the CALICE SiW-ECAL prototype

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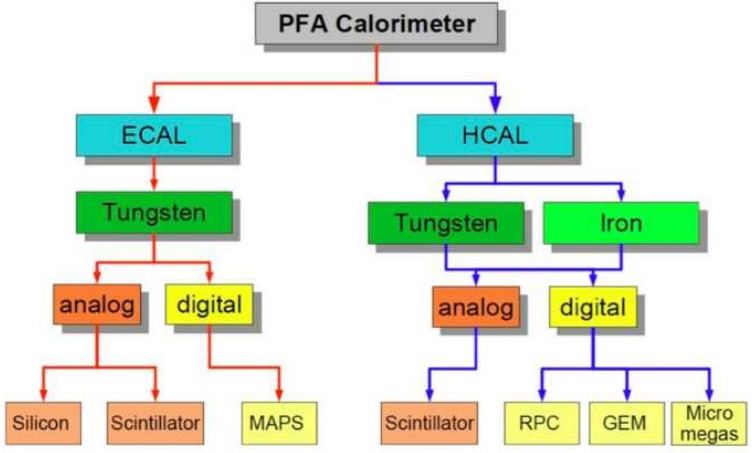
GOBIERNO DE ESPAÑA MINISTERIO DE CIENCIA E INNOVACIÓN
Plan de Recuperación, Transformación y Resiliencia
GENERALITAT VALENCIANA Conselleria d'Innovació, Universitats, Ciència i Societat Digital
Financiado por la Unión Europea NextGenerationEU
Gen-T

SiW-ECAL



CALICE

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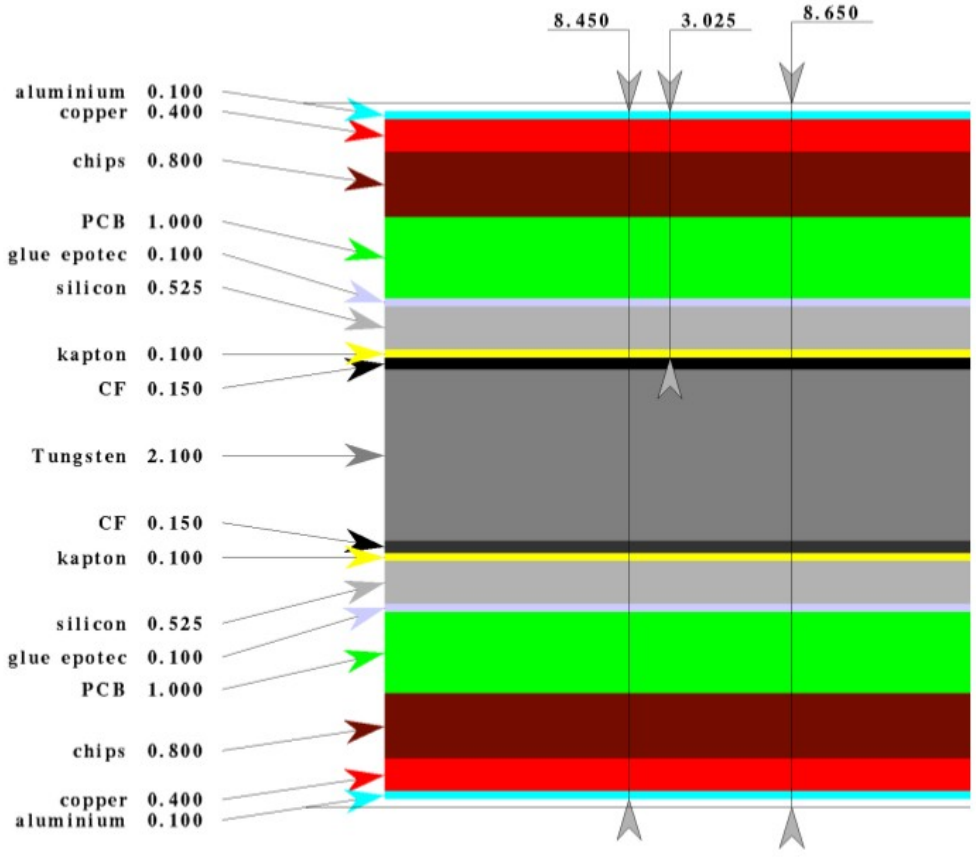
Ultra thin PCB: Chip On Board

- **ILD tight spatial constrains:** Total space for ASICs and PCB 1.8mm (was 1.2mm since ~2007)
  - BGA pcbs + ASICs are ~2.5-3mm



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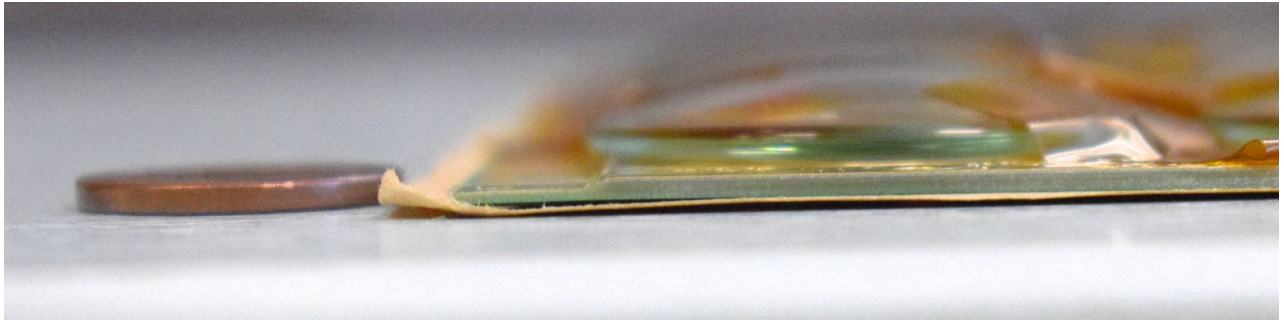
Ultra thin PCB: Chip On Board

▶ **Chip-On-Board proposal:**

- Naked ASICs wirebonded.
- Cavities (~250um) for the ASICs

▶ **IJCLab & OMEGA** collaboration with **ITAEC/SKKU** (Sungkyunkwan University, Suwon – Korea) and **EOS company** for the PCB production.



LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

OMEGA Microelectronics

SUNG KYUN KWAN UNIVERSITY(SKKU)

EOS CORPORATION

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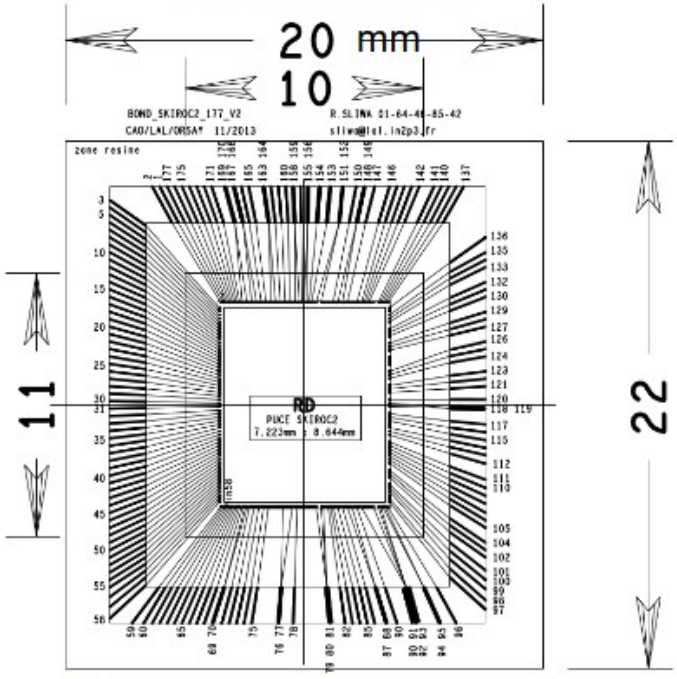
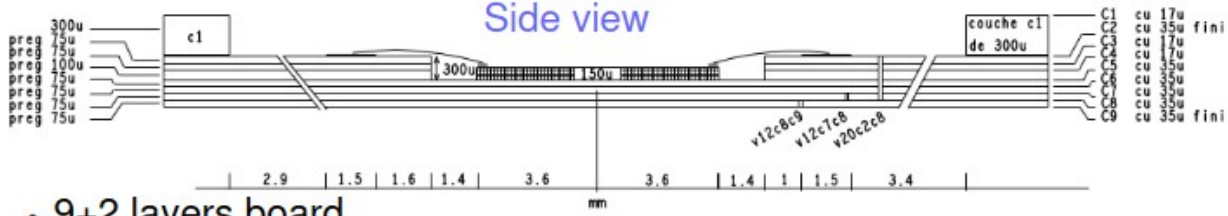
COB: chip-on-board

Bonding scheme



- ~177 Bonding wires
- Bonding by CERN Bondlab
- Regular exchange allowed to iron out early shortcomings

Side view



- 9+2 layers board
- Overall height ~1.2mm
- ASICs buried in cavities to ensure overall flatness
  - Need to make sure that bonding wires don't pass board surface

Stephane Callier

More info

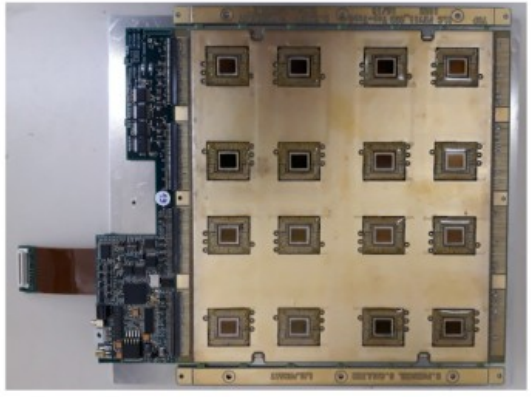
FEV zoo

- In recent years the SiW ECAL has developed and used several PCB variants
  - To make sure that you don't get lost, here comes an introduction

FEV10-12

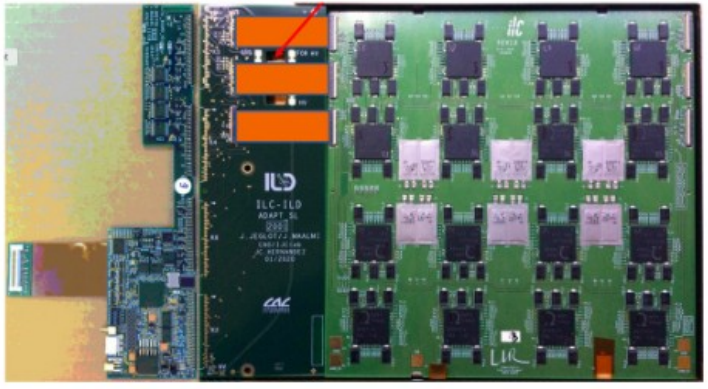
- ASICs in BGA Package
- Incremental modifications From v10 -> v12
- Main “Working horses” since 2014

FEV_COB



- ASICs wirebonded in cavities
  - COB = Chip-On-Board
- Current version FEV11_COB
- Thinner than FEV with BGA
- External connectivity compatible with BGA based FEV10-12

FEV13



- Also based on BGA packaging
- Different routing than FEV10-12
- Different external connectivity

Current prototype (see later) is equipped with all of these PCBs

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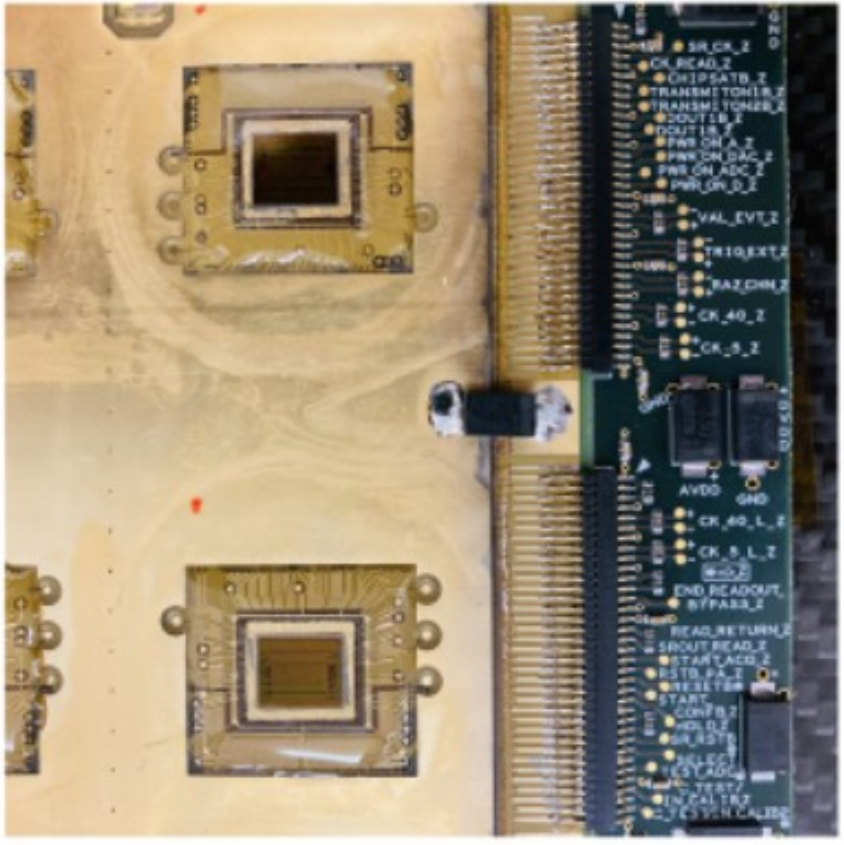
Part of the FEV zoo at DESY and CERN

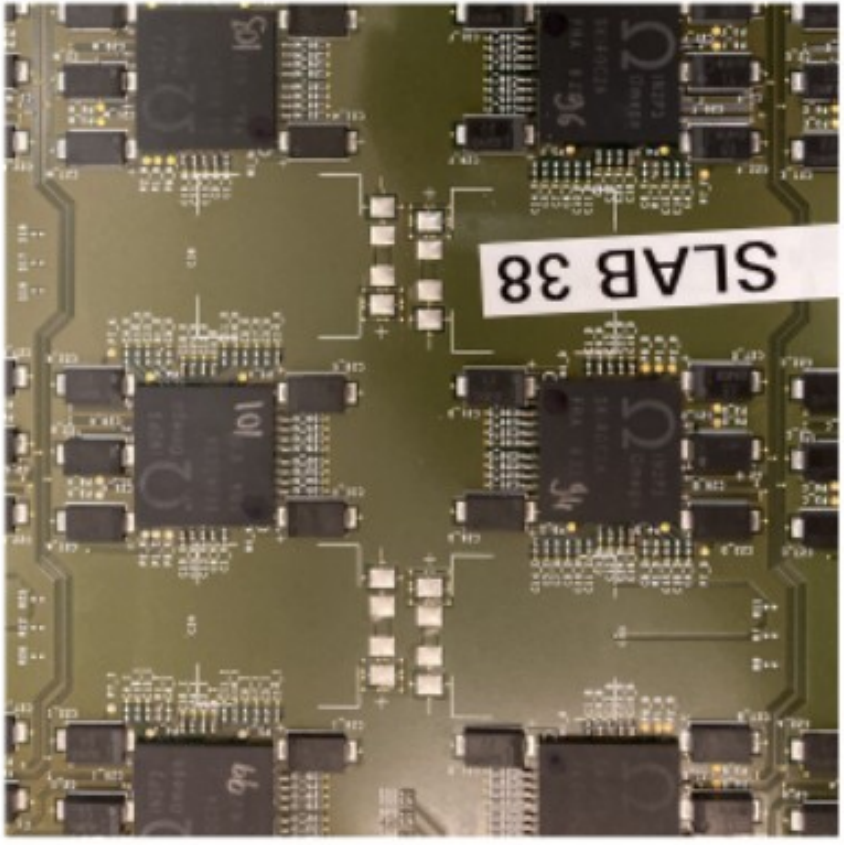
- In this study, we only consider 6 FEVs (equipped all with 500um)

Pos.	Id	ASU type	An. PS. Dec.	Dig. PS. Dec.
5th	slab 38	FEV13	$(1nF \times 32)$ & $(10nF \times 32)$ & $(100nF \times 32)$ & $(1\mu F \times 32)$ & $(68\mu F \times 32)$ PA : $(1nF \times 32)$ & $(10nF \times 32)$ & $(100nF \times 32)$ & $(1\mu F \times 32)$ & $(120\mu F \times 32)$	$(100nF \times 33)$ & $(33\mu F \times 16)$
6th	slab 39	FEV13	$(1nF \times 32)$ & $(10nF \times 32)$ & $(100nF \times 32)$ & $(1\mu F \times 32)$ & $(68\mu F \times 32)$ $(PA$:$)(1nF \times 32)$ & $(10nF \times 32)$ & $(100nF \times 32)$ & $(1\mu F \times 32)$ & $(120\mu F \times 32)$	$(100nF \times 33)$ & $(33\mu F \times 16)$
7th	slab 29	COB	$(100nF \times 12)$ & $(150\mu F \times 2)$& $(330\mu F \times 5)$	$(100nF \times 14)$ & $(330\mu F \times 5)$
8th	slab 30	FEV12	$120\mu F \times 16$	$120\mu F \times 16$
9th	slab 33	COB	$(100nF \times 8)$ & $(150\mu F \times 2)$& $(330\mu F \times 5)$	$(100nF \times 8)$ & $(330\mu F \times 5)$
10th	slab 31	FEV12	$120\mu F \times 16$	$120\mu F \times 16$

Table 1: Summary of devices under study and their main properties. Column by column: Position in the 15 layer stack; ID; ASU type; amount of decoupling capacitors (with their value) for the Analogue Power Supplies and the Digital Power Supplies. Notice that for the FEV13, the preamplifier analogue power supplies (PA) are separated from the other analogue power suplies.

Part of the FEV zoo at DESY and CERN





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Commissioning: pedestal and noise

channel i is:

$$\sigma_i^2 = \sigma_{I_i}^2 + \sum_{j=1}^{N_c} \sigma_{C_i^j}^2 \quad (1)$$

The covariance matrix element from the two channels i and k is expressed by:

$$cov(i,k) = \delta_{ik}\sigma_{I_i}\sigma_{I_k} + \sum_{j=1}^{N_c} \sigma_{C_i^j}\sigma_{C_k^j} \quad (2)$$

where:

$$\delta_{ik} = \begin{cases} 1 & \text{if } i = k \\ 0 & \text{if } i \neq k \end{cases} \quad (3)$$

The covariance matrix element can also be determined from the data:

$$cov_{Data}(i,k) = \frac{\sum_{n=1}^{N_{event}} (A_i(n) - \mu_{A_i})(A_k(n) - \mu_{A_k})}{N_{event}} \quad (4)$$

Measured amplitude if no hit

Pedestal position calculated as simple histogram Mean

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Commissioning: pedestal and noise

- For the calculation of the pedestal position for each readout channel and each SCA, the following procedure was followed (at DESY and CERN)
  - 1. Use the default trigger thresholds of ~ 0.5 MIP and the ILC-gain (6pF)
  - 2. Mask all readout channels except channel 0
  - 3. Set-up the injection system to inject 15 signals of between 0.75-1.5 MIP 2 in channel 0. These signals were separated by 100μs each.
  - 4. Make sure that all ASICs from all modules in the stack were recording 15 injected signals.
  - 5. Record 10000 readout cycles of 2ms each.
  - 6. Repeat the process 3 times more but using channels 9, 18 or 27 instead of 0

- **The analysis is done, chip-wise (treating all chips independently!)**

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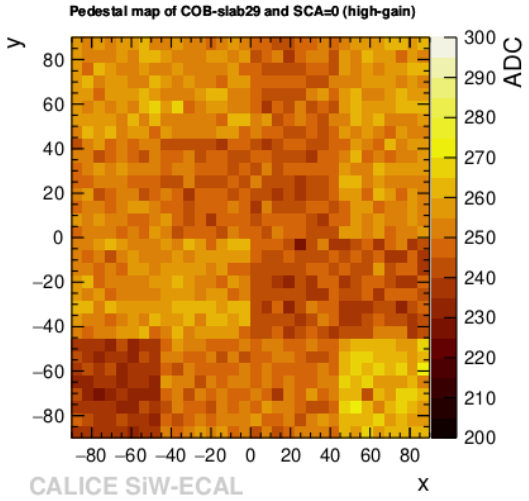
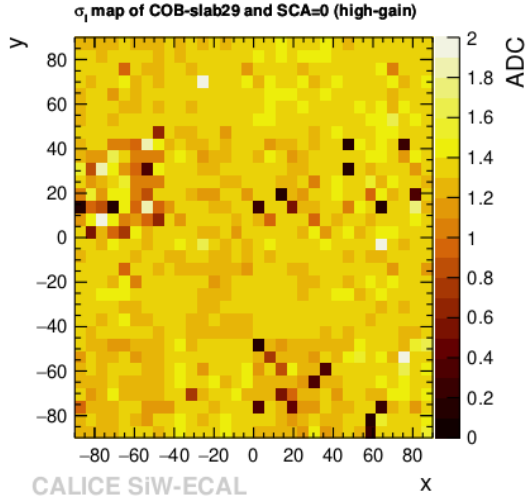
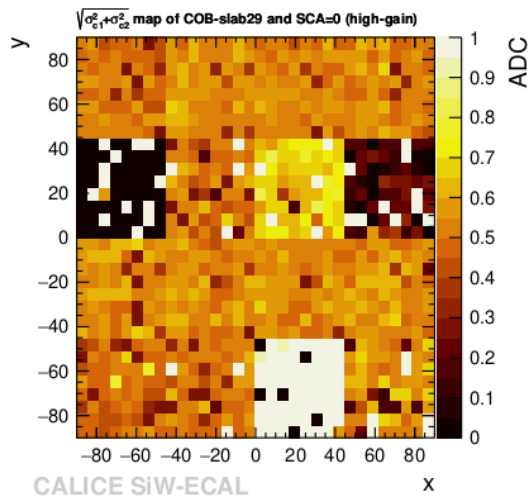
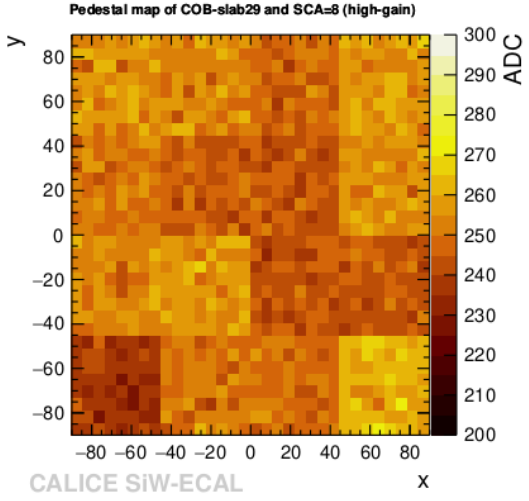
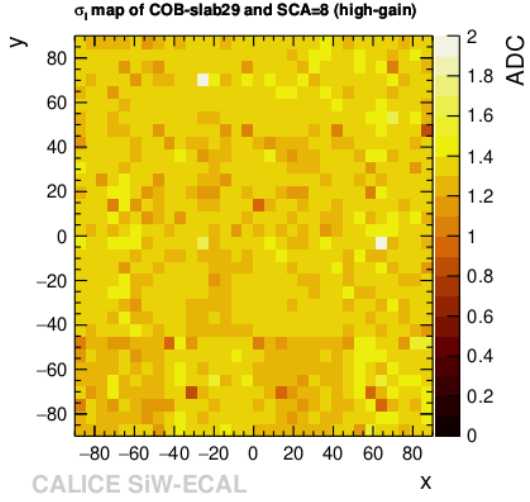
Pedestal and noise, COB -slab29

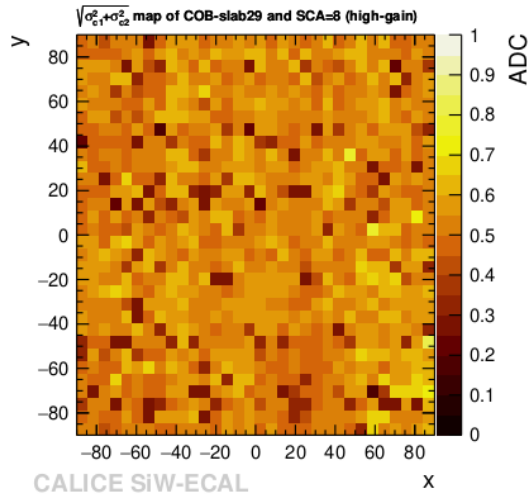




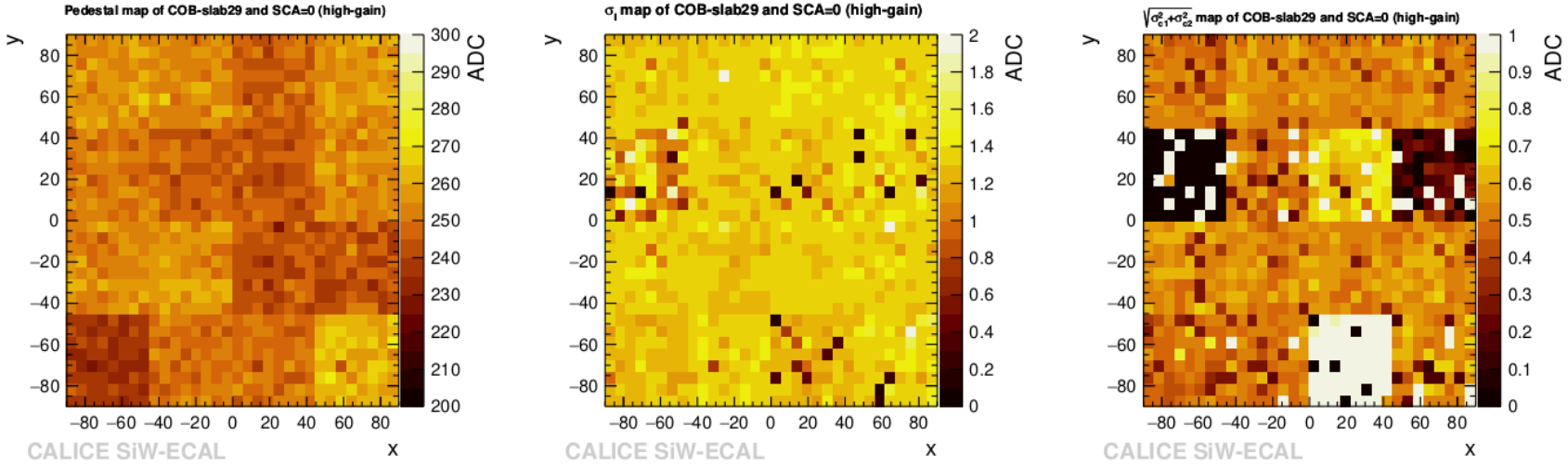






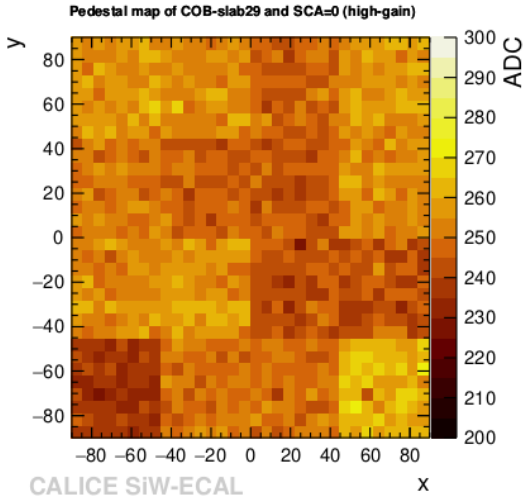


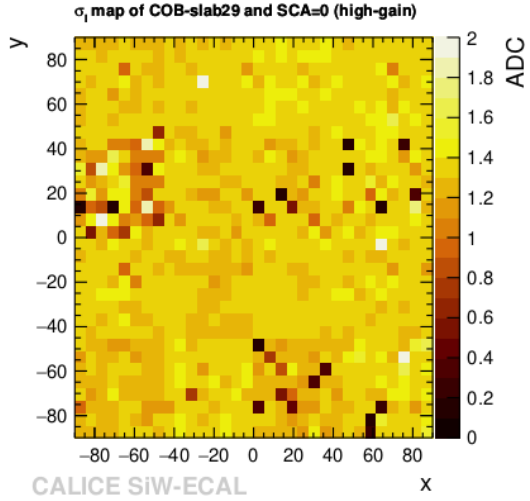
Pedestal and noise, COB -slab29

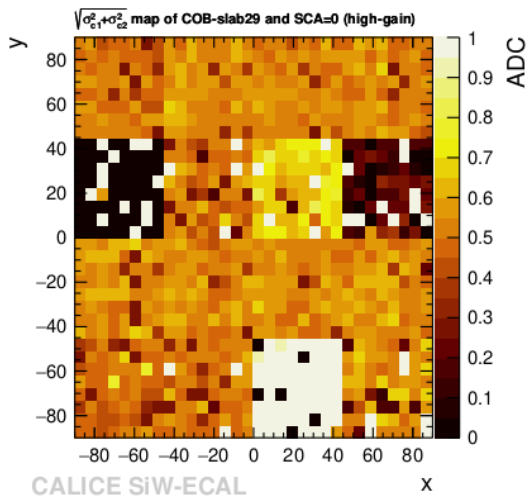


- For the SCA 0, large variations are observed, specially in the ASICs situated in the second and fourth row.
- Non-convergence due to **non-gaussian noise sources**
  - voltage drops (?) which are translated into pedestal shifts, observed in the data as double pedestal peaks
- Effect enhanced in the sectors with more digital routing lines

Pedestal and noise, COB -slab29

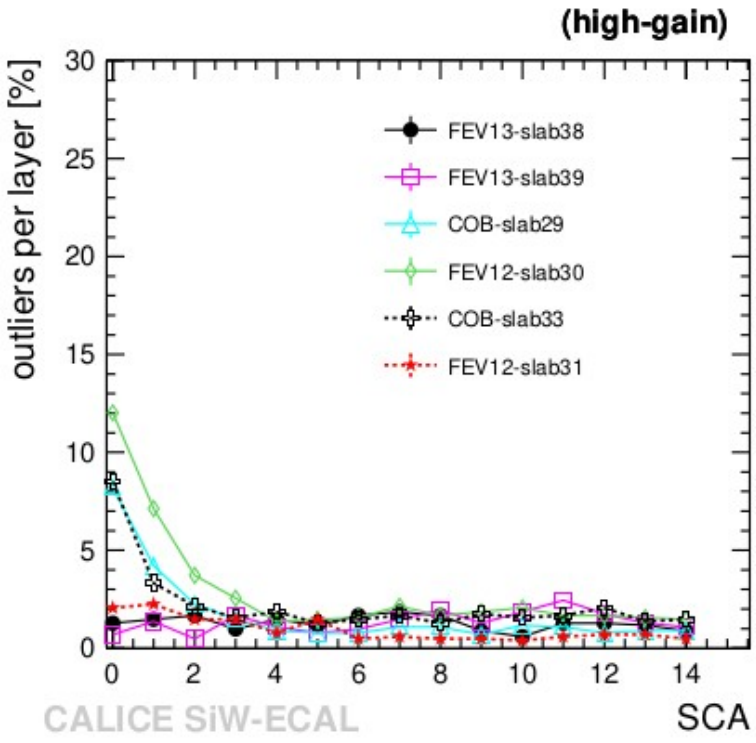


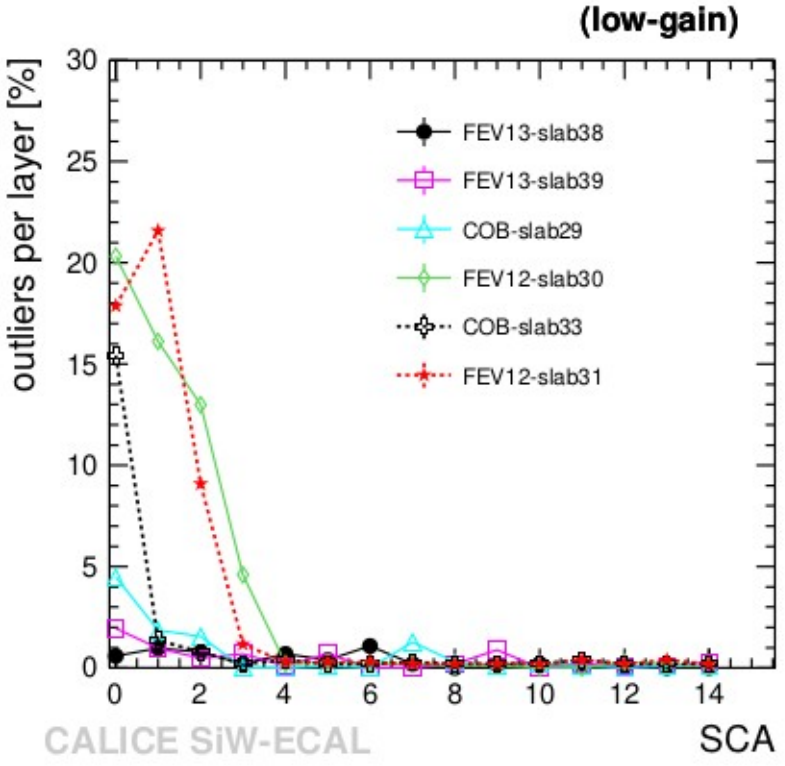




- We define a set of ***"outliers"***
  - Channels that are at more than 3 sigmas of the average noise (incoherent + coherent in quadrature) of the chip
  - Process done iteratively : first we remove the 5sigma outliers for the recalculation of the average
  - **Removed from the analysis**

Outliers per PCB





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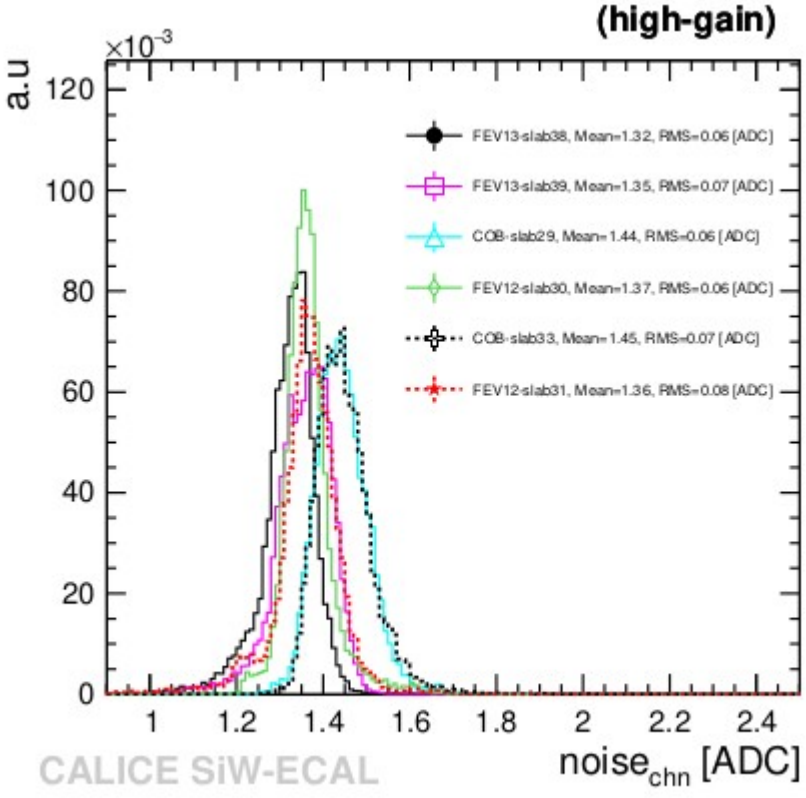
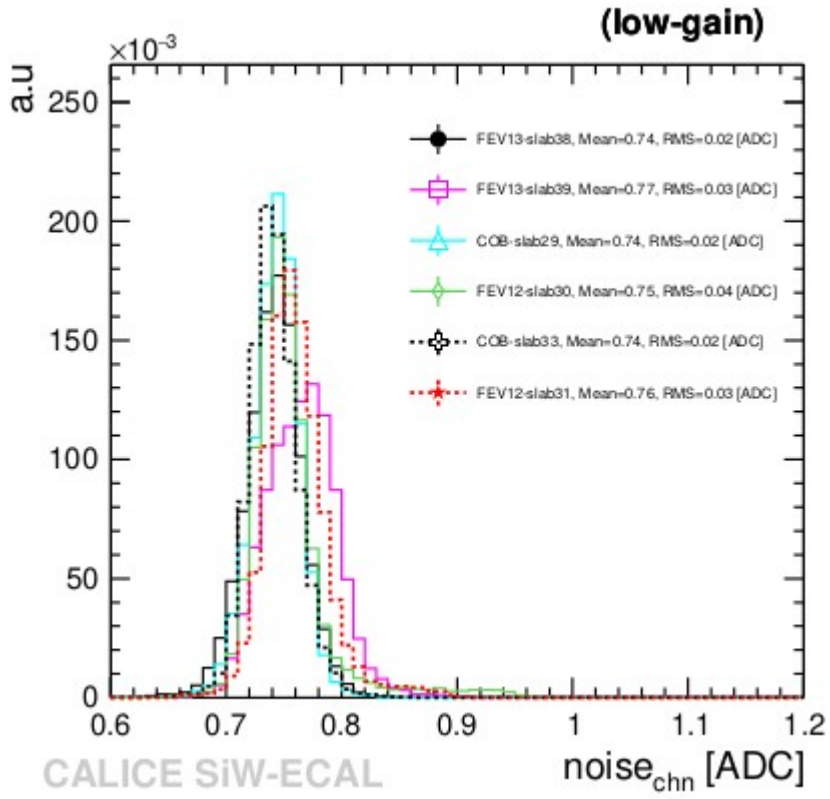
Important remark: before adding the decoupling capacitances to the COBs, the non-gaussian noise source was saturating the readout

Noise (excluding outliers)





Masked channels

- Iterative process using 0.5 MIP thresholds as goal and requiring the noise not competing with cosmic signals
- **FEV12s: (BGA)**
  - **3%** of channels always masked (37 + few channels in near the digital line connectors)
  - Less than 1% of random channels
- **FEV13s (BGA)**
  - **~1.5%** of channels always masked (37 + few channels in near the digital line connectors)
  - Less than 1% of random channels
- **COBs**:
  - **6-7%** of channels systematically masked (not the 37!, all in the digital-lines rows)
  - Less than 1% of random channels

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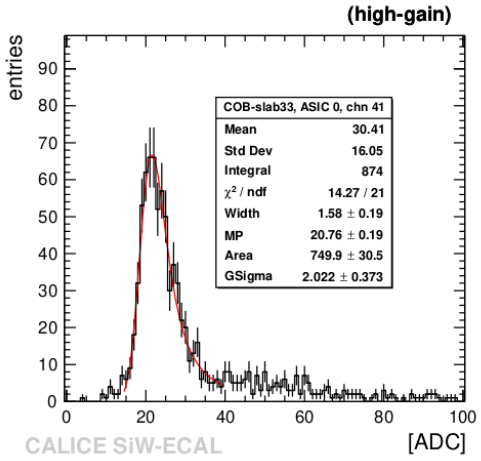
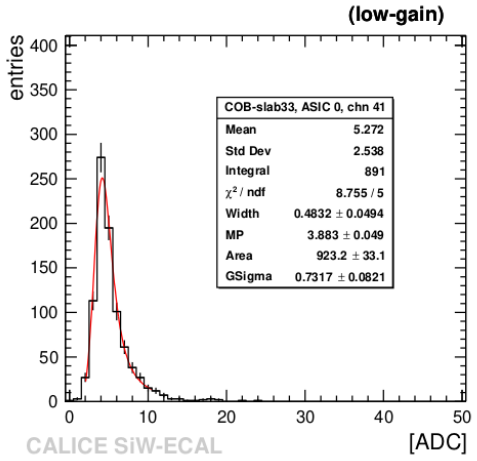
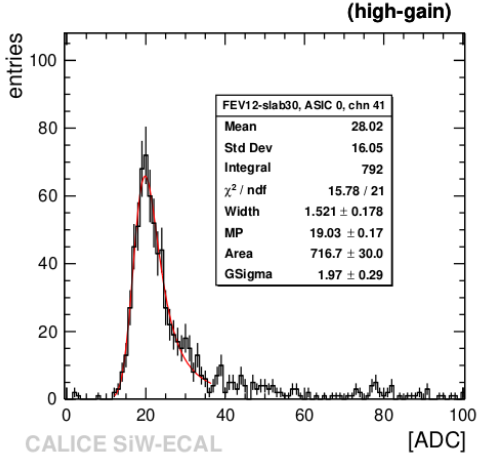
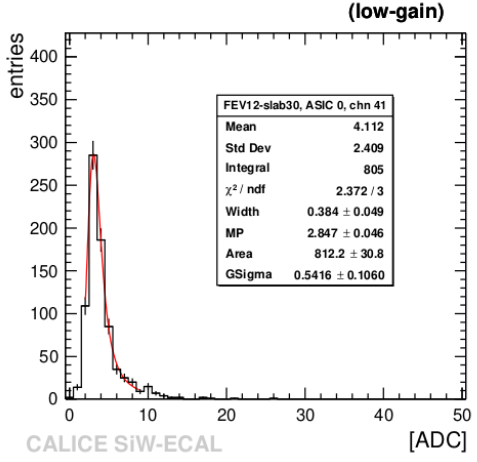
MIPs







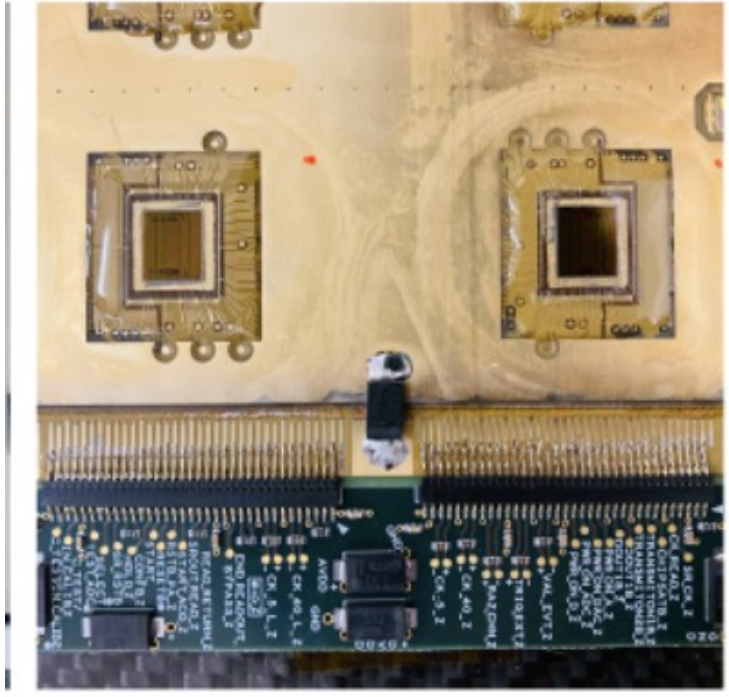


Id	ASU type	$< MIP_{HG} >$ [ADC]	$< MIP_{LG} >$ [ADC]
slab 38	FEV13	16.9 ± 1.3	2.7 ± 0.8
slab 39	FEV13	17.3 ± 1.3	2.8 ± 0.8
slab 29	COB	19.0 ± 1.1	3.2 ± 0.9
slab 30	FEV12	17.9 ± 1.0	2.9 ± 0.9
slab 33	COB	18.9 ± 1.6	3.0 ± 0.9
slab 31	FEV12	18.5 ± 1.1	2.9 ± 0.9

Table 3: Summary of devices under study and their average single cell MIP calibration values.

Summary

- Noise levels of the COB are similar to the other solutions.
  - Amount of decoupling capacitances seems crucial
- The systematically masked channels is larger
  - For all the PCBs, the digital sectors seem critic.
- Next generation of PCBs (FEV2.X) in BGA already existing.
  - Preliminary tests show promising prospects in terms of noise



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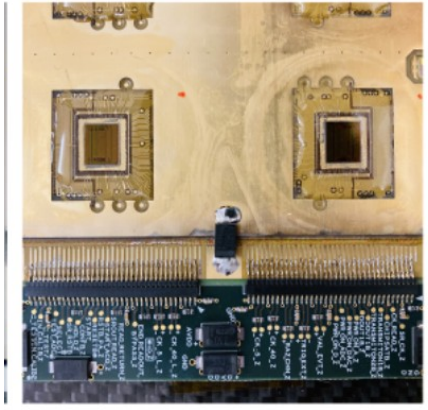

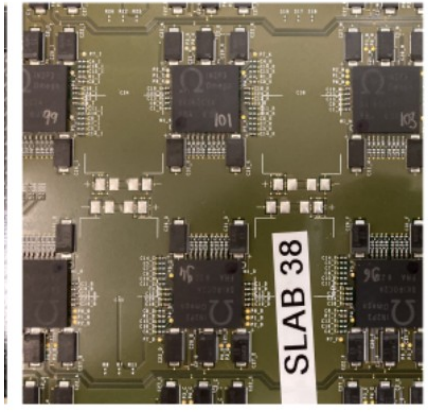

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Contribution of the coherent noise

$$R_{C1}(chn) = 1 - \frac{\sqrt{\sigma_I^2(chn) + \sigma_{C2}^2(chn)}}{\sqrt{\sigma_I^2(chn) + \sigma_{C1}^2(chn) + \sigma_{C2}^2(chn)}} \quad (2)$$

$$R_{C2}(chn) = 1 - \frac{\sqrt{\sigma_I^2(chn) + \sigma_{C1}^2(chn)}}{\sqrt{\sigma_I^2(chn) + \sigma_{C1}^2(chn) + \sigma_{C2}^2(chn)}} \quad (3)$$

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Contribution of the coherent noise

$$R_{C1}(chn) = 1 - \frac{\sqrt{\sigma_I^2(chn) + \sigma_{C2}^2(chn)}}{\sqrt{\sigma_I^2(chn) + \sigma_{C1}^2(chn) + \sigma_{C2}^2(chn)}} \quad (2)$$

$$R_{C2}(chn) = 1 - \frac{\sqrt{\sigma_I^2(chn) + \sigma_{C1}^2(chn)}}{\sqrt{\sigma_I^2(chn) + \sigma_{C1}^2(chn) + \sigma_{C2}^2(chn)}} \quad (3)$$

Id	ASU type	$< noise >_{HG}$ [ADC]	$< noise >_{LG}$ [ADC]	$< R_{C1,HG} >$ [%]	$< R_{C2,HG} >$ [%]	$< R_{C1,LG} >$ [%]	$< R_{C2,LG} >$ [%]
slab 38	FEV13	1.32 ± 0.06	0.74 ± 0.02	4 ± 1	2 ± 1	7 ± 1	$\leq 1 \pm 1$
slab 39	FEV13	1.35 ± 0.07	0.77 ± 0.03	5 ± 1	2 ± 1	9 ± 1	$\leq 1 \pm 1$
slab 29	COB	1.44 ± 0.06	0.74 ± 0.02	5 ± 2	2 ± 1	6 ± 1	$\leq 1 \pm 1$
slab 30	FEV12	1.37 ± 0.06	0.75 ± 0.04	5 ± 1	3 ± 1	8 ± 2	$\leq 1 \pm 2$
slab 33	COB	1.45 ± 0.09	0.74 ± 0.02	6 ± 2	2 ± 1	6 ± 1	$\leq 1 \pm 1$
slab 31	FEV12	1.36 ± 0.08	0.76 ± 0.03	5 ± 2	2 ± 1	8 ± 2	$\leq 1 \pm 1$

Table 2: Summary of devices under study and their noise parameters. Column by column: ID; ASU type; average measured noise values for the *high-gain* and *low-gain* branches; the relative contribution of the coherent noise sources 1 and 2.