LLRF & Controls
Cold Copper Collider Workshop

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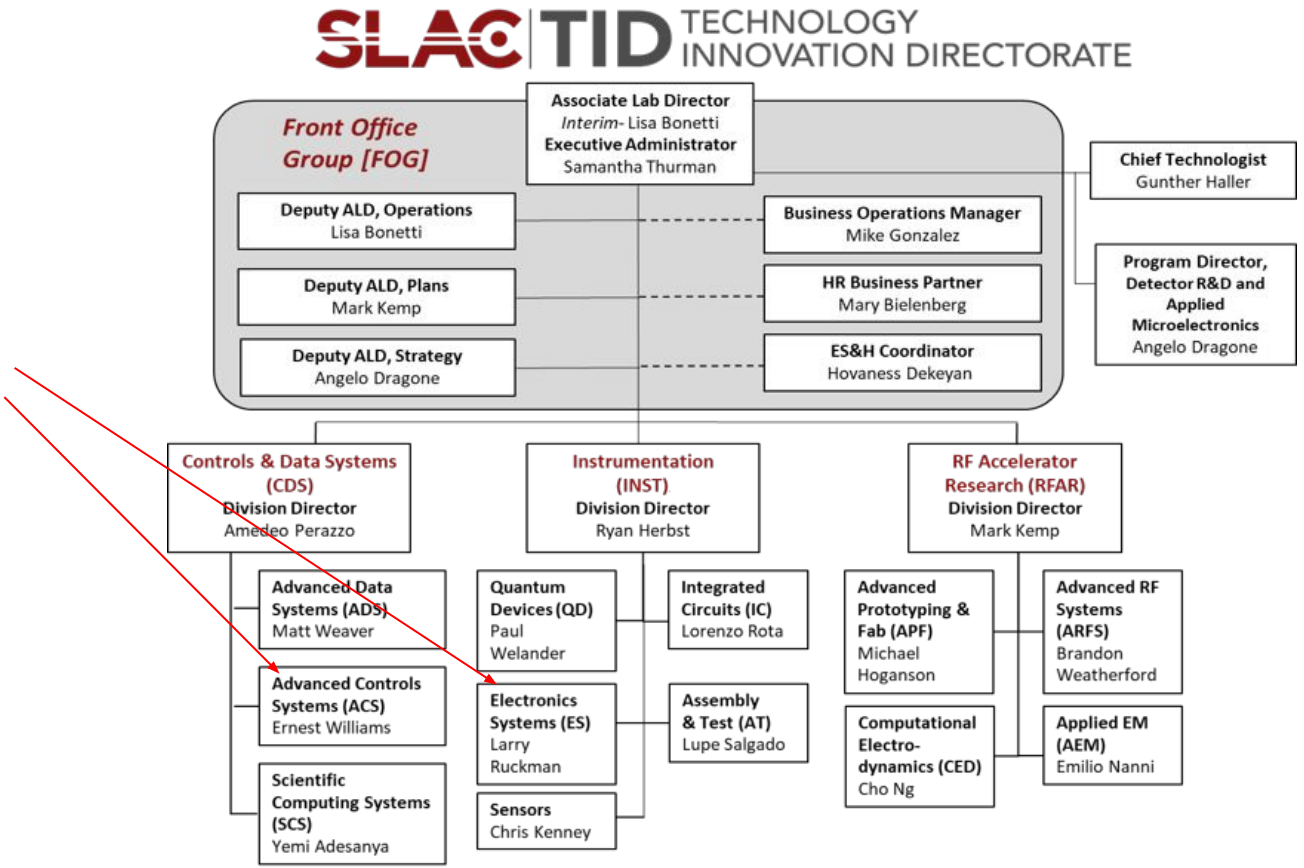
Outline

- TID Structure
  - Platforms Choices
- History Of Controls Development For LCLS2
  - ATCA Platform
  - Firmware/Software Modular CO-Design
  - Common Platform Software
  - LLRF Specific
- DARPA Accell LLRF Development
  - Requirements
  - Next Generation RFSOC Platform
  - Firmware / Software Structure
- Conclusions

TID Overview

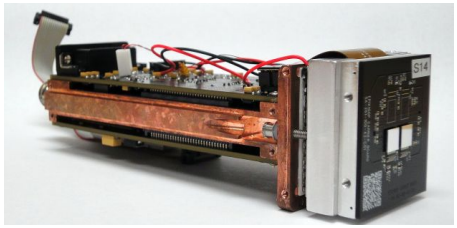
Controls Hardware / Firmware & Software Teams



TID ID & CDS Deliver A Variety Of Platforms

Crate based solutions

- Advanced Telecommunications Computing Architecture (ATCA)
  - Growing multi-billion dollar market
- Backplane carries all global signals
- 1-14 slot crates available.

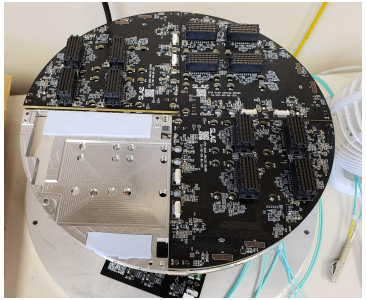


"Pizza Boxes"

- Network attached devices. (BPM)

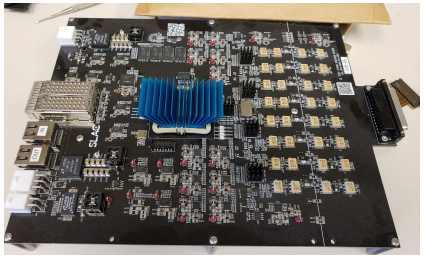
Embedded systems

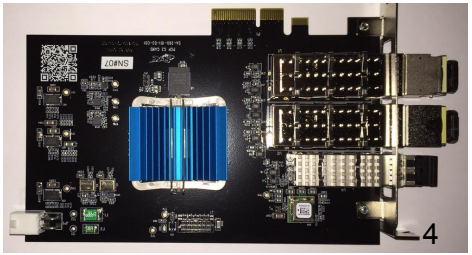
- Supports stand-alone / embedded cards
- Commercial and custom cards available.



Custom Detectors

- In vacuum detectors for LCLS.



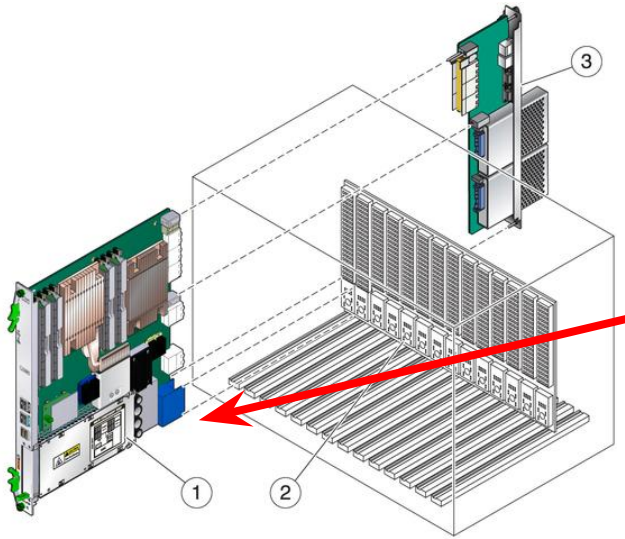


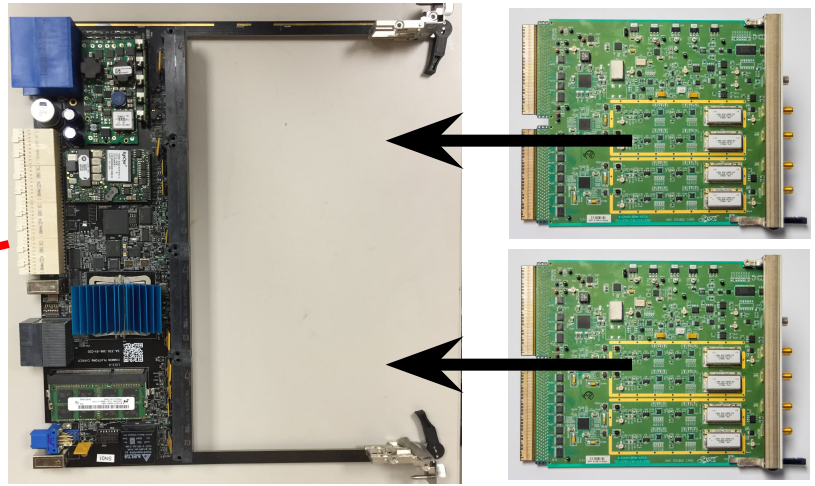
LCLS2 Controls
High Performance Systems (HPS)

SLAC

- HPS supports the following sub-systems for LCLS2
  - Timing
    - Per bunch experimental timing
    - Precision laser locker timing
    - Phase Reference Line distribution
  - Machine Protection System (MPS)
  - Beam Position Monitor System (BPM)
  - Bunch Charge Monitor System (BCM)
  - Bunch Length Monitor System (BLM)
  - LLRF Demonstration System
- Process 1Mhz beamline data in realtime firmware

ATCA Common Controls Platform
LCLS1 / LCLS2 / FACET

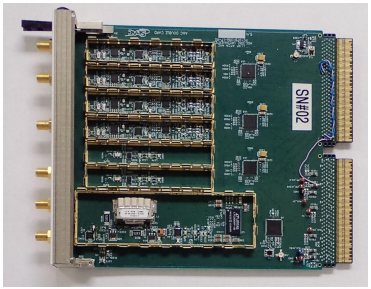




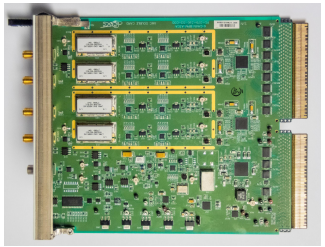
1: Carrier Card
2: Crate
3: RTM
Each carrier supports 2 AMC application cards

- **Carrier card**: FPGA, memory, backplane connections
- **AMC cards**: ADCs, DACs, high performance front end electronics
- **RTM**: General purpose IO, extra networks, miscellaneous

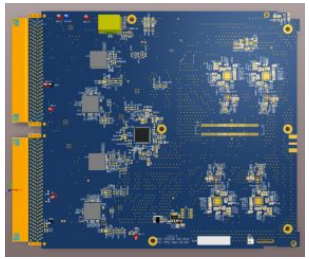
LCLS / LCLS2 / FACET Control Hardware



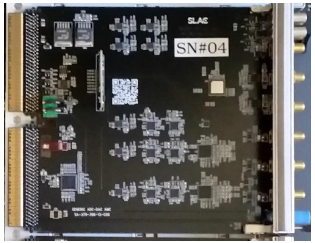
LLRF Up/Down Convert



LCSL-2 BPM board

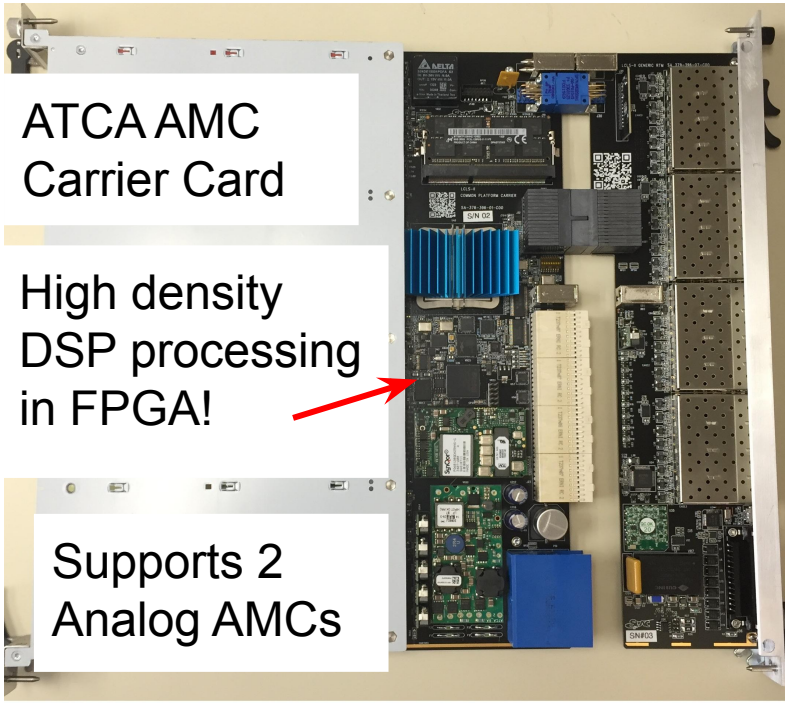


TES detector
RF board
4000 channels



Generic ADC/DAC
For machine
protection sys.

ATCA provides the space, power & cooling required for LCLS-2!



ATCA AMC
Carrier Card

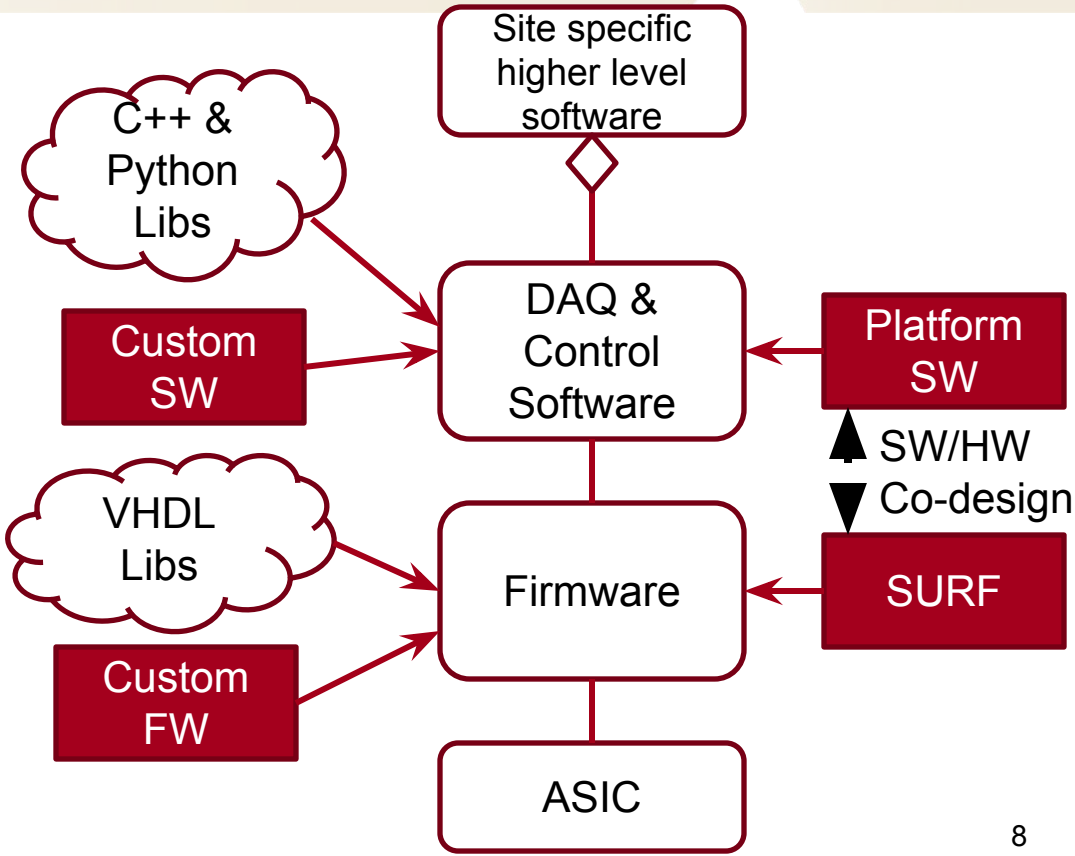
High density
DSP processing
in FPGA!

Supports 2
Analog AMCs

10/40Gbps Ethernet Backplane

Maximize Firmware / Software Reuse With Common Building Blocks With Standard Interconnects

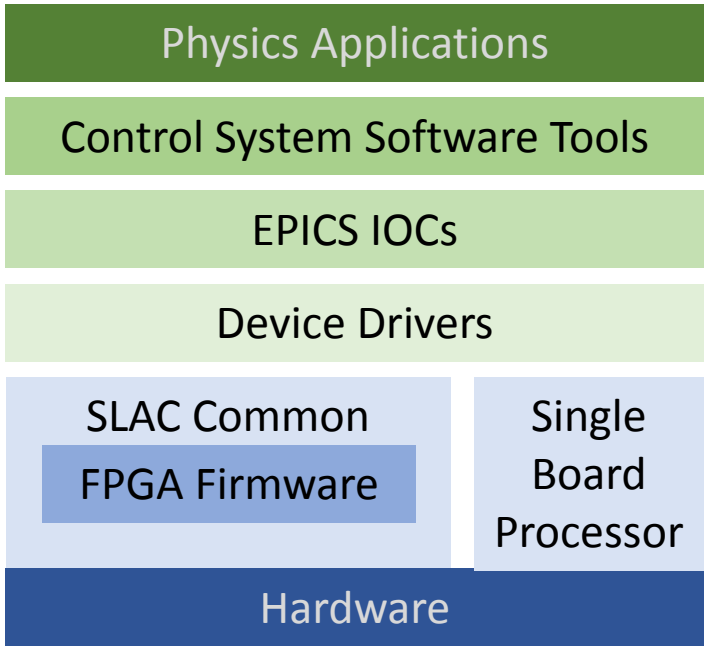
- Platform Software
  - Python/C++ framework to deploy custom DAQ systems
  - Enables register level and stream communication
  - Enables remote control
- Surf
  - VHDL firmware library
  - Contains a library of protocols, device access and commonly used modules
- Software and Firmware are tightly integrated providing firmware/software parallel development
  - Application firmware in HLS, System Generator, etc



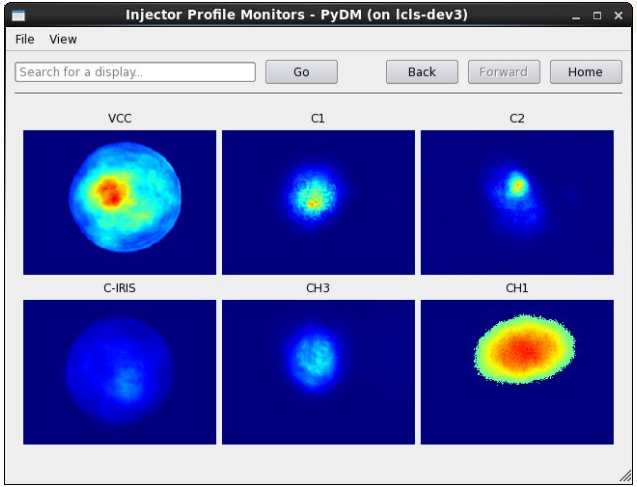
Common Platform Software

Integration with higher level DAQ and slow-control systems at experiment facilities, allowing application specific plugins to be developed and added to our software platform.

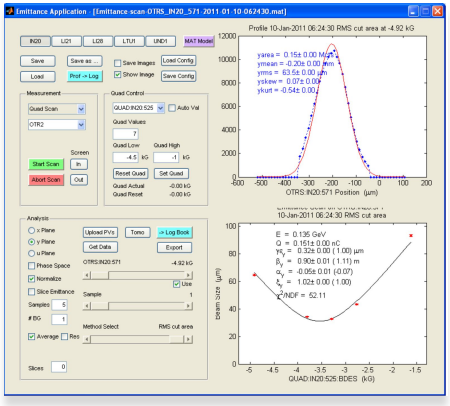
- Can be embedded into any C++ application
  - For Heavy Photon Search (JLAB) we integrated into CODA
  - LCLS2 DAQ integration
- Interface libraries for a variety of controls platforms
  - EPICS PV access layer
  - Karabo (EuXFEL) Python API auto generation
  - Fermilab ARTDAQ
  - Ignition controls platform for LZ
- Variety of interfaces
  - Shared memory interface for key/value pair access
  - Mysql mirror for key/value monitoring and control
  - ZeroMq based socket control in development
- Easy early testing and standalone debug
  - Python command line scripting
  - Auto generated GUI
- No assumptions made about higher level software choice!

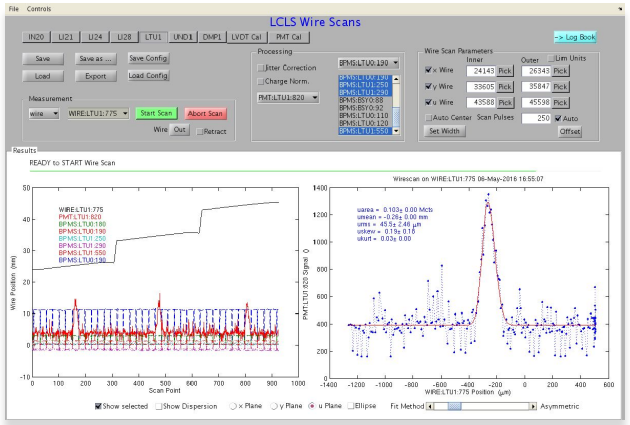


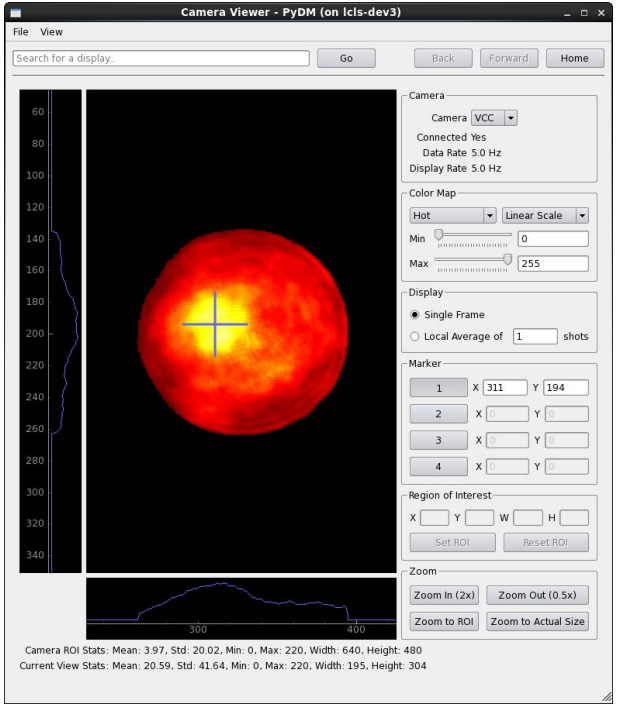
Accelerator Controls High Level Applications



High Level Physics applications diagnose and optimise the accelerator, combining model, geometry, PV names and PV values.

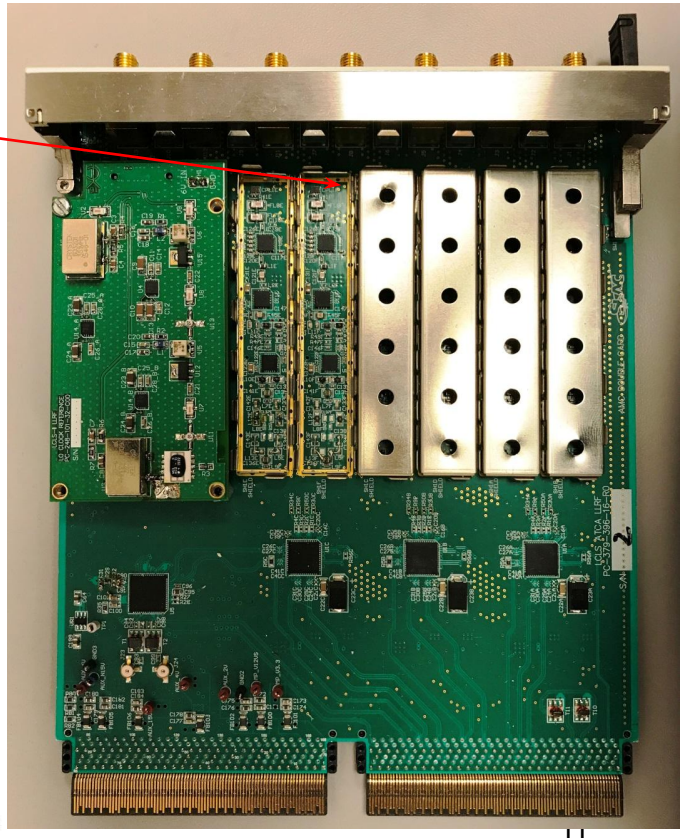


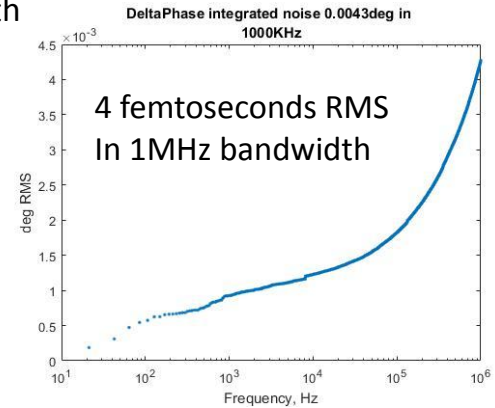




LCLS / FACET Low Level RF Controller

- 2 AMC cards on a single carrier
  - (receiver shown).
- 10X RF input channels
- 1X RF output channel
- 2X fast DC ADC (370Ms/s)
- 300MHz to 3GHz range with different oscillator daughter cards
- Clocks and LO phase locked to timing reference system.
- FPGA provides closed loop RF control.
- Very low measurement noise
  - 4.3 femtoseconds RMS in 1MHz bandwidth
  - 1 femtosecond RMS in 1KHz bandwidth
- **Status**: Operational on LCLS LINAC





DARPA ACCEL LLRF System Requirements

- Mechanical: Physically compact and noise resistant
- RF Frequency: 5712 MHz
- Number of klystrons: 26 (52 cavities)
  - 1 buncher
- LLRF channels per klystron
  - 1X 300W (target 1KW) drive
  - 2X receivers: forward from klystron and reflected from dual cavities
- LLRF pulse length: <= 5 microseconds (1 expected)
- LLRF pulse repetition rate <= 60Hz
- LLRF stability <1°, <1% variation RMS shot to shot
- LLRF pulse shaping: Arbitrary I/Q modulation with BW > 10MHz

Next Generation Hardware (RFSOC)

Example commercial RFSoC board: Pentek Quartz 6003

- 2.5x4 inches
- Includes 16Gbyte DRAM
- Similar boards available from other manufacturers

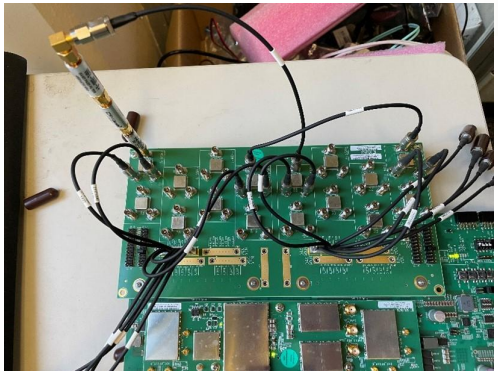
RFSoC integrates full digital radio system on a chip

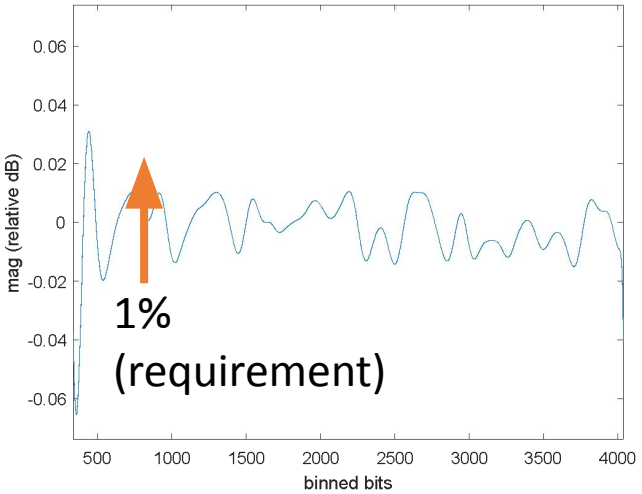
- 8X 5Gs/s 14 bit ADC, 6GHz analog bandwidth
- 8X 10Gs/s 14 bit DAC 6GHz analog bandwidth
- Programmable logic >4700 DSP slices
- CPU: quad core ARM processor + Dual core real time ARM processor
- Memory management, system management, high speed serial, etc.
- Everything needed for a LLRF system on a single chip!
- Allows for direct sampling without external analog up and down converters

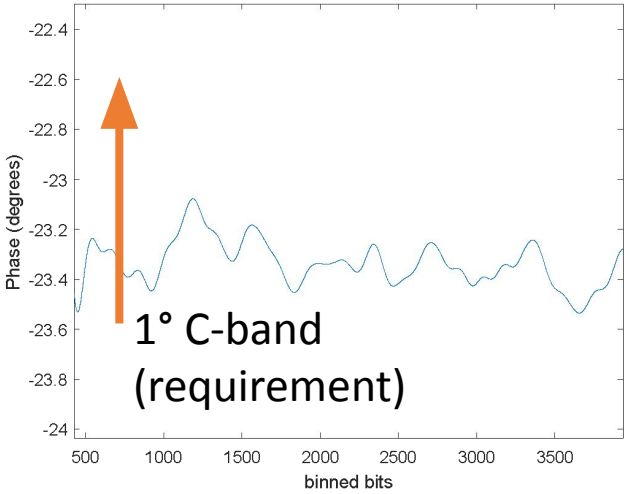
Note that initial testing can be done with Xilinx evaluation boards.

- Lower cost, simpler electrical / mechanical interface
- Code can easily be ported to compact boards

RFSOC Performance Testing







Evaluation board tested at SLAC

Xilinx Gen3 RFSoC board

- DAC operate in 2nd Nyquist band
- ADC operated in 5th Nyquist band

Amplitude noise measurement

1 microsecond loopback test

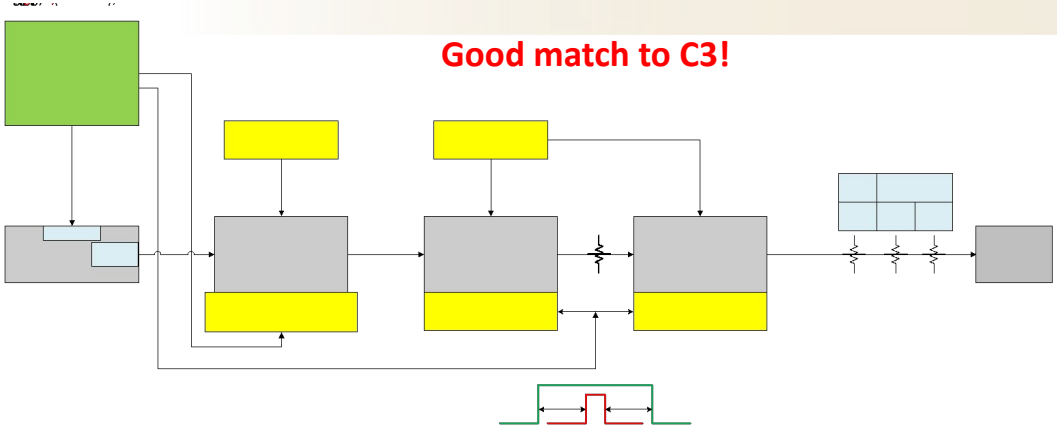
- RMS amplitude variation during pulse and pulse to pulse meets requirements

Phase noise measurement

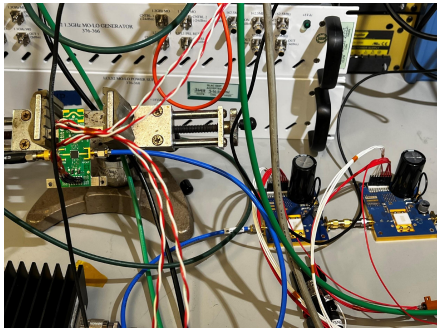
1 microsecond loopback test

- RMS phase variation during pulse and pulse to pulse meets requirements

DARPA ACCEL Solid State Amplifier



Good match to C3!



GaN Amplifier

Wolfspeed CGHV59350

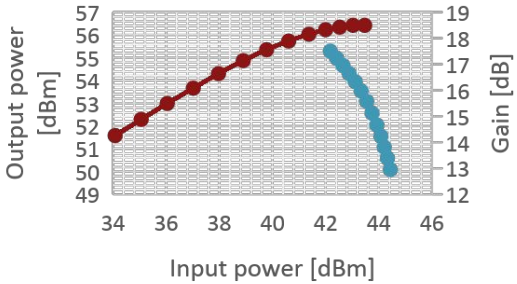
- 5.2-5.9GHz, 350W pulsed output
- 11dB gain
- 50V drain voltage

Tested at SLAC

400W output power measured

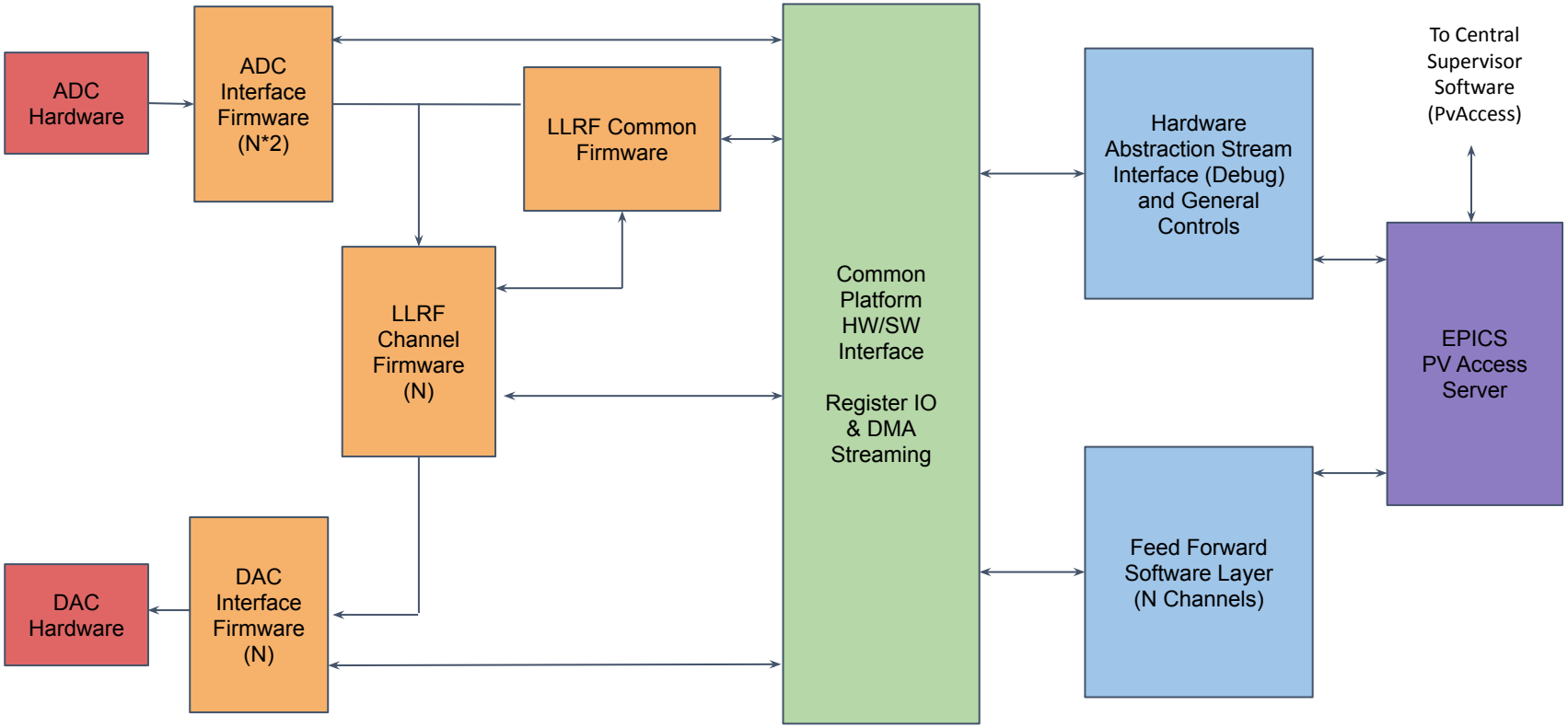
- 1 microsecond pulse
- Integrated board under development

Output power from the last stage amp



Measured Performance: 400W

DARPA ACCEL LLRF Firmware / Software



C3 LLRF System Requirements

- RF Frequency: 5712 MHz
- Number of klystrons: 18
  - 4 S-Band bunchers
- LLRF channels per klystron
  - 1 drive 300W (target 1KW) drive
  - 2X receivers: forward and reflected
- LLRF pulse length: <= 5 microseconds (1 expected)
- LLRF pulse repetition rate <= 60Hz (demonstrator)
- LLRF stability <1°, <1% variation RMS shot to shot
- LLRF pulse shaping: Arbitrary I/Q modulation with BW > 10MHz

- Good match to existing DARPA ACCEL requirements

Conclusions

- Goals for demonstrator are to use existing hardware, firmware & software as much as possible
  - Designs will be optimized for full accelerator post demonstrator

- TID has a LLRF solution compatible with C3 demonstrator requirements
  - RFSOC based LLRF design deployed for DARPA ACCEL meets C3 requirements

- We have both hardware and a framework for controls hardware & software
  - Team is ready to collaborate on requirements and both short term and long term controls & LLRF solutions