(fast) MAPS developments

C^3 workshop

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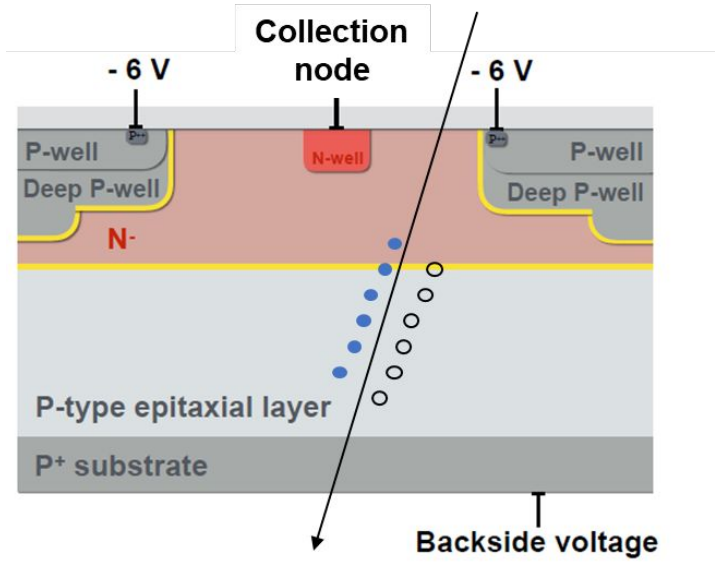
MAPS

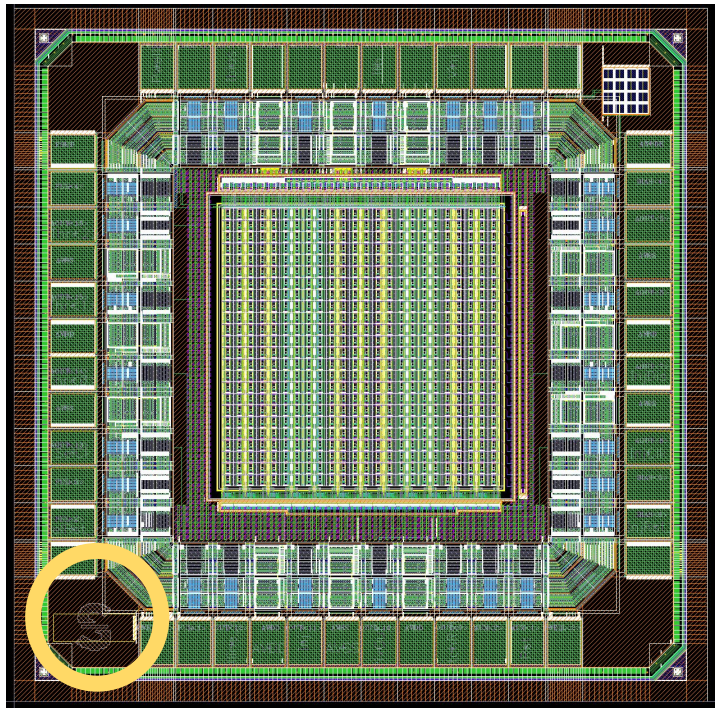
Monolithic Active Pixel Sensors (MAPS) for high precision tracker and high granularity calorimetry

- Monolithic technologies have the potential for providing higher granularity, thinner, intelligent detectors at lower overall cost.
- Significantly lower material budget: sensors and readout electronics are integrated on the same chip
  - Eliminate the need for bump bonding : thinned to less than 100µm
  - Smaller pixel size, not limited by bump bonding
  - Lower costs : implemented in standard commercial CMOS processes



Existing efforts

- The CERN WP1.2 collaboration is investigating the possibility of realizing wafer-scale MAPS devices on the novel TowerSemi 65 nm CMOS imaging process.
  - Increased density for circuits
  - Higher spatial resolution
  - Better timing performance
  - Lower power consumption.
- SLAC is participating in CERN WP 1.2
  - Shared submission with a SLAC prototype on-going
  - With LDRD funds, we will focus in the future on the development of fast MAPS with **improved timing resolution**



Layout of MAPS SLAC prototype for WP1.2 shared submission

Why FAST MAPS?

The detectors at future e^+e^- machines will need unprecedented precision on Higgs & SM physics measurements.

- These ambitious physics goals translate into very challenging detector requirements on tracking and calorimetry.
- High precision and low mass trackers, as well as highly granular calorimeters, will be critical
  - O(ns) timing capabilities are key to suppress beam induced backgrounds

Monolithic Active Pixel Sensors (MAPS), which combine the sensing element and readout electronics on the same device, are a key technology to further reduce dead material

State-of-the-art MAPS can achieve ~µsec timing resolution - our plan is to achieve simultaneously:

- **improved timing resolution by an order of magnitude beyond the state-of-the art**
- **low power consumption compatible with large area and low material budget constraints**

Fast MAPS: challenges

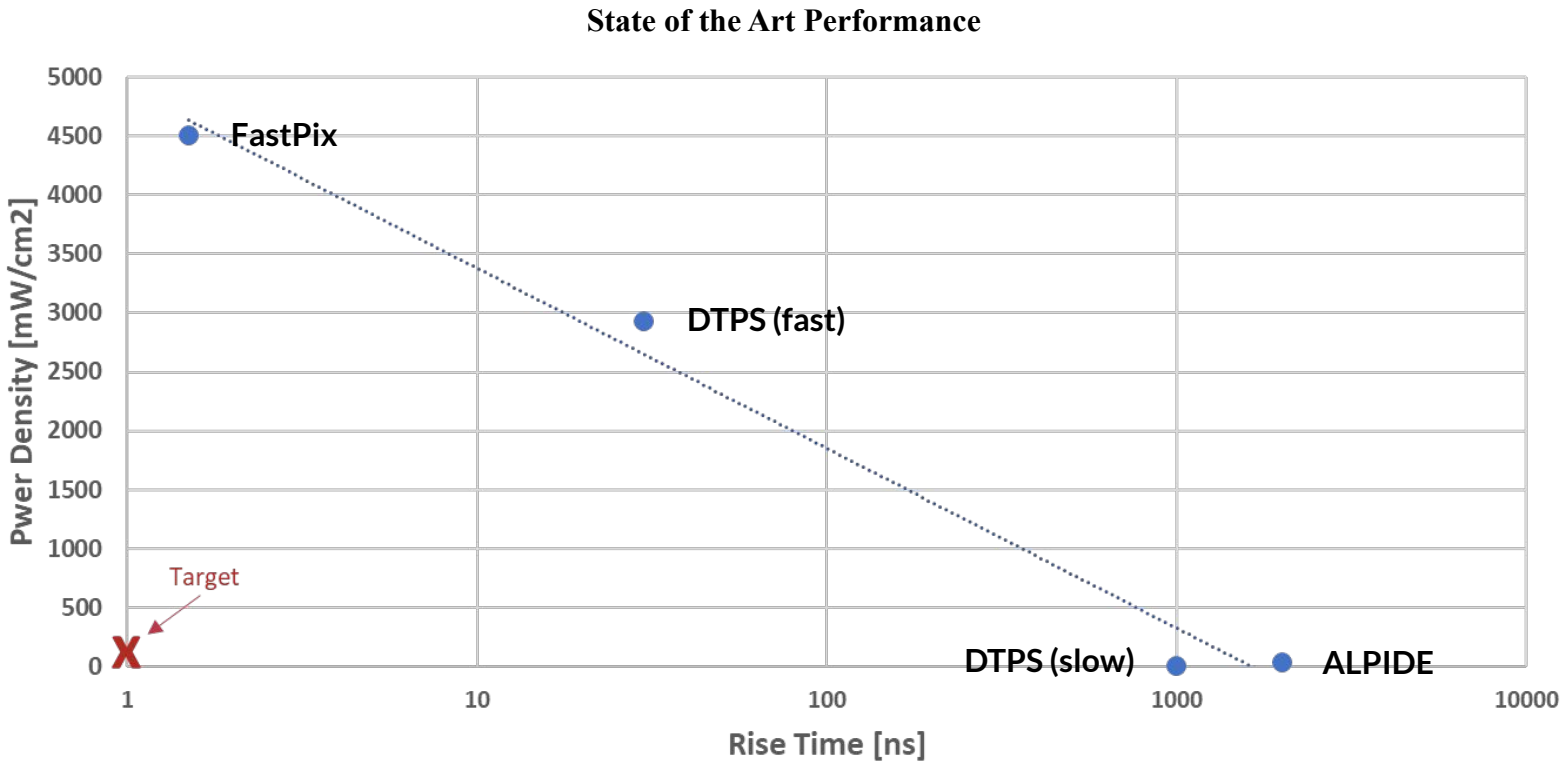
Achieving ns timing while maintaining low-power consumption requires a dedicated strategy

- One major design challenge for MAPS is achieving fast timing while maintaining low-power consumption
  - The average power consumption must be minimized to permit gas cooling, as well as to minimize the voltage drop over long metal lines.
- Three main strategies will be investigated :
  - **Power pulsing scheme**: the analog front-end circuitry will be powered off during the dead-time between different bunch trains, thus reducing the average power consumption.
    - With low duty cycle machines this technique enables a power reduction by more than two orders of magnitude - leveraging the experience with KPiX
  - **Front-end architecture timed with the accelerator**
    - the noise and timing performance of the circuitry can be optimized while maintaining low-power consumption - leveraging ASICs developed for LCLS
  - **Sparse asynchronous readout**

State-of-the-art & our target

Initial specifications for fast MAPS

Parameter	Value
Sensitive thickness	10 µm
Time resolution	1 ns
Minimum Threshold	200 e-
Noise	30 e-
Maximum particle rate	1000 hits/cm^2
Power density	20 mW/cm^2
Spatial Resolution	7 µm



AISC	Technology	Rise time [ns]	Power density [mW/cm2]
FastPix	TJ 180	1.5	4500
DTPS(Fast)	TJ 65	30	2933
DTPS(Slow)	TJ 65	1000	6.4
ALPIDE	TJ 180	2000	40

All chips developed by CERN, all in prototype phase except ALPIDE

Our approach

Challenges

Low power consumption is essential to allow :

- Large active area design (~10x10 cm^2)
- Compatibility with gas cooling

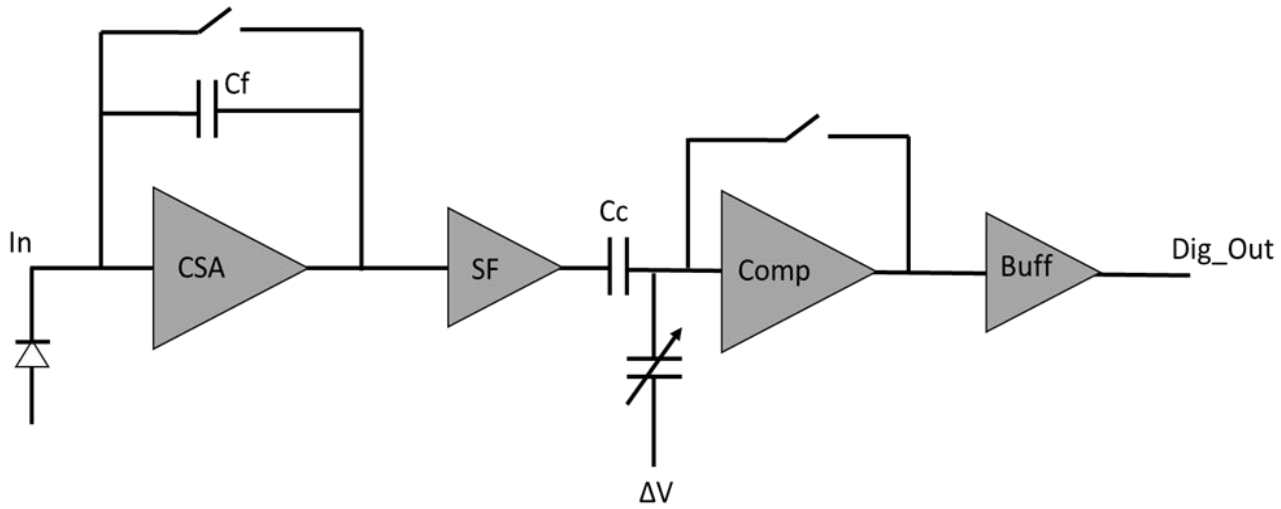
To be able to achieve fast timing while maintaining low power consumption the design must include:

- Power pulsing scheme: the analog front-end circuitry will be powered off during the dead-time between different bunch trains, thus reducing the average power consumption.
- Asynchronous sparse readout: No clock distribution across matrix

SLAC will leverage a decade of expertise with synchronous readout architectures operating with fast integration times

Approach

Possible Architecture for the Front-end with Power Pulsing



Key elements

- Charge Sensitive Amplifier (CSA) with a synchronous reset, which can be powered down during inactive time
- A comparator with auto-zero technique, removing the need for per-pixel threshold calibration
- A fast buffer to transmit the 'hit' information to the circuit periphery (balcony)

Approach

Time Encoding

As clock distribution along the matrix is not feasible, therefore, possible solutions are that each pixel:

- encodes the timing information as an analog signal, which is then converted to digital at the periphery.
- transmits a very fast 'Hit' signal to the periphery where a Time-to-Digital Converter (TDC) is implemented

Prototyping

- The study of the feasibility of the main ideas will be implemented in TowerJazz 65nm technology.
- Two small prototypes of 5 mm x 5 mm will be fabricated through a shared submission with CERN's WP 1.2
- The prototypes will be mounted on carrier boards and characterized at SLAC
- Timing performance will be evaluated with calibration electrical signals, pico-second laser infrared source or with a pulsed X-ray source. Further tests can be done with an electron test-beam

Collaborations and perspectives

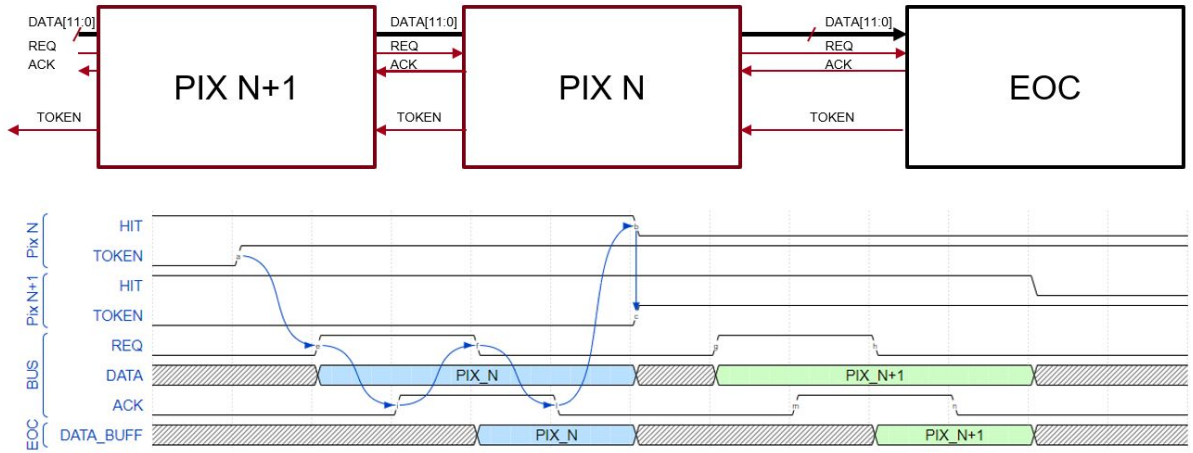
- Fast timing MAPS are of interest to many scientific collaborations, especially within the HEP community.
- SLAC has an established collaboration with CERN, in particular the WP1.2 where a shared effort can be imagined in the development of fast MAPS.
  - Leverage SLAC-CERN collaboration to deepen our core competencies in MAPS detectors, which will have an impact across different directorates:
  - Fast MAPS can be of interest for ultra-fast X-ray science: *e.g.*, next-gen ePixM and SparkPix-T
- The know-how developed for this project will benefit other HEP/BES applications requiring low-power designs, fast inter-pixel communications, synchronous architectures, *etc.*

Backup

Approach

Asynchronous Sparse Readout

- Most timing circuits rely on time stamping within the pixel. This requires a fast clock distribution along the matrix, yielding a high-power consumption beyond our target consumption budget.
- Therefore, we will investigate the performance of a sparse asynchronous readout: only pixels containing a hit will transmit hit information to the circuits located in the periphery.
- A possible implementation consists in a 'hand-shaking' protocol where each pixel is only communicating with the neighboring allowing an efficient and fast communication with the EoC circuitry.



A similar architecture has been successfully implemented for the SparkPix-T (Tixel) ASIC developed at SLAC

Beam Format and Detector Design Requirements

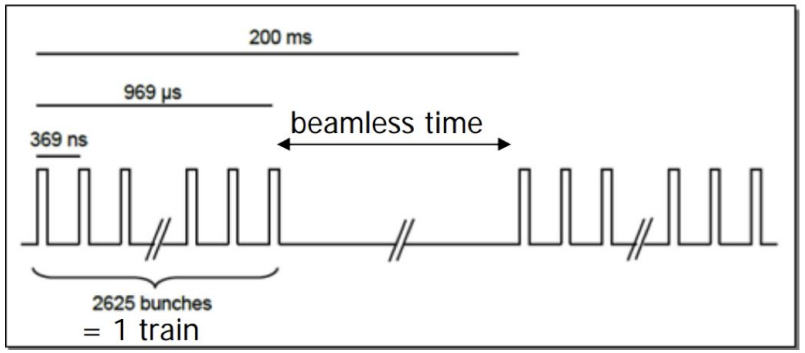
ILC timing structure: Fraction of a percent duty cycle

- **Power pulsing possible**, significantly reduce heat load
  - Factor of 50-100 power saving for FE analog power
- Tracking detectors **don't need active cooling**
  - Significantly reduction for the material budget
- **Triggerless readout** is the baseline

Collider	ILC	CCC
σ_z	300 μm	100 μm
β_x	8.0 mm	13 mm
β_y	0.41 mm	0.1 mm
ϵ_x	500 nm/rad	900 nm/rad
ϵ_y	35 nm/rad	20 nm/rad
N bunches	1312	133
Repetition rate	5 Hz	120 Hz
Crossing angle	0.014	0.020
Crab angle	0.014/2	0.020/2

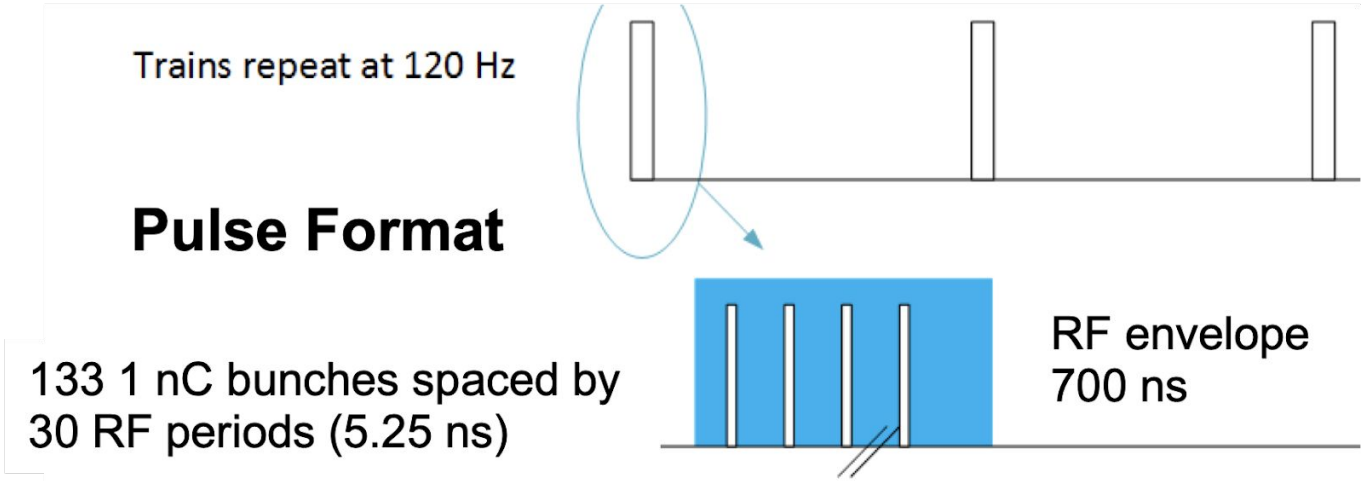
C^3 time structure is compatible with SiD-like detector overall design and ongoing optimizations

ILC timing structure



1 ms long bunch trains at 5 Hz
2820 bunches per train
308ns spacing

C^3 timing structure



Physics Requirements for detectors at e+e-

Need new generation of ultra low mass vertex detectors with dedicated sensor designs

- ZH process: Higgs recoil reconstructed from Z →μμ
  - Drives requirement on charged track momentum and jet resolutions
  - Sets need for high field magnets and high precision / low mass trackers
  - Bunch time structure allows high precision trackers with very low X0 at linear lepton colliders
- Higgs → bb/cc decays: Flavor tagging & quark charge tagging at unprecedented level
  - Drives requirement on charged track impact parameter resolution → low mass trackers near IP
  - <0.3% X0 per layer (ideally 0.1% X0) for vertex detector
  - Sensors will have to be less than 75 μm thick with at least 5 μm hit resolution (17-25μm pitch)