Instrumentation Frontier

U.S. DEPARTMENT OF ENERGY | Stanford University

SLAC NATIONAL ACCELERATOR LABORATORY

List of papers submitted to Snowmass

1	Searches for New Particles, Dark Matter, and Gravitational Waves with SRF Cavities	https://arxiv.org/abs/2203.12714	Zhou
2	Photon counting from the vacuum ultraviolet to the short wavelength infrared using semiconductor and superconducting technologies	https://arxiv.org/abs/2203.12542	Dragone, Shen, Turner, Rota, Kenney
3	Monolithic Active Pixel Sensors on CMOS technologies	https://arxiv.org/abs/2203.07626	Breidenbach, Vernieri, Dragone, Rota
4	4-Dimensional Trackers	https://arxiv.org/abs/2203.13900	Dragone, Markovic, Schwartzman
5	Innovations in trigger and data acquisition systems for next-generation physics facilities	https://arxiv.org/abs/2203.07620	Bartoldus, Bernius
6	Electronics for Fast Timing	https://arxiv.org/abs/2204.00149	Dragone, Markovic, Schwartzman
7	Recent Progress and Next Steps for the MATHUSLA LLP Detector	https://arxiv.org/abs/2203.08126	Ruckman, Russell, Xu, Young
8	Superconducting Sensor Fabrication Capabilities for HEP Science	https://arxiv.org/abs/2203.15978	Li
9	Enabling Capabilities for Infrastructure and Workforce in Electronics and ASICs	https://arxiv.org/abs/2204.07285	Dragone, Herbst, Rota
10	Smart sensors using artificial intelligence for on-detector electronics and ASICs	http://arxiv.org/abs/2204.13223	Doering, Dragone, Herbst, Rota, Ruckman
11	RF Electronics	https://arxiv.org/abs/2204.01809	Frisch
12	Cryogenics Readout	TBD	Shutt, Pena Perez, Gupta, Dragone, Kenney
13	Strange quark as a probe for new physics in the Higgs sector	https://arxiv.org/abs/2203.07535	Orrc, Su Dong, Schwartzman, Va'vra, Vernieri, Young

- **Motivation:** Skipper-CCD are fabricated with dedicated scientific CCD processes, but demand is low → foundries are disappearing
- **Goal:** implement a fast “Skipper detector” on a CMOS process with 1 kHz frame-rate for a wide range of applications
- **SLAC contribution:** development of a prototype of Skipper-in-CMOS (in collaboration with Fermilab, Centro Atomico Bariloche and TowerSemi)

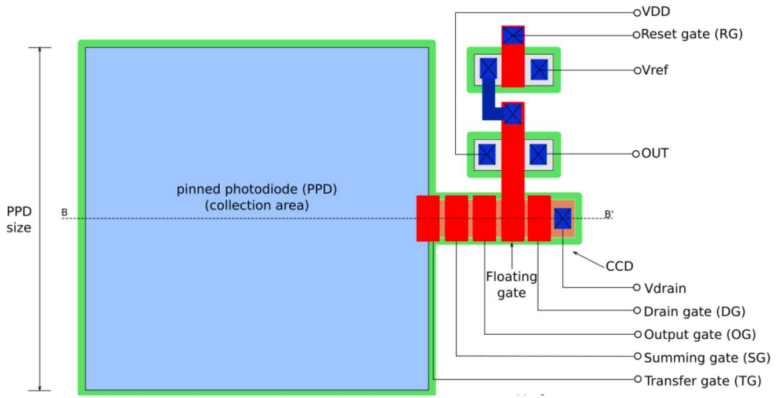


Figure 9: Pixel concept of the Skipper-CMOS imager.

Monolithic Active Pixel Sensors on CMOS technologies

- MAPS are one of the key technologies described in DOE's BRN for HEP
  - Reduce mass and interconnections
  - Remove expensive and delicate bump-bonding process
- **SLAC contribution:**
  - R&D efforts towards a wafer-scale MAPS on TowerJazz 65 nm
  - Design optimized for both tracker and EM calorimeter at future e+e- colliders
  - C^3 taken as example application for initial specifications

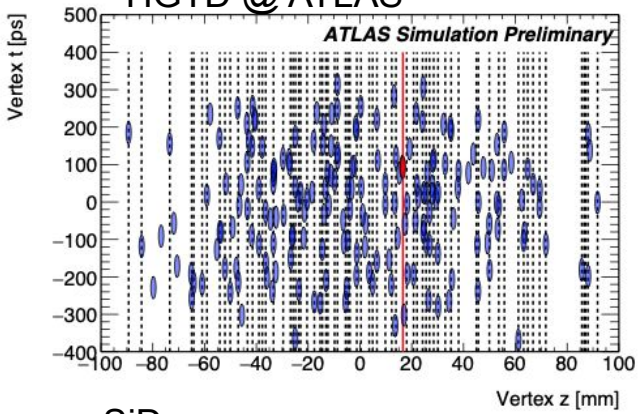
Parameter	Value
Min. Threshold	140 e^-
Spatial resolution	7 μm
Pixel size	25 x 100 μm^2
Chip size	10 x 10 cm^2
Chip thickness	300 μm
Timing resolution (pixel)	~ns
Total Ionizing Dose	100 kRads
Hit density / train	1000 hits / cm^2
Hits spatial distribution	Clusters
Power density	20 mW / cm^2

Table 1: Target specifications for 65 nm prototype.

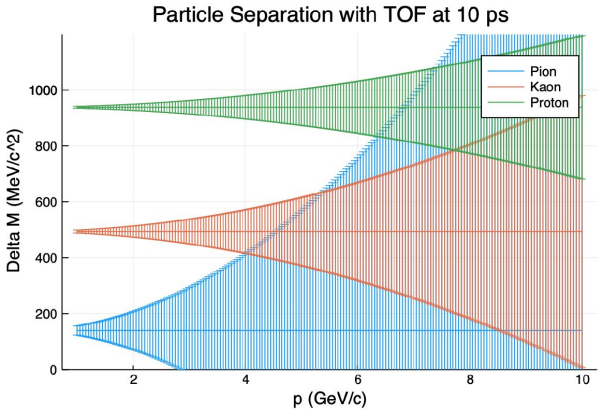
4-Dimensional Trackers

- Precision timing at 10-30ps levels will be transformative for detectors at future collider experiments:
  - Hadron colliders (Pileup suppression)
  - *e*+*e*− colliders (Time-of-Flight, Long Lived Particles, Calorimetry)
  - Muon collider (Beam Induced Background)
  - Electron Ion collider
- SLAC contributions:
  - Design of high-precision timing-electronics in 28nm CMOS technology
  - Physics case/performance and layout optimization

HGTD @ ATLAS



SiD



Electronics for Fast Timing

- Time resolutions shorter than track propagation or shower development times can give us insight into the characteristics of complex physics events beyond our current capabilities. This is enabled by:
  - rapid and continuous advance of fast electronics
  - ability to generate fast signals with good signal/noise from a variety of solid-state sensors, photodetectors, and micropattern gas-based detectors
- SLAC contribution:
  - Design of high-precision timing-electronics in 28nm CMOS technology

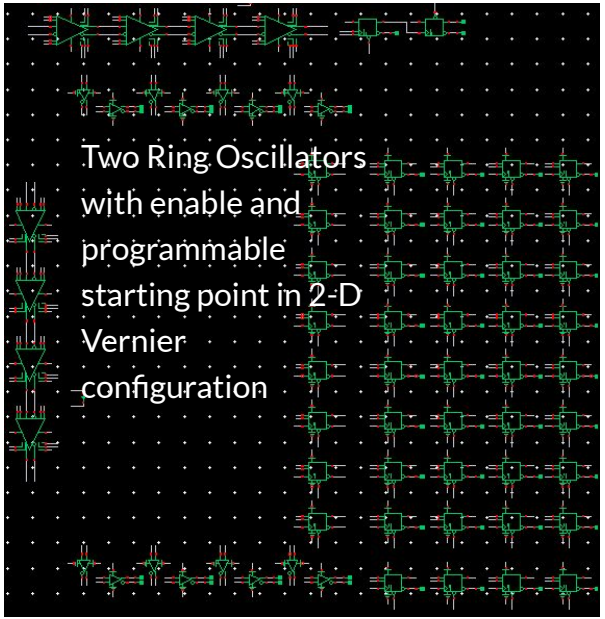
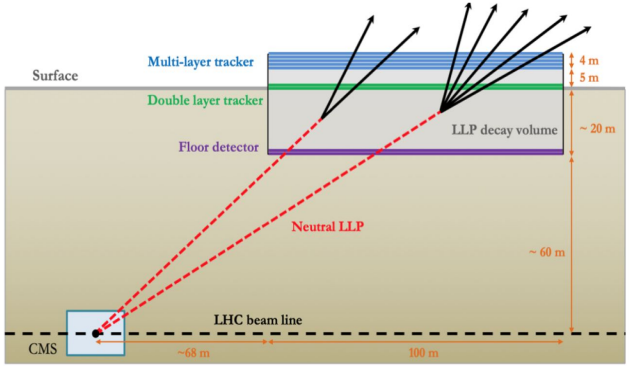
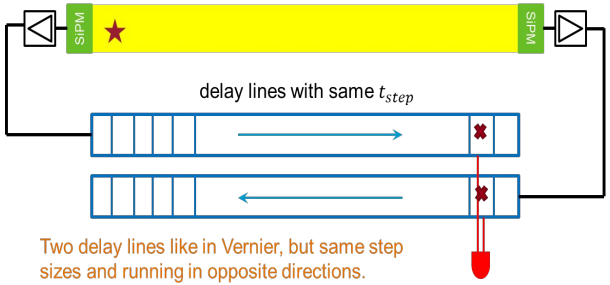


Figure: TDC design in 28nm CMOS technology

Recent Progress and Next Steps for the MATHUSLA LLP Detector

- MATHUSLA looking for very rare upward going tracks from CMS beam crossings (No existing solution)
- Readout and triggering of 10 layers of scintillator
  - Arranged in a 10x10 grid of 10m x 10m modules sitting 60m above CMS pit
- Preliminary latency study has been performed and a 9us latency budget required by the CMS trigger appears to be possible
- Next Steps …
  - Prototyping of 32-bar assembly with electronics
  - Develop the low latency FPGA-based vertex algorithm



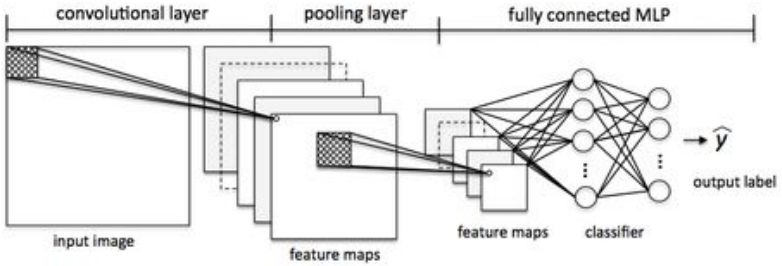


Front-end readout concept

Enabling Capabilities for Infrastructure and Workforce in Electronics and ASICs

- R&D challenges of future Instrumentation for HEP are at a scale requiring multi-institution teams in particular in the areas of Electronics (FPGA) and ASICs.
- Key needs:
  - shared infrastructure and organizational network
    - Access to affordable common tools and IPs
    - Legal framework to share databases (multi-institution NDAs)
  - development and retention of experts in academia, national laboratories, and the private sector
    - Traineeship programs to transfer specific domain knowledge to future generations of Instrumentation experts

Smart sensors using artificial intelligence for on-detector electronics and ASICs



Typical AI network consisting of feature extraction followed by classification.

Initial deployment will consist of PCIE based FPGAs, future advances will support ASIC hosted inference

Scientific Achievement

Enabling high rate/high bandwidth data processing as well as low latency feedback control systems by deploying AI inference engines in FPGAs and detector ASICs.

Significance and Impact

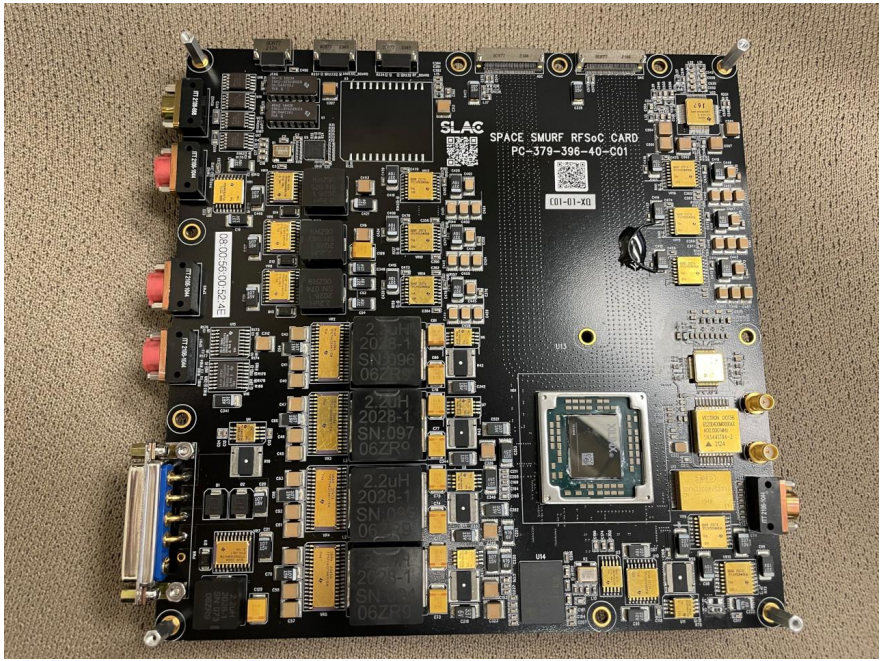
By deploying AI inference engines in FPGAs and ASICs the massive amount of data generated by high rate detectors sources can be processed early in the data pipeline, enabling rapid feature extraction, triggering and vetoing tasks which result in feedback of actionable information to experiments.

Research Details

- Develop a structured AI inference library in High-Level Synthesis (HLS)
- Explore the impacts of using lower precision (quantized) computations on latency and resource utilization
- Targeting AI networks with 10+ layers
- Support rapid redeployment of weights and biases, allowing for networks to adapt to changing experimental conditions.

RF Electronics

- Broad applicability of technology
  - Radio Telescopes
  - Accelerator controls / diagnostics
  - Cryogenic detector readout
  - Quantum systems
- Rapidly Developing Technology
  - XIlinx RF System on Chip
  - Improvements in performance, size, weight, power and cost
- Firmware / DSP development



Prototype space flight capable board based on RFSoC for cryogenic detector readout

Cryogenics Readout

- CRYO is a system-on-chip for charge readout in the nEXO experiment to enable the study of rare events such as neutrinoless double beta (0νββ) decay
  - Architecture with combined analog and digital functions including on-chip supply regulation to avoid external active components (low background)
  - Small chip size (7 mm x 9 mm) to meet radiopurity requirements and optimized to operate at 160K
- Dual-scale charge readout for fine-grained readout of liquid noble TPCs
  - Solution aimed for LAr TPCs that could be suitable for the 3rd & 4th DUNE modules and calibration of a galactic supernova (SN) signal in DUNE. Also, it would be ideal for measuring 0.1 – 10 MeV gamma rays (essentially an unexplored energy range in the sky)
- **SLAC contribution:**
  - Performance characterization of the CRYO ASIC in an LXe TPC setup
  - Design of the core cryogenic pixel-based ASIC with power cycling and low noise profile for fine-grained readout

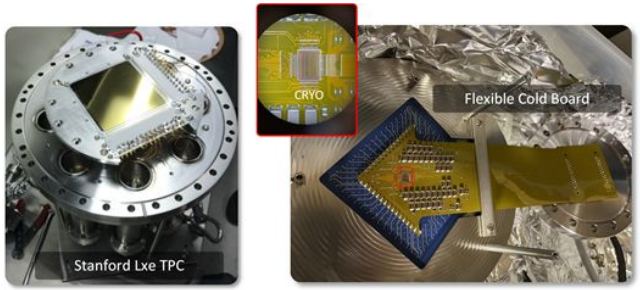


Figure: CRYO ASIC and the LXe TPC setup (under development)

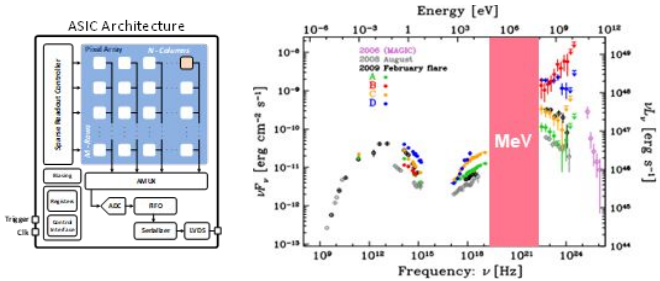


Figure: Pixel-based charge readout ASIC and gamma-ray range