Cryogenic Control and Readout Circuits

Shaorui Li

Outline

- Why do we use cryogenic circuits?

  → User cases: DUNE LAr TPC & IBM superconducting quantum computer

- How do transistors perform at cryogenic temperature?

  → Higher gain, lower noise, but worse matching and shorter lifetime

- How do we design cryogenic circuits?

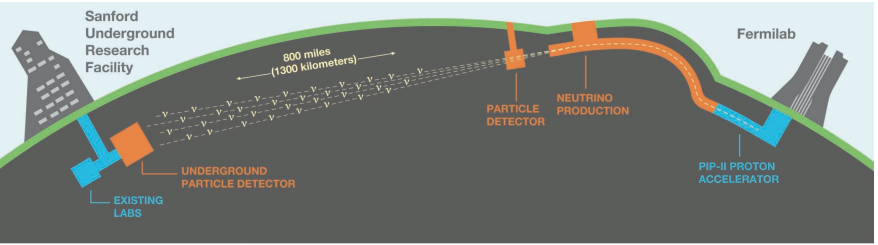
  → Optimize analog front-end for low noise in particle detectors

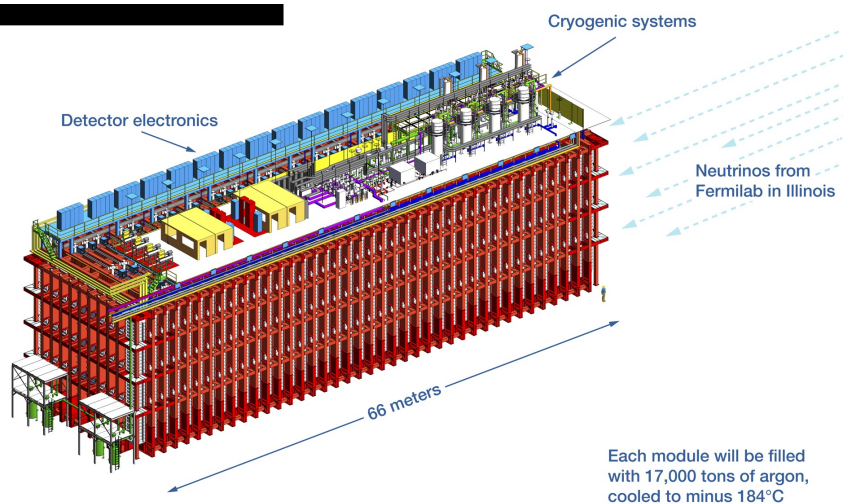
  → Optimize data converters for low power in quantum systems

It's the little details that are vital. Little things make big things happen.

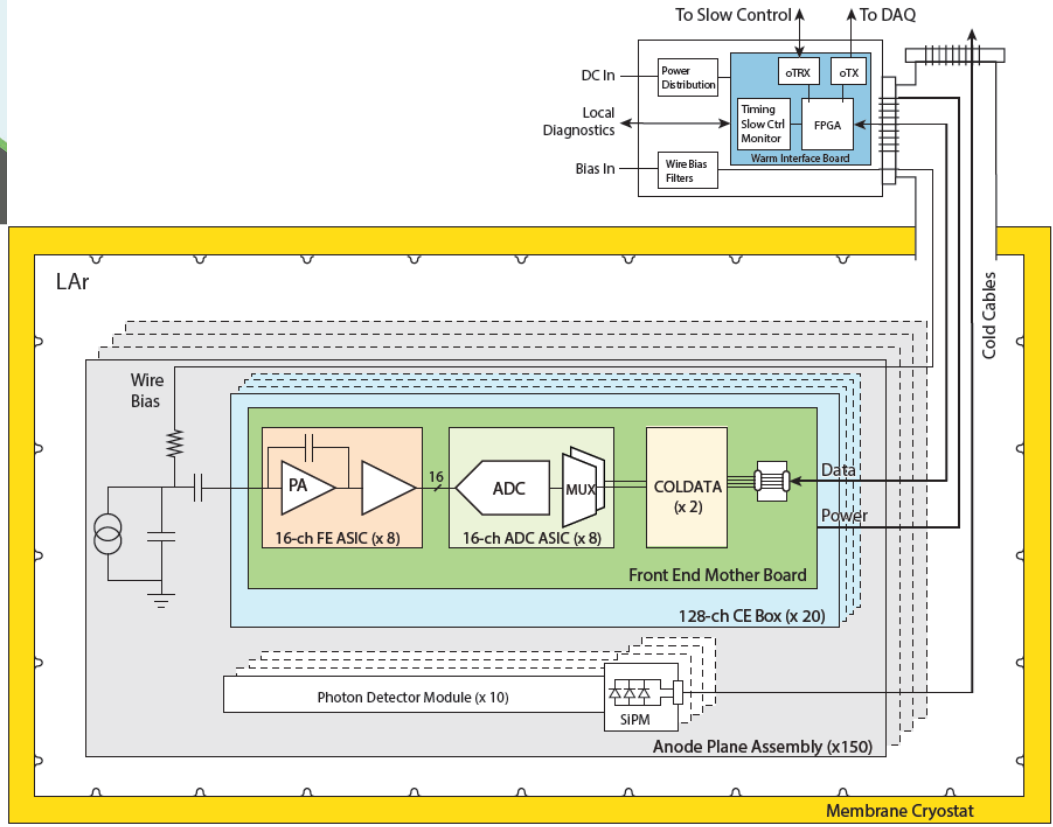
- John Wooden

A Readout Scheme of DUNE LAr TPC





Each module will be filled with 17,000 tons of argon, cooled to minus 184°C



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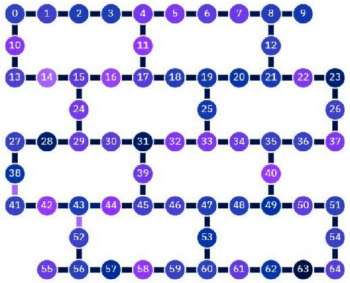
IBM Superconducting Quantum System



Zettles et al. (IBM), ISSCC 2022

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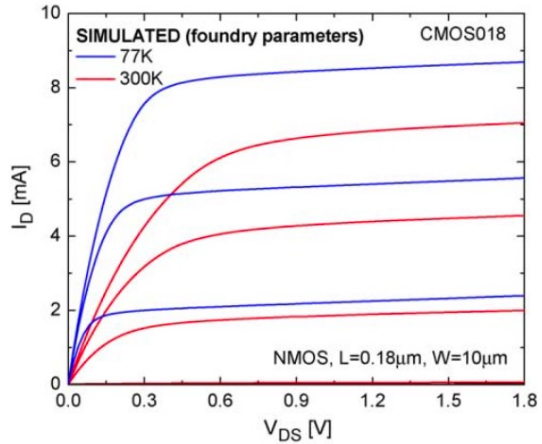
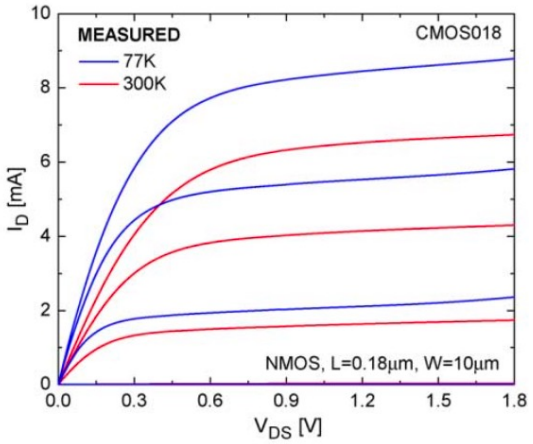
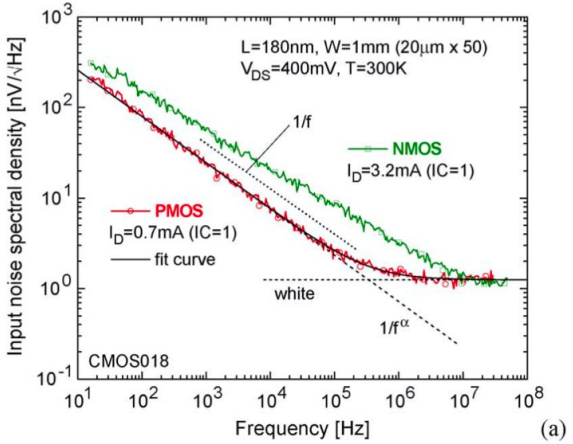
Design Considerations and Constraints

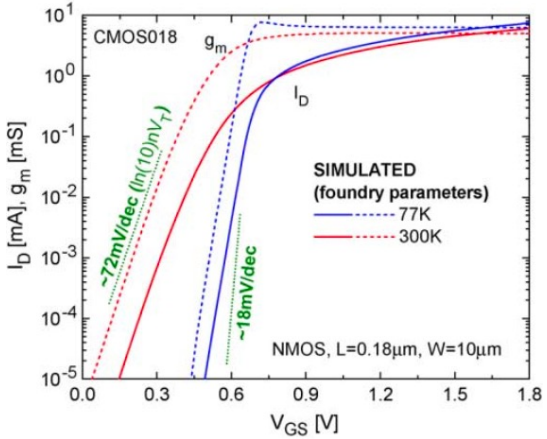
- **Low Noise**: to achieve sufficient SNR to perform both calorimetry and particle identification. Mounting the readout electronics close to the sensor minimizes the input capacitance, which is typically a dominant factor for noise.
- **Low Power Dissipation**: to avoid large cross-section power cables and formation of bubbles of gaseous Ar, ~35 mW/channel.
- **Low Cross Talk:** to avoid interference with scaled-up channels (0.5 million in DUNE; long-term target of 1 million for superconducting quantum system).
- **Reliability**: reliable for the duration of the experiment (>20 years for DUNE); packaging and bonding must survive repeated thermal cycling.
- **Operation Across Temperatures:** functional at room temperature to simplify screening and prototype testing; prior to installation, all readout modules are to be characterized immersed in liquid nitrogen at 77K for DUNE (4K for control and readout in superconducting quantum systems).

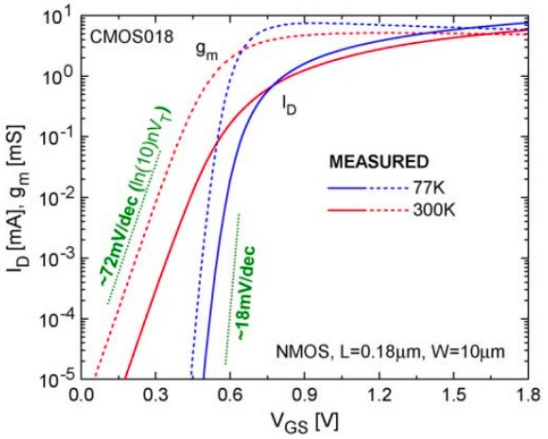
180-nm CMOS: DC & Noise Characteristics at 300 K & 77 K

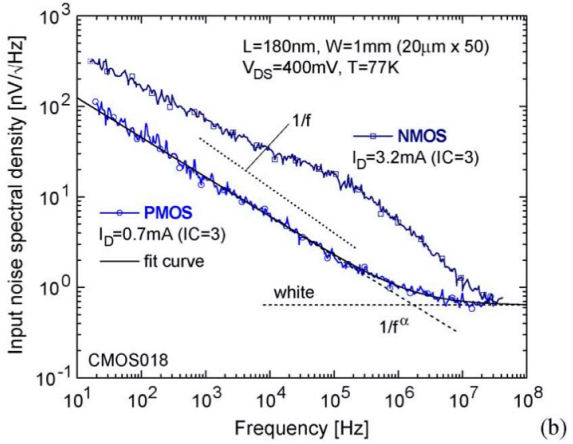












De Geronimo et al. (BNL), TNS 2011

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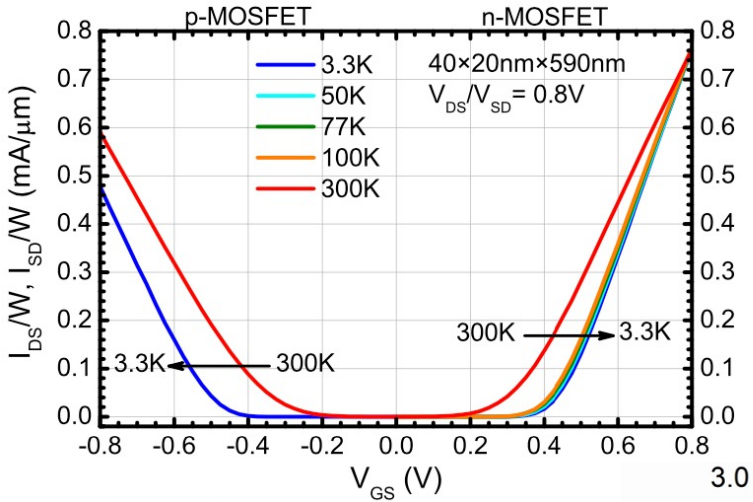
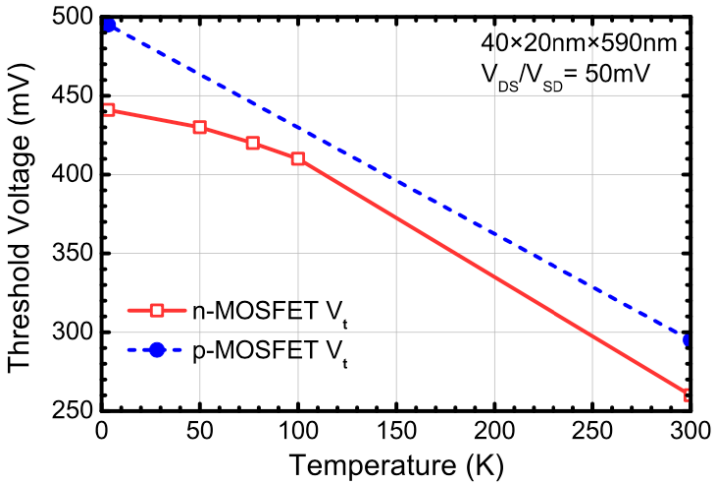
22-nm FDSOI MOSFET Characterization

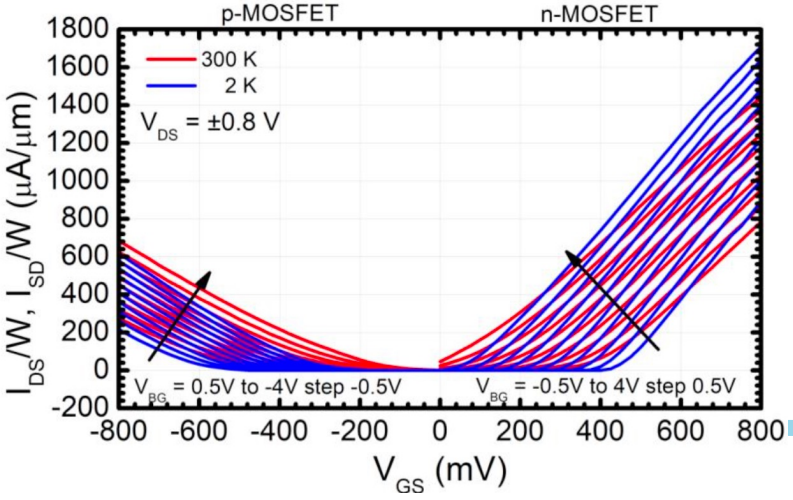
S. Voinigescu et al.,
U. Toronto





[Bonen et al._EuMW_2020]

[M. Gong_MS thesis/RFIC2019]



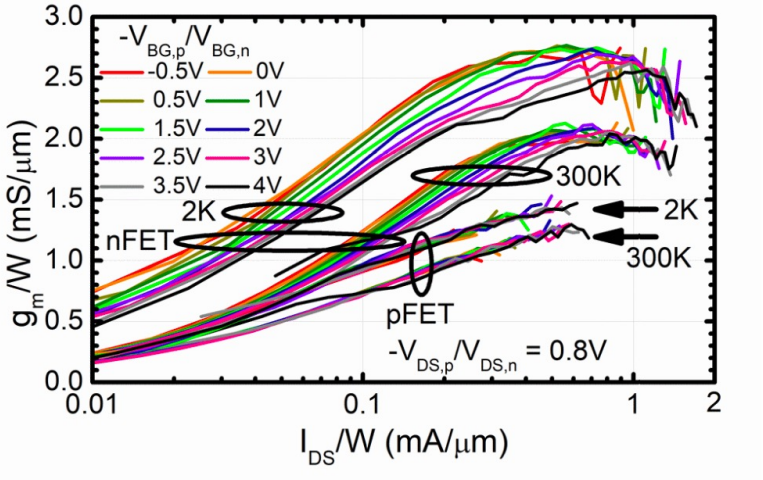


Fig. 8. Measured 20nmx80nm MOSFET g_m/W vs. I_{DS}/W and V_{BG} at 2 K and 300 K.

32-nm SOI MOSFET Noise Characterization Coskun et al. (U. Mass), MTT 2014

- With cooling from 293 to 6 K, intrinsic minimum noise temperature, Tmin, improves by approximately **one order of magnitude** at frequencies below 20 GHz and the improvement lessens at higher frequencies.
- Optimum source resistance, Ropt, decreases significantly with cooling: $R_{opt} = \sqrt{\left(\frac{f_t}{f}\right)^2 \frac{r_{gs}}{g_{ds}} \frac{T_g}{T_d} + r_{gs}^2}$

TABLE II
CRYOGENIC NOISE LIMITS OF SEMICONDUCTOR TECHNOLOGIES

Technology	Ref	T_a	T_{min}@5 GHz	T_{min}@20 GHz
-	-	K	K	K
130 nm SiGe HBT	[13]	18	2.2	8.1
130 nm InP HEMT*	[14]	10	1.2	5.6
32 nm SOI NMOS	This	6	0.8	3.8

*Results based upon model parameters provided in [14] and ignore gate leakage current.

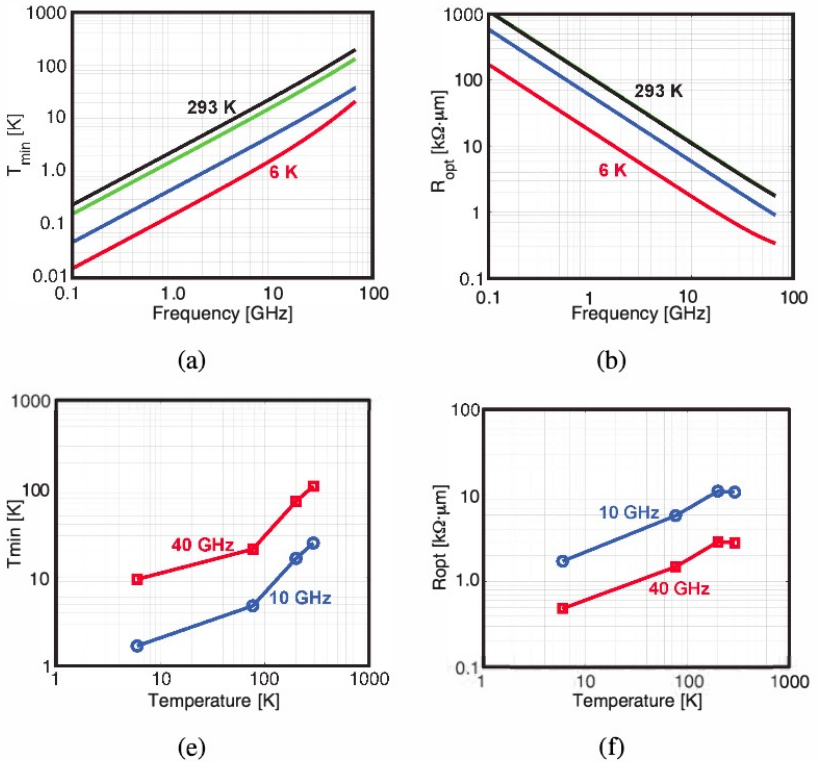


Fig. 5. Frequency dependence of (a) T_{min}, (b) R_{opt}, (c) X_{opt}, and (d) R_n. Temperature dependence of (e) T_{min}, (f) R_{opt}, (g) X_{opt}, and (h) $N = R_n$

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40-nm Bulk MOSFET Mismatch Characterization

Hart et al. (Delft U./EPFL), JEDS 2020

- For most analog circuits operating in saturation region, current mismatch increase slightly from room to cryogenic temperature.
- For switches, mismatch degrades significantly during switching region from room to cryogenic operation, which may not affect functionality much, but may impact synchronization.
- Increasing length minimizes mismatch.

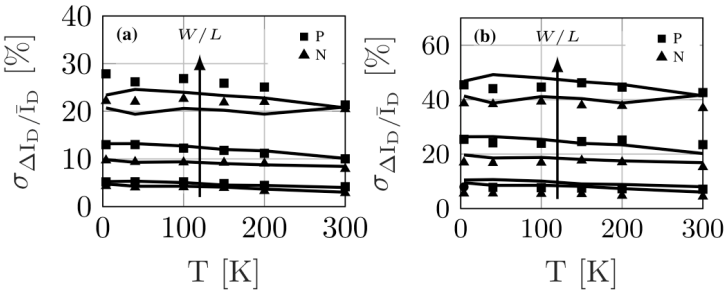


FIGURE 11. Drain-current mismatch as a function of temperature at a fixed G_m/I_D in saturation (V_{DS} = 1.1 V). a) G_m/I_D = 5 V^{-1}; b) G_m/I_D = 10 V^{-1}. Marks: measured data, lines: simplified Croon model as in Eq. (2). Arrow points in direction of decreasing W/L: 1.2 µ/40n, 360n/120n and 120n/40n.

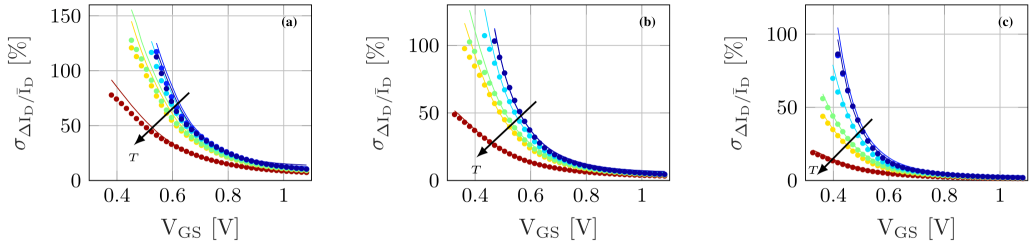


FIGURE 9. Drain-current mismatch for NMOS devices as a function of temperature (V_{DS} = 50 mV). T = 4.2, 40, 100, 150, 200 and 300 K. a) W/L = 120n/40n; b) W/L = 360n/120n; c) W/L = 1.2µ/400n. Dots: measured data; lines: simplified Croon model as in Eq. (2).

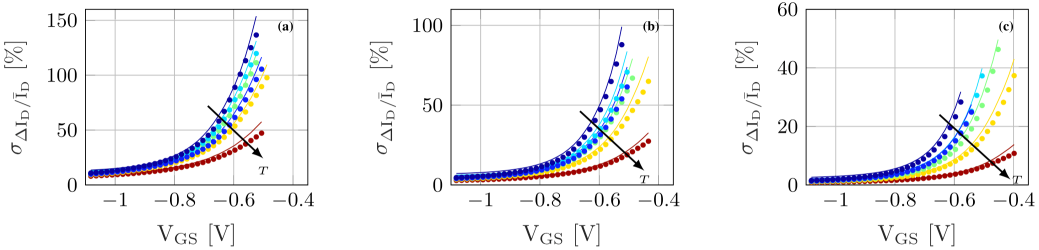
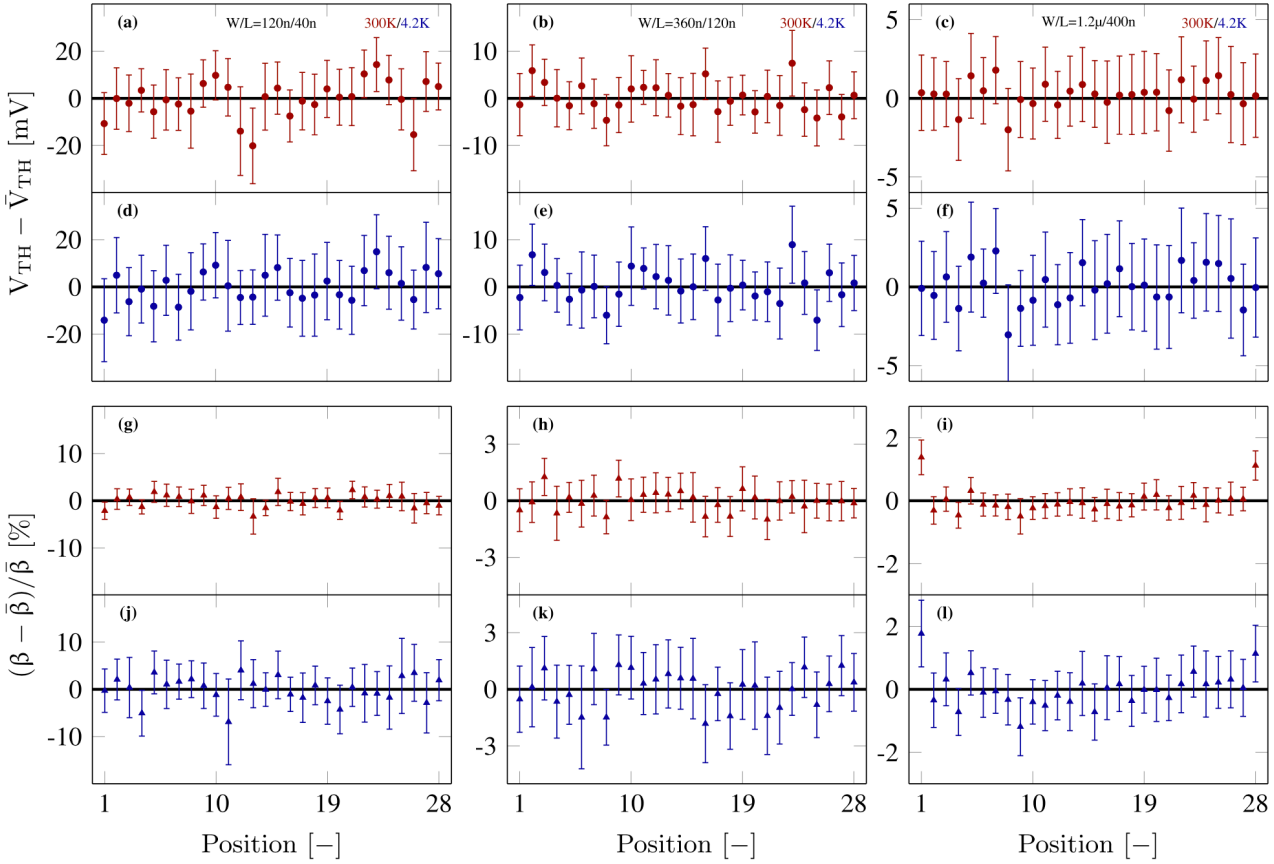


FIGURE 10. Drain-current mismatch for PMOS devices as a function of temperature ($|V_{DS}|$ = 50 mV). T = 4.2, 40, 100, 150, 200 and 300 K. a) W/L = 120n/40n; b) W/L = 360n/120n; c) W/L = 1.2µ/400n. Dots: measured data; lines: simplified Croon model as in Eq. (2).

40-nm Bulk MOSFET Mismatch Characterization

Hart et al. (Delft U./EPFL), JEDS 2020



- Threshold mismatch at 4.2 K is slightly higher than at 300 K.
- Gain mismatch at 4.2 K is about twice higher than at 300 K.
- Increasing length minimizes mismatch.

FIGURE 14. Normalised V_{TH} (circle) and β (triangle) as a function of device position for NMOS devices at RT (red) and LHT (blue). First column: W/L = 120n/40n; second column: W/L = 360n/120n; third column: W/L = 1.2μ/400n. Error bars indicate 95% confidence intervals.

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180-nm, 130-nm, and 65-nm CMOS Cryogenic Lifetime Study

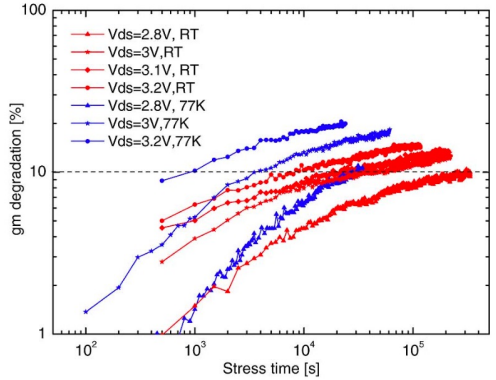


Fig. 4. Measured transconductance degradation versus time of an NMOS transistor ($L = 180$ nm, $W = 5 \times 2$ μm) in accelerated stress tests at room temperature (RT) and at 77 K.

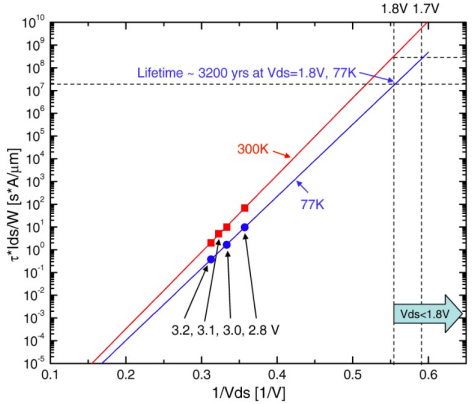
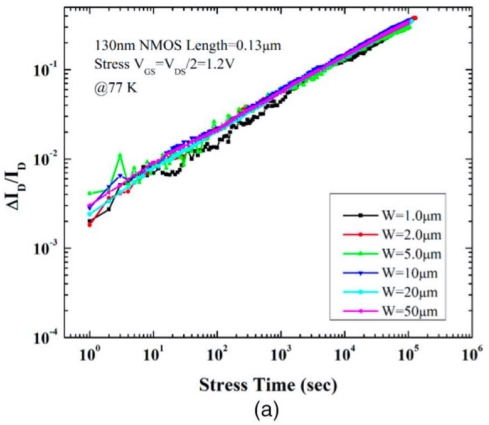


Fig. 6. Projected lifetime vs. $1/V_{ds}$ extracted from the stress measurement results shown in Fig. 5.



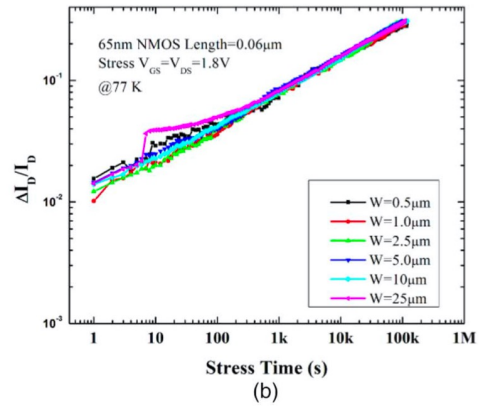
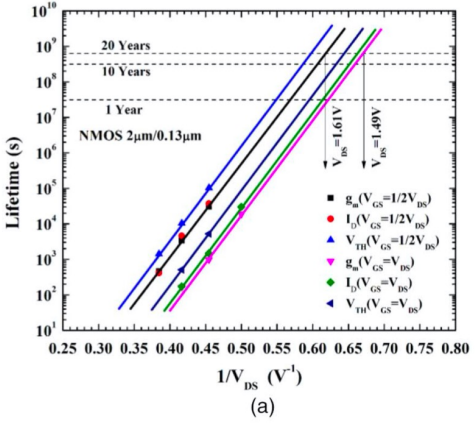


Fig. 5. Normalized change in drain current with stress time at 77 K for transistors with different widths: (a) 130 nm technology, (b) 65 nm technology. The 20 μm/0.13 μm and 50 μm/0.13 μm transistors in 130 nm technology have 2 and 5 fingers, respectively, The 10 μm/0.06 μm and 25 μm/0.06 μm transistors in 65 nm technology, likewise, have 2 and 5 fingers, respectively.



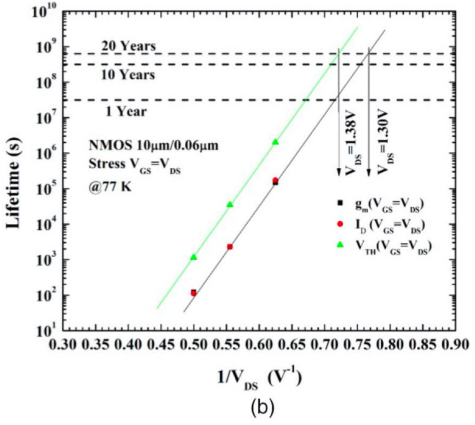
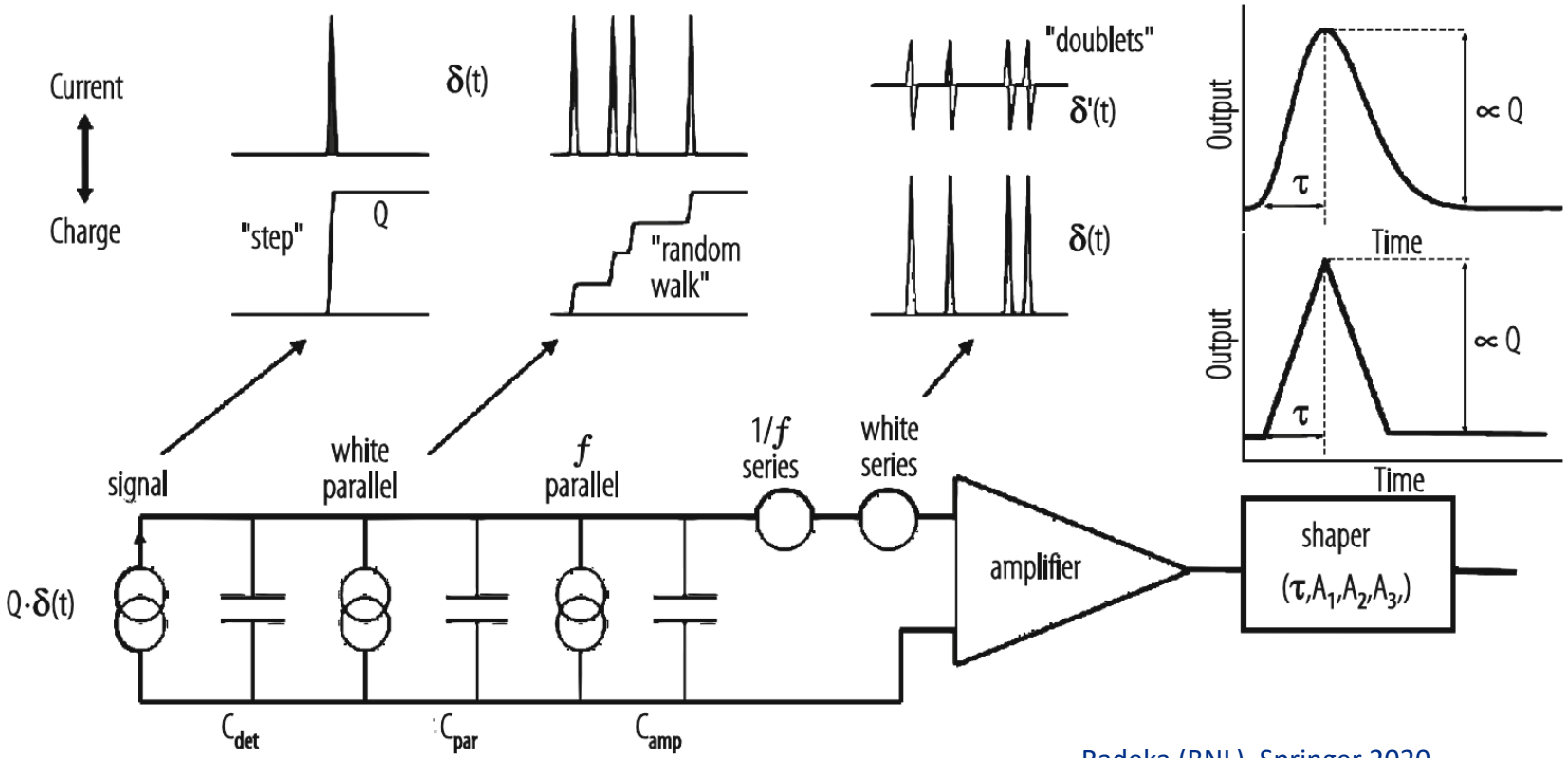


Fig. 6. Preliminary lifetime predictions for the 2 μm/0.13 μm and 10 μm/0.06 μm transistors at 77 K by degradation of g_m and I_{DS} and by increase of V_{TH}.

Li et al. (BNL), TNS 2013

Hoff et al. (Fermilab), TNS 2015

Noise Sources in Readout Chain



Radeka (BNL), Springer 2020.

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ENC vs. Peaking Time

$$ENC^2_{M_1\&lk} = ENC^2_{M_1-1/f} + ENC^2_{M_1-white} + ENC^2_{leakage}$$

$$= 2\pi A_{1/f} K_f \frac{(C_{det}+C_g)^2}{C_g} + A_w \frac{e^2_{n,M_1}(C_{det}+C_g)^2}{\tau_p} + qA_{lk}I_{lk}\tau_p$$

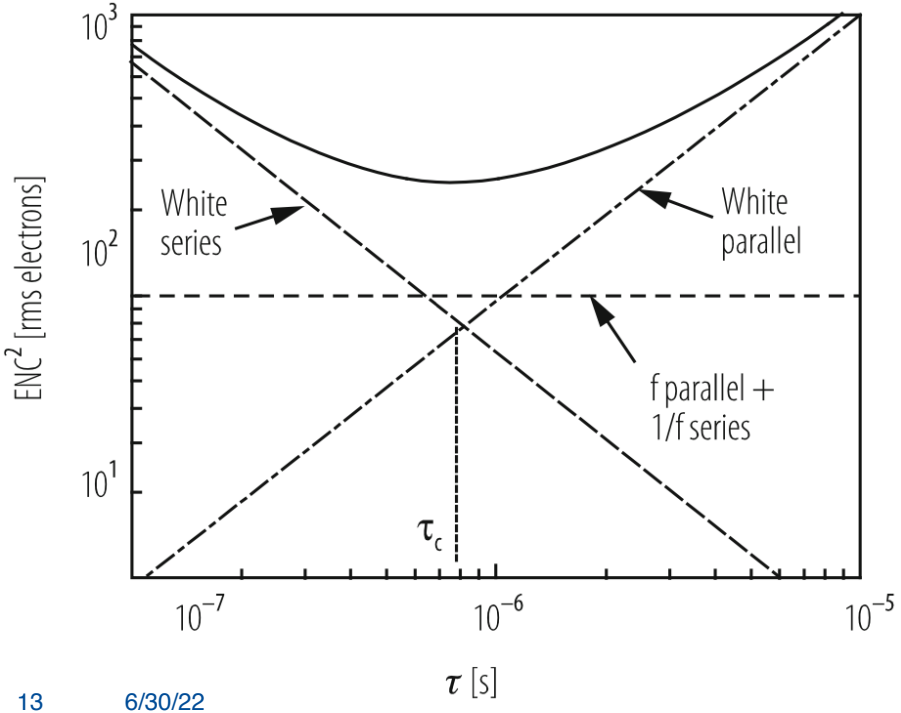

TABLE I. COMPARISON OF NOISE COEFFICIENTS OF DIFFERENT SHAPER WEIGHTING FUNCTIONS

Weighting Function	$A_{1/f}$	A_w	A_{lk}
Semi-Gaussian 3rd-order	0.54	0.82	0.66
Semi-Gaussian 7th-order	0.51	0.94	0.48
Trapzoidal (Δ=tc/tp)	0.69 @ Δ=1 0.46 @ Δ=0.1	1	0.83 @ Δ=1 0.38 @ Δ=0.1
Triangular (Δ=tc/tp→0)	**0.44**	1	0.33

Radeka (BNL), Springer 2020.

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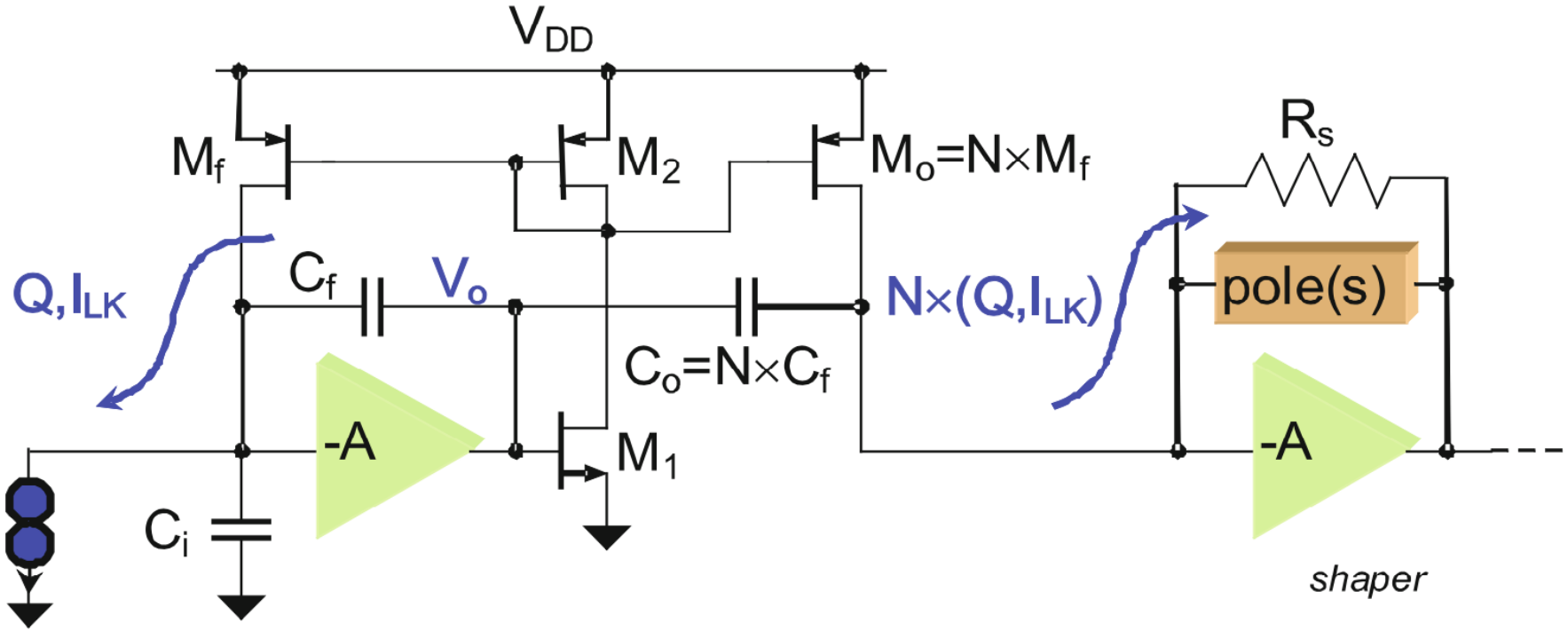
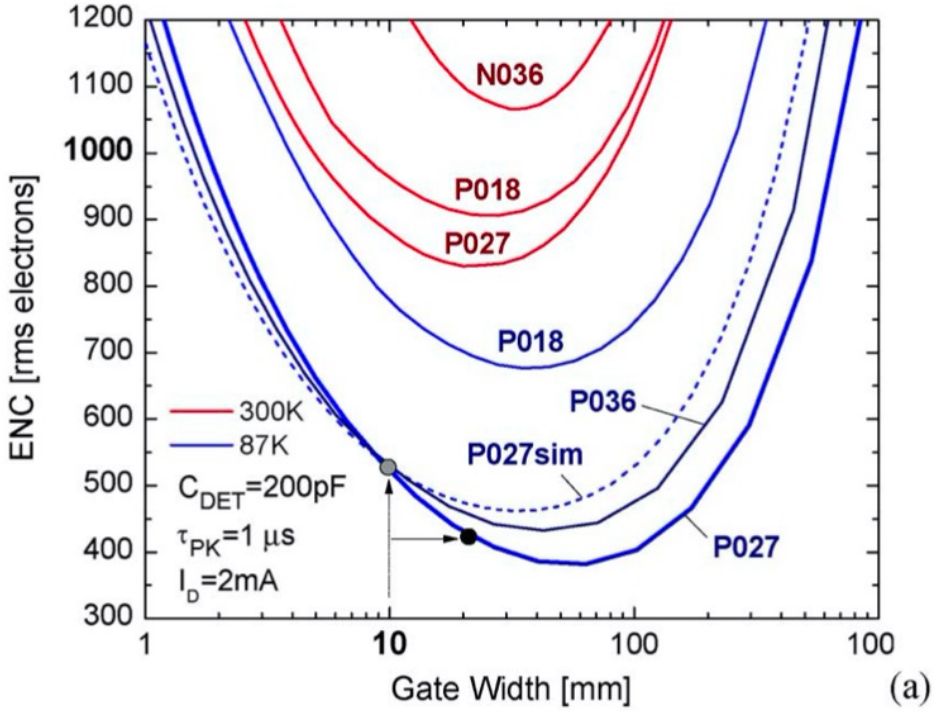
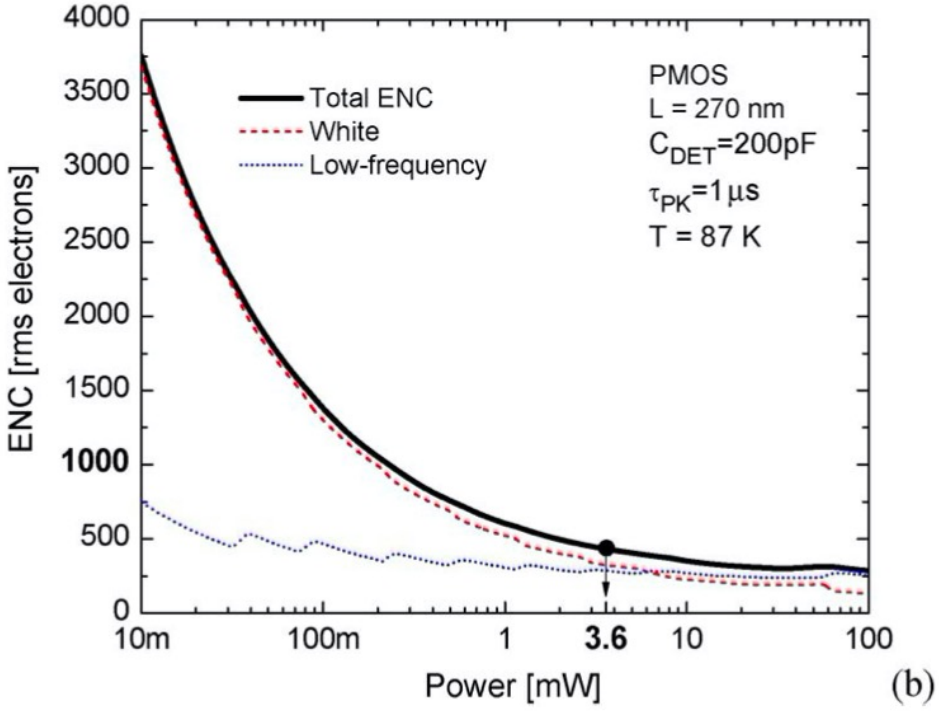
Charge Amplifier with Pole-Zero Cancellation



De Geronimo (BNL), Wiley 2009.

Optimizing Charge Amp Input Transistor





De Geronimo et al. (BNL), TNS 2011

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Shaper with Delayed Dissipative Feedback

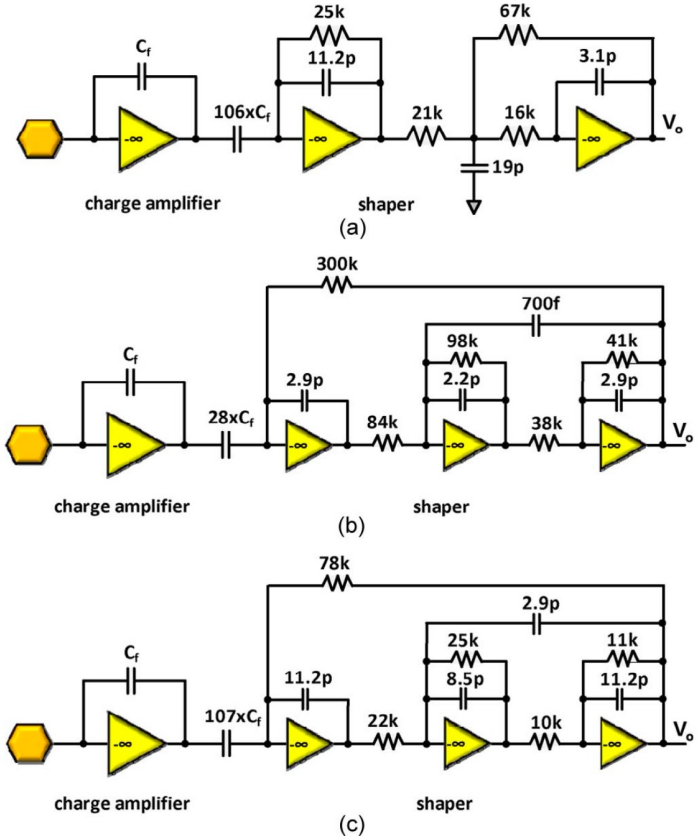
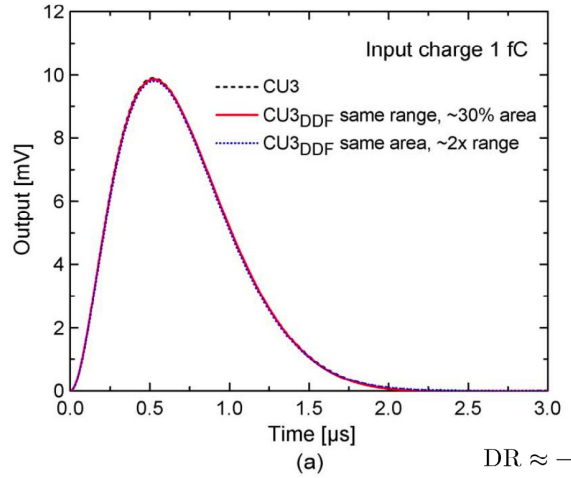
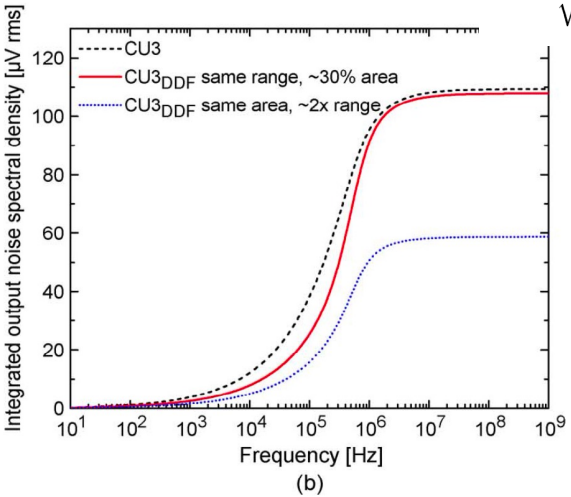


Fig. 10. Examples of realizations using the approach in Fig. 5 (a) and the DDF in Fig. 8 at equal dynamic range (b) and at equal total capacitance (c).



$$DR \approx \frac{Q_{max}}{\sqrt{\nu \cdot ENC_s^2}} = \frac{V_{1\,max}}{\sqrt{\nu \cdot a_p \varepsilon_p 4kT\left(\frac{1}{C_1} + \frac{\chi}{C_s}\right)}}$$



De Geronimo & Li (BNL), TNS 2013

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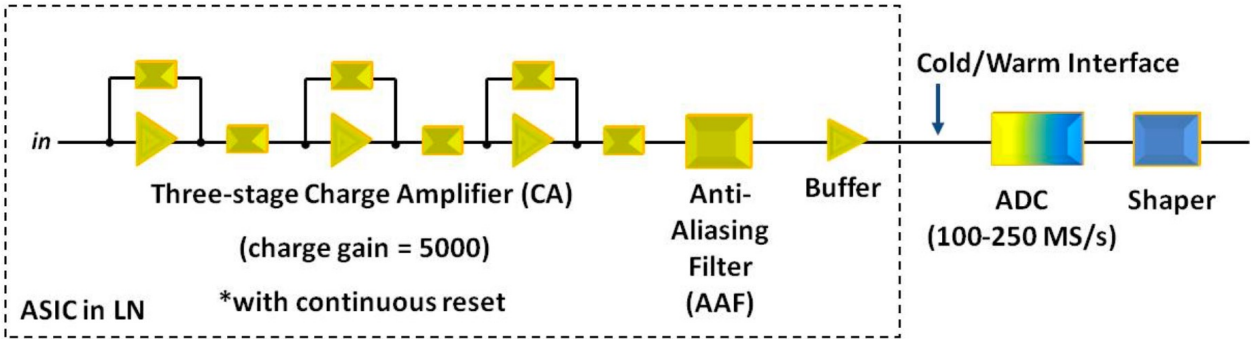
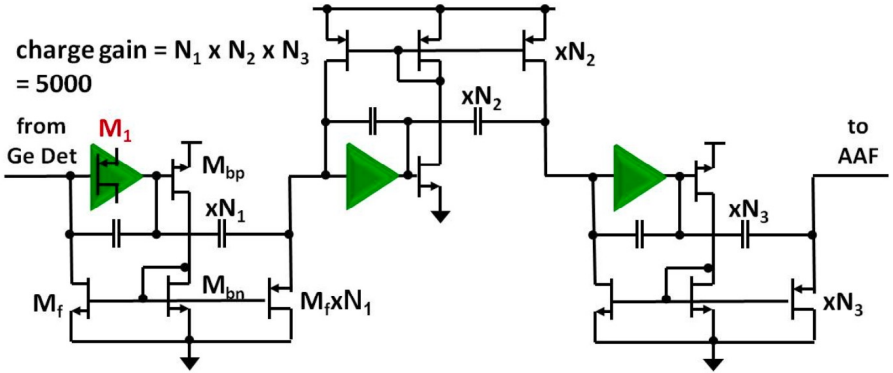
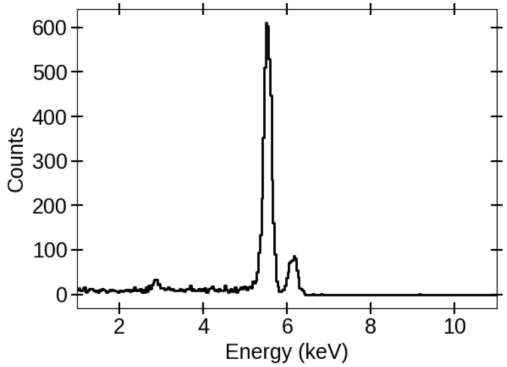
A Low-Noise Silicon Photodiode Detector for X-ray Capillary Optics

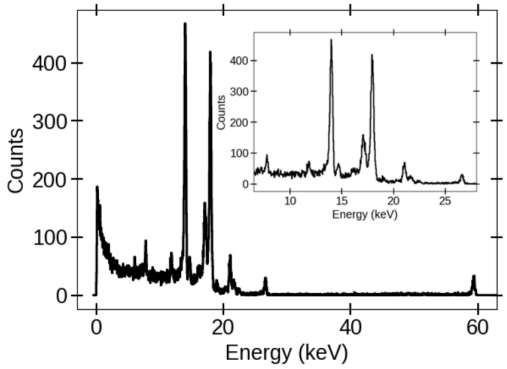
Li et al. (BNL), TNS 2013; Sleator et al. (NRL & BNL), TNS 2020







(a)



(b)

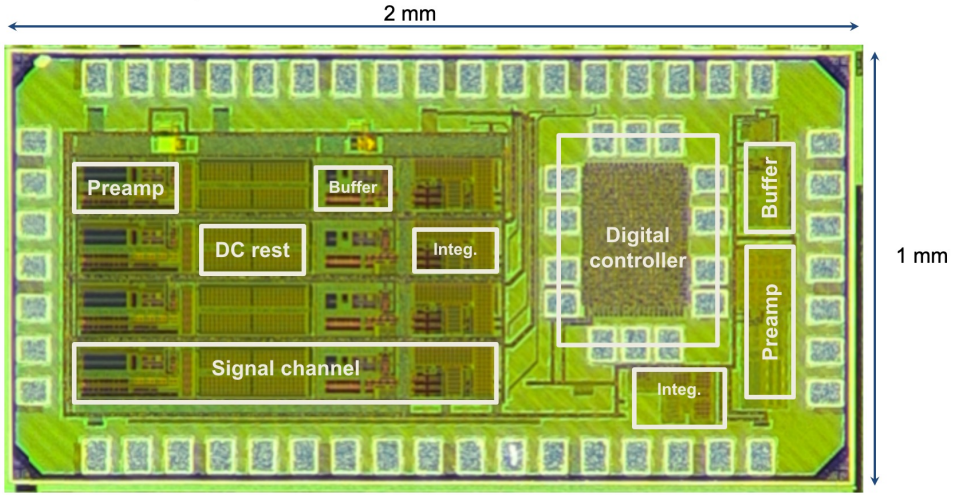
Fig. 10. Spectra from (a) ^{55}Fe and (b) ^{241}Am taken with the ASIC as the front end. The inset in the lower plot shows the ^{241}Am spectrum zoomed in around the low energy lines. The FWHMs of the prominent lines are 211±8 eV at 5.9 keV, 283±7 eV at 13.9 keV, 302±7 eV at 17.8 keV, 296±24 eV at 20.8 keV, and 438±39 eV at 59.5 keV.

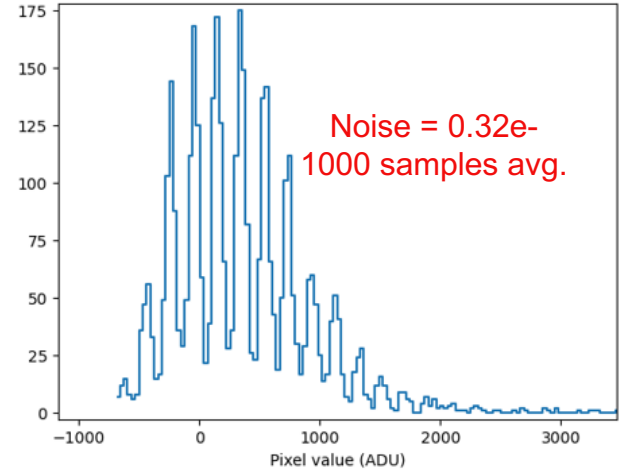
MIDNA: Low-Noise Skipper CCD Readout w/ Chopping Integrator

FNAL: Troy England, Hongzhi Sun, Davide Braga, Shaorui Li, Juan Estrada, Farah Fahim
CNEA: Fabricio Alcalde Bessia, Miguel Sofo Haro

- Midna1 demonstrated very low noise performance
- Midna2: implemented on-chip reference and buffers to further improve low-noise performance and isolate coupling between channels; improved integrator dynamic range to facilitate larger pile-up range for off-chip processing, and improved integrator sensitivity by further lowering the input offset.

Channel size: 150μm x 1mm





State-of-the-Art Cryo-Electronics for Quantum Computing

- Commercial instruments at room temperature is only feasible for < 100 qubits. > 1000 physical qubits will be required to encode 1 error-corrected qubit
- A practical quantum computer will need cryo-operation for **compact and scalable control and readout** circuits at 3~4K for 1 million qubits!

  Low power: < 1mW/qubit; **High resolution**: 10~12 bit; **Low noise**: < 100nV/sqrt(Hz)
- Issues reported in recent publications (e. g. IBM_ISSCC'22, Intel_ISSCC'21, Delft/Intel_ISSCC'20, Google_ISSCC'19):

  -Power consumption was 10x larger than the goal.

  -DACs at 3K were significantly nonlinear and non-monotonic.

  -Insufficient SNR, and high RMS error (e. g. 2.5% @300K -> 11.7% @3K).

KEY SPECIFICATIONS FOR CRYOGENIC *XY* CONTROLLER

Bardin et al., Google, JSSC 2019

	Amb. Temp.	RF Frequency	Envelope	Env. Amp	Pulse Duration	Amp. err.	Phase err	Inst. Set	AC+DC Power
Prototype Goal	3 K	4-to-8 GHz	Symmetric	> 10 mV	10-to-30 ns	< 0.25%	< 0.22°	16 (4-bit)	< 2.50 mW
Long-term Goal	3-to-4.2 K	TBD	DRAG	> 1 mV	< 10 ns	< 0.25%	< 0.22°	TBD	< 250 μW

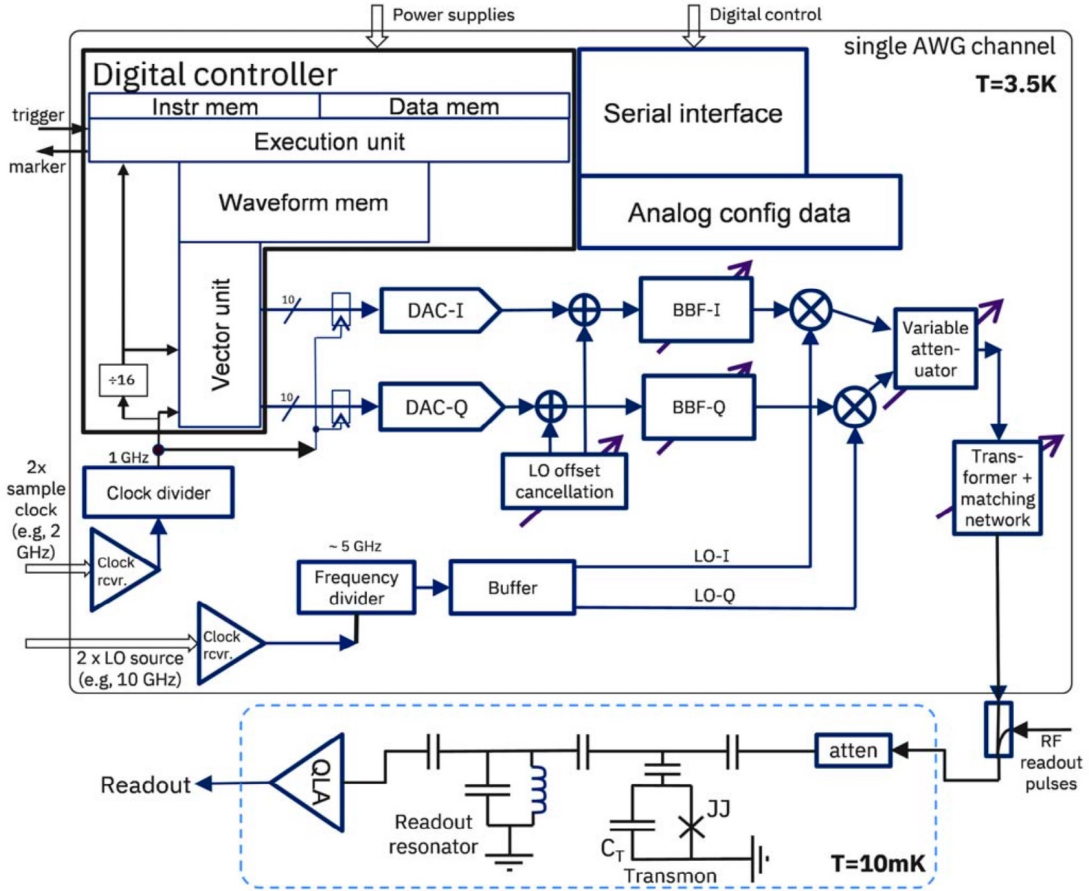
Performance Comparison

	IBM ISSCC'22	Delft/Intel ISSCC'21	Delft/Intel ISSCC'20	Google ISSCC'19
Ambient temperature (K)	3	4	3	3
Qubit type	transmon	spin	spin & transmon	transmon
Waveform type	arbitrary	arbitrary	arbitrary	envelope modulated RF pulse
RF freq range (GHz)	4.5-5.5	11-17	2-20	4-8
IF freq range (GHz)	DC-0.3	DC-0.7	DC-0.5	low-freq. envelope
# channels	2	4	4	1
NCOs	updateable phase rotations	64	64	0
Sideband method	SSB	SSB	SSB	IQ mod
DAC speed (GS/s)	1	2.5	1	1
DAC bits	10	10	10	~11
Output gain/attenuation range	50x	>56x	225x	n/a
Waveform points	8K	16K	40K	22x16
Pulse sequence length	4K or unlim	2K	2K	-
General purpose instruction set	yes, 37 instructions	no (special only)	no (special only)	no
Power/qubit under active control (mW)	23	90 (estimated)	190	2
Chip area/channel (mm^2)	1.61	~4	4	1.6
Technology	14nm FinFET	22nm FinFET	22nm FinFET	28nm bulk

Frank et. al (IBM), ISSCC 2022

14-nm FinFET 4-to-6 GHz Controller for Transmon Qubits

Frank et al. (IBM), ISSCC 2022



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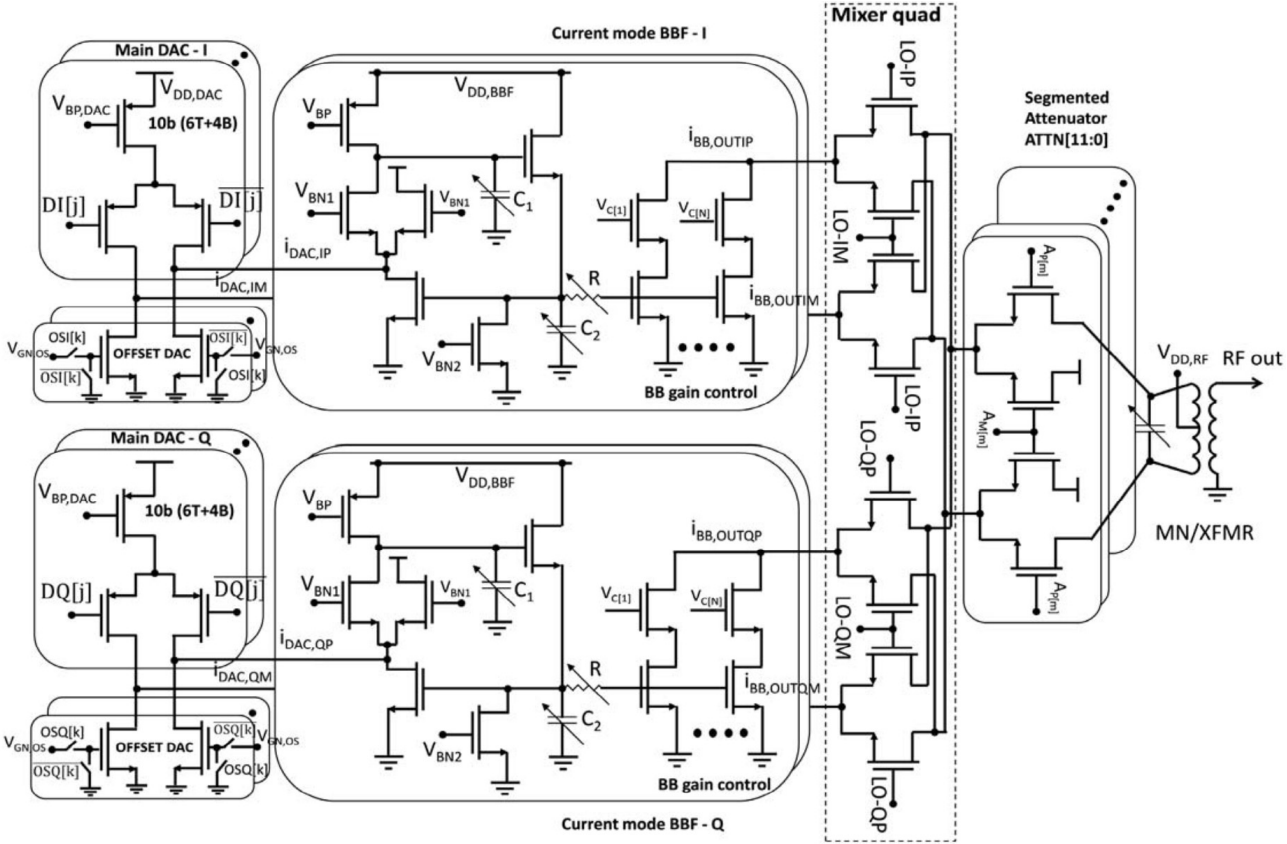
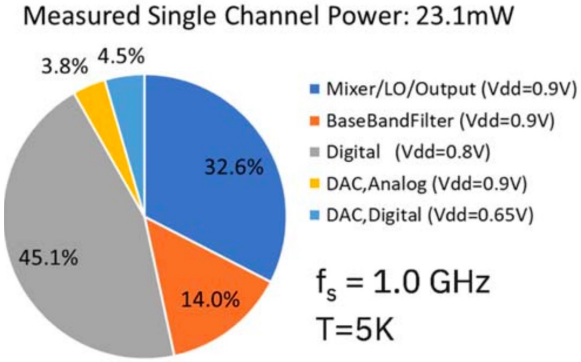
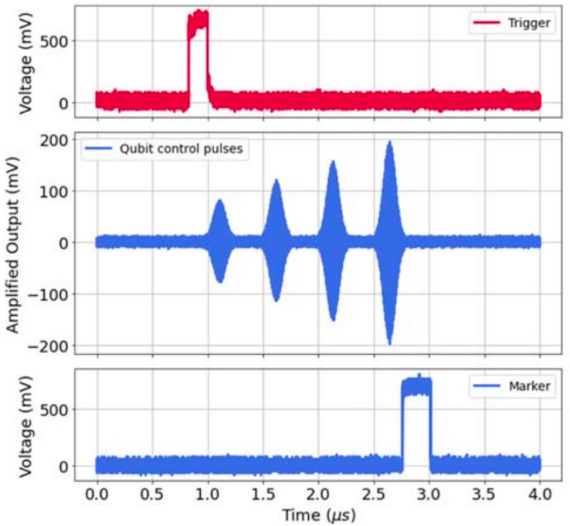
14-nm FinFET 4-to-6 GHz Controller for Transmon Qubits

Frank et al. (IBM), ISSCC 2022







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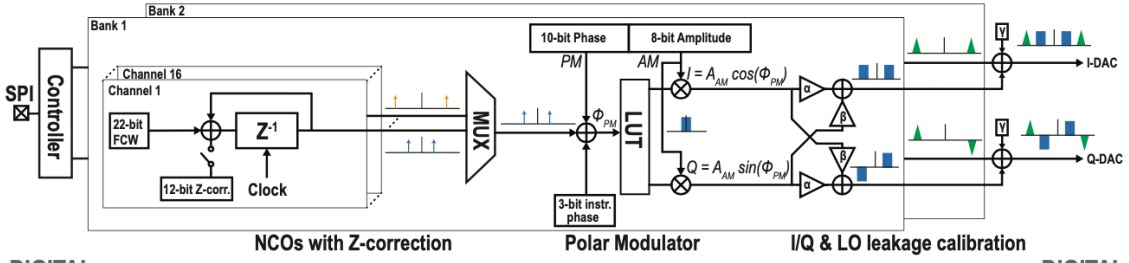
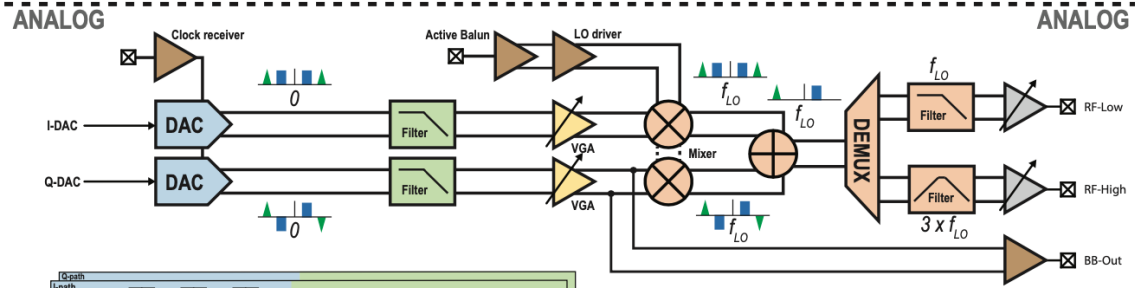
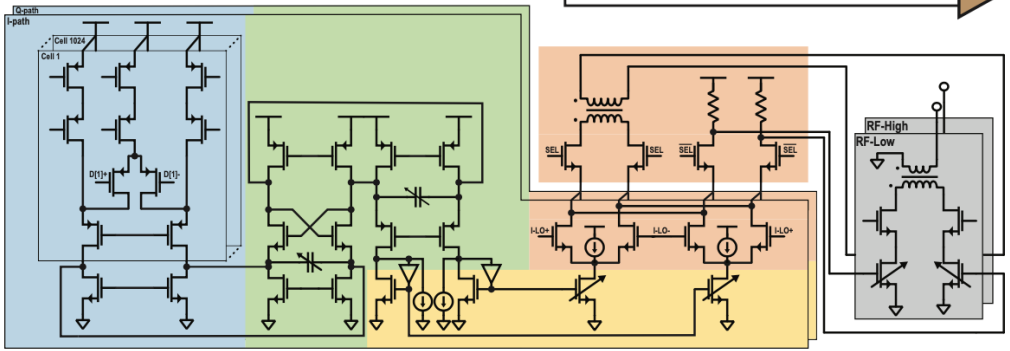
22-nm FinFET 2-to-20GHz Readout and Control SoC for 16/32 Spin Qubits

Park et al. (Intel), ISSCC 2021, Patra et al. (Delft/Intel), ISSCC 2020, van Dijk et al. (Delft/Intel), JSSC 2020







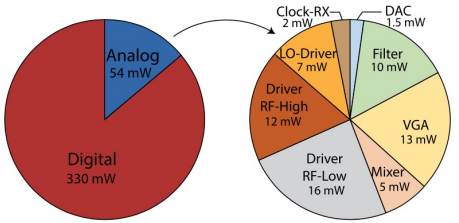
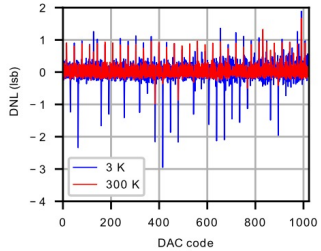
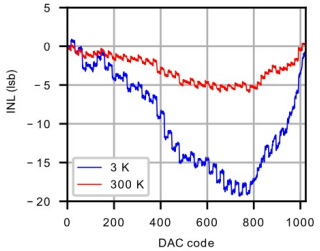
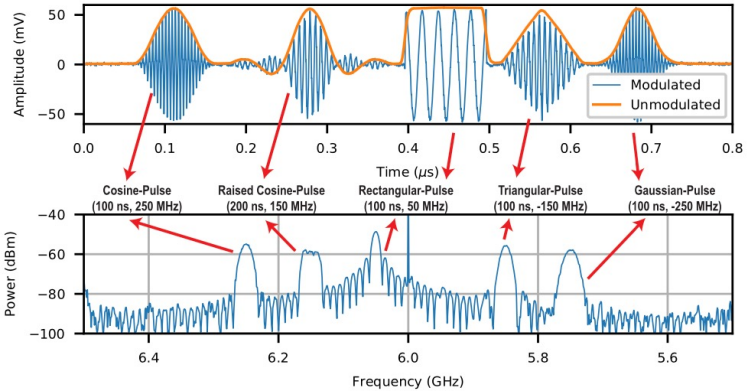


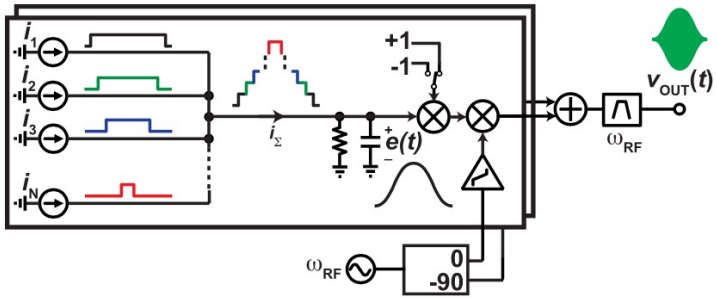
Fig. 15. Power consumption breakdown, resulting in a total power consumption per qubit of (330 mW + 54 mW)/32 qubits = 12 mW/qubit.

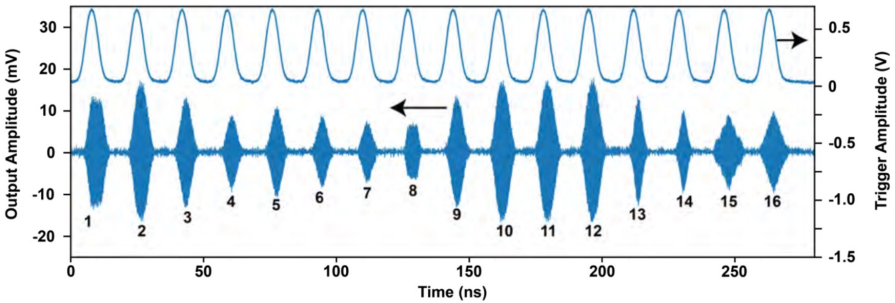


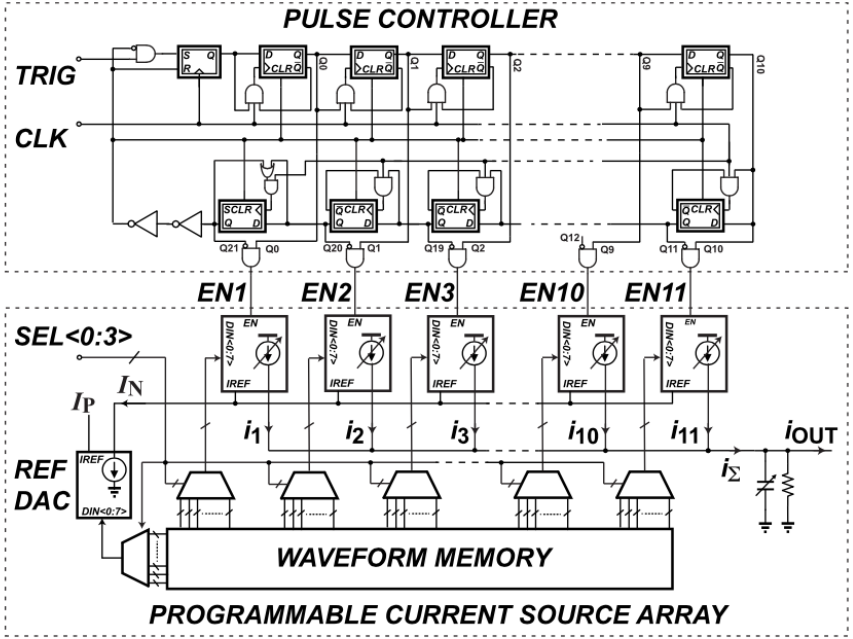




28-nm CMOS 4-to-8GHz <2mW Pulse Modulator for Transmon Qubits Bardin et. al, UMass/Google, ISSCC/JSSC 2019







	Form Factor	Phys. Temp.	Update Freq.	Dig. Data Rate	π-Rabi P{|1⟩}*	3-gate RMS err†	AC+DC Power
Standard XY	Rack Mount	300 K	1 Gsps	28 Gbps	~95%	2.5%	> 1 W
This work	Integrated Circuit	3 K	1 Gsps	< 0.5 Gbps	~95%	11.7%	< 2 mW

*In both cases, the measured probabilities were limited by the readout error rate

†Error defined as the difference between the ideal result and the measured result. The ideal result has been corrected to account for readout fidelity. X and Y axes for CMOS IC are uncalibrated.

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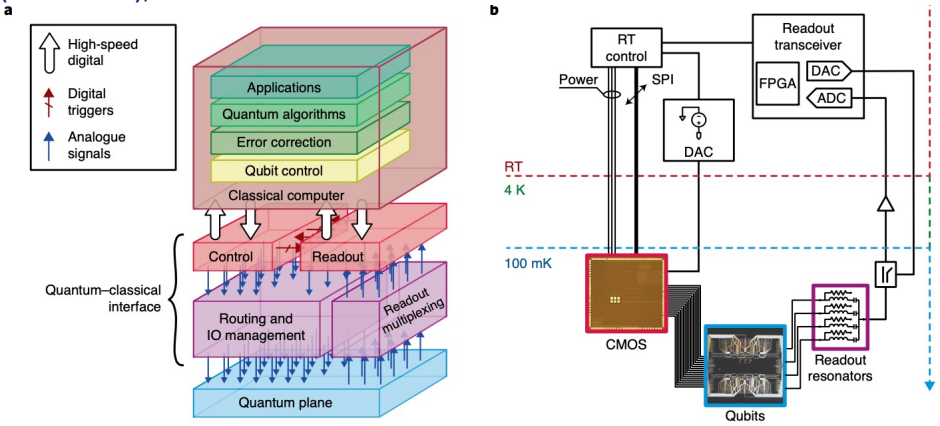
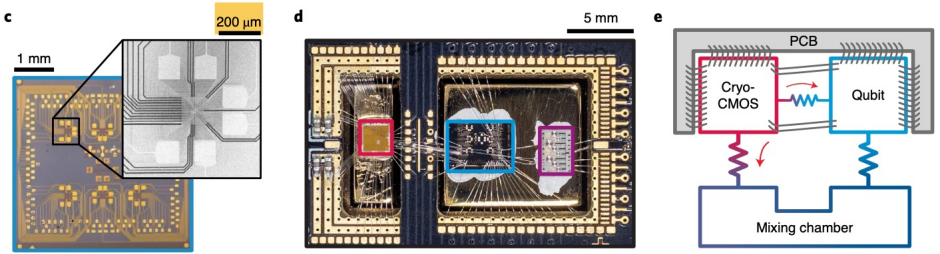
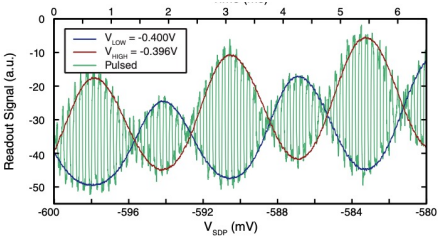
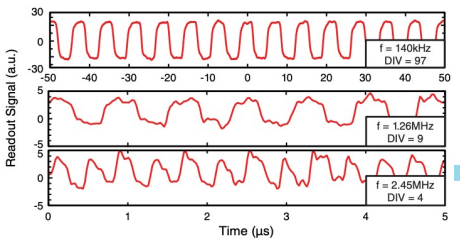
28-nm FDSOI Controller at 100-mK for GaAs Quantum Dots

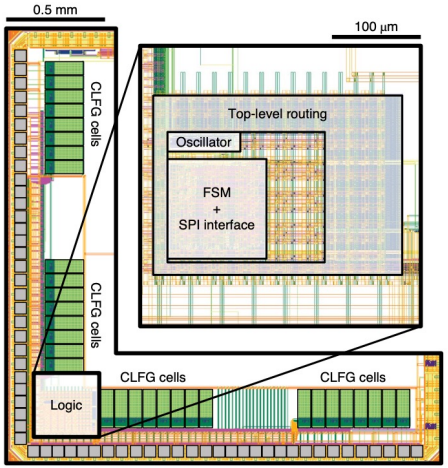
Pauka et al (Microsoft), Nature Electronics 2021

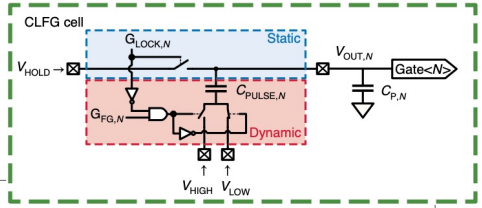


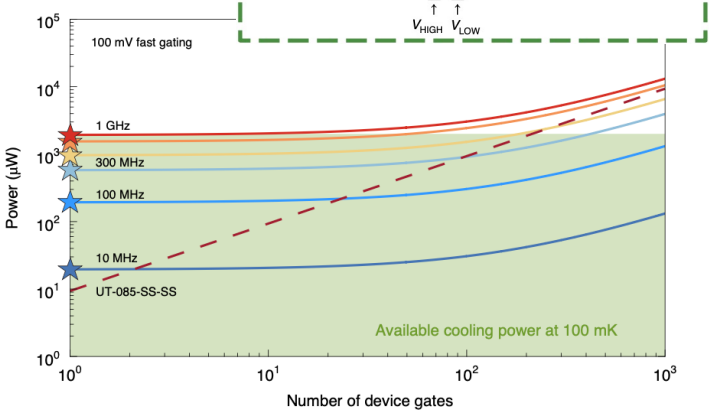












Cryogenic Ion Trap Controller

FNAL: Farah Fahim, Shaorui Li, Hongzhi Sun, Xiaoran Wang
ORNL: Chris Seck, John Comish, Gilles Buchs, Raphael Pooser (ORNL)
SBU: Dyumaan Arvind, Milutin Stanacevic

Design Challenges:

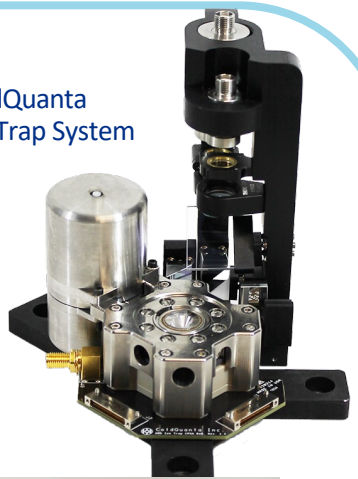
- Low output noise: < 100nV/sqrt(Hz) around axial frequency (0.5 – 5 MHz) and at low frequency
- Low power: < 5 mW/channel (limited by the cooling power of the cryostat) of +/- 10 V full scale at 1-10 MHz waveform updating rate
- Voltage resolution: 1mV for precise control
- Designed for the ion trap electrode with capacitance of 800 pF, leakage current of 10nA

Our Solutions:

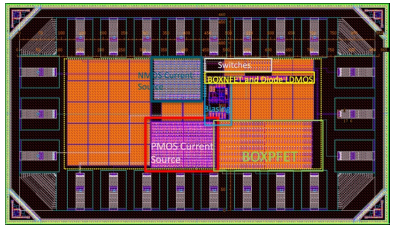
- Ultra low-noise low-power solution using charge-mode arbitrary waveform generation
- High-voltage CMOS devices capable of +/- 5V range, along with low-power digital control
- High-density memory for storage of base sets of waveforms

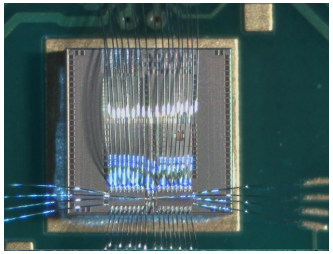
Sandia Phoenix Ion Trap chip

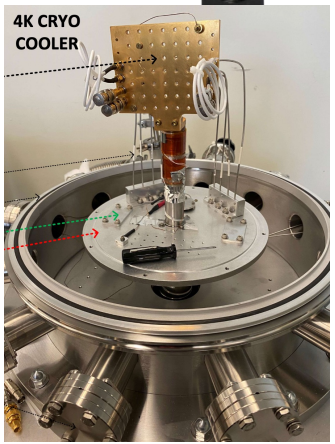
ColdQuanta
Ion Trap System



CITC1 ASIC Block







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