Timing Circuits for HEP experiments

HEPIC Summer Week 2022

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28 June 2022

SLAC NATIONAL ACCELERATOR LABORATORY | TID TECHNOLOGY INNOVATION DIRECTORATE | TID-ID INTEGRATED CIRCUITS DEPARTMENT

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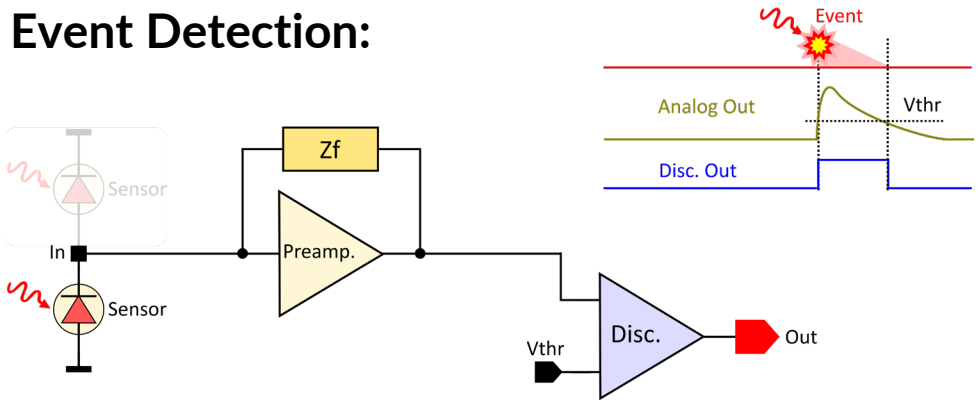
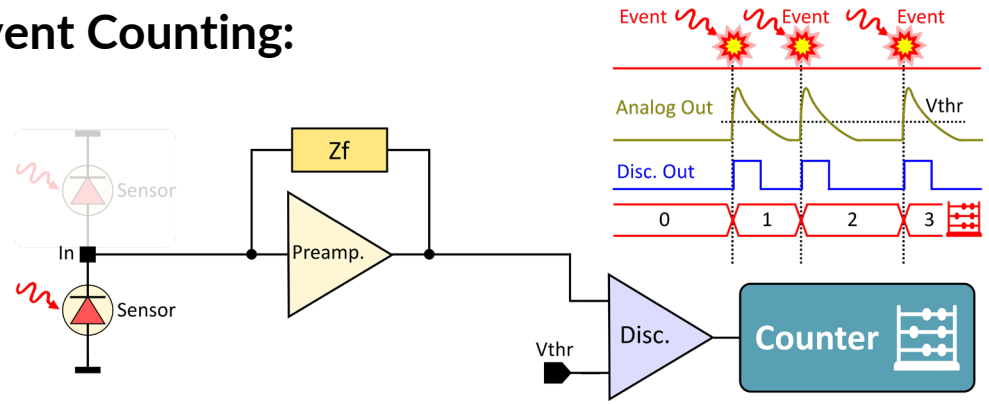
Detector Front-End: what are we measuring?

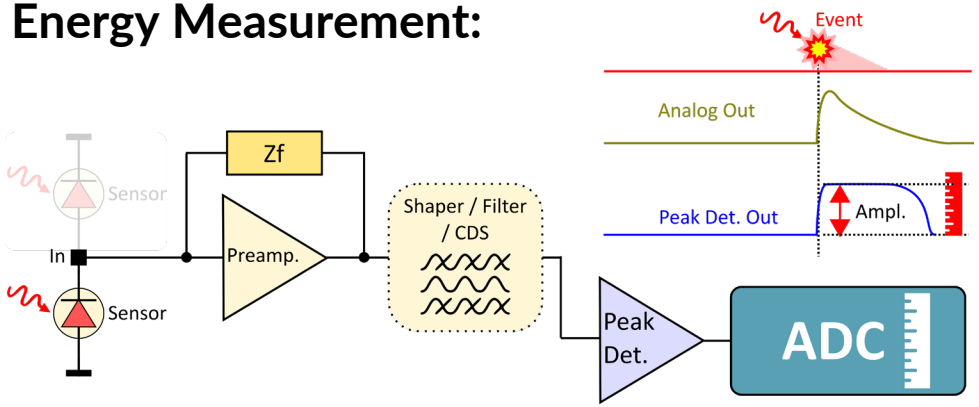
Event Detection:



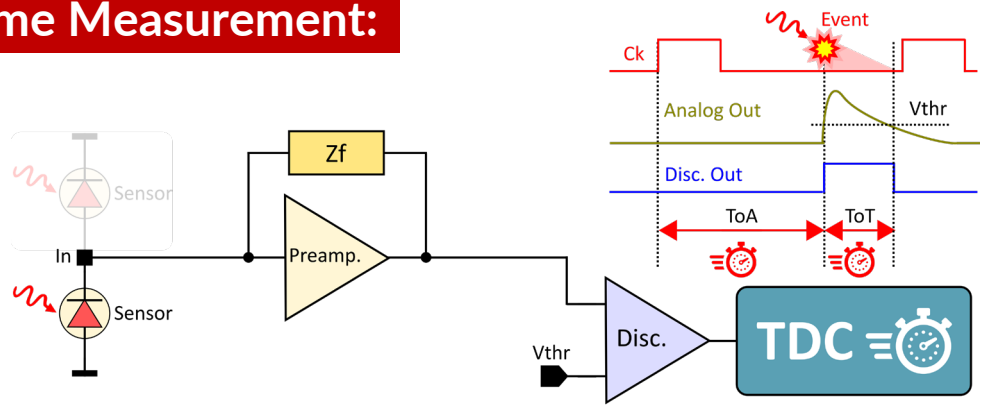
Event Counting:



Energy Measurement:



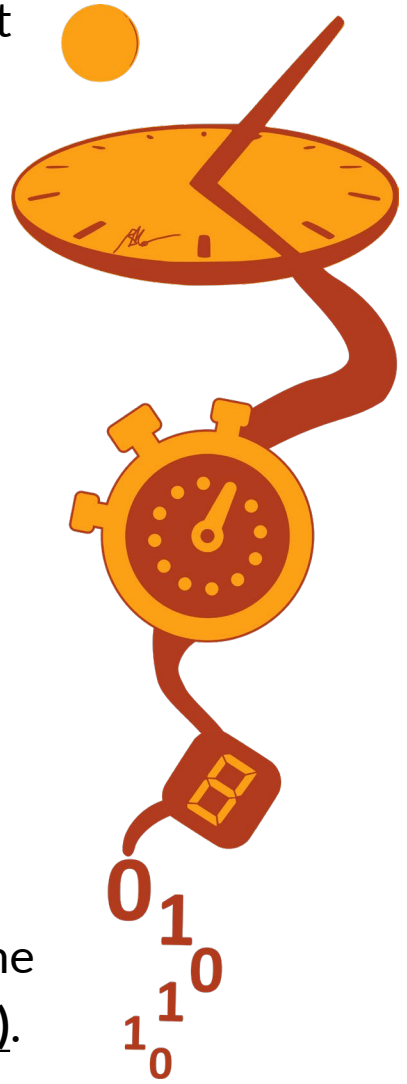
Time Measurement:



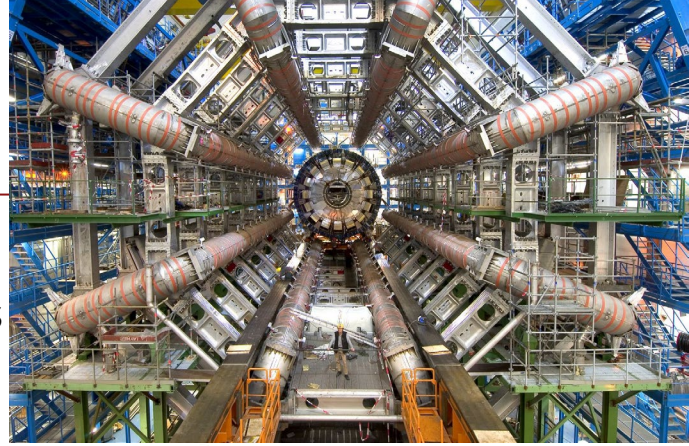
- ToA = Time-of-Arrival [ToF = Time-of-Flight]
- ToT = Time-over-Threshold
- TDC = Time-to-Digital Converter

Time Measurement

- **Time Measurement** is a lose term as time has no physical properties to measure. What we are really measuring is the duration separating two events, thus a more accurate term is **Time Interval Measurement**.
- Examples of ways of keeping track of passage of time throughout history include: sunrise/sunset, phases of the moon, sundials, water clocks, sandglasses, pendulum clocks, all the way to today's quartz clocks and atomic clocks.
- Nowadays official sources of time are provided by caesium atomic clocks, such as the ones operated by National Institute of Standards and Technology (NIST).
- The international standard (SI) unit of time [official definition]: *the second, symbol s, is defined by taking the fixed numerical value of the cesium frequency* Δv_{Cs}*, the unperturbed ground-state hyperfine transition frequency of the cesium-133 atom, to be 9,192,631,770 when expressed in the unit Hz, which is equal to* s^{-1}.
- Electronic high-precision time measurement circuits are called by different names: Time Interval Meters (TIM), time counters, time digitizers, **Time-to-Digital Converters (TDC)**.



Time-to-Digital Converters (TDC)



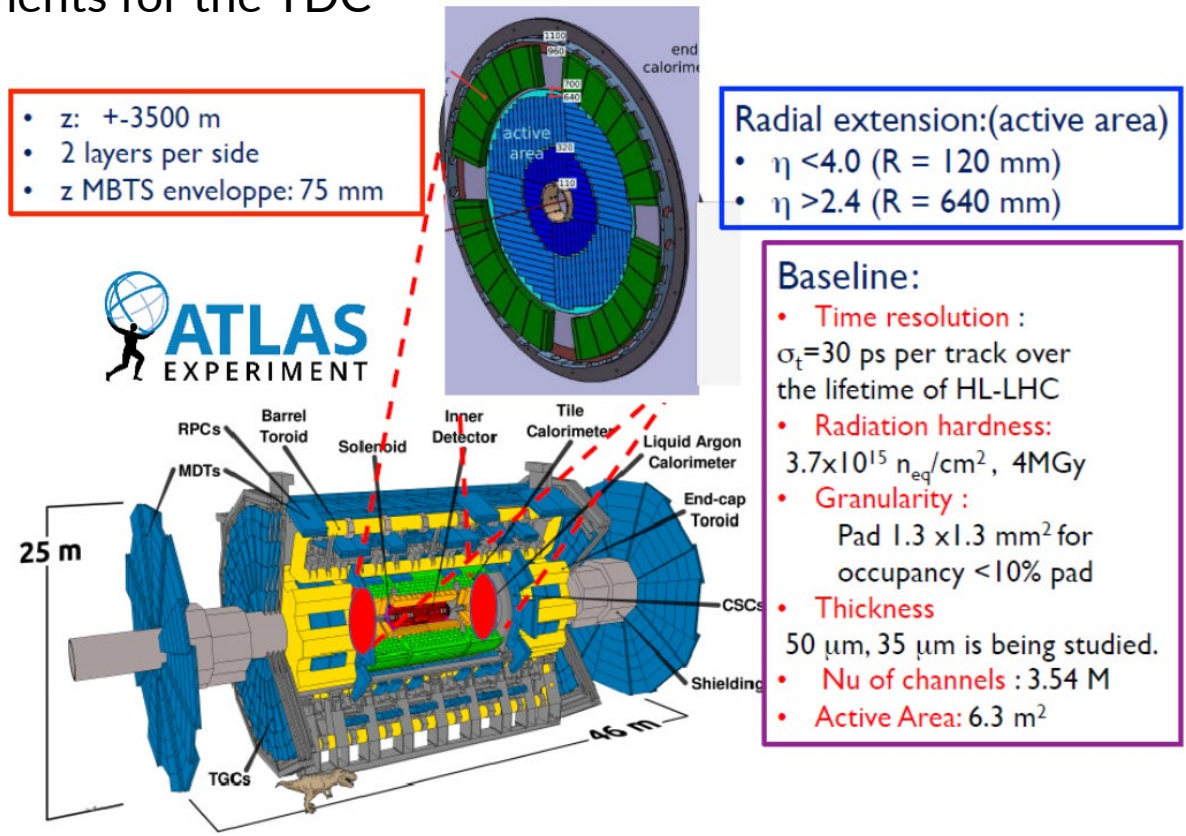
TDC applications in HEP:

- Systems with hundreds of thousands channels or more, distributed across large area; time precision/stability across whole system is critical
- Detector/Sensor time resolution sets the requirements for the TDC

- Drift time in gas-based tracking detectors:
  - Low resolution: ~1ns
  - Examples: ATLAS and CMS muon drift tubes
- Timing/TOF detectors:
  - High resolution: 10ps – 100ps
  - Examples: ATLAS HGTD, CMS MTD, ALICE TOF

Other TDC application include:

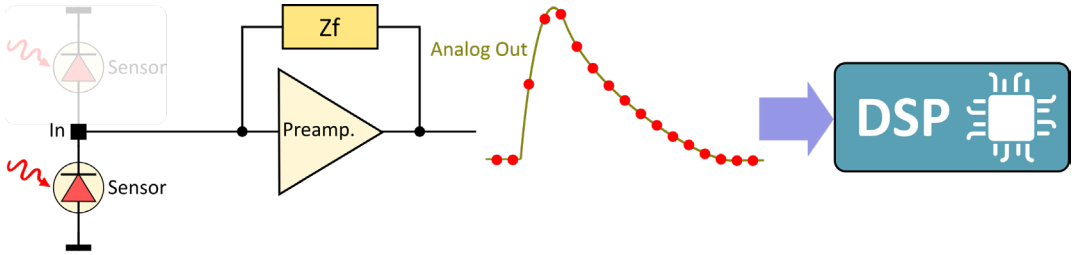
- communication systems (frequency synthesis, ADPLL, CDR, …);
- distance measurements (LiDAR, 3D imaging, …);
- biomedical imaging (TOF PET, FLIM, …);
- photon science (COLTRIMS, …);
- general instrumentation (jitter measurement, …);



ATLAS High-Granularity Timing Detector (HGTD) for HL-LHC upgrade

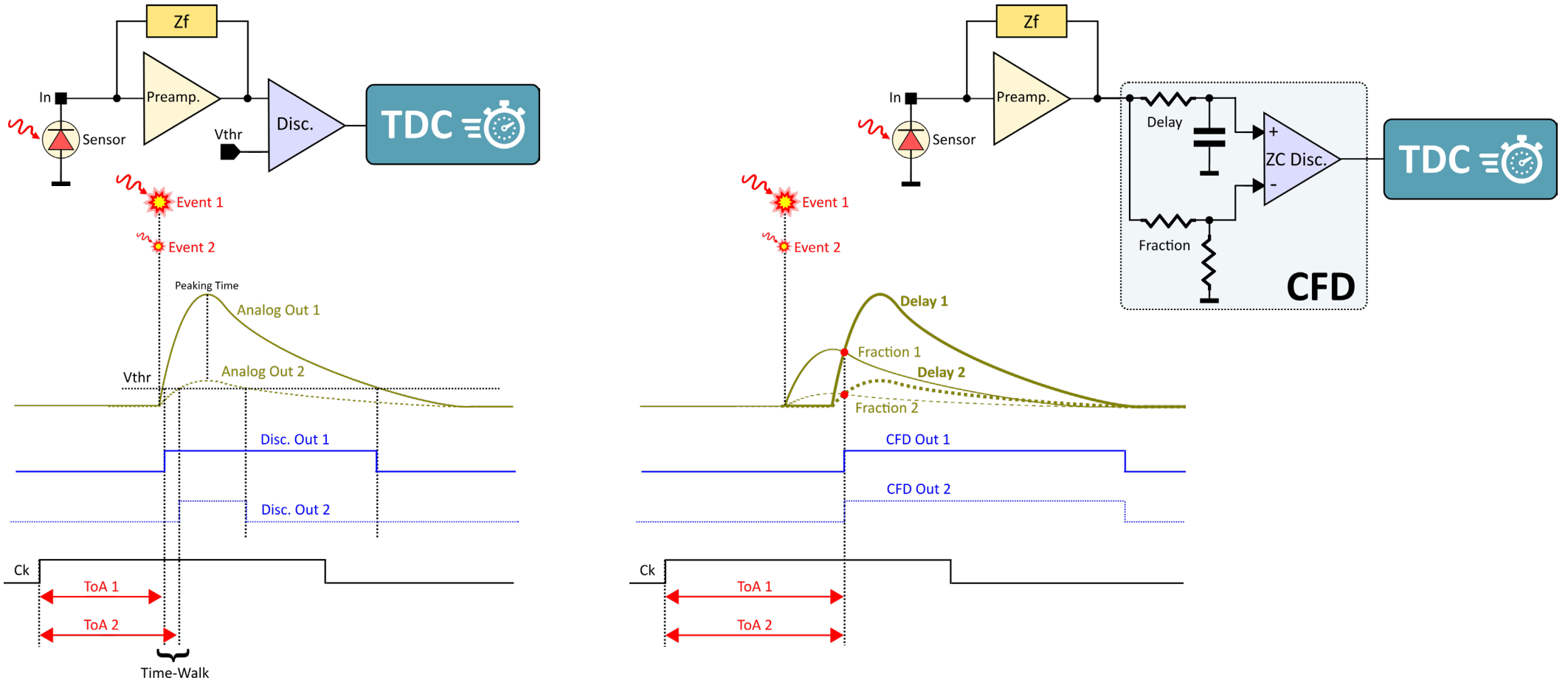
Analog Waveform Sampling + DSP post-processing

- Picosecond time resolution can be extracted using high-speed sampling of analog waveform followed by digital signal processor (DSP) post-processing performing matching to a known pulse shape:



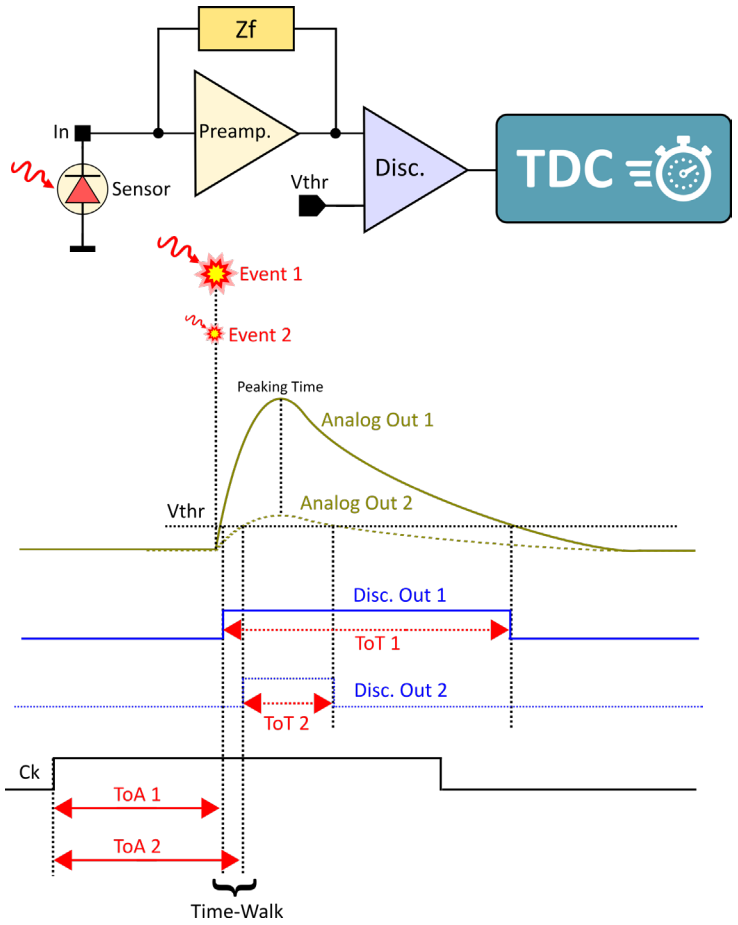
- For applications with hundreds/thousands of channels/pixels, the use of high-speed waveform sampling with DSP processing becomes cost and power prohibitive.
- To simplify timing measurements, **discriminators** are used to translate analog signals into digital ones, preserving only timing information of interest (losing analog amplitude/shape information)

Time-Walk, Constant Fraction Discriminator (CFD)

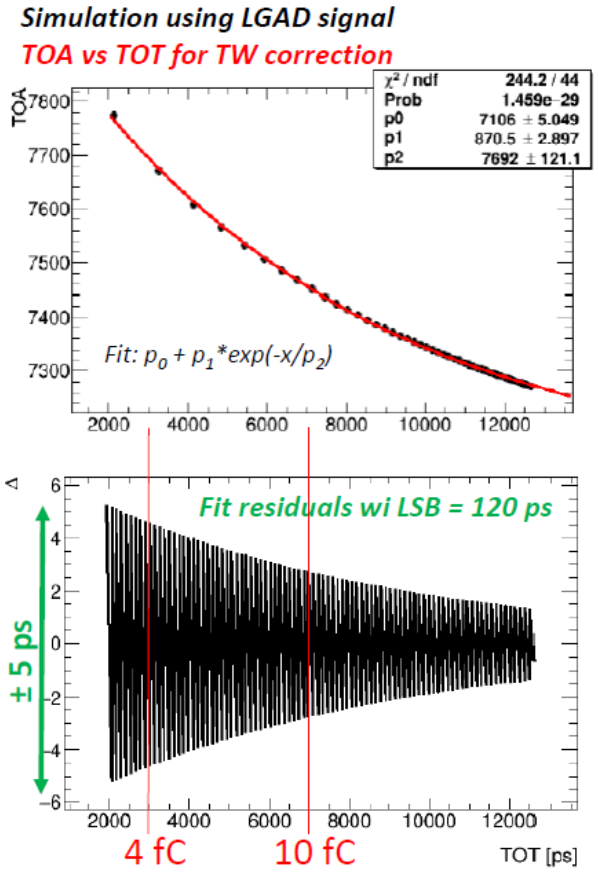


- Constant Fraction Discriminators (CFD) are not simple to implement in channel-dense ICs.

Time-Walk, Time-over-Threshold (TOT)



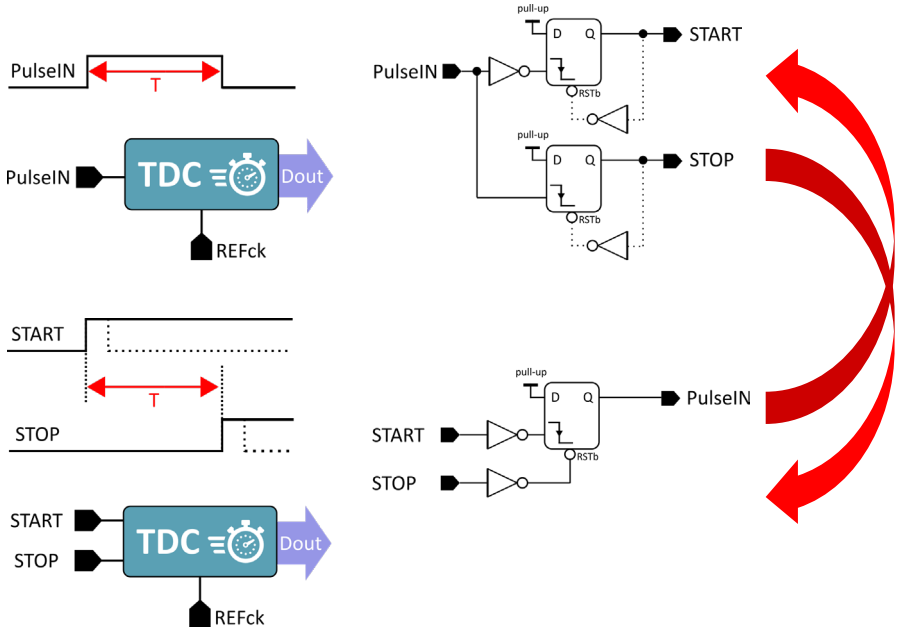
- Altiroc (front-end ASIC for ATLAS HGTD detector) - example of estimation of TW correction accuracy:



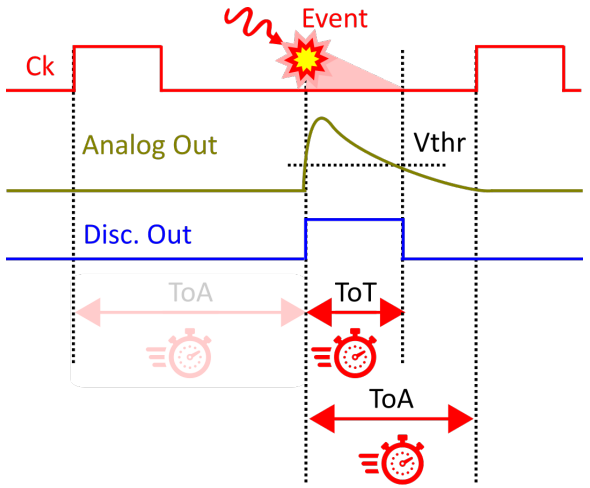
- Constant Fraction Discriminators (CFD) are not simple to implement in channel-dense ICs; in HEP designs, most often ToT measurement (i.e., an indirect coarse measurement of amplitude) is used for offline Time Walk correction. [Other ways of dealing with Time Walk exist, but are rarely used]

Inputs of a TDC

- **Time interval** (T) to be measured is defined by:
  - Width of an input pulse signal (**PulseIN**)
  - Time elapsed between two input steps/pulses (**START** and **STOP**)
- Measurement is referred/calibrated to a high accuracy reference clock (quartz/atomic clock)



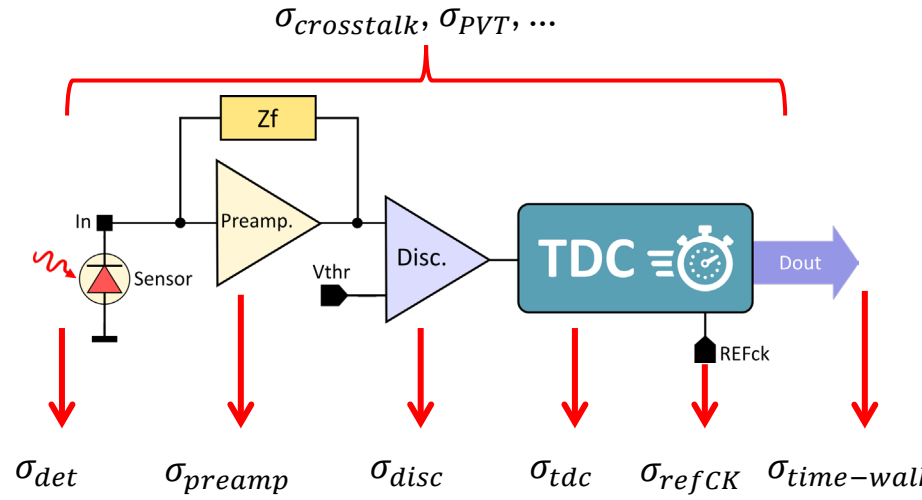
Easily interchangeable; all following TDC architectures can be implemented using either representation



- *ToA – time elapsed between discriminator output rise time and clock edge*
- *ToT – pulse-width of discriminator output*

TDC Performance Metrics

- **Resolution**: quantization step of the conversion, i.e. LSB [ps, ns]
- **Single-Shot Precision (Jitter)**: statistical variation of results for measurement of the same time-interval; expressed as standard deviation (rms) or full width at half maximum (FWHM) [ps, ns]
- **Dynamic Range (Measurement Range)**: maximum time interval that can be measured [ns]
- **Conversion Time (Dead Time)**: minimum time between end of one conversion and the start of next conversion [ps, ns]
- **Conversion Non-Linearities (INL and DNL)**: deviation of the conversion characteristics from the ideal/fitted one [%LSB]
- **Power Consumption** [mW]
- **Area** [µm²]
- **Technology** [nm]
- **Radiation Tolerance** (specific to HEP applications) [TID: Mrad, Grad]



$$\sigma_{single-shot} = \sqrt{\sigma_{det}^2 + \sigma_{preamp}^2 + \sigma_{disc}^2 + \sigma_{refCK}^2 + \sigma_{tdc}^2 + \cdots}$$

$$\sigma_{tdc} \geq \sigma_q = \frac{LSB}{\sqrt{12}}$$

$$\sigma_{av} = \frac{\sigma_{single-shot}}{\sqrt{N_{samples}}}$$

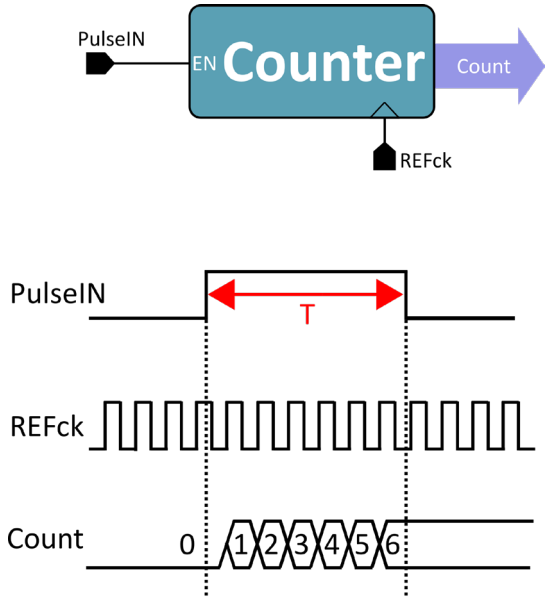
Counter

- Simplest method of measuring time intervals is by using a counter.
- Resolution is given by the period of reference clock: LSB = Tck (1GHz clock → LSB = 1ns)

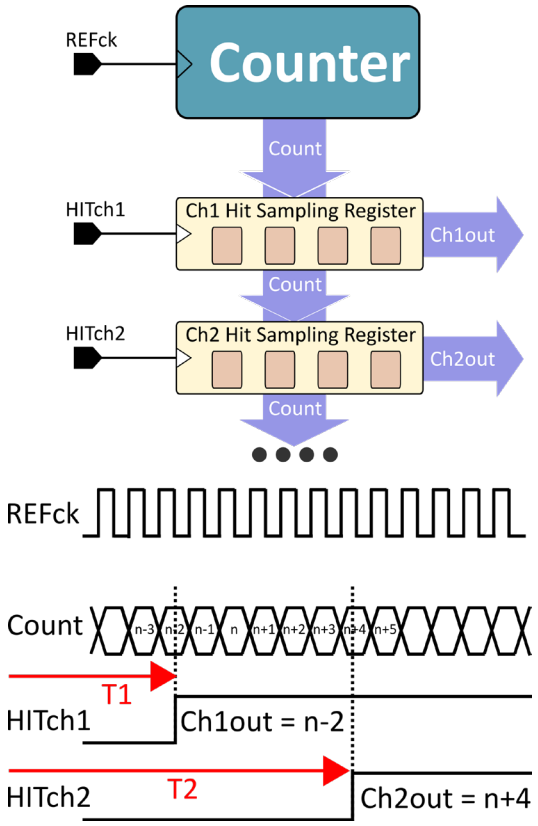
$$\sigma_{tdc} = \frac{T_{CK}}{\sqrt{12}}$$

- Range is defined by number of bits of the counter
- **PROS:** simplicity, reliability, easily extendable range
- **CONS:** resolution limited by clock frequency (not practical for resolutions lower than 1ns)
- Usually employed as a 'coarse' stage to extend the measurement range

- *Local counter in each channel:*

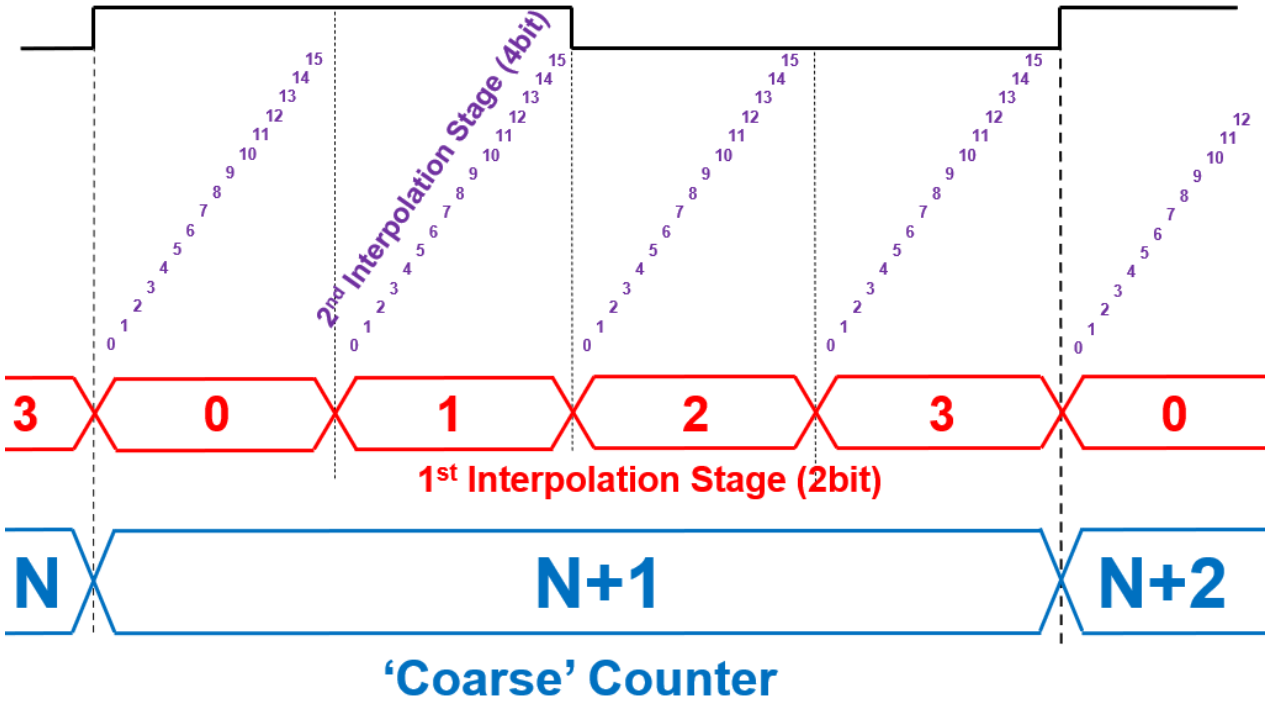


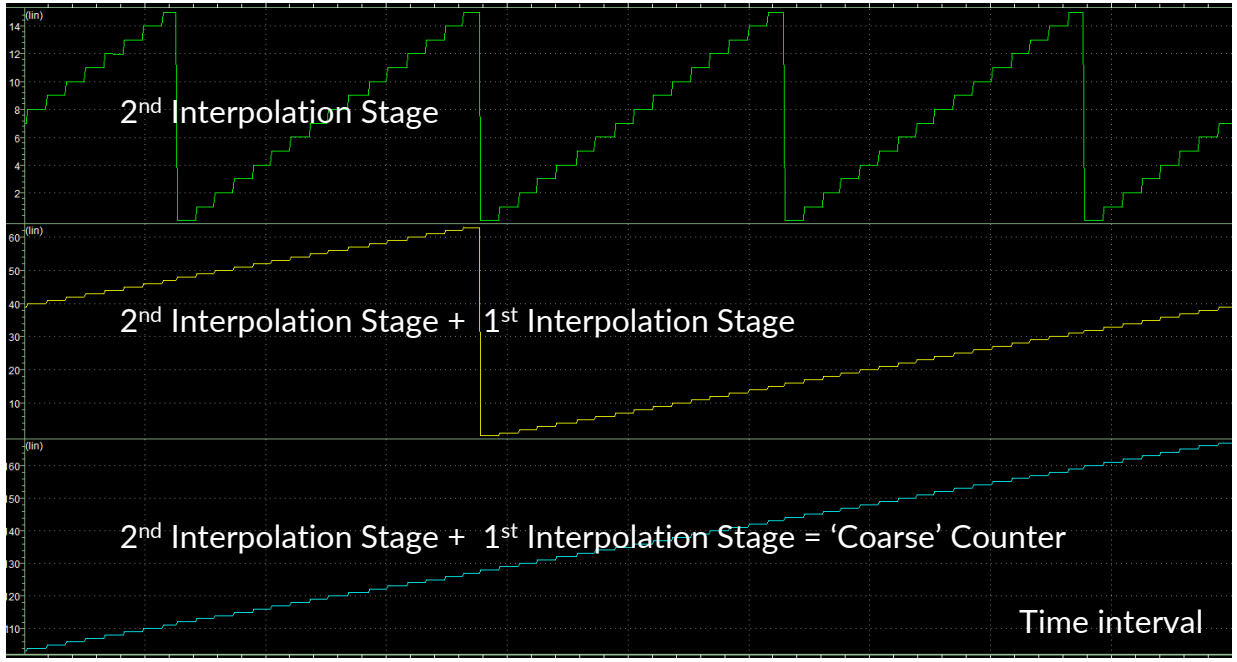
- *Global counter with sampling per channel (grey code and/or synchronization of HIT to CK necessary) :*



Multistage/Interpolating/Nutt-method TDC

- Most **multistage/interpolating** TDCs (sometimes referred to as Nutt method TDCs) use counters as a **'coarse'** stage to extend the dynamic range, while some of the **'fine'** (sub-ns) measurement methods, described in following slides, are used as interpolators to provide high resolution:

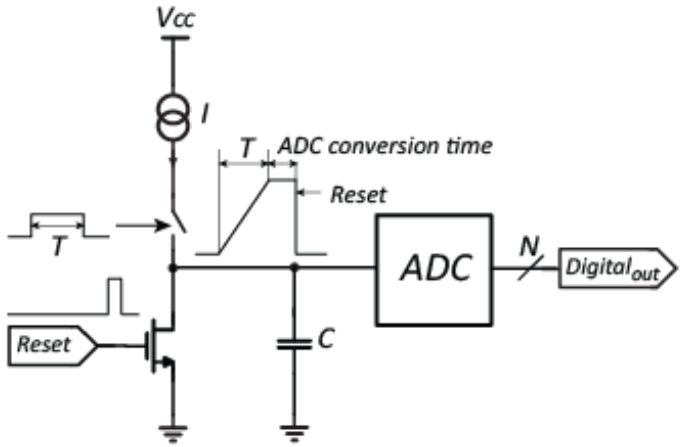




Indirect/Analog 'Fine' Measurement Methods

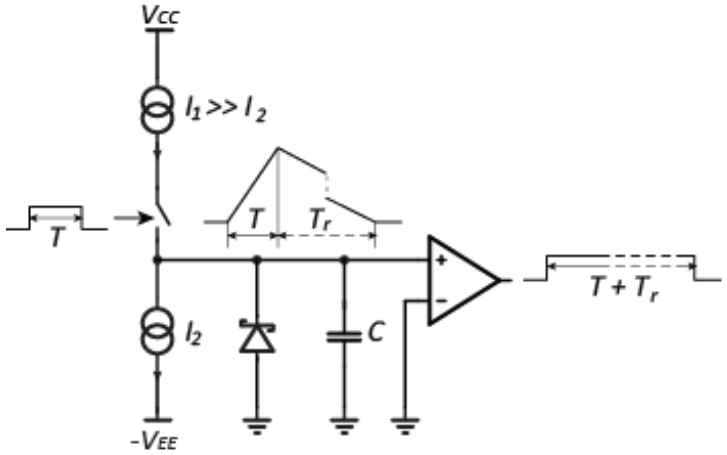
- *This methods perform an indirect conversion of time to digital code by passing through an intermediate step of conversion to an analog voltage.*

- Time-to-Amplitude Converter (TAC) followed by ADC:



- Charging a capacitor with constant current during time interval T performs the conversion to analog voltage that can then be digitized by an ADC. Moves the complexity to ADC domain.
- **CONS:** requires and ADC.

- Dual-Slope Pulse Stretching followed by a Counter:

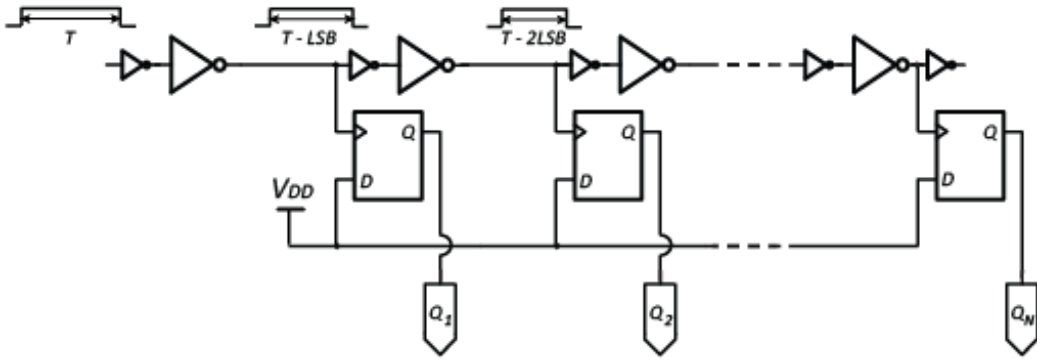


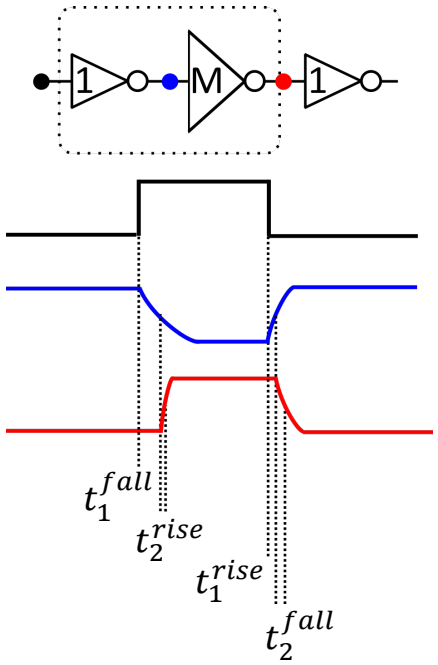
- Charging a capacitor during time interval T and discharging it with much smaller current "stretches" the interval so that it can be accurately measured with a basic counter (similar to dual-slope ADC)
- **CONS:** long conversion time.

- *Architectures used extensively in past but not very suitable for implementation in modern scaled technologies and applications requiring hundreds/thousands of channels/pixels.*

Direct/Digital 'Fine' Measurement Methods: Pulse Shrinking

- Pulse Shrinking:





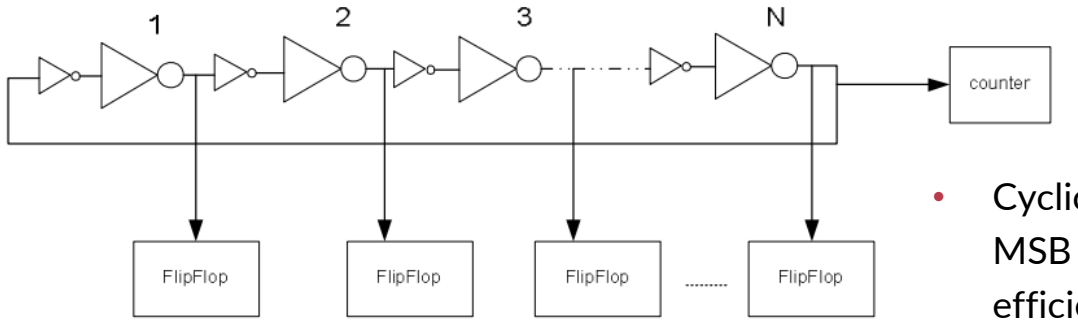
- Unequal rise/fall times between two inverters that compose the elementary cell (buffer) perform shrinking of the pulse-width by the quantity:

$$LSB = \left(t_1^{fall} + t_2^{rise}\right) - \left(t_1^{rise} + t_2^{fall}\right)$$

- This LSB can theoretically be arbitrarily small (not limited by technology logic propagation delay)
- Dynamic range (DR) is given by number of elementary cells (N) multiplied by LSB (thermometric scale → area inefficient):

$$DR = N \cdot LSB$$

- Cyclic Pulse Shrinking:



6-bit conversions requires 64 cells and 64 flip-flops in the regular pulse-stretching method; cyclic configuration can use just 4 cells and 4+4=8 flip-flops

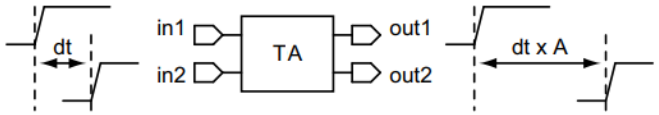
- Cyclic configuration allows to extend the dynamic range by delegating the MSB part of the conversion result to a counter (binary representation → area efficient). Still DR is limited by total propagation delay of the loop:

$$DR = N \cdot t_p \quad \textit{where } t_p \textit{ is cell propagation delay and } t_p > LSB$$

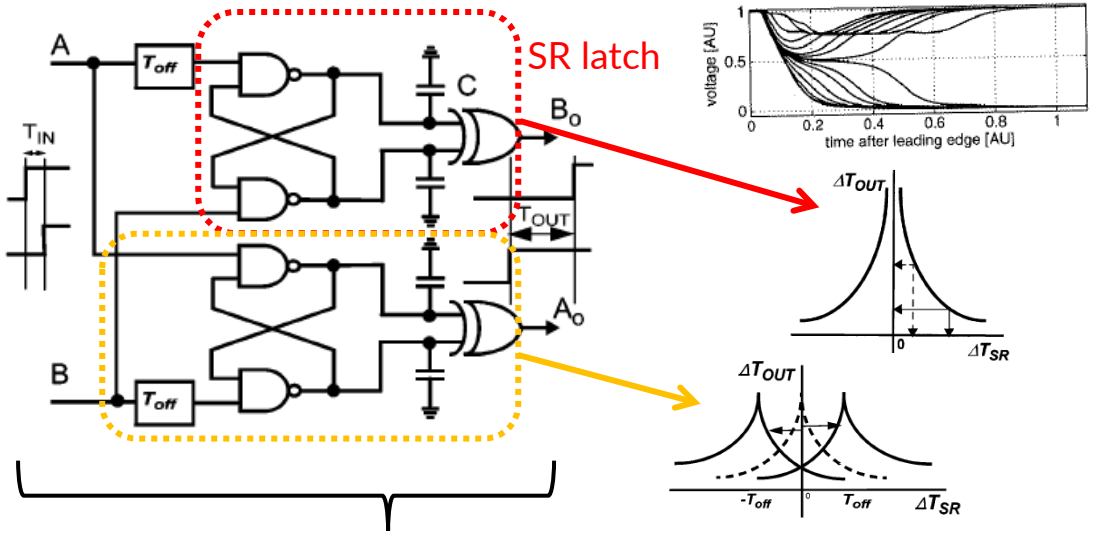
- While LSB can be smaller than technology propagation delay, pulse stretching is used less often than Vernier delay lines due to difficulty of maintaining the rise/fall time ratios with PVT variations.

Direct/Digital 'Fine' Measurement Methods: Time Amplifiers

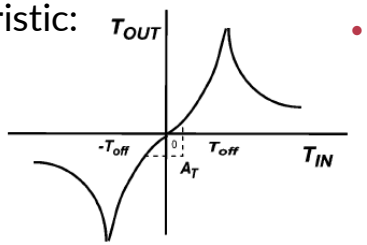
- Amplifies the time interval relaxing the LSB requirements of the following stage (counter or another 'fine' time measurement method like delay lines etc.)



- **SR latch based TA** – exploits the input dependent propagation delay of a SR latch in metastable region:

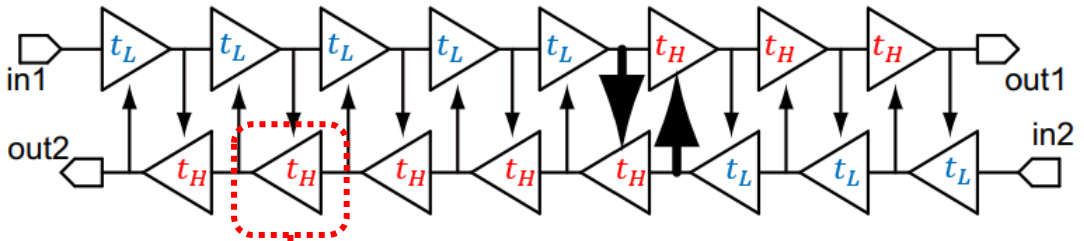


TA Characteristic:

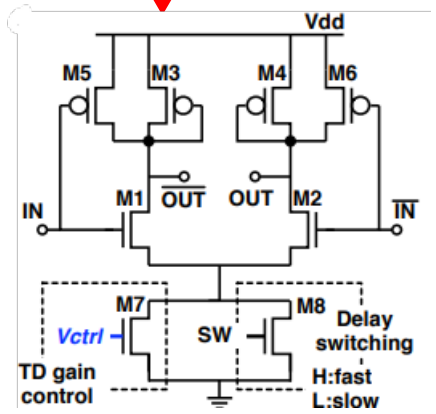


- **CONS:** very limited linear range; gain not well predictable → necessitates calibration; hard to use in practice

- **Cross-coupled Delay Line TA** – delay cells with two possible propagation delays (low t_L and high t_H); two delay lines where cells in one switch the delay of corresponding cell in the other line from low to high delay:



Delay Cell example:

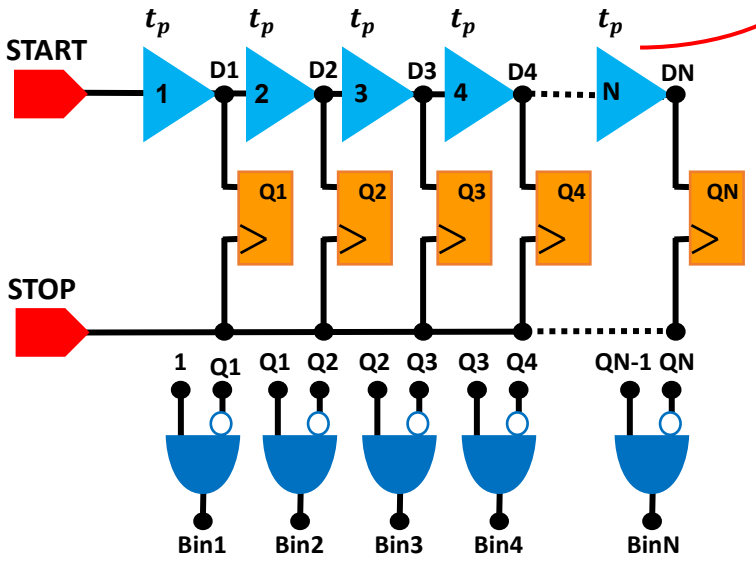


$$Gain = \frac{t_H}{t_L}$$

- DLL used to fix propagation delays against PVT variations
- **CONS:** long dead-time

Direct/Digital 'Fine' Measurement Methods: Delay Line

- Majority of modern TDCs is based on some variation of a Delay-Line structure.
- Regular (Tapped) Delay Line:



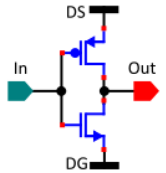
- TDC resolution given by the propagation delay of the elementary cell:

$$LSB = t_p$$

$$DR = N \cdot LSB$$

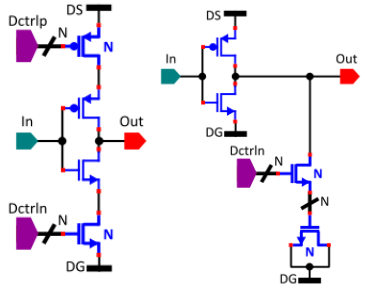
- Basic element: **Delay Cell**

  - Simple Logic

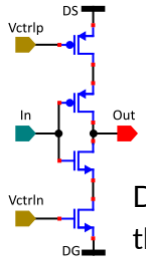


    - Used in FPGA TDCs (carry chain mux, etc.)
    - Requires constant calibration

  - Digitally-Controlled Delay Cell:

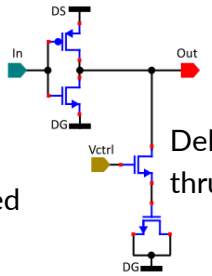


  - **Voltage-Controlled Delay Cell (VCDC):**
    - Current starved:



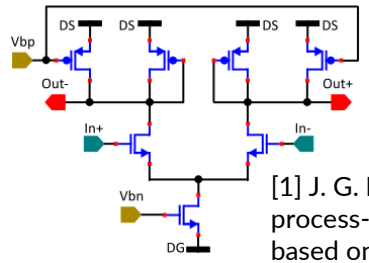
Delay controlled thru current

    - Shunt capacitor:



Delay controlled thru load

    - Differential delay cell with symmetric loads (Maneatis cell [1]):



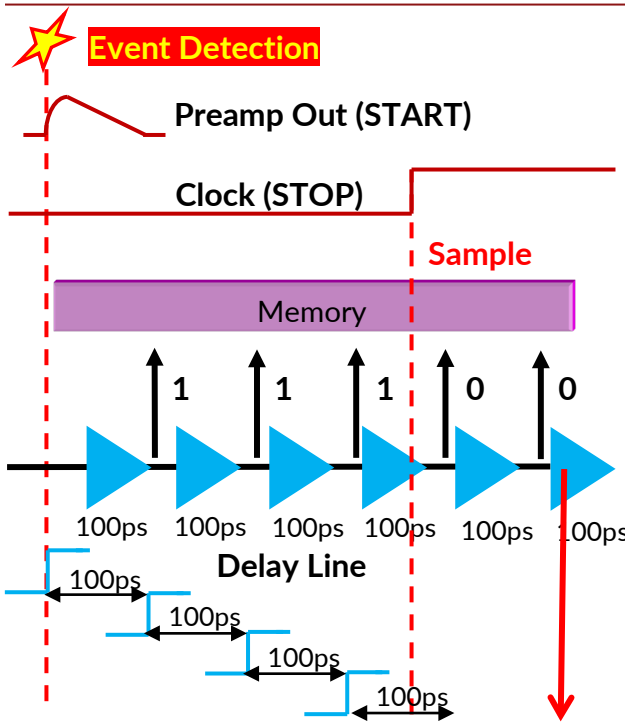
      - Frequently used in PLL VCOs and DLLs
      - Consumes Static Bias Current

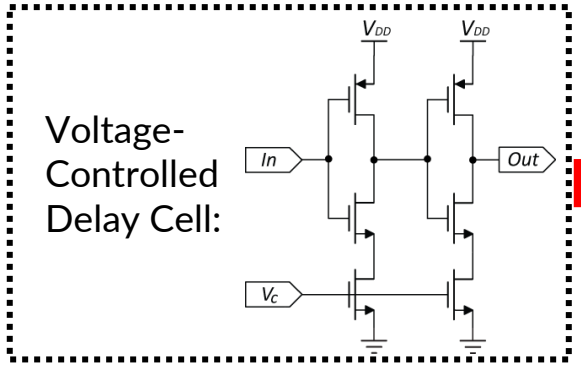
[1] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," IEEE J. Solid-State Circuits, vol. 31, no. 11, pp. 1723–1732, Nov. 1996.

Fully Digital - minimum delay limited by fastest achievable logic propagation delay in target technology

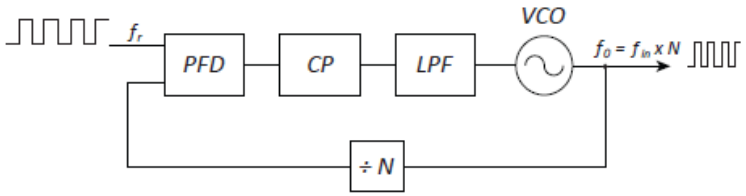
Rise & fall times (pmos & nmos strength) do not match well over PVT variations → single inverters are less often used as delay cells; usually series of 2 inverters or differential buffers are used as delay elements → propagation delay doubles

VCDC propagation delay control: trimming, PLL, DLL

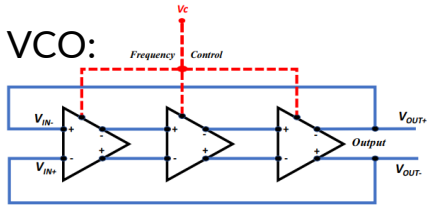




- Trimming using resistor voltage dividers or DACs – open loop control → delay value varies with PVT variations → necessitates frequent recalibration (usually used for off-chip Vctrl control during prototype characterization)
- Phase-Locked Loops (PLL) - closed loop: PLL acts on Vctrl in order to lock the VCO (Voltage-Controlled Oscillator) **frequency** to a desired value regardless of PVT variations.

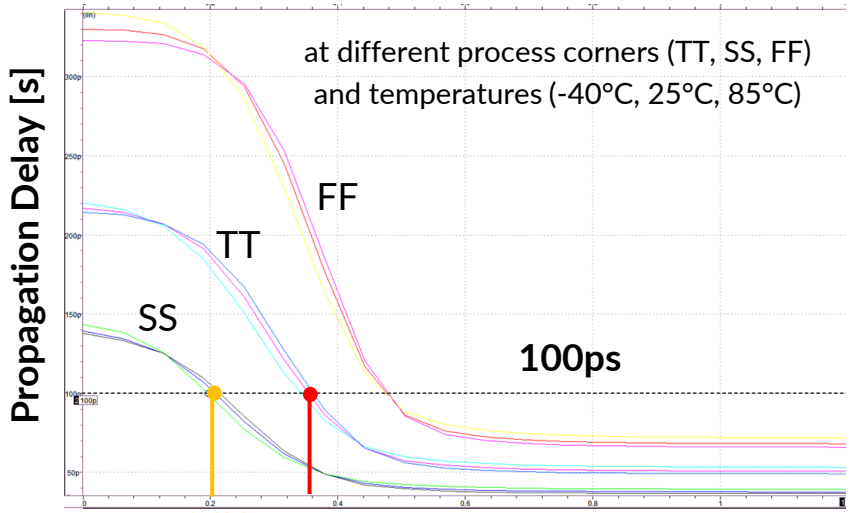


VCO:

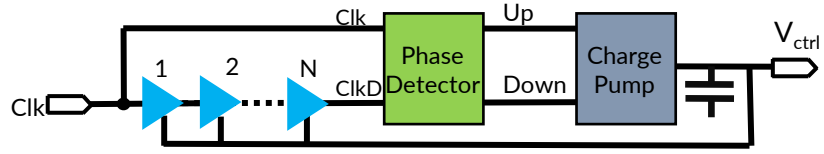


$$t_{p_DelayCell} = \frac{1}{f_{VCO} \cdot N_{cellsVCO}}$$

Voltage-Controlled Delay Cell Characteristic:



- Delay-Locked Loops (DLL) - closed loop: DLL acts on Vctrl in order to lock **delay** line propagation delay to the period of input clock regardless of PVT variations.

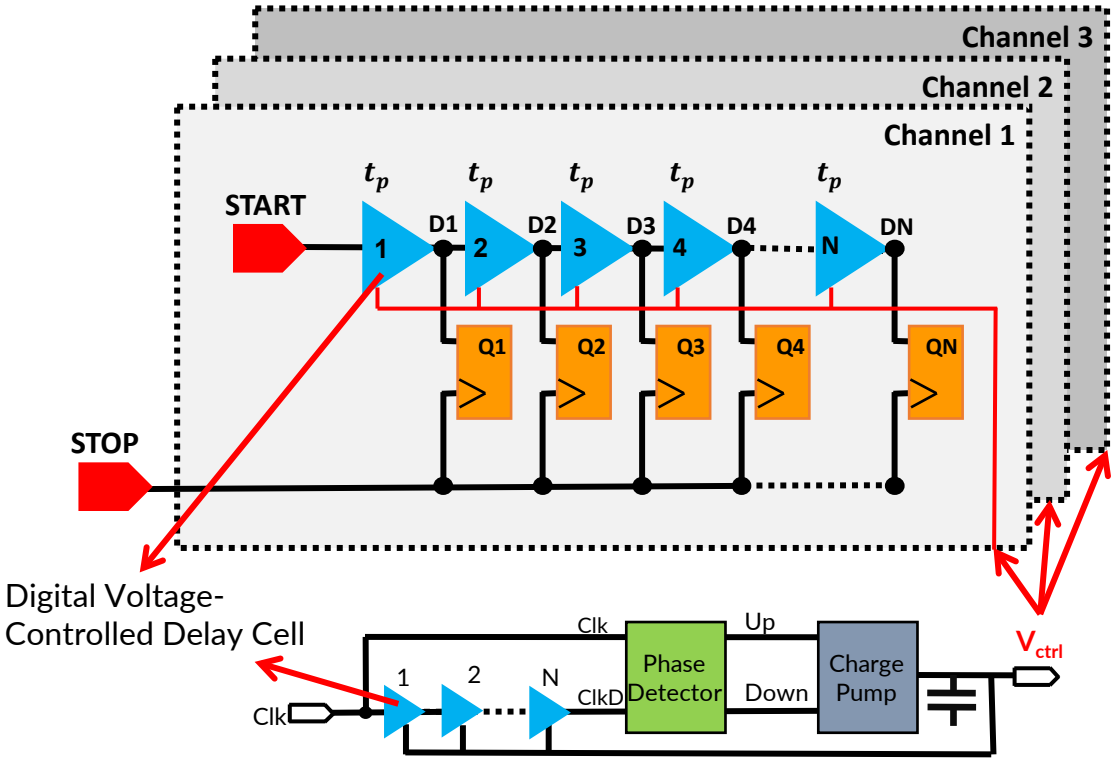


$$t_{p_DelayCell} = \frac{T_{CK}}{N}$$

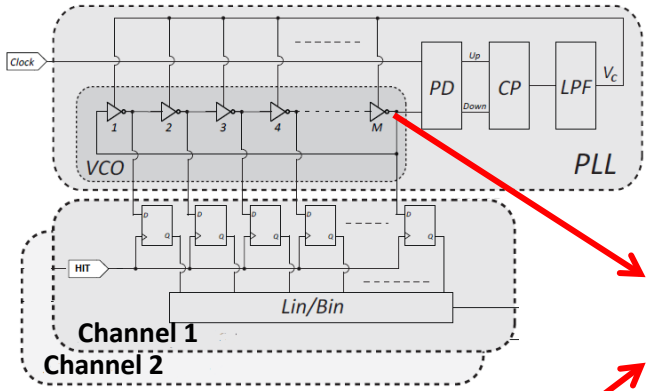
- Most widely used method for VCDC delay control;
- Simpler than PLLs; usually one dominant pole;
- Doesn't filter input clock jitter
- False Locking Issue.

Delay Line, Multiphase Clock

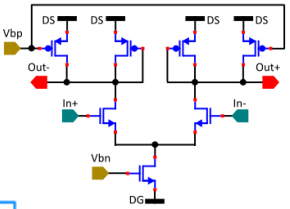
- Delay Line per channel/pixel, global DLL generates Vctrl that is propagated to each channel (most common approach for high channel count implementations):
  - Mismatch (process, supply) between DLL delay cells and channel delay cells is a possible issue



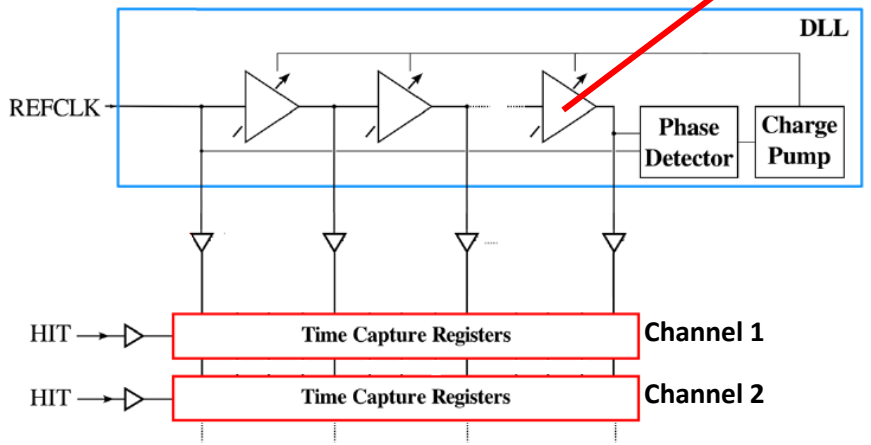
- Global DLL or PLL provides multiphase clock that is propagated and sampled in correspondence of each channel/pixel HIT event:
  - PLL-based multiphase:



Differential Voltage-Controlled Delay Cell:



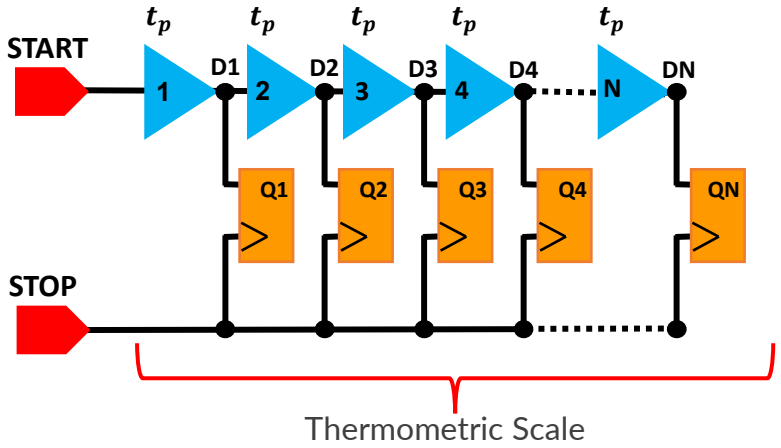
  - DLL-based multiphase:



- DLL-multiphase TDC per channel/pixel. Theoretically best delay accuracy but usually power and area prohibitive

Delay Line Configurations

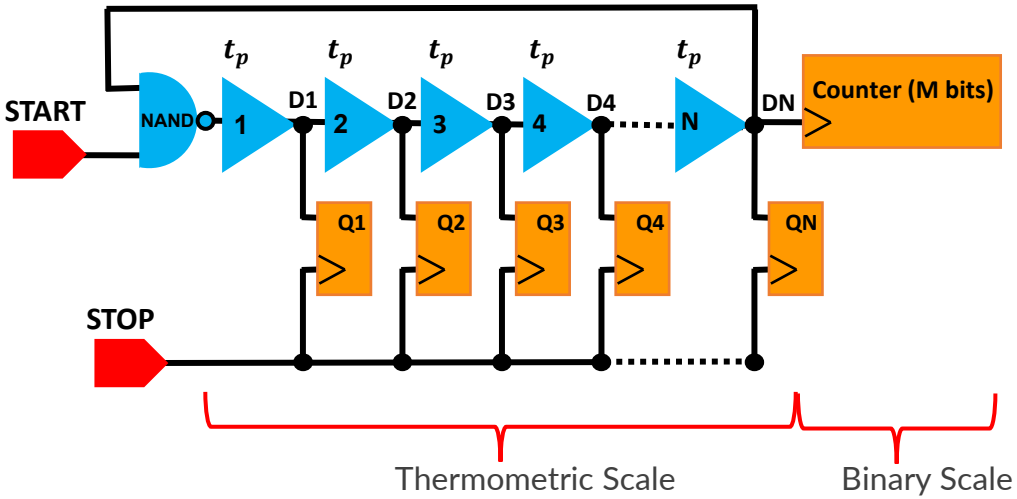
- (Regular/Linear) Delay Line:



$$LSB = t_p$$

$$DR = N \cdot LSB$$

- Ring Oscillator:

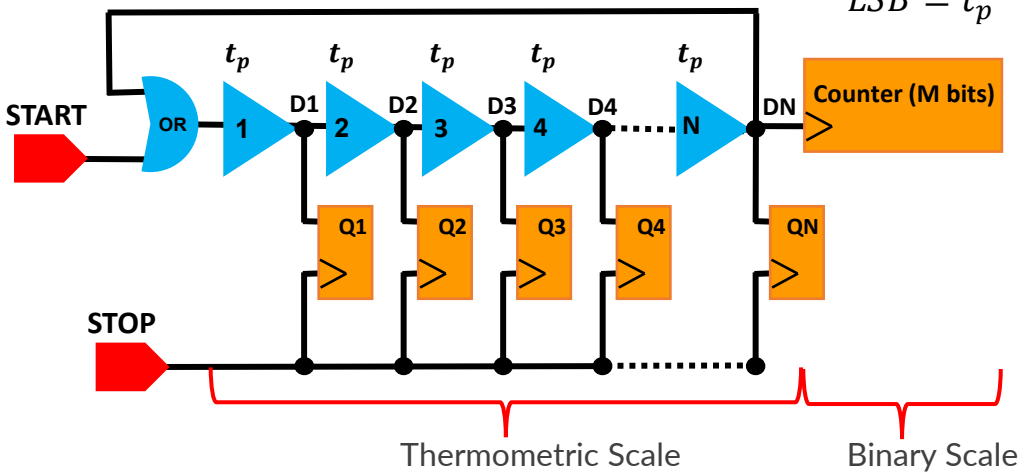


$$LSB = t_p \qquad DR = (N + 2^{M+1}) \cdot LSB$$

- Timing on both rising and falling edges; unequal rise/fall times introduce non-linearities (issue relaxed/avoided with differential / pseudo-differential delay cells)
- Bringing signal back to the input causes non-linearity (wider bin/bins)
- Special versions of the Ring Oscillator:
  - Gated Ring Oscillator (GRO);
  - Switched Ring Oscillator (SRO).

  Perform noise shaping; require repetitive measurement o the time-interval (ADPLL)

- Cyclic Delay Line:



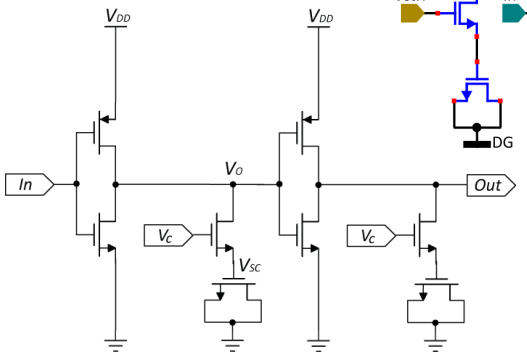
$$LSB = t_p \qquad DR = (N + 2^M) \cdot LSB$$

- Timing always on the same edge
- Bringing signal back to the input causes non-linearity (wider bin/bins)
- START pulse-width must be lower than $N \cdot t_p$. Unequal rise/fall times cause pulse-shrinking or pulse-stretching → limits maximum number of cycles before the pulse is lost; requires pulse-width regeneration (issue relaxed with differential / pseudo-differential delay cells)

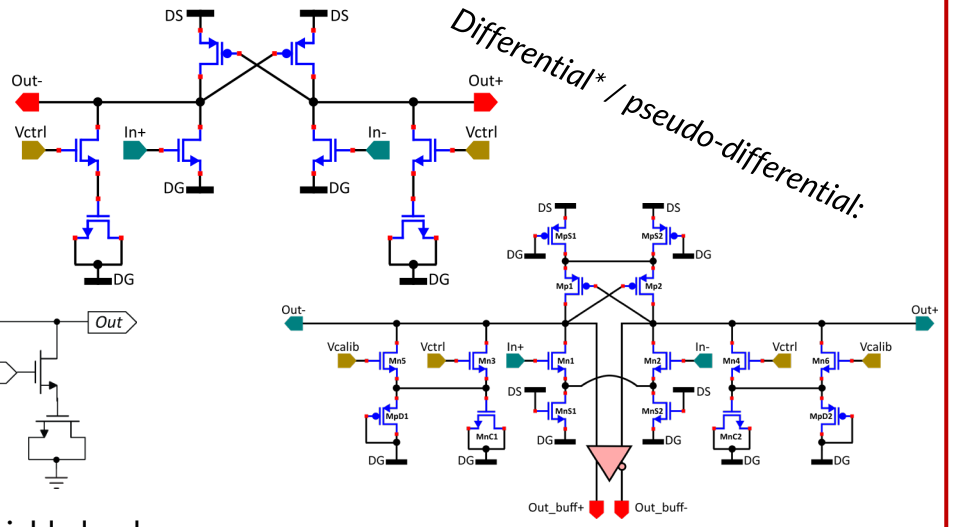
Digital Voltage-Controlled Delay Cells

❑ Shunt-Capacitor Delay Cell:

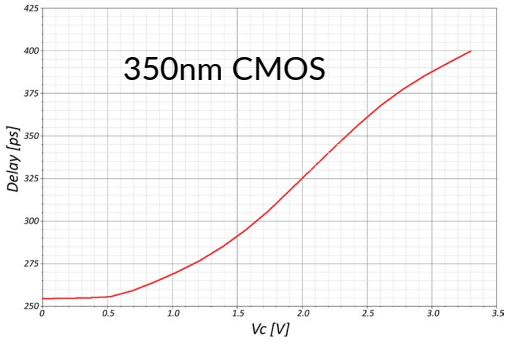
Single-ended:

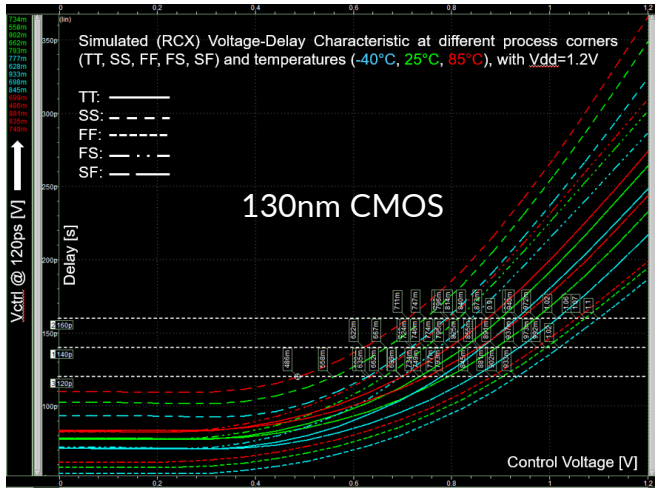


Differential / pseudo-differential:*



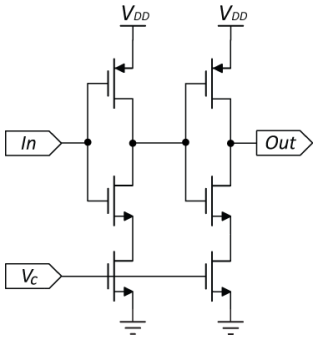
- Delay controlled thru variable load
- **PROS**: more contained and linear voltage-delay characteristic.
- **CONS**: bigger area.



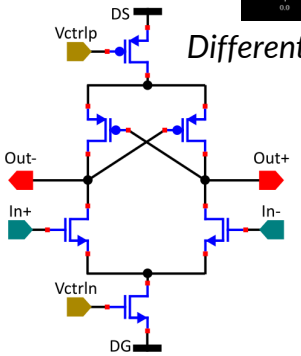


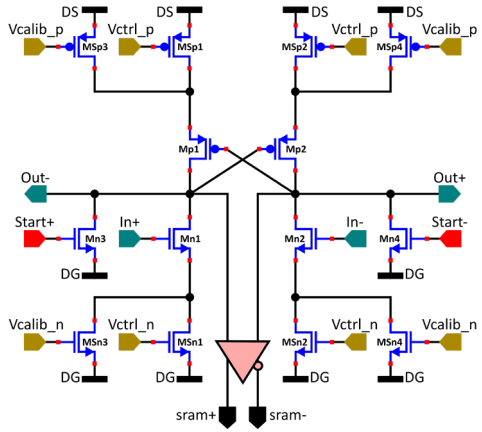
❑ Current-Starved Delay Cell:

Single-ended:

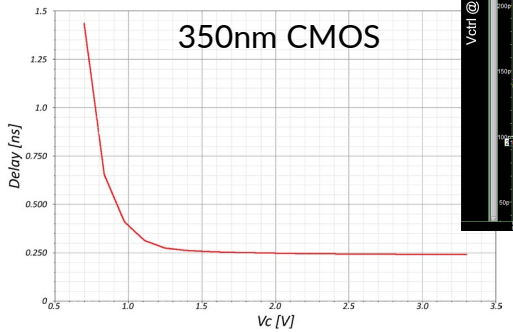


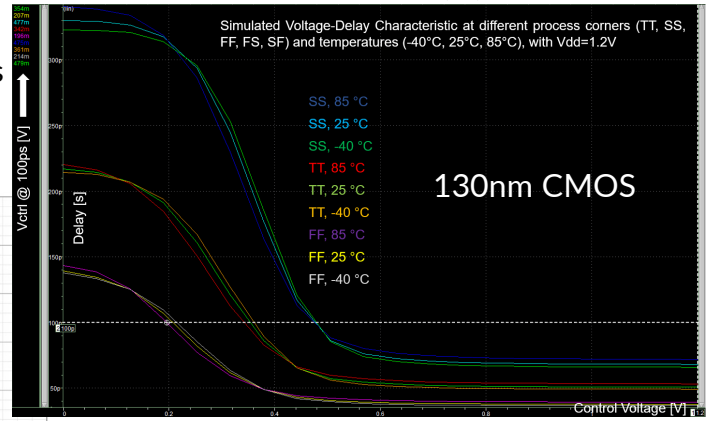
Differential / pseudo-differential:*

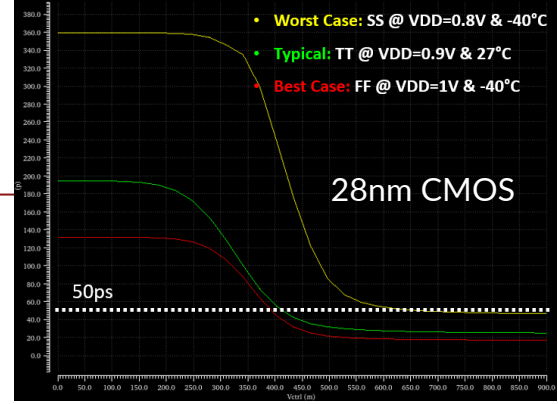




- Delay controlled thru variable current (nmos side, pmos side, both)
- **PROS**: smaller area.
- **CONS:** highly non-linear voltage-delay characteristics (less pronounced in newer/scaled technologies)



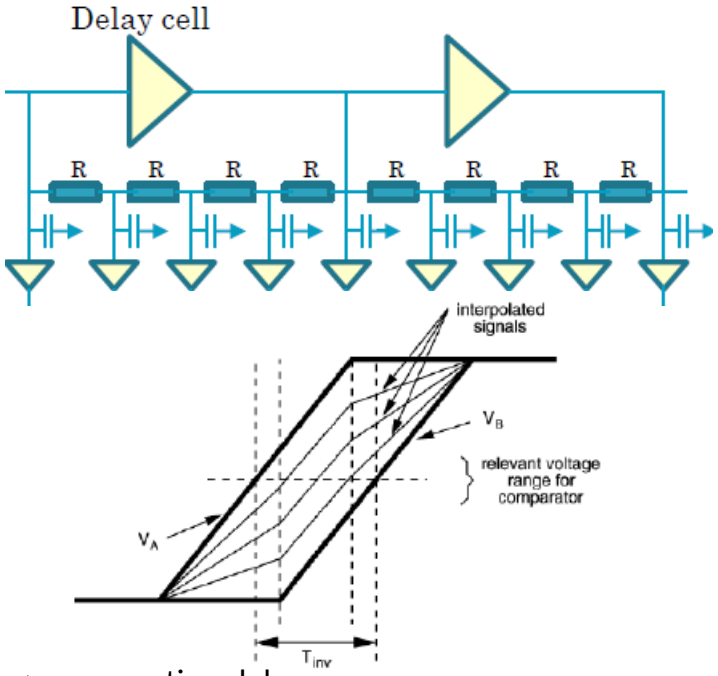




**Differential Cascode Voltage Switch Logic (DCVSL)*

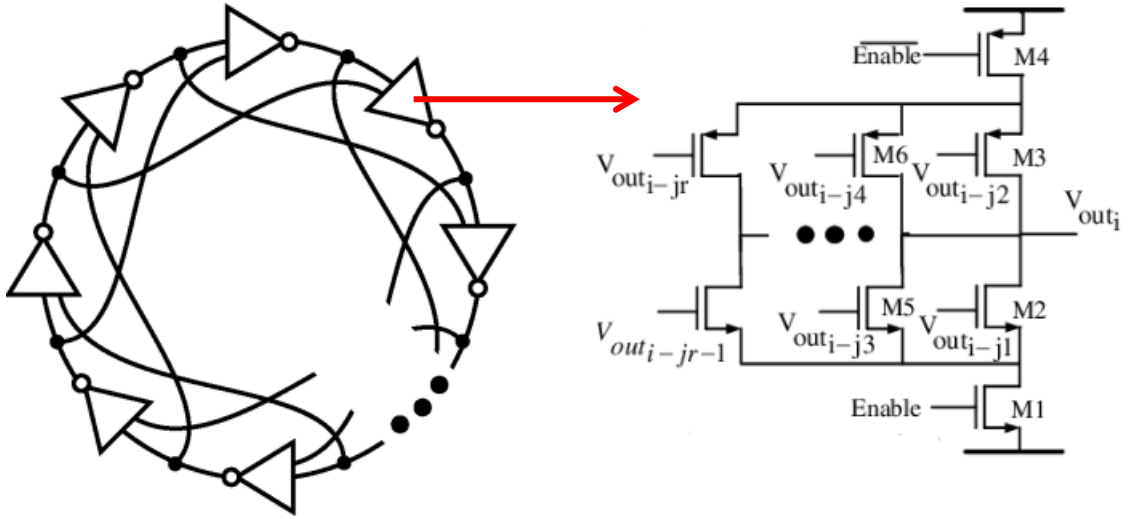
Direct/Digital 'Fine' Measurement Methods: Sub-gate delay

- Resistive interpolation across neighboring delay cells:



- Rise time > propagation delay
- Parasitic capacitances make this resistive division a mixture of R division and RC delays:
  - Low resistor values required to prevent RC component from dominating;
  - With equal resistances the bins are not evenly spaced; needs optimization of individual resistors
  - Does not fully auto-scale with propagation delay of the cell

- Multipath Delay Cells:

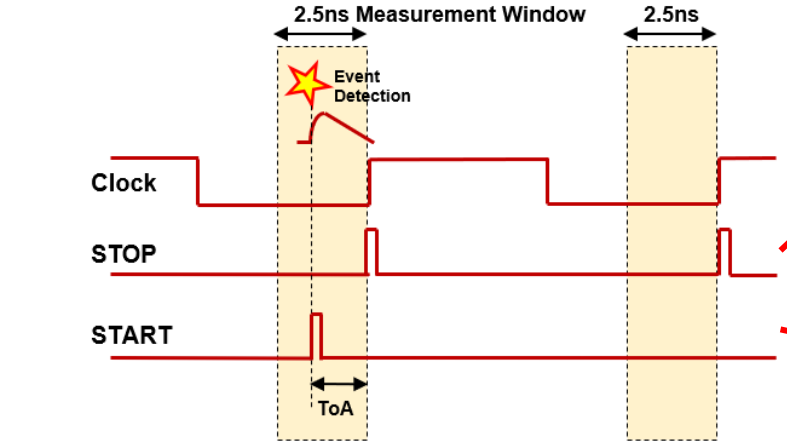


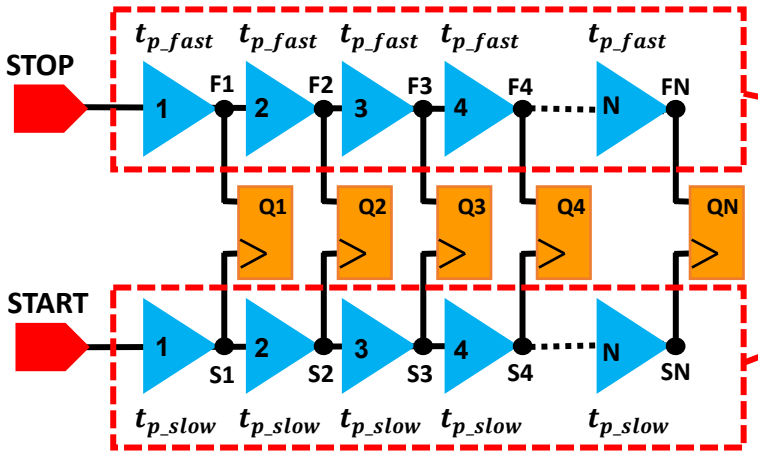
- Requires constant operation/oscillation or gated ("freezing" of charge on internal nodes) function (i.e. GRO) with repetitive/periodic measurements of the time intervals. Used in ADPLL applications but not very suitable for single-shot measurements with rare events (like most HEP applications).

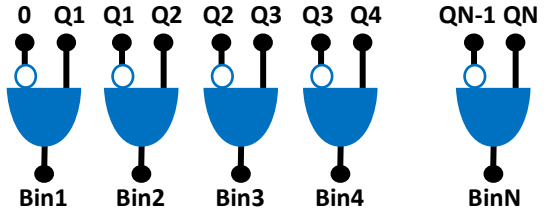
- **Vernier Delay Line**
  - Resolution not based on propagation delay of a single cell but on the difference of propagation delays of two delay cells → LSB smaller than logic gate delay in the target technology is possible

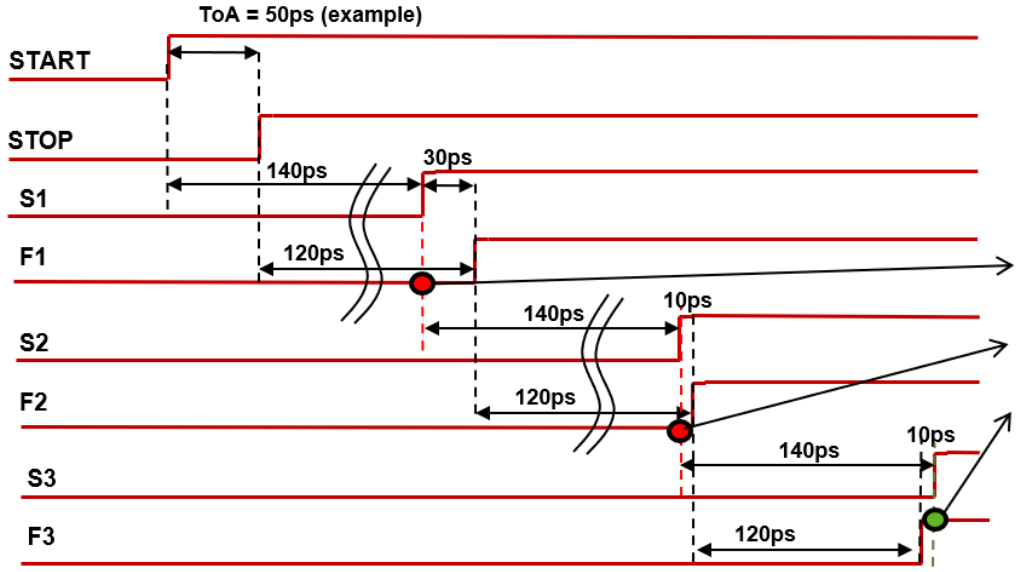
More on the next slide

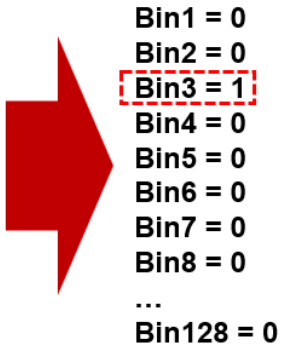
Vernier Delay Line











- **START** signal propagates in the **Slow Delay Line** ($t_{p_slow} > t_{p_fast}$)
- **STOP** signal propagates in the **Fast Delay Line**

- The **START** pulse comes first and initializes the TDC operation.
- The **STOP** pulse follows the **START** with a delay that represents the time interval to be digitalized.
- At each tap of the Delay Line the **STOP** signal catches up to the **START** signal by the deference of the propagation delays of cells in Slow and Fast branches, i.e., $t_{p_slow} - t_{p_fast}$ represents the **LSB** of time measurement.
- The number of cells necessary for **STOP** signal to surpass the **START** signal represents the result of TDC conversion.

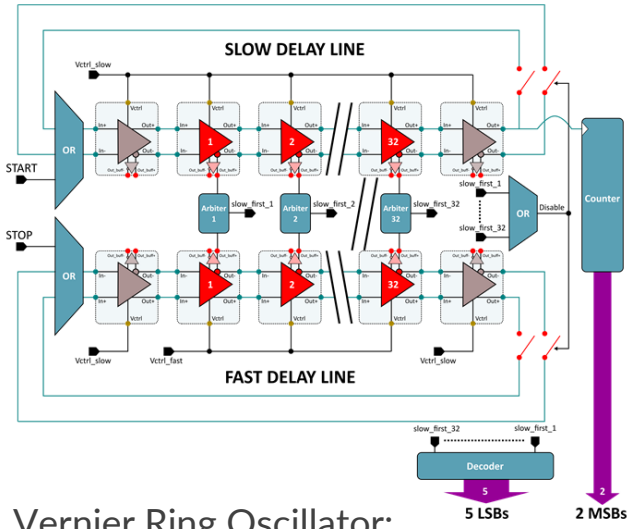
$$LSB_{TDC} = t_{p_slow} - t_{p_fast}$$

$$DR = N \cdot LSB$$

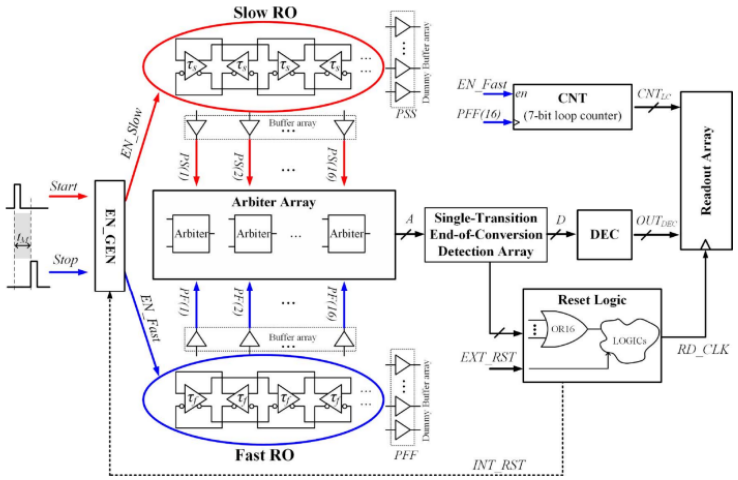
- As with the regular delay line, cyclic and oscillator configurations possible.

Vernier Delay Line – Variants:

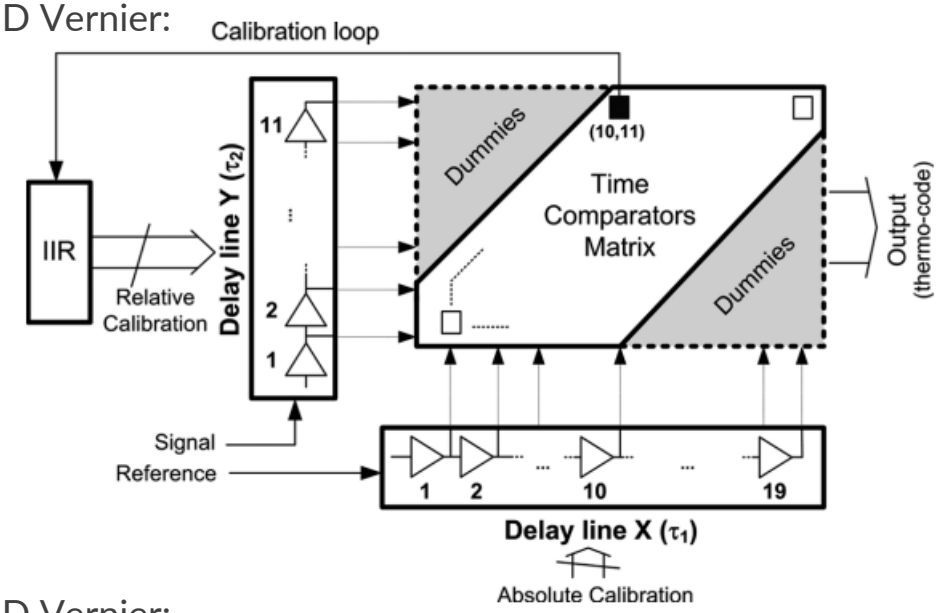
- Cyclic Vernier Delay Line:



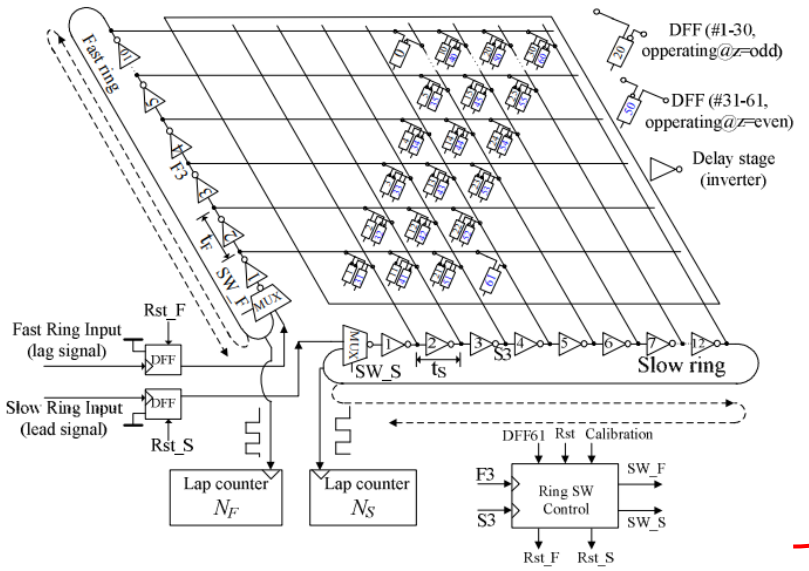
- Vernier Ring Oscillator:



- 2D Vernier:



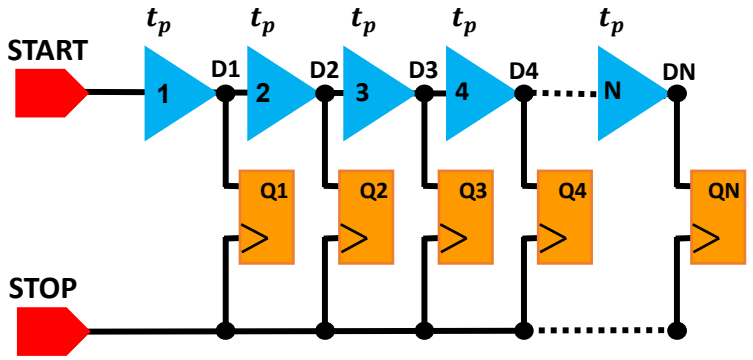
- 3D Vernier:



Extends range, lowers area, power consumption and conversion time compared to traditional linear Vernier delay line

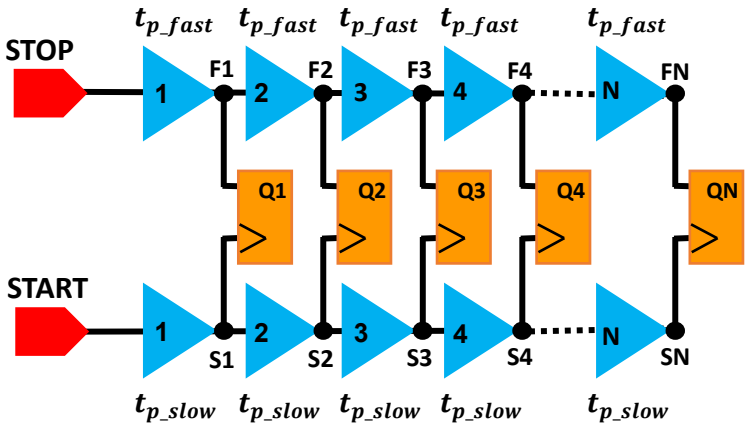
Regular VS Vernier Delay Line (1/3)

❑ Regular (Tapped) Delay Line:



VS

❑ Vernier Delay Line:



- Simpler
- Resolution (LSB) limited by technology
- Smaller Area
- Shorter Conversion Time (independent on time interval being measured)
- Lower Power Consumption

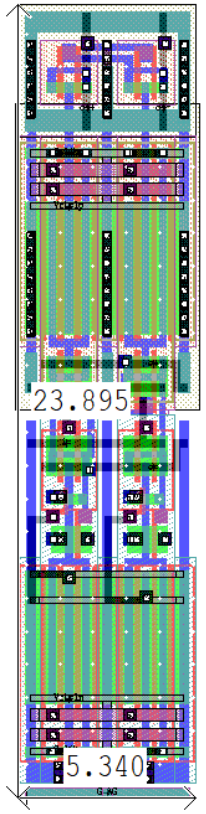
- More complex
- Resolution (LSB) not limited by technology
- Bigger Area:
  - 2 delay lines instead of one
  - Bigger delay cells due to more stringent mismatch requirements
- Longer Conversion Time (dependent on time interval being measured)
- Higher Power Consumption

Regular VS Vernier Delay Line (2/3)

- Regular (Tapped) Delay Line:

Tixel (130nm CMOS; 100ps resolution)

Delay Cell Layout [area ≈ 127.6µm²]:

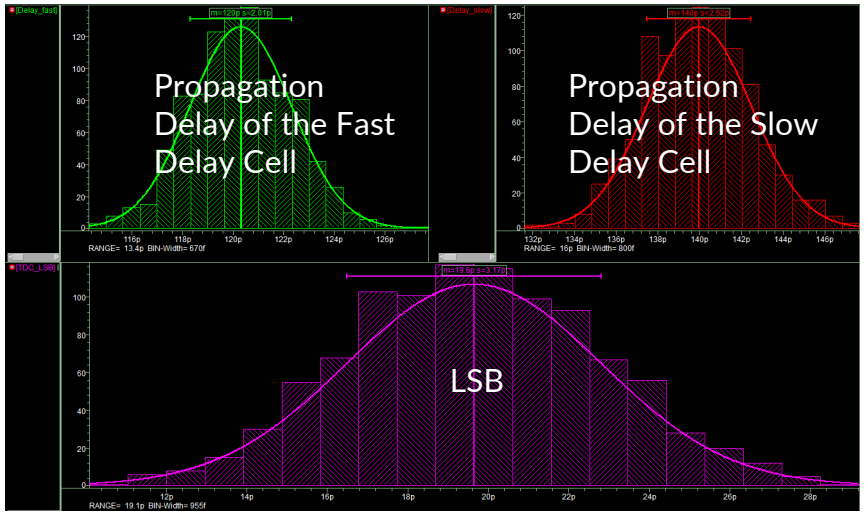


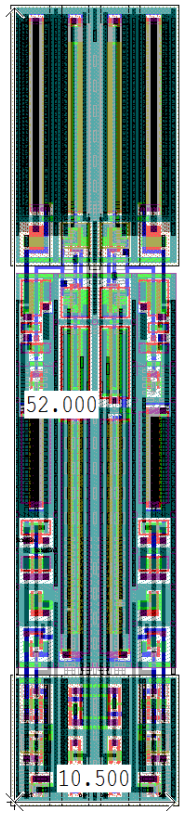
VS

- Vernier Delay Line:

Altiroc (130nm CMOS; 20ps resolution)

Delay Cell Layout [area ≈ 546µm²]:



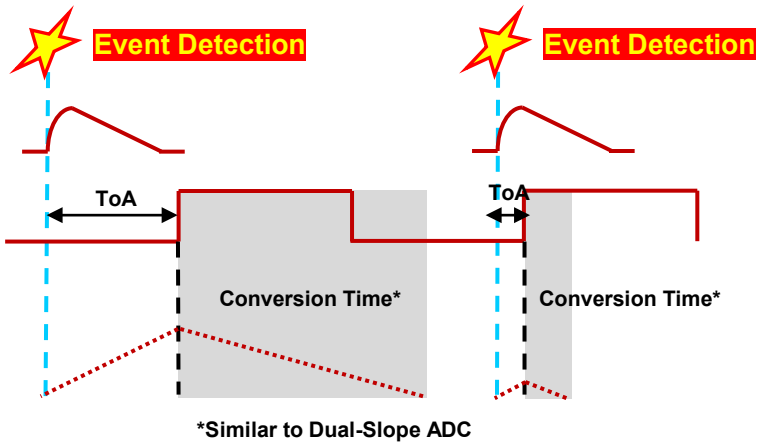


- Simpler
- Resolution (LSB) limited by technology
- Smaller Area
- Shorter Conversion Time (independent on time interval being measured)
- Lower Power Consumption

- More complex
- Resolution (LSB) not limited by technology
- Bigger Area:
  - 2 delay lines instead of one
  - Bigger delay cells due to more stringent mismatch requirements
- Longer Conversion Time (dependent on time interval being measured)
- Higher Power Consumption

Regular VS Vernier Delay Line (3/3)

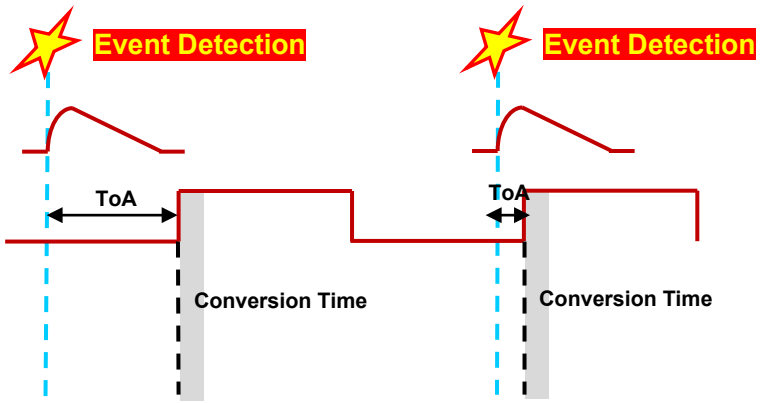
❑ Regular (Tapped) Delay Line:



- Simpler
- Resolution (LSB) limited by technology
- Smaller Area
- Shorter Conversion Time (independent on time interval being measured)
- Lower Power Consumption

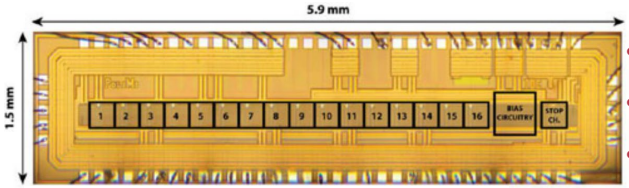
VS

❑ Vernier Delay Line:

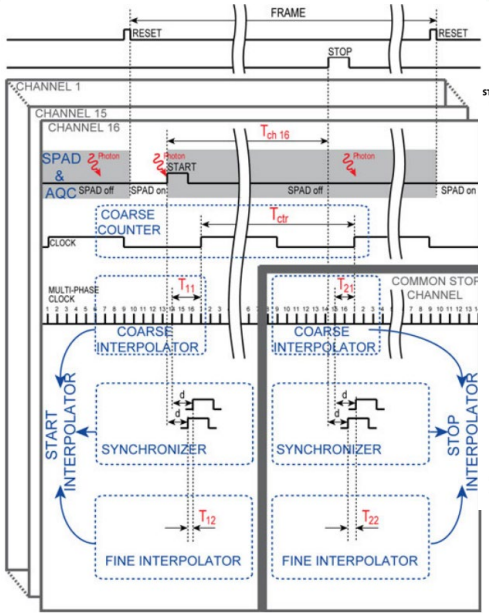


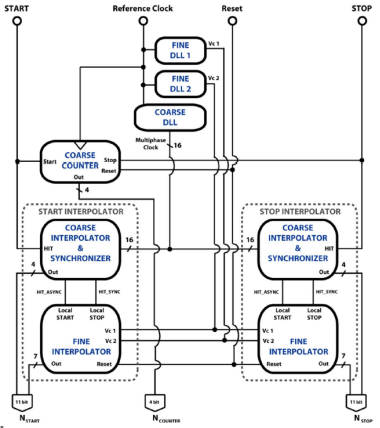
- More complex
- Resolution (LSB) not limited by technology
- Bigger Area:
  - 2 delay lines instead of one
  - Bigger delay cells due to more stringent mismatch requirements
- Longer Conversion Time (dependent on time interval being measured)
- Higher Power Consumption

Examples of different TDC architectures:



- 350nm CMOS
- Resolution: 10ps
- Range: 160ns
- 16 channels

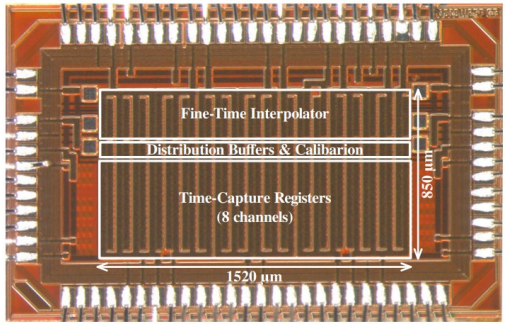




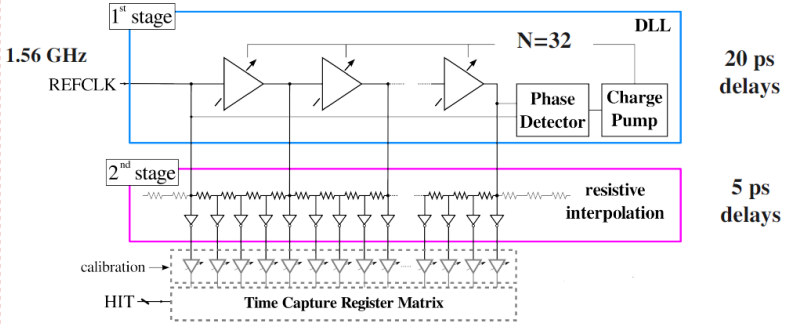
- Global DLL generates multiphase clocks

- 'Coarse' Counter, multiphase clock sampling (1st interpolation stage) and Cyclic Vernier DI (2nd interpolation stage) per channel
- 2 additional global DLLs for Vernier stage biasing

D. Tamborini, B. Markovic, F. Villa and A. Tosi, "16-Channel Module Based on a Monolithic Array of Single-Photon Detectors and 10-ps Time-to-Digital Converters," in *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 20, no. 6, pp. 218-225, Nov.-Dec. 2014, Art no. 3802908, doi: 10.1109/JSTQE.2014.2327797.

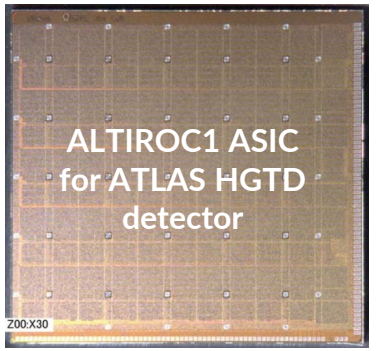


- 130nm CMOS
- Resolution: 5ps
- Range: 640ps
- 8 channels



- Global DLL with resistive interpolation generates multiphase clocks
- Multiphase clock sampling per channel

L. Perktold and J. Christiansen, "A fine time-resolution (≪ 3 ps-rms) time-to-digital converter for highly integrated designs," *2013 IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*, 2013, pp. 1092-1097, doi: 10.1109/I2MTC.2013.6555583



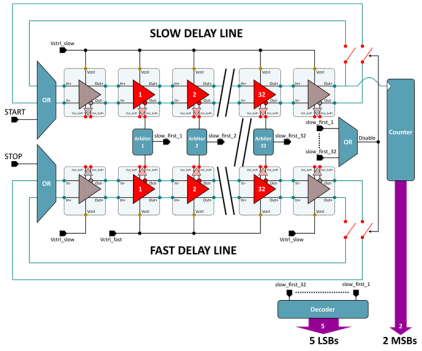
- 130nm CMOS
- Resolution: 20ps (TOA), 40ps/160ps (TOT)
- Range: 2.5ns TOA, 20n TOT
- 5x5=25 channels (altiroc1)
- 15x15=225 channels (altiroc2)

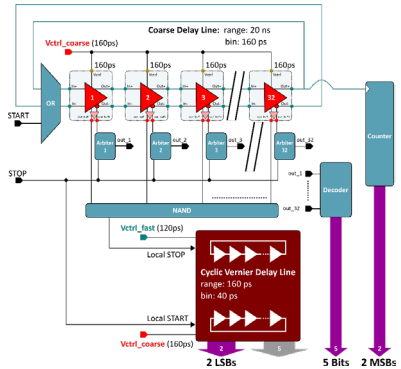
TOA TDC:

- Cyclic Vernier Delay Line

TOT TDC:

- Cyclic Delay Line with Vernier Delay Line interpolation





- TOA and TOT TDCs inside each pixel
- 3 Global DLLs

B. Markovic *et al.*, "ALTIROC1, a 20 ps time-resolution ASIC prototype for the ATLAS High Granularity Timing Detector (HGTD)," *2018 IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings (NSS/MIC)*, 2018, pp. 1-3, doi: 10.1109/NSSMIC.2018.8824723

Some design considerations

- Simpler is better
  - Alignment between interpolation stages is not trivial and must be done with the precision of the final resolution.
  - Stacking multiple interpolation stages one after the other allows for reduced area, power consumption and conversion time, but must be done with care (1 or 2 interpolation stages are usually enough; more than 3 is extremely tricky).
- With technology scaling routing/parasitic contributions to propagation delay are becoming more and more pronounced
- Routing of timing critical signals must be done with care
- For ps-level designs device mismatches (both systematic and statistical) can have major impact on the performances

- Perfectly aligned 'Coarse' and 'Fine' Stages:

- Effect of offset in the connection between 'Coarse' and 'Fine' stages:

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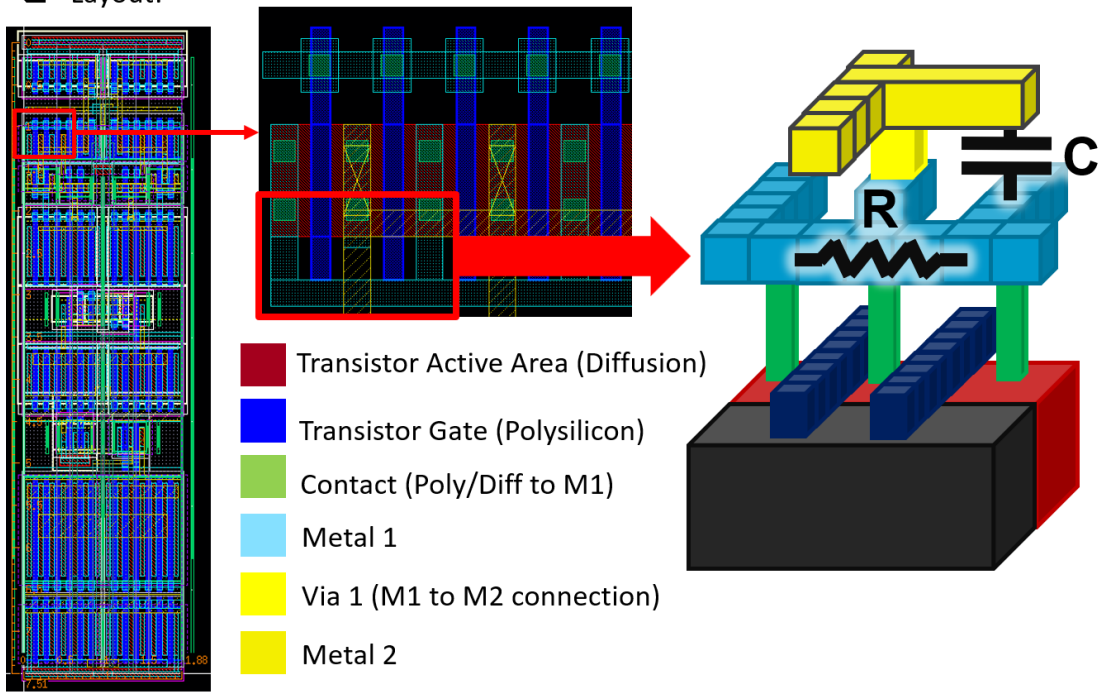
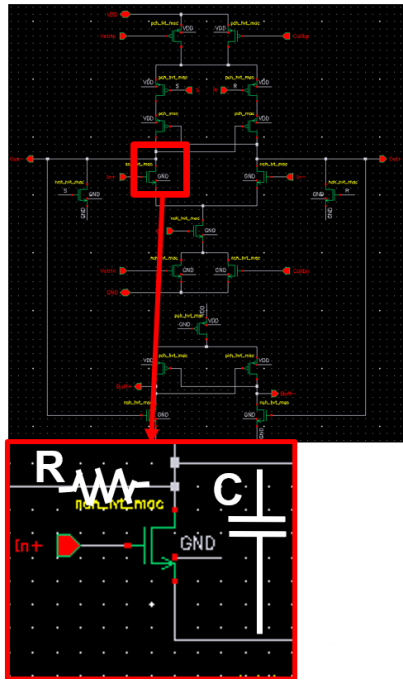
- Layout:



- Schematic:



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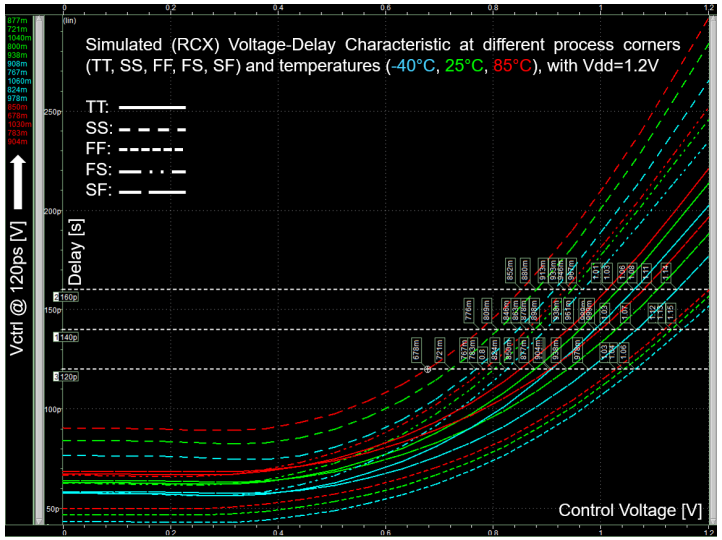
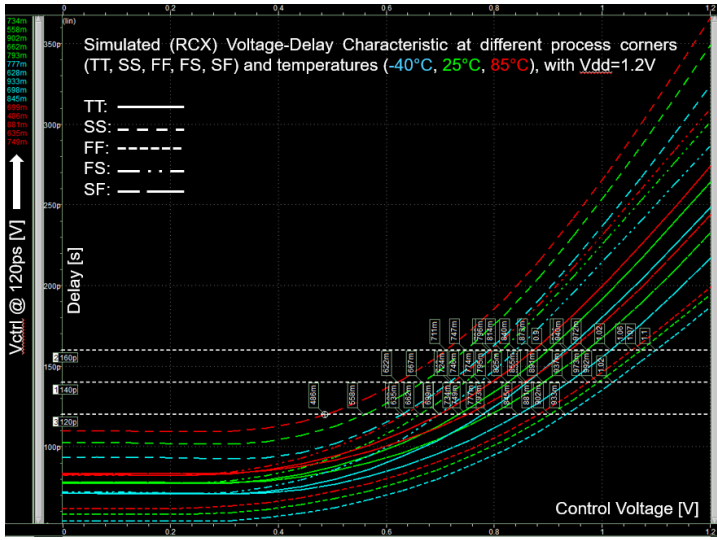
130nm CMOS Delay Cell (SCH):

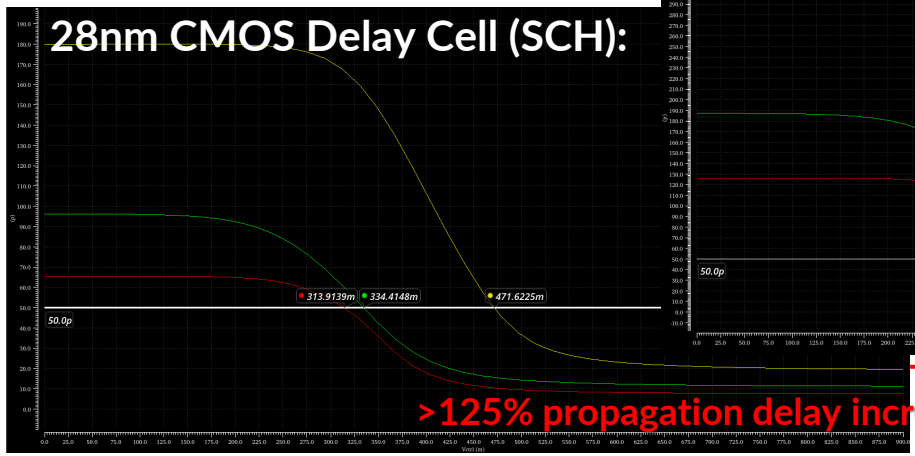


130nm CMOS Delay Cell (RCX):



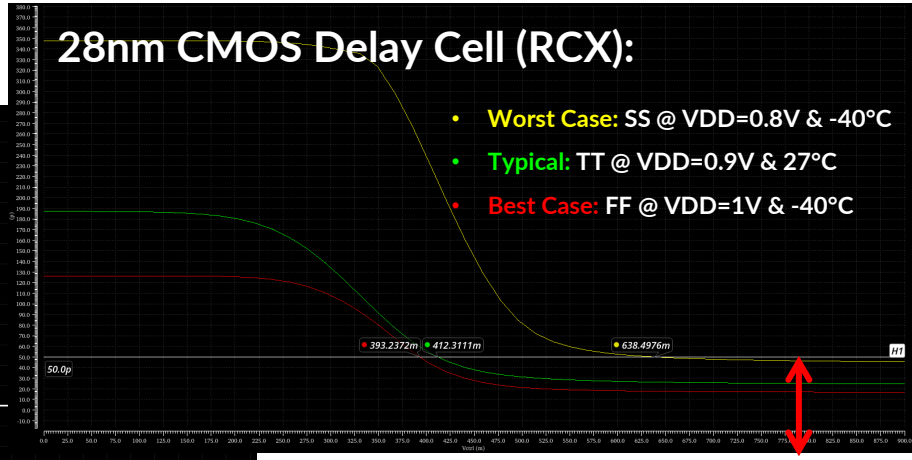
~25% propagation delay increase due to parasitic

28nm CMOS Delay Cell (SCH):



28nm CMOS Delay Cell (RCX):

- **Worst Case:** SS @ VDD=0.8V & -40°C
- **Typical:** TT @ VDD=0.9V & 27°C
- **Best Case:** FF @ VDD=1V & -40°C



>125% propagation delay increase due to parasitic

Some design considerations

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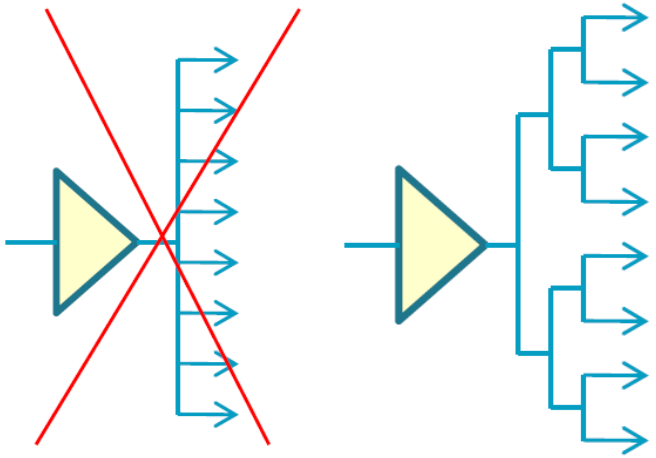

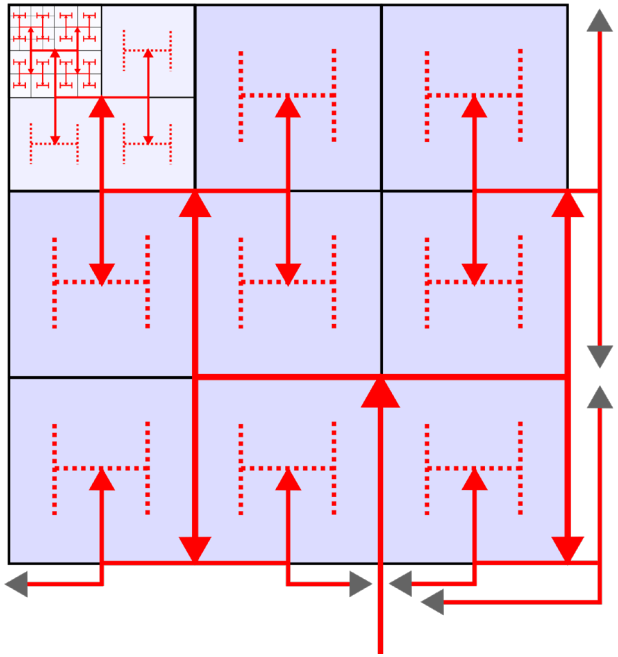

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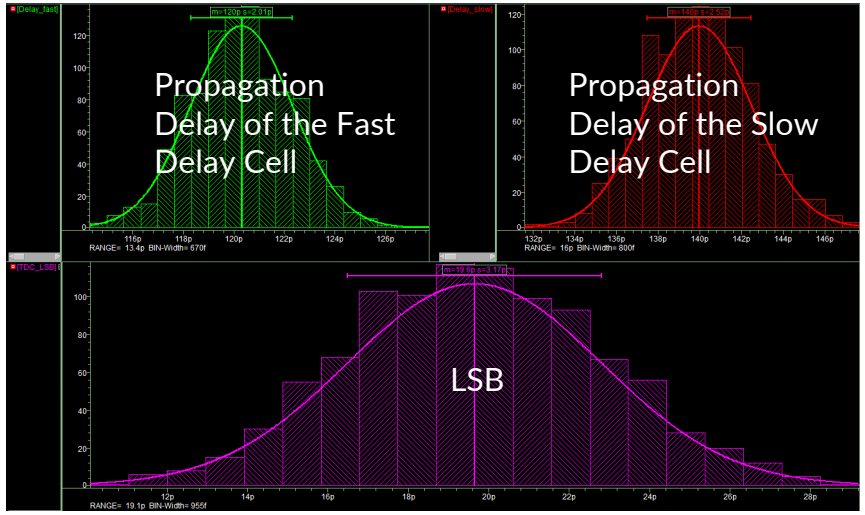
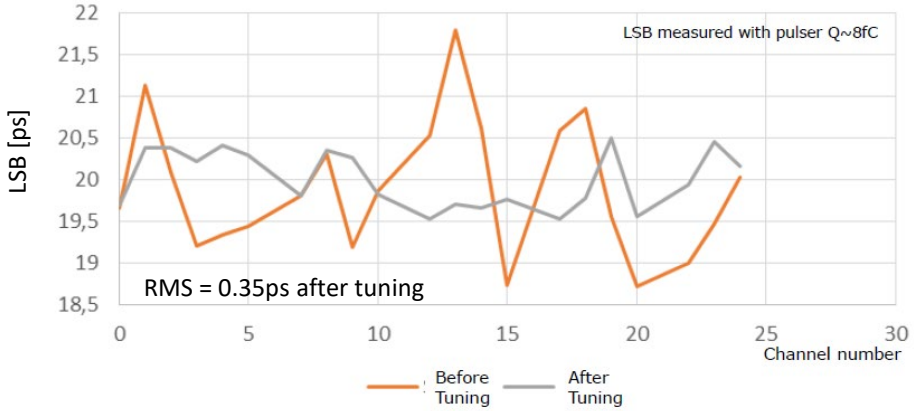
- For ps-level designs device mismatches (both systematic and statistical) can have major impact on the performances

- **Statistical Mismatches:**

- Altiroc Delay Cell Mismatches – Monte-Carlo simulations:



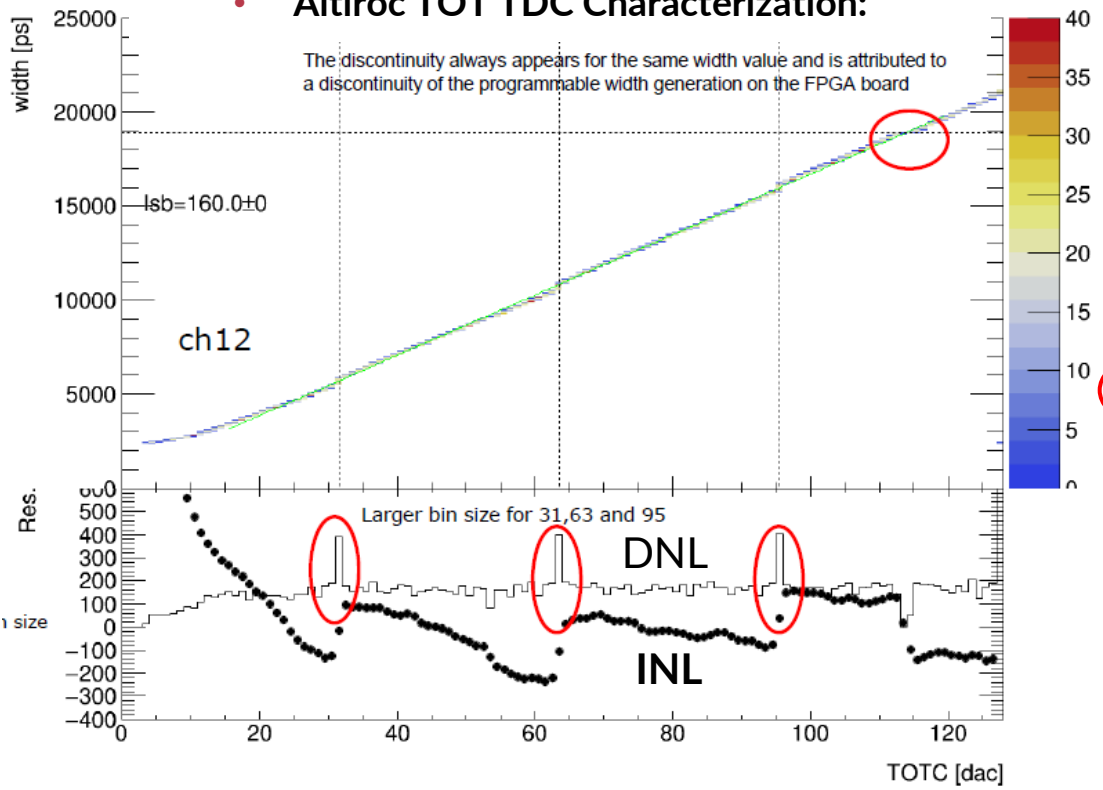
- Altiroc measured LSB dispersion per channel:



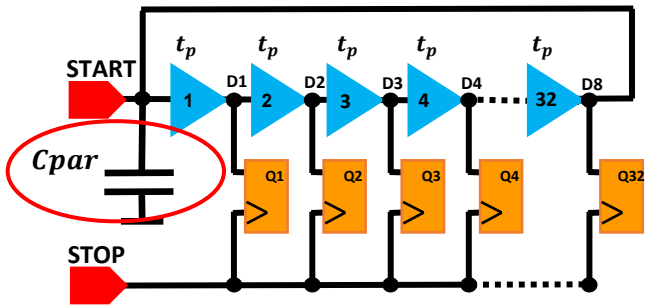
Calibration is a must; tunning capabilities desirable

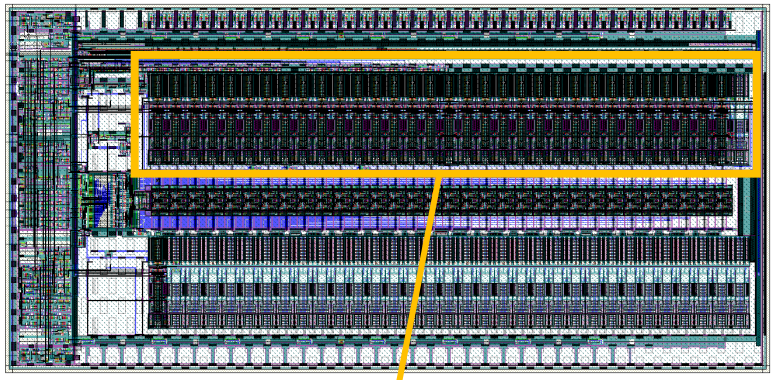
Some design considerations

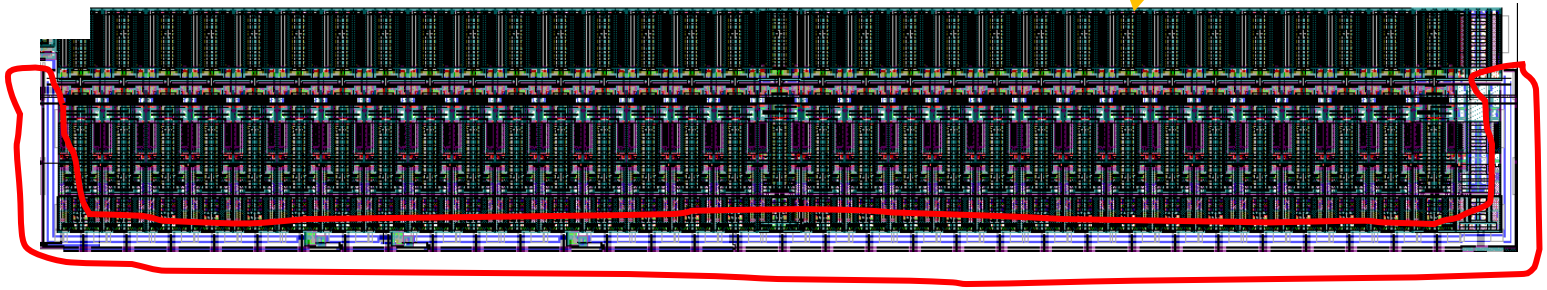
- **Altiroc TOT TDC Characterization:**



- **Systematic Mismatches:**
  - **Altiroc TOT TDC:**





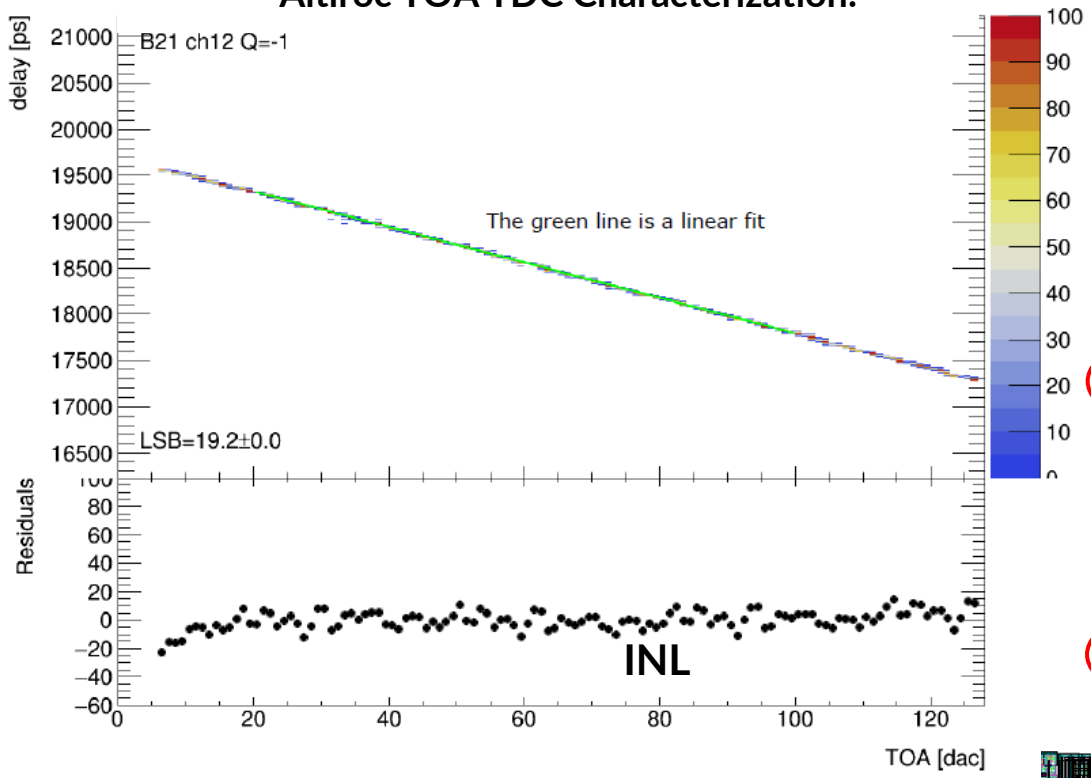


- For ps-level designs device mismatches (both systematic and statistical) can have major impact on the performances

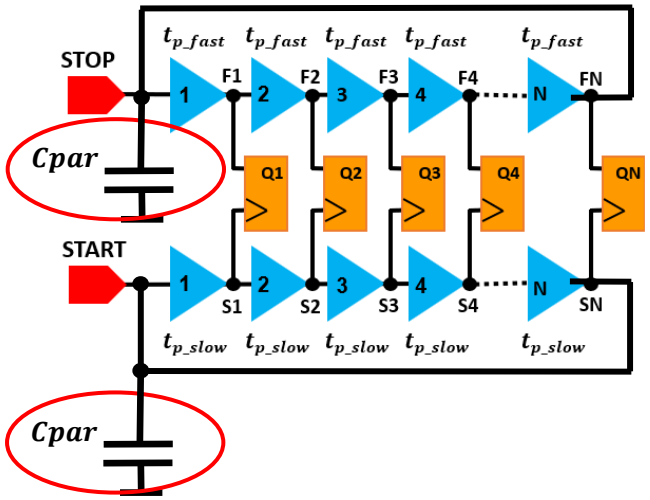
Systematic mismatch shown in parasitic extracted simulation

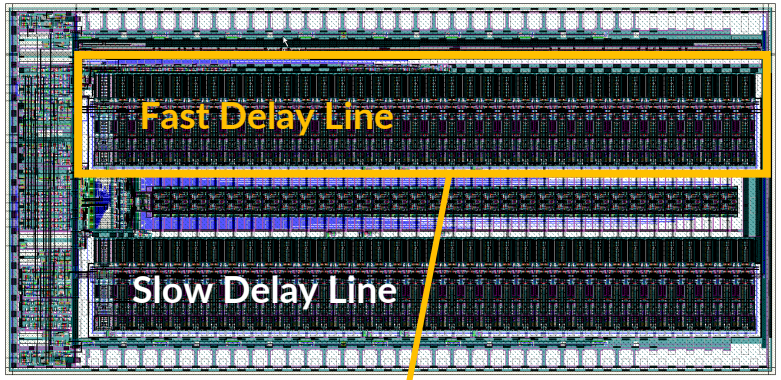
Some design considerations

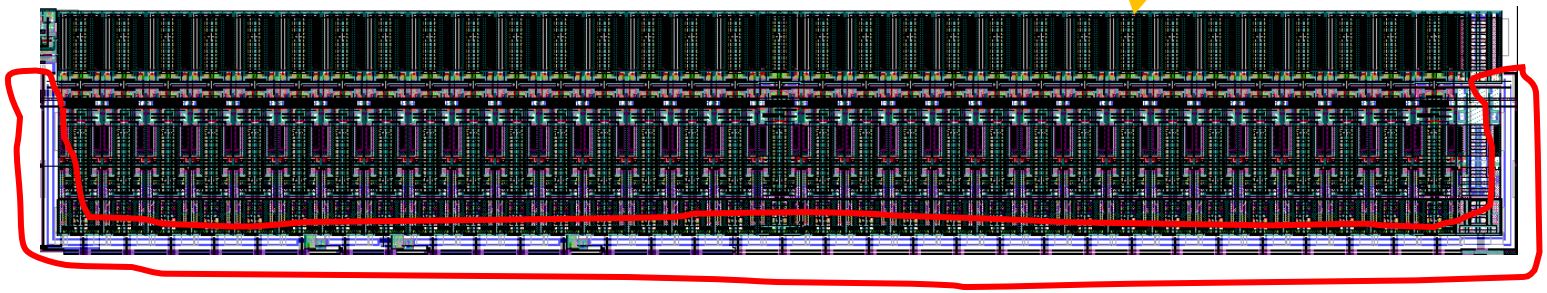
- **Altiroc TOA TDC Characterization:**



- **Systematic Mismatches:**
  - **Altiroc TOA TDC:**







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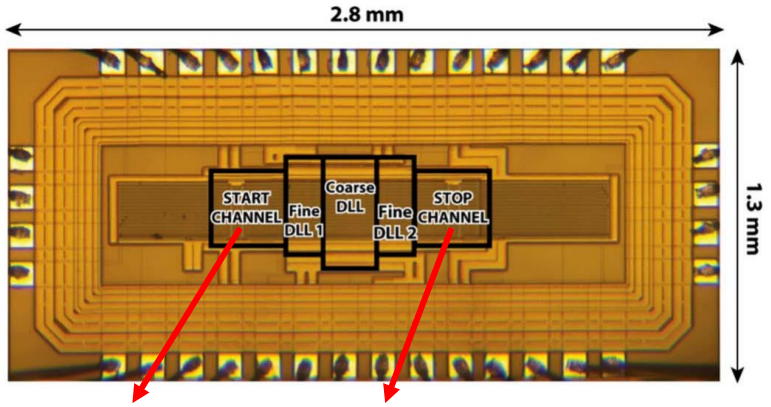
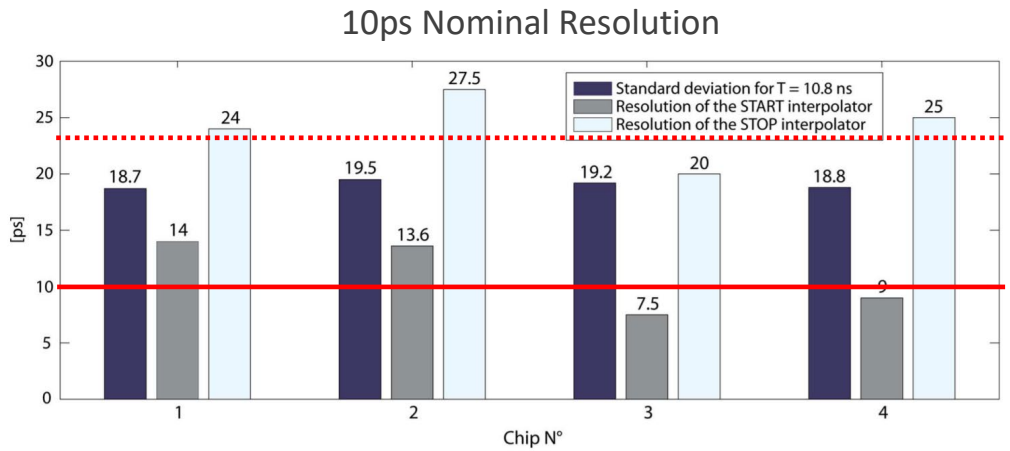
- **Systematic Mismatches:**



B. Markovic, S. Tisa, F. A. Villa, A. Tosi and F. Zappa, "A High-Linearity, 17 ps Precision Time-to-Digital Converter Based on a Single-Stage Vernier Delay Loop Fine Interpolation," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 3, pp. 557-569, March 2013, doi: 10.1109/TCSI.2012.2215737.

START Channel orientation same as bias DLLs

STOP Channel orientation vertically mirrored compared to bias DLLs



Not all systematic mismatches always show in parasitic extracted simulations

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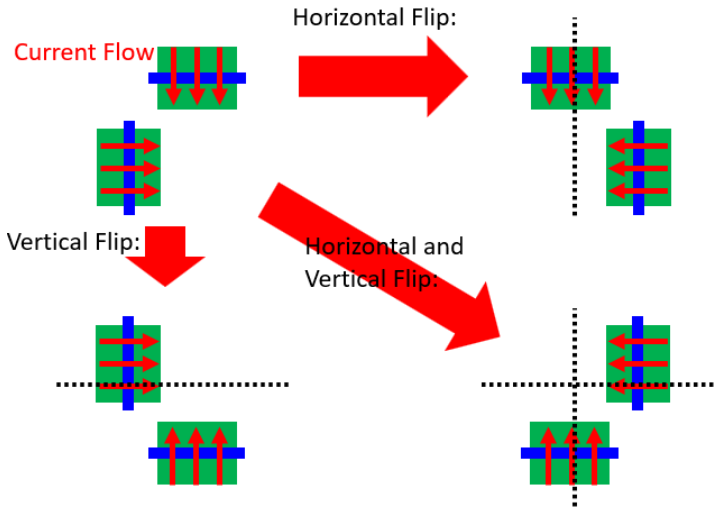
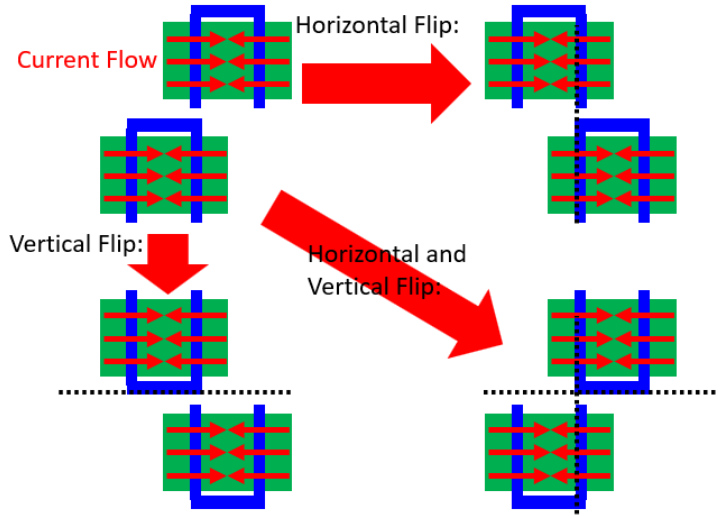
- **Systematic Mismatches:**



- Good layout practice for matching sensitive circuits:
  - Keep gates with the same orientation
  - Use even number of fingers per transistor



Linearity Improvement: Sliding Scale Technique

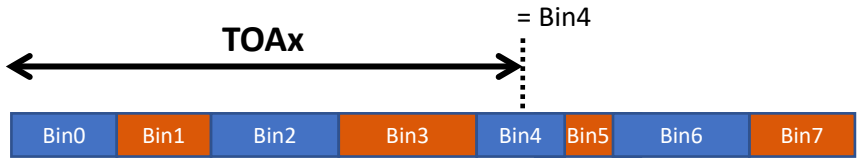
Ideal Converter:

Real Converter:

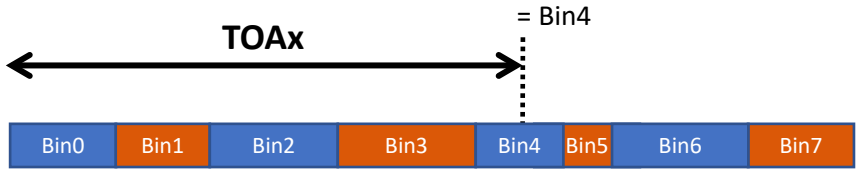
[1] C. Cottini, E. Gatti, and V. Svelto, "A new method for analog to digital conversion," Nucl. Instr. Meth., vol. 24, p. 241, Aug. 1963.
[2] E. Gatti, P. F. Manfredi, and D. Marino, "Analysis and characterization of cyclic-scale compensated analog-to-digital converters," Nucl. Instrum. Methods, vol. 165, no. 2, pp. 225–230, Oct. 1979.

- Regular Converter:

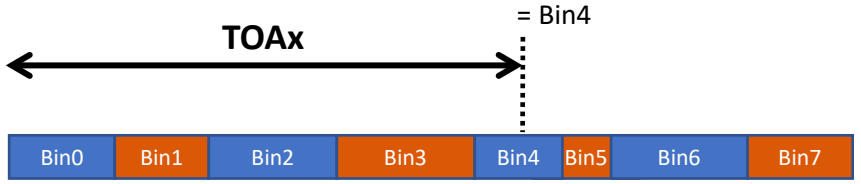
Measurment1:



Measurment2:

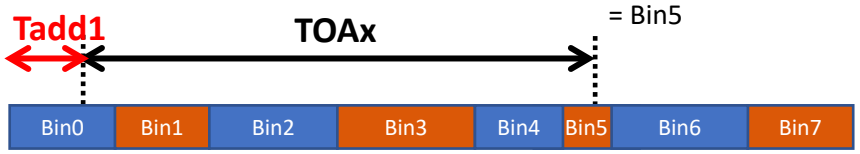


Measurment3:

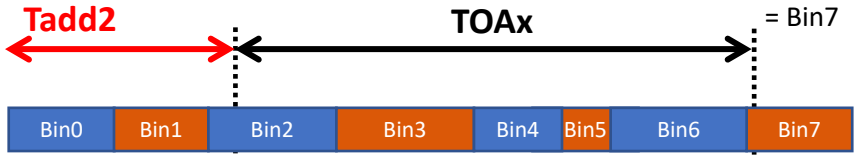


- Sliding Scale [1][2] / Dithering

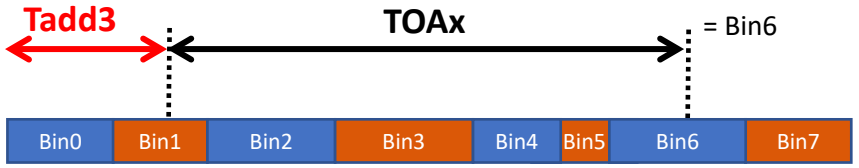
Result = Tmeas - Tadd



Result = 5 – 0 = 5



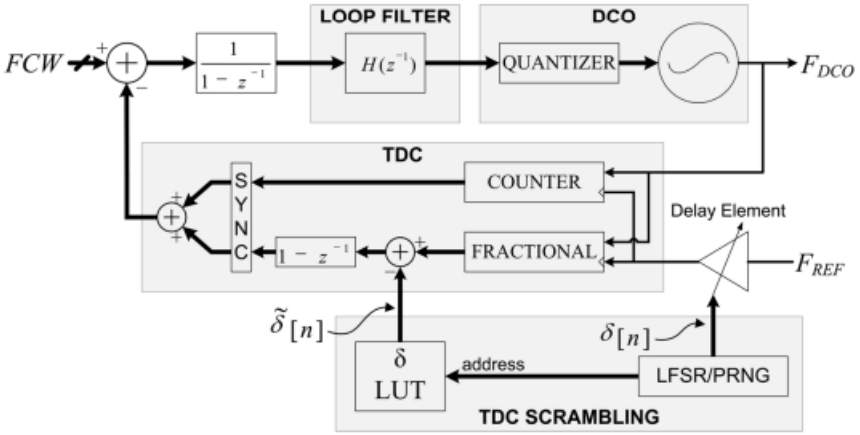
Result = 7 – 2 = 5



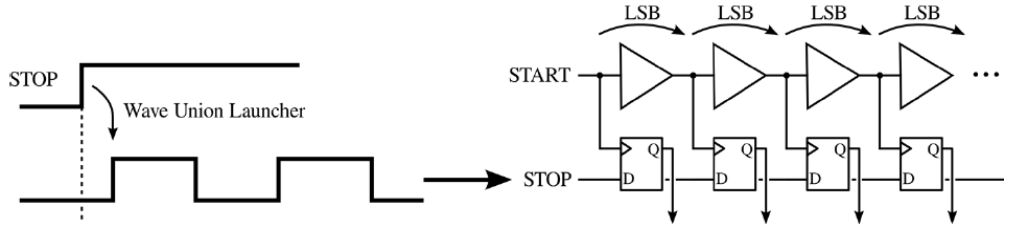
Result = 6 – 1 = 5

Linearity Improvement

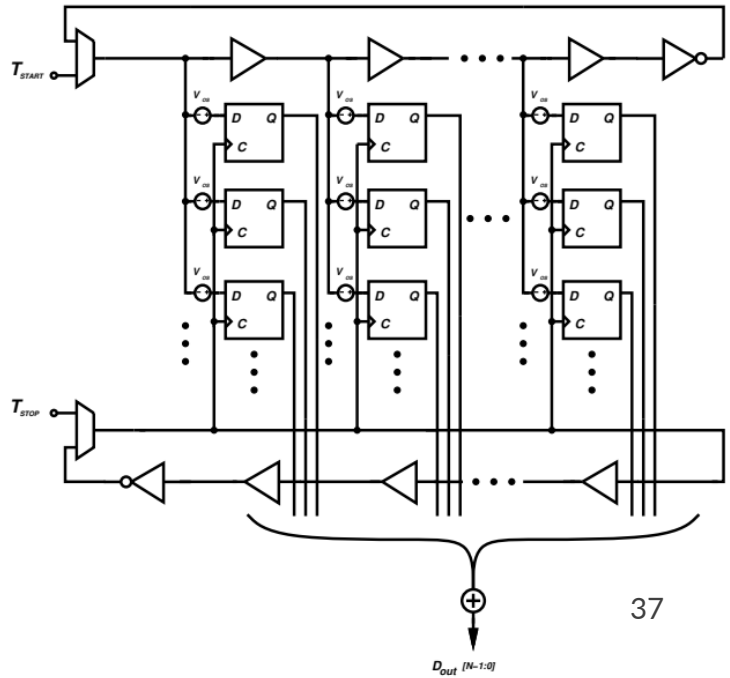
- TDC with scrambling/dithering logic:



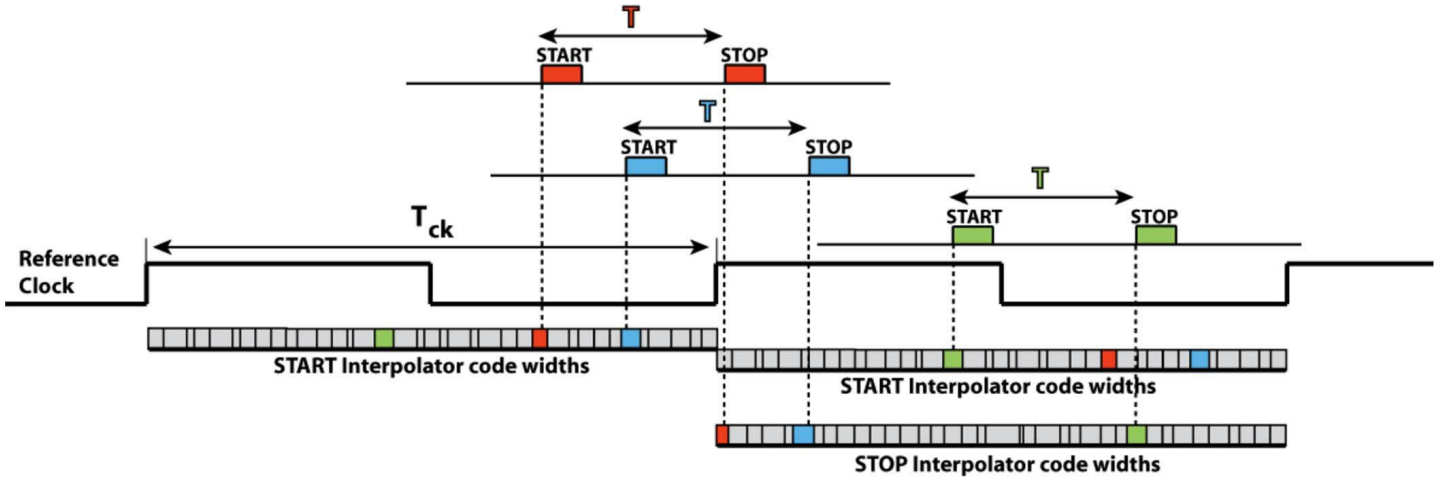
- Wave Union TDC (often used in FPGA implementations to overcome large bin sizes) :



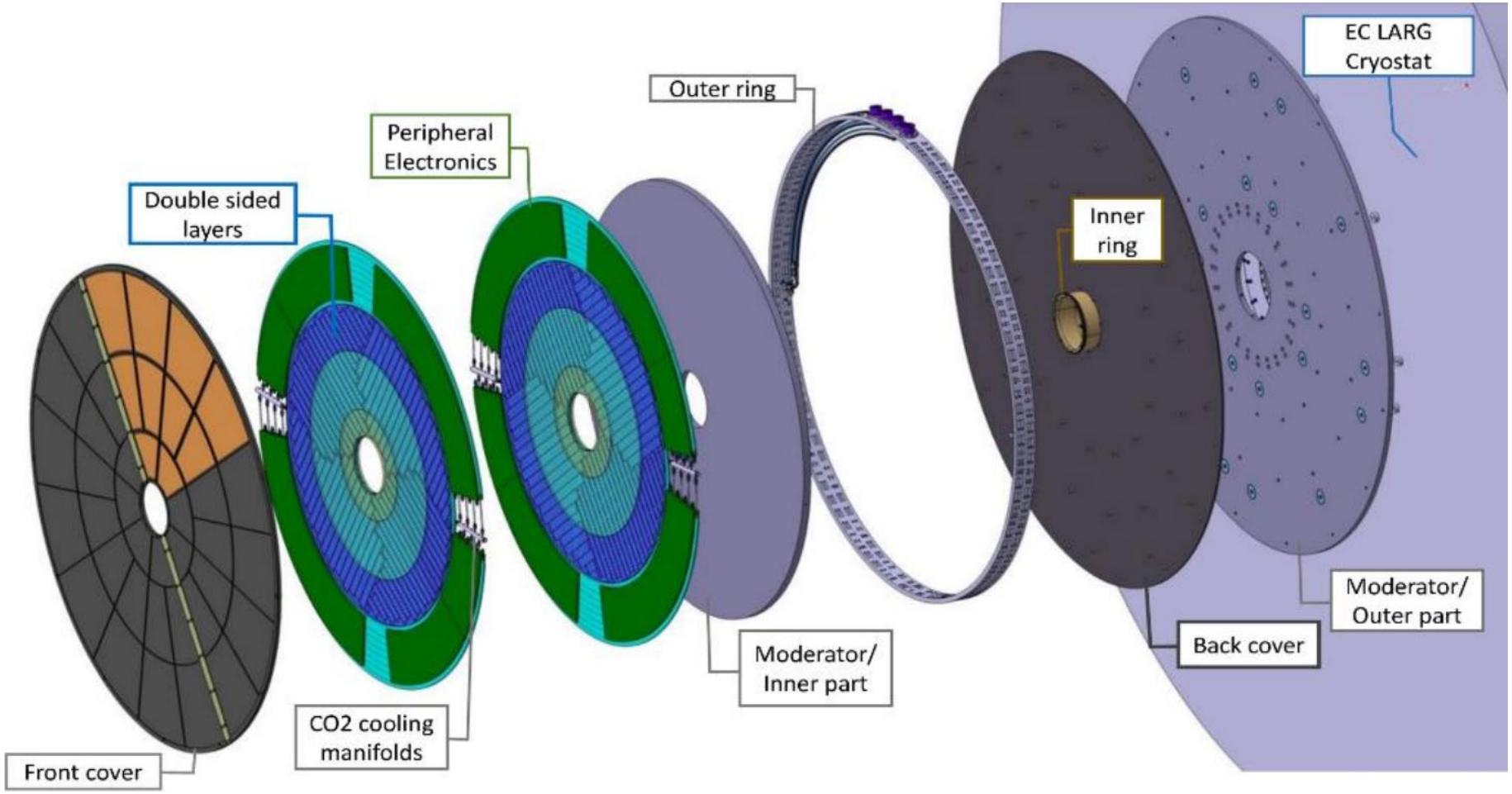
- Stochastic TDC (exploits mismatch and jitter to perform dithering):



- Asynchronous START and STOP signals (requires 2 interpolators):

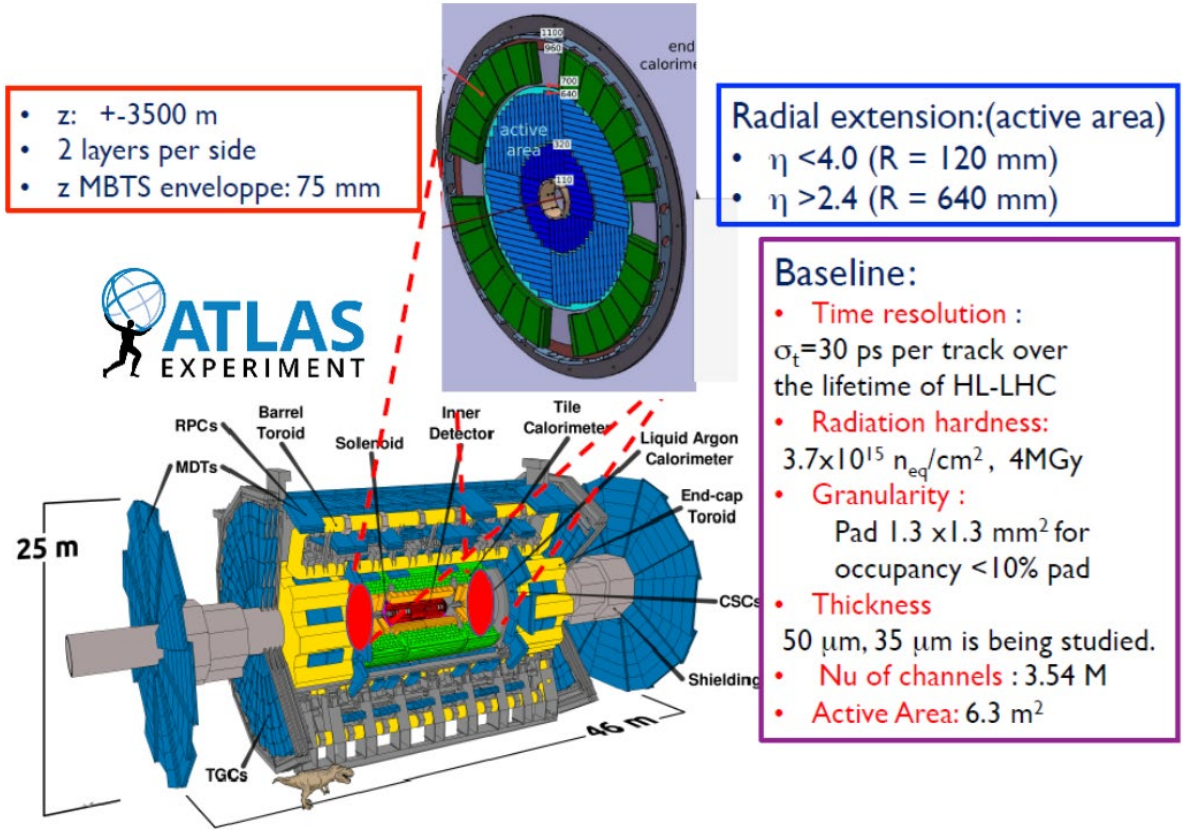


HEP timing ASIC example: Altiroc ASIC for ATLAS HGTD



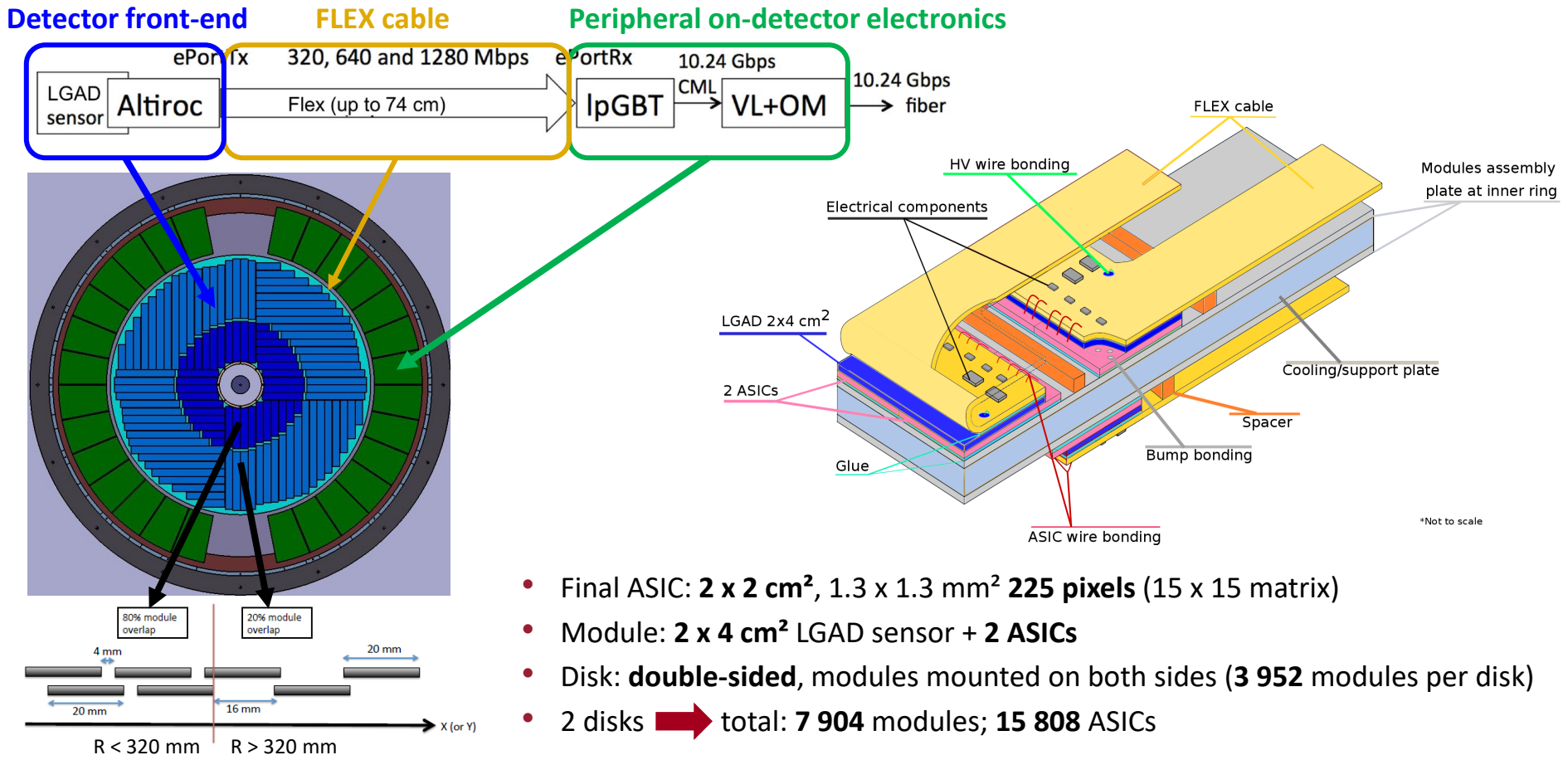
High-Granularity Timing Detector (HGTD) for ATLAS Phase II

- **High-Luminosity Large Hadron Collider (HL-LHC)** beginning in 2026
- on average **200 interaction** per **bunch crossing** ➡ **Pile-up** challenge
- **High-Granularity Timing Detector (HGTD)** for pile-up mitigation



- Placed in the **forward region**, between the **Inner Tracker** and the **endcap of EM Calorimeter**
- **2 disks**, **2 layers/disk** containing **modules** with **sensors** and on-detector **electronics**
- Time resolution: **30 ps**
- Granularity (<10% Occupancy): **1.3 x 1.3 mm²**
- **50 µm** thick **Low Gain Avalanche Diodes (LGAD)** n-on-p Si detectors

HGTD electronics: general architecture



- Final ASIC: **2 x 2 cm²**, 1.3 x 1.3 mm² **225 pixels** (15 x 15 matrix)
- Module: **2 x 4 cm²** LGAD sensor + **2 ASICs**
- Disk: **double-sided**, modules mounted on both sides (**3 952** modules per disk)
- 2 disks ➡ total: **7 904** modules; **15 808** ASICs

ASIC requirements

- **ALTIROC** (ATLAS LGAD Timing Read-Out Circuit) – **Front-End ASIC** for LGAD sensor **readout** and **time-measurement** of each hit of events selected by L0/L1 trigger with a resolution smaller than **30 ps/MIP**

Key requirement: Time resolution per track, combining multiple hits, is 30 ps at the start of lifetime to 50 ps after 4000 fb-1 => Time resolution /hit must be < 35 ps at start and 70 ps at the end of lifetime.

Maximum jitter (σ_{elec})	25 ps at 10 fC at the start of the HL-LHC and 70 ps for 4 fC at the end
TDC contribution	< 10 ps
Time walk contribution	< 10 ps
Clock contribution	< 15 ps

TDC conversion time	< 25 ns

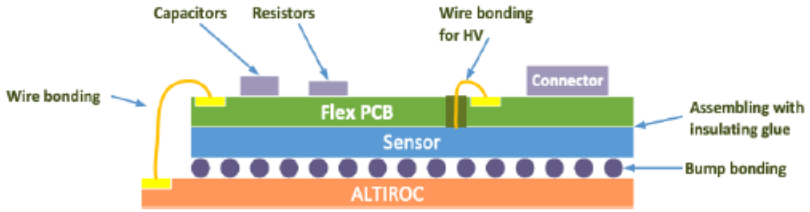
Clock phase adjustment	100 ps

Main contributors to time resolution

$$\sigma_{hit}^2 = \sigma_{Landau}^2 + \sigma_{clock}^2 + \sigma_{elec}^2$$

with $\sigma_{elec}^2 = \sigma_{Time\ walk}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2$

PAD size	1.3 x 1.3 mm^2 x 50 µm => Cdet = 4 pF
ASIC size and channels /ASIC	2x2 cm^2 15x15=225 channels/ASIC
Single PAD noise (ENC)	< 3000 e- or 0.5 fC
Minimum threshold	2 fC
Dynamic range	4 fC to 50 fC



TID Tolerance	2 MGy (inner modules replaced after each 1000 fb^{-1}, middle ring after 2000 fb^{-1})
Full chip SEU probability	< 5 % / hour

ASIC designed in CMOS 130 nm

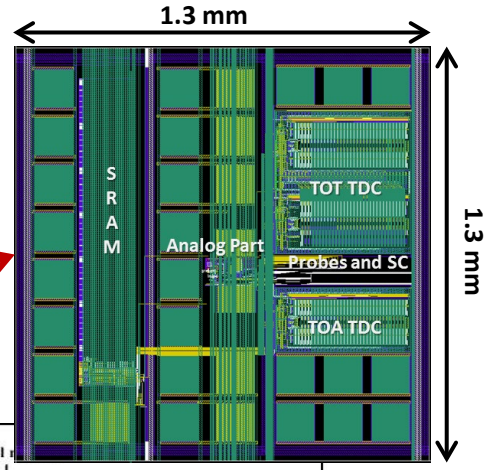
Trigger rate (latency)	1 MHz L0 (10 µs) or 0,8 MHz L1 (35 µs)

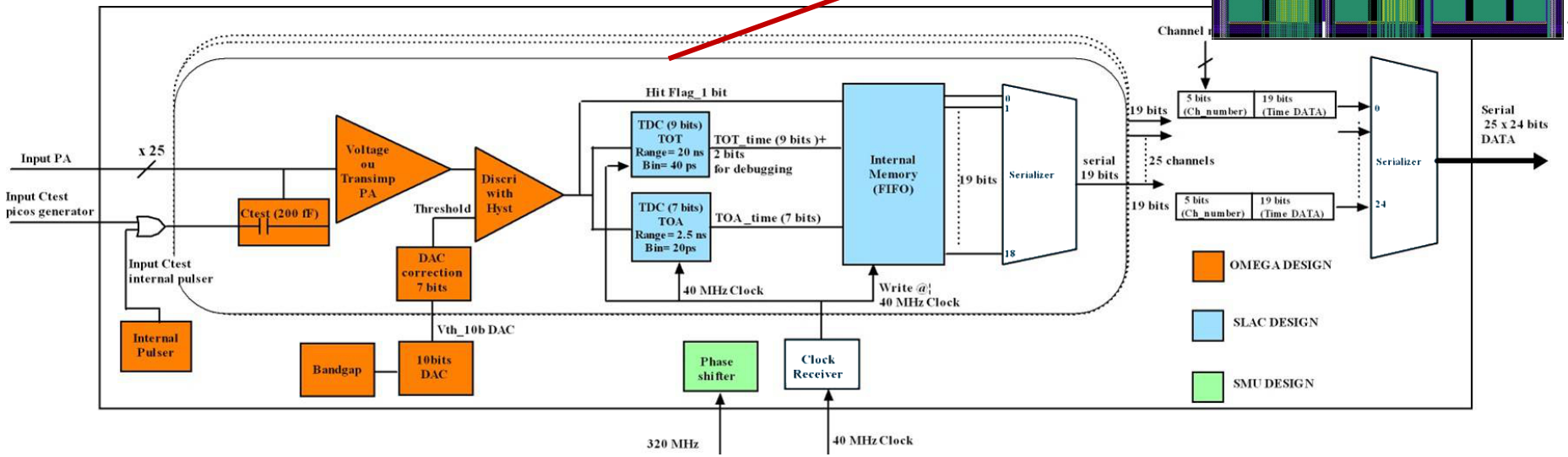
e-link driver bandwidth	320 Mbit/s, 640 Mbit/s and 1,28 Gbit/s

Voltage and Power dissipation per ASIC	1.2V and 300 mW cm^{-2} => 1.2 W/ASIC (225 ch) or 4.4 mW/channel and 200 mW for the common part

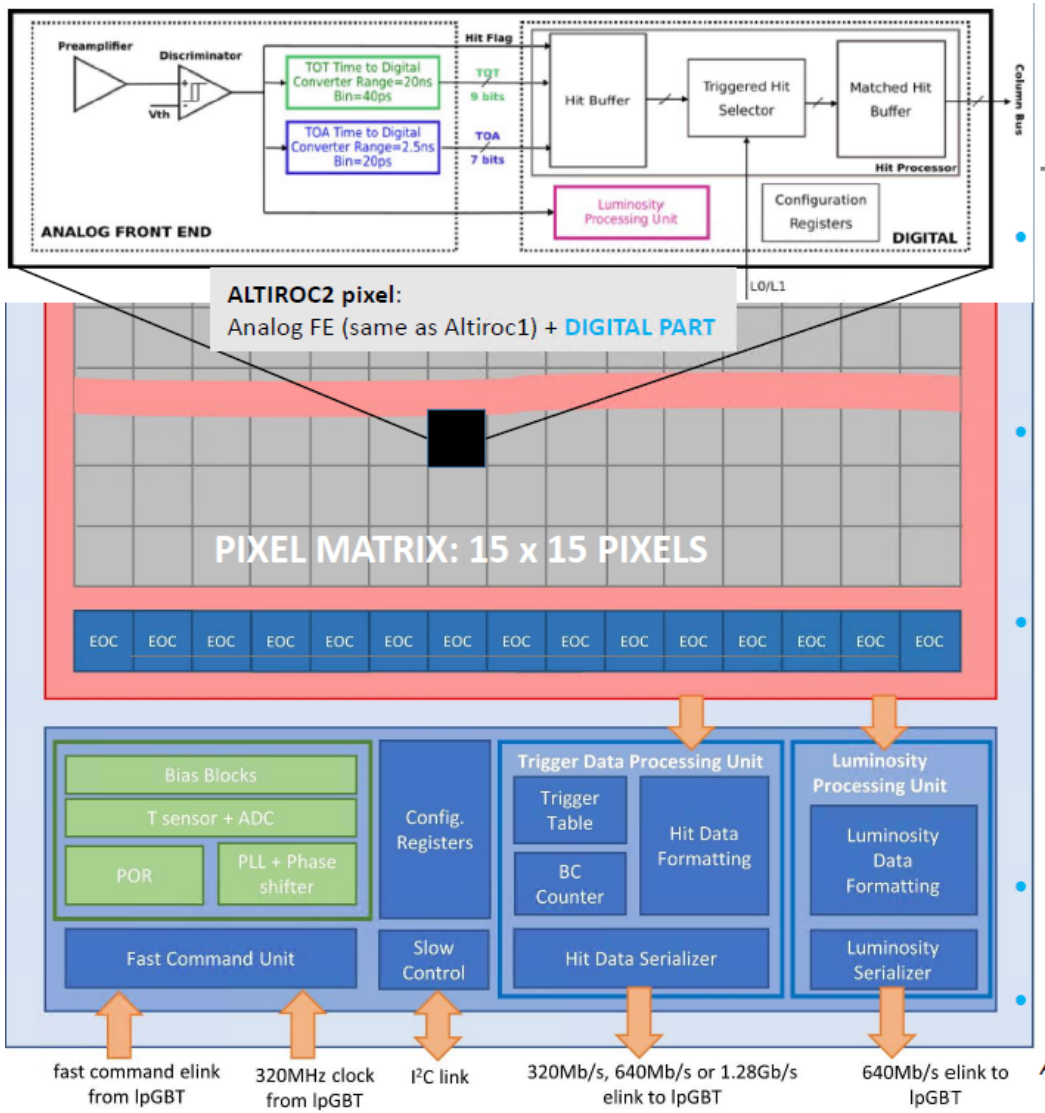
ALTIROC1 architecture

- **ALTIROC1** = Second ALTIROC ASIC prototype with **25 complete FE channels** to readout **5 x 5** sensor cells of **1.3 mm x 1.3 mm** (6.5 mm x 6.5 mm) + **Phase shifter**
- 3 Labs involved: **OMEGA (analog Part** & Full-chip Integration**), SLAC (Digital part: TDCs, DLLs & FIFO), SMU (Phase shifter)**
- ASIC size: **7 x 7.5 mm²**, fabricated in **TSMC 0.13 µm CMOS** technology





ALTIROC2 architecture

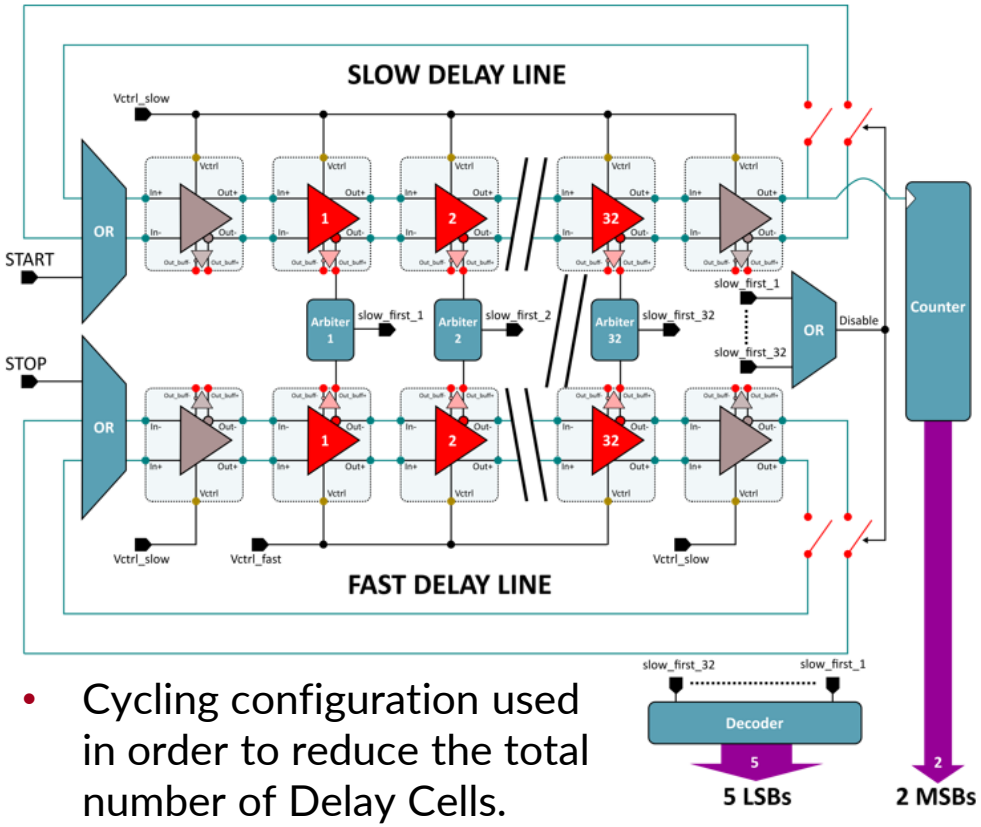


ALTIROC2 (225 ch): Pixel digital part

- **Hit buffer**: SRAM 1536 x 19 bits
  - Circular buffer to store timing data for each BC, until a trigger arrives
  - Data= Hit and TOT and TOA bits, only in case of hit to save power
  - Control unit to handle R/W pointers
- **Trigger Hit Selector** =
  - Each received trigger associated to a trigger tag
  - If data stored in Hit buffer related to received trigger, TOA/TOT data + trig tag stored into Matched Hit Buffer
- **Matched Hit Buffer**: 32 positions FIFO
  - Control Unit: looks for data related to a trigger event when requested by the End Of Column
  - Matched flag handled through a priority OR chain. Pixel at the top of the column with highest priority
  - Synchronous readout at 40 MHz
- **Luminosity process unit**
  - checks if hits are within 2 programmable windows
- **I2C configuration registers**

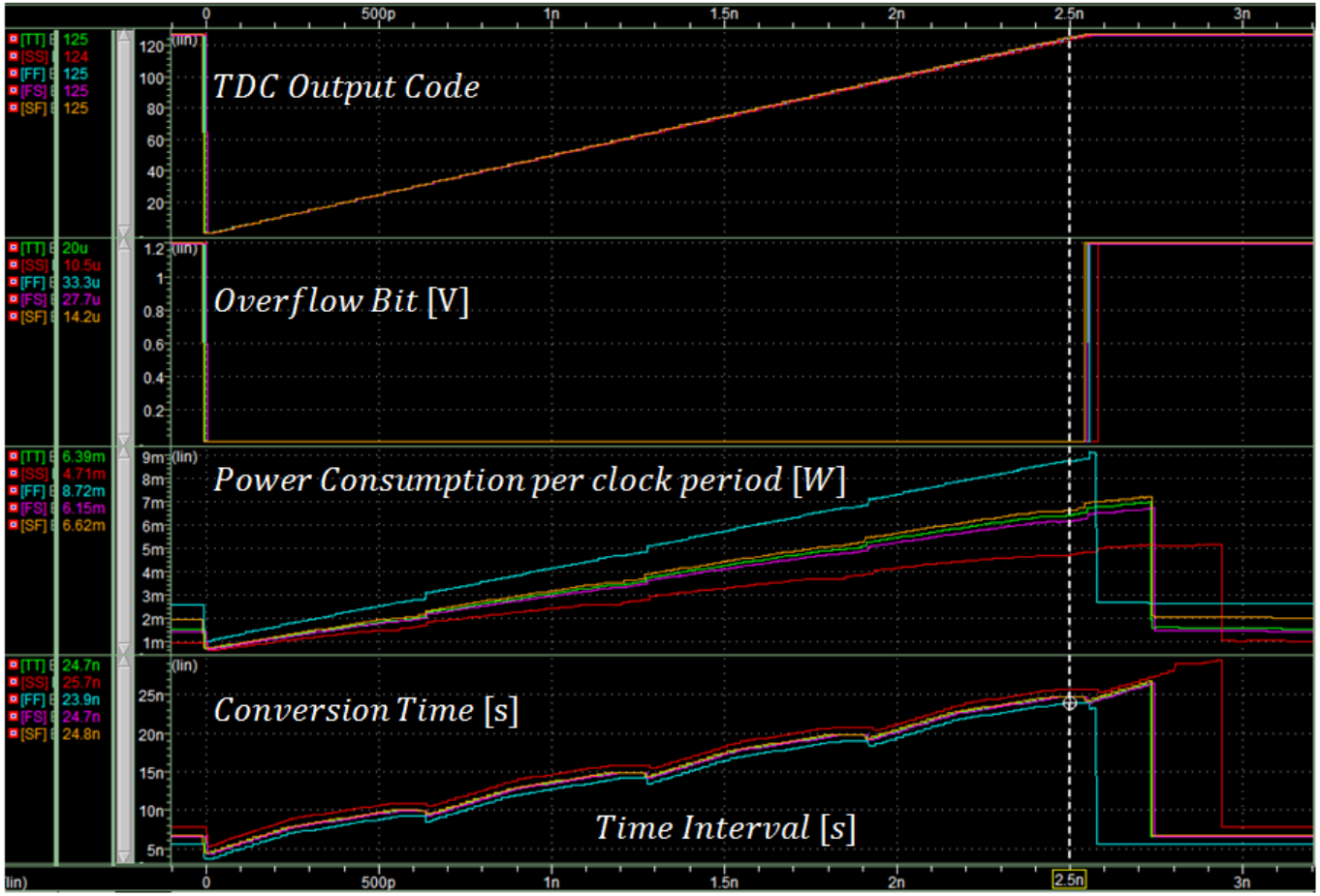
All these digital blocks are integrated in Altipix prototype, first tests in July 2020

TOA TDC



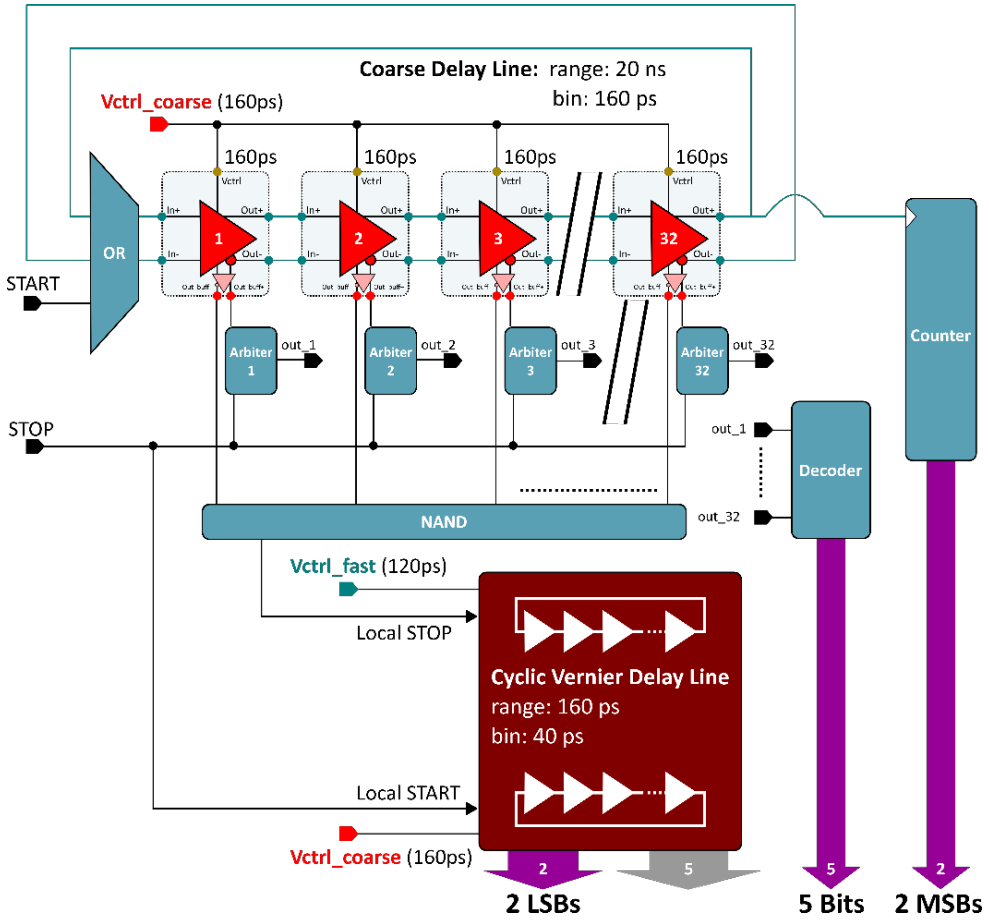
- Cycling configuration used in order to reduce the total number of Delay Cells.

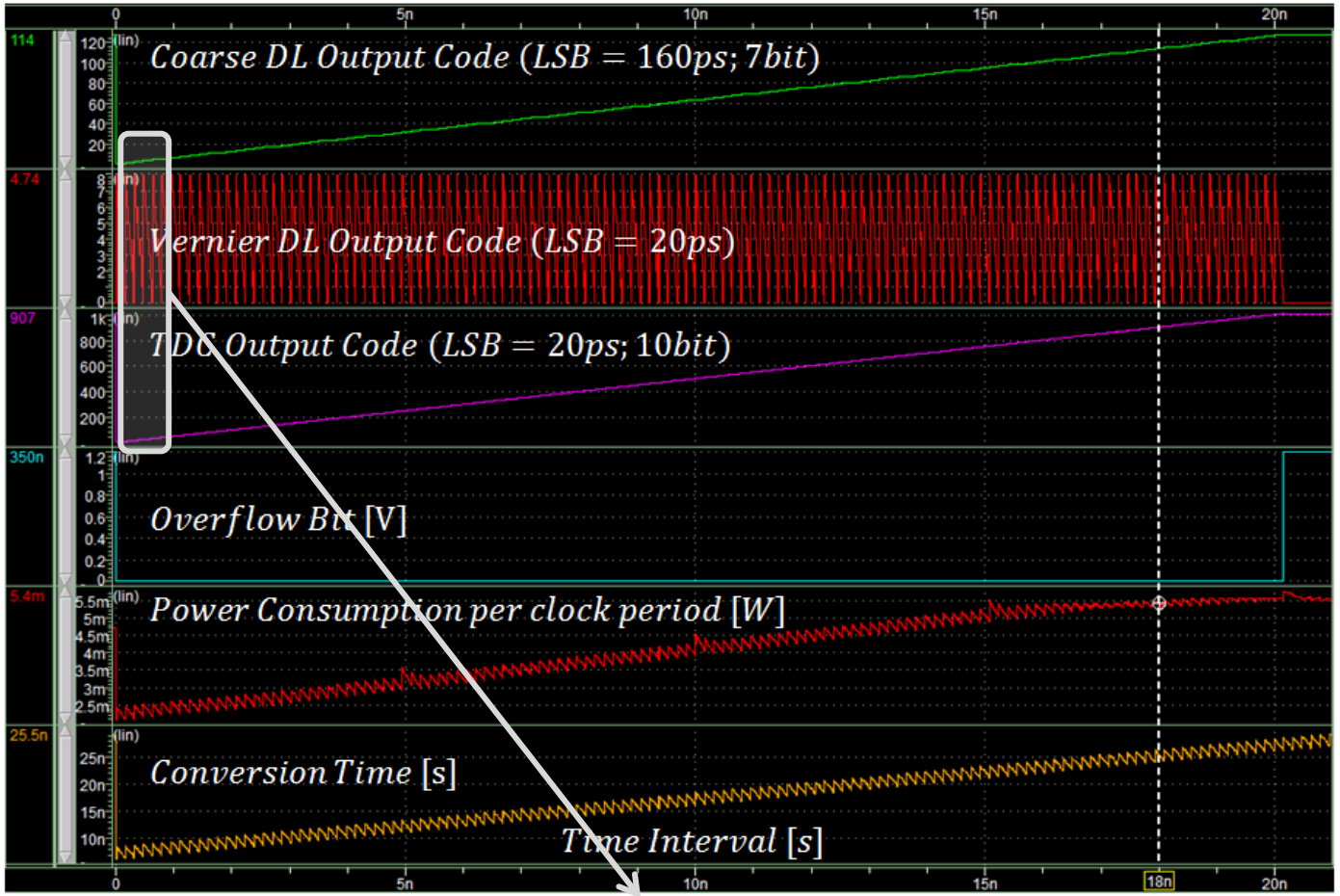
- Resolution: 20ps
- Range: 2.5ns
- 7 bits

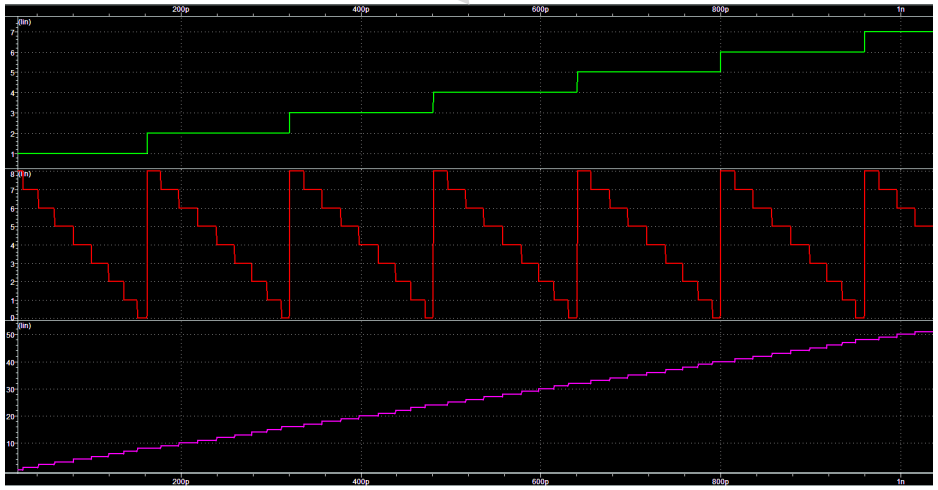


TOT TDC

- Delay Line with Vernier Delay Line Interpolation

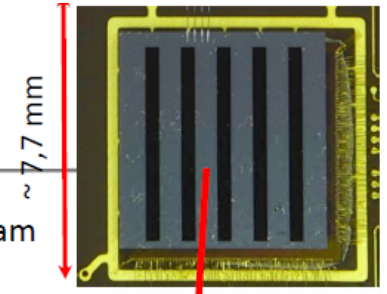






Altiroc1 Testbench (1/2)

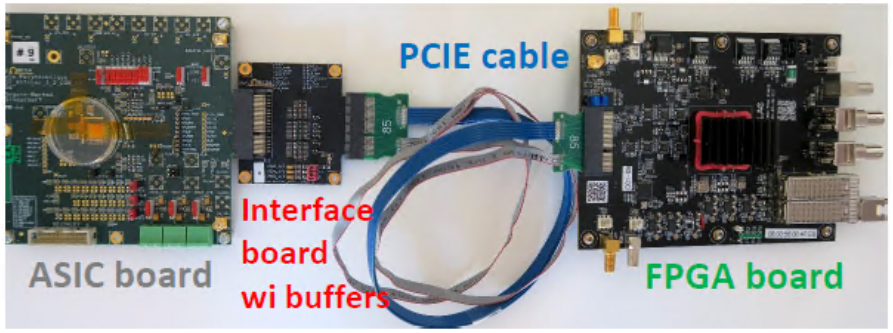
TESTBENCH

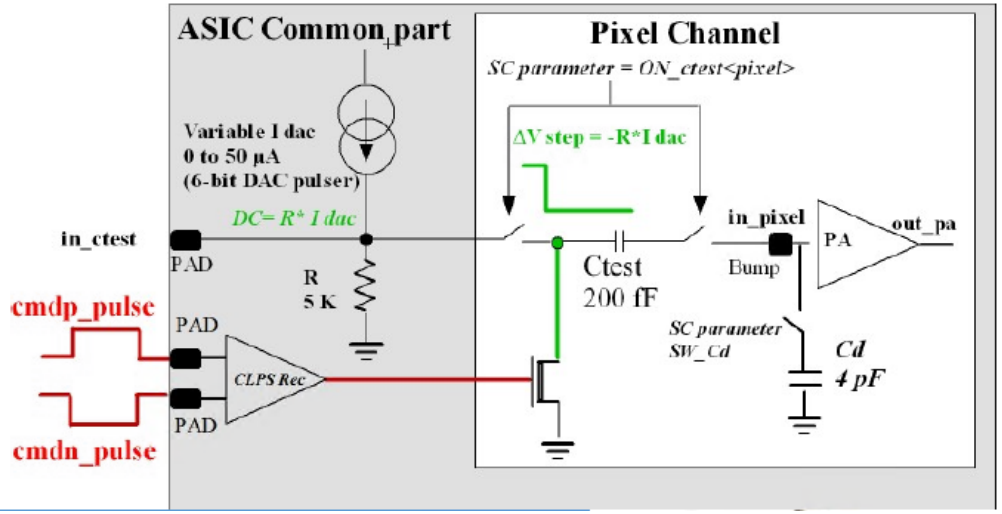


- **ALTIROC1_V1, ALTIROC1_V2**: testbench measurements (ASIC alone or with sensor), irrradiation tests, testbeam

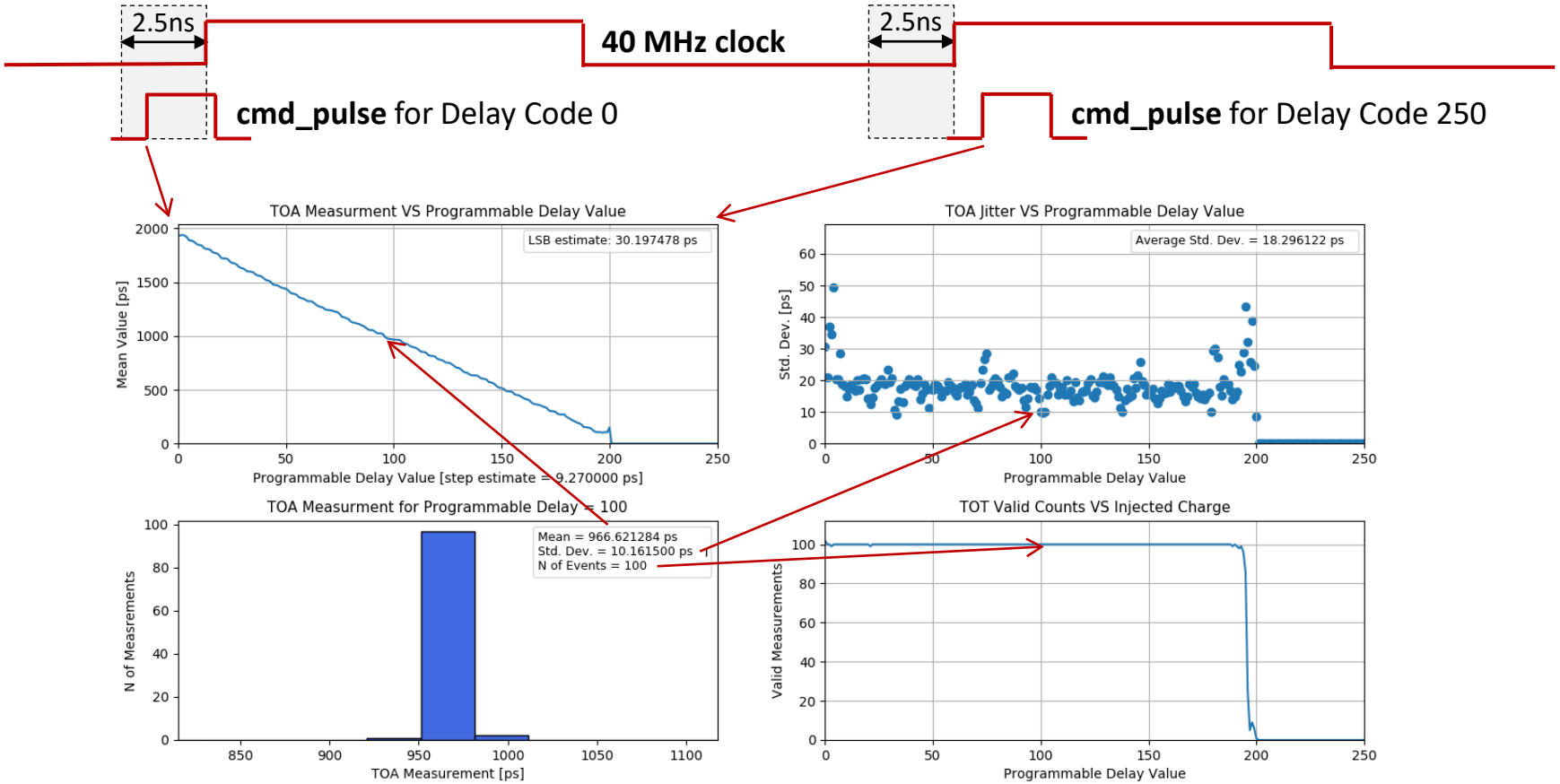
- **Setup:** ASIC board (ASIC alone or bump bonded onto sensor) + FPGA board
  - Charge injection (0 up to 50 fC) using **ASIC** internal calibration pulser controlled by **cmd_pulse** input, generated by the FPGA, synchronous to 40 MHz clock
  - ASIC alone: Cd=4 pF can be set by SC to mimic sensor capacitor
  - **External trigger,** width and delay tunable by 10 ps steps **:** used to characterize the TOA and TOT TDC alone

- **Tests at system level**: need to add interface board to filter FPGA signals (3 MHz noise DC DC converters) => Vth could be set < 2fC

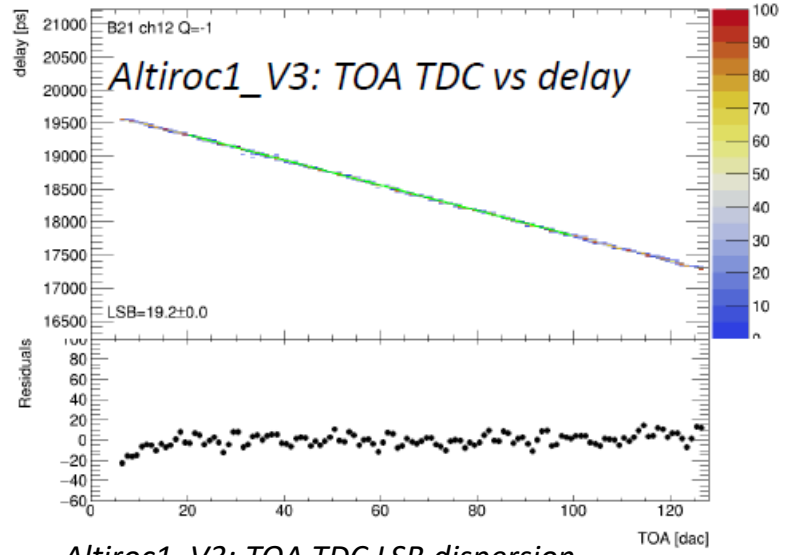




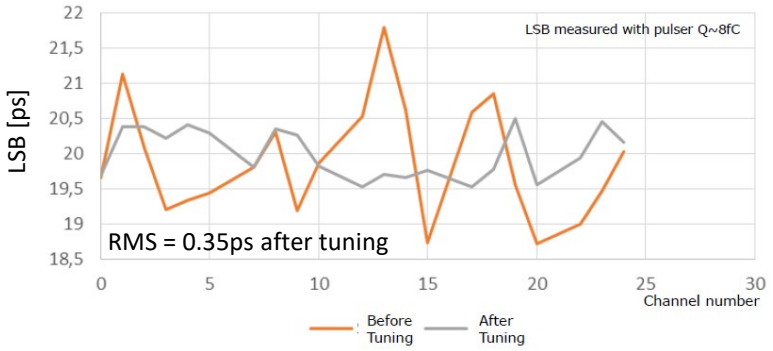
Altiroc1 Testbench (2/2)

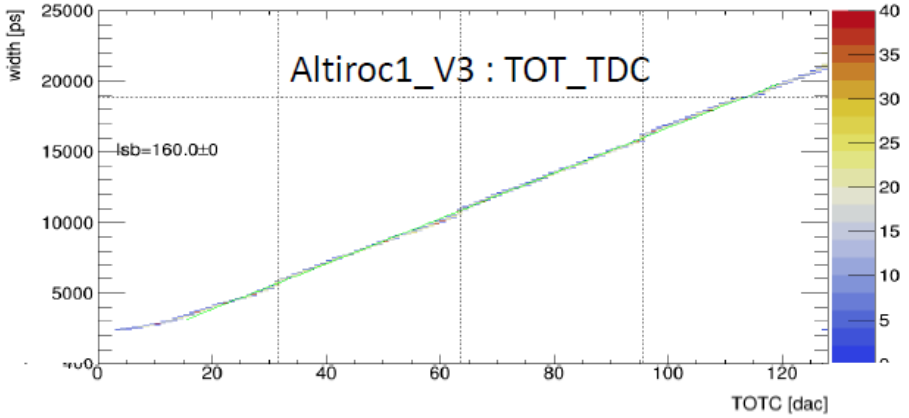


Altiroc1 Characterization (1/4)

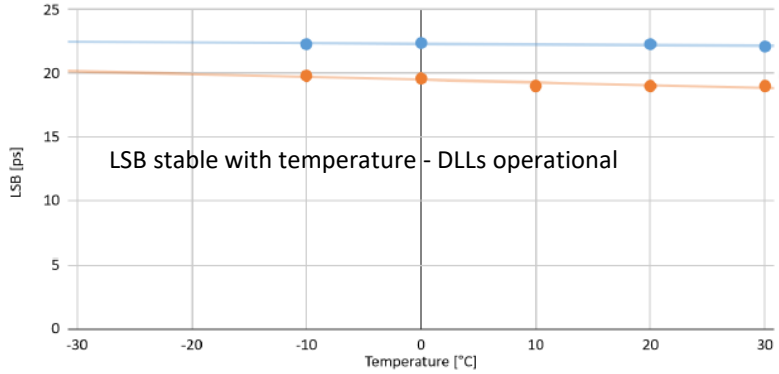


Altiroc1_V3: TOA TDC LSB dispersion

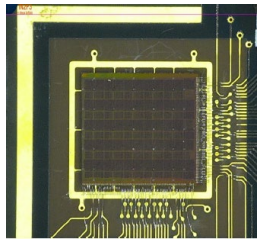




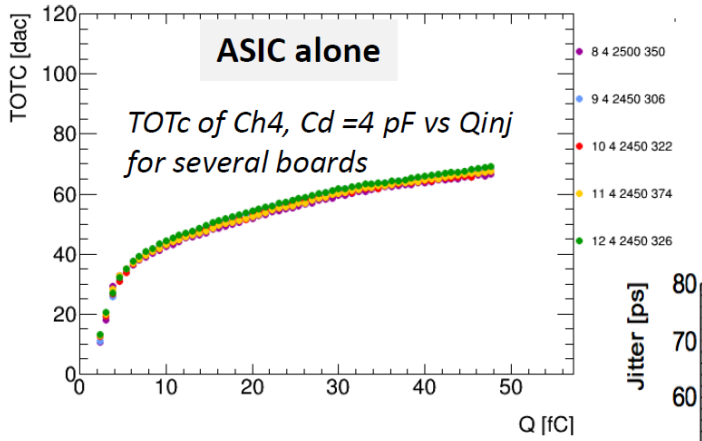
Altiroc1_V3: LSB vs Temperature



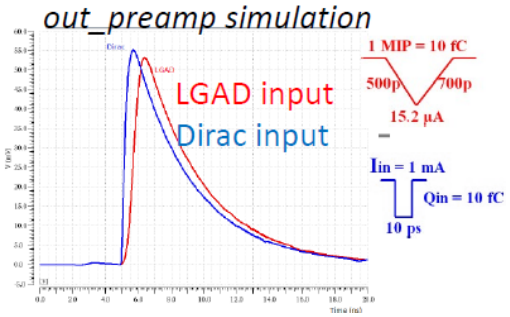
Altiroc1 Characterization (2/4)



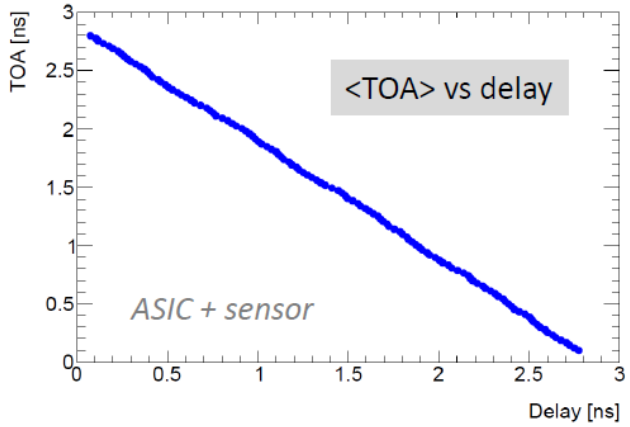
Altiroc1_V2: TOT vs Qinj

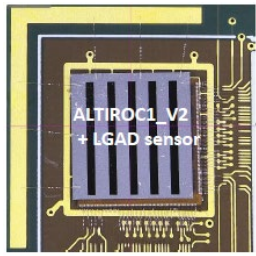


out_preamp simulation

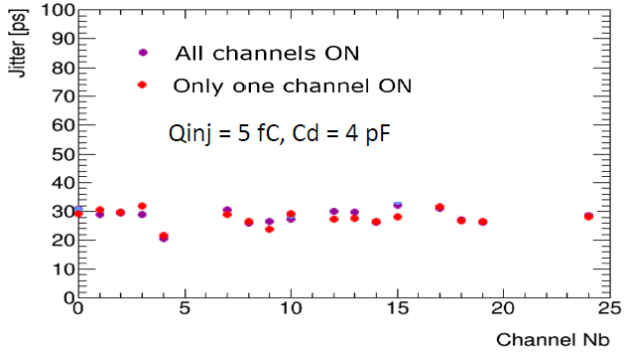


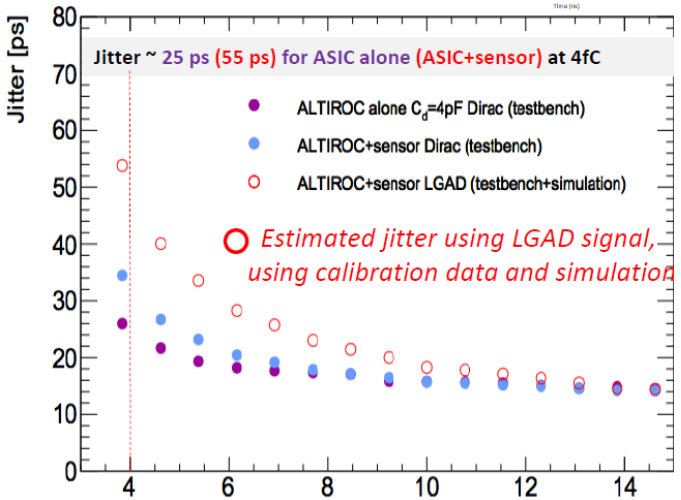
Altiroc1_V2: TOA vs delay



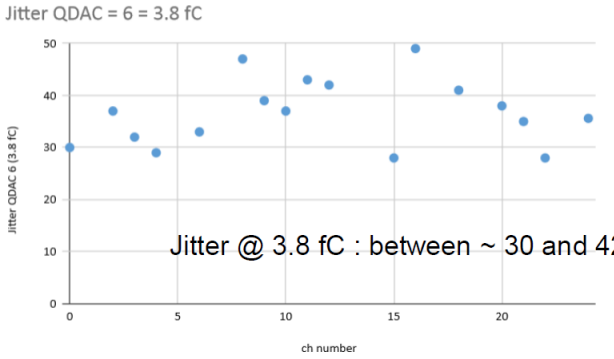


Altiroc1_V3: Jitter vs channel (ASIC alone)





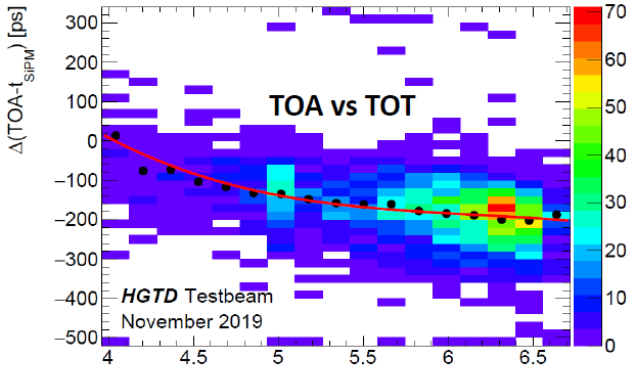
Altiroc1_V3: Jitter vs channel (ASIC + sensor)



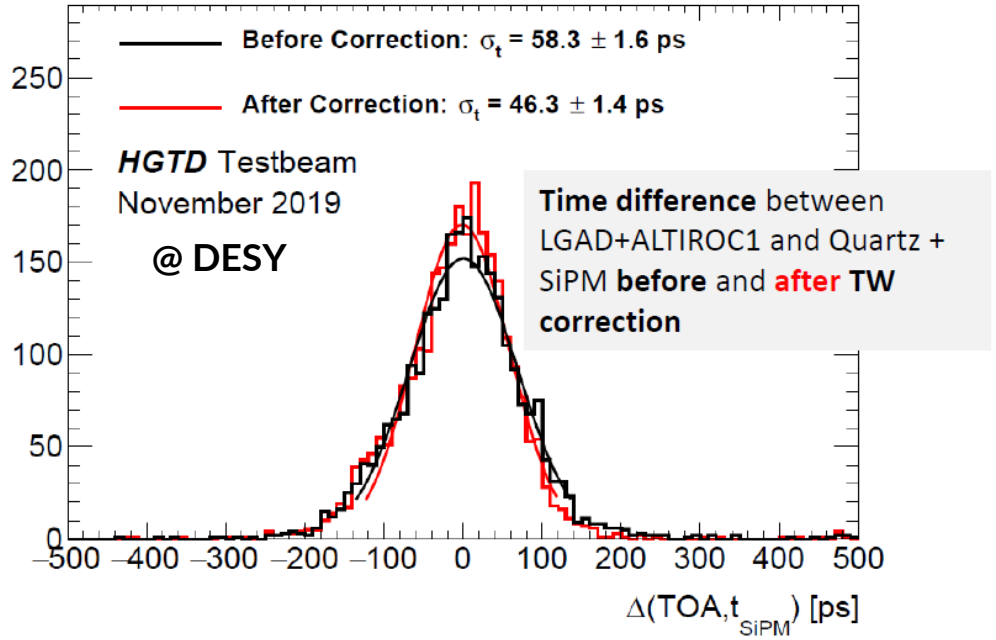
Jitter @ 3.8 fC : between ~ 30 and 42 ps for most of the channels

Altiroc1 Characterization (3/4)

Altiroc1_V2: TEST BEAM measurement



Limited region for TW correction due to TOT disconitinuities as soon as TOA_busy signal is output. Solved in Altiroc1_V3



Time resolution= 46 ps => electronics jitter 39 ps after substracting Landau fluctuations (25 ps) $\sigma_{hit}^2 = \sigma_{Landau}^2 + \sigma_{clock}^2 + \sigma_{elec}^2$

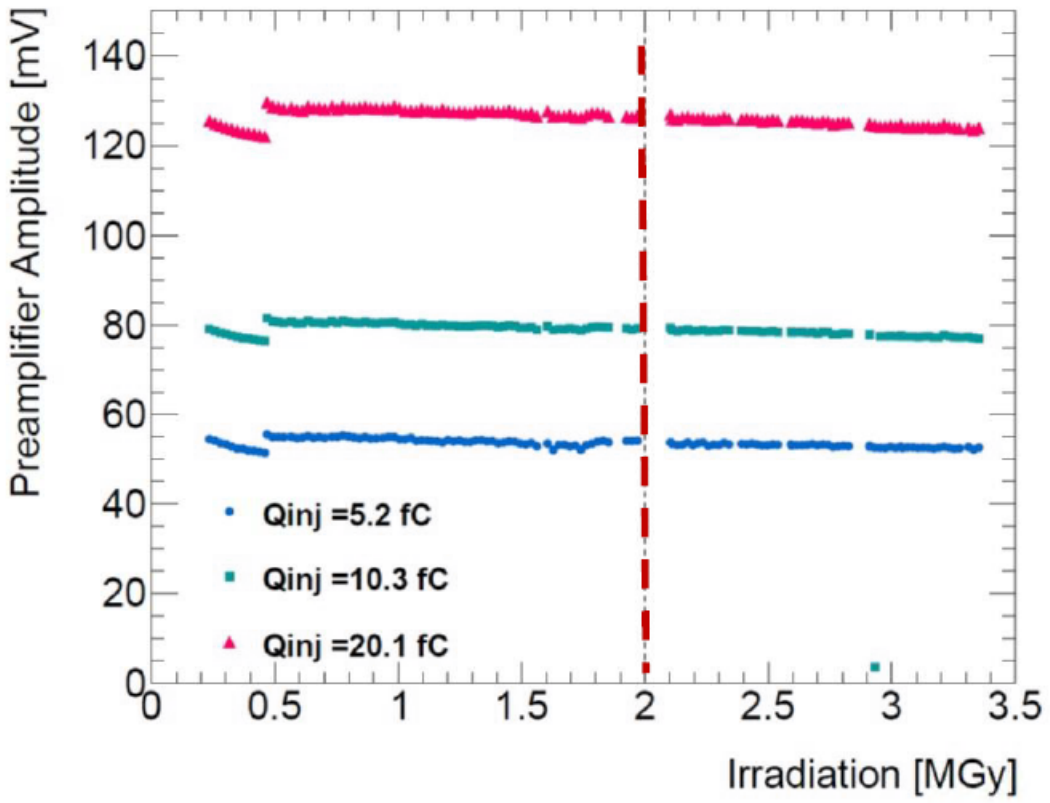
New interface boards designed after this TB => jitter should be reduced by 35 % and so electronic jitter contribution should be 26 ps in testbeam (36 ps for time resolution)

Altiroc1 Characterization (4/4)

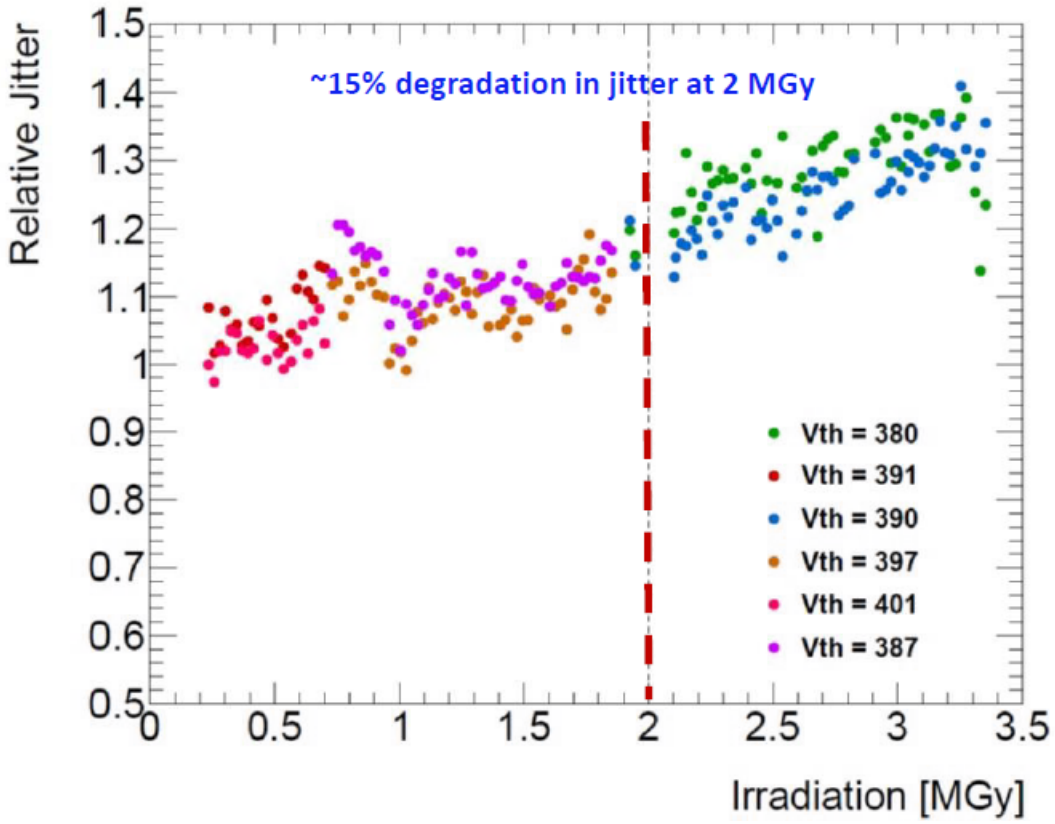
Irradiations tests with Altiroc1_V1 (June 28- July 8, 2019)

CERN facility, TID up to 340 Mrad, requirement: 200 Mrad max

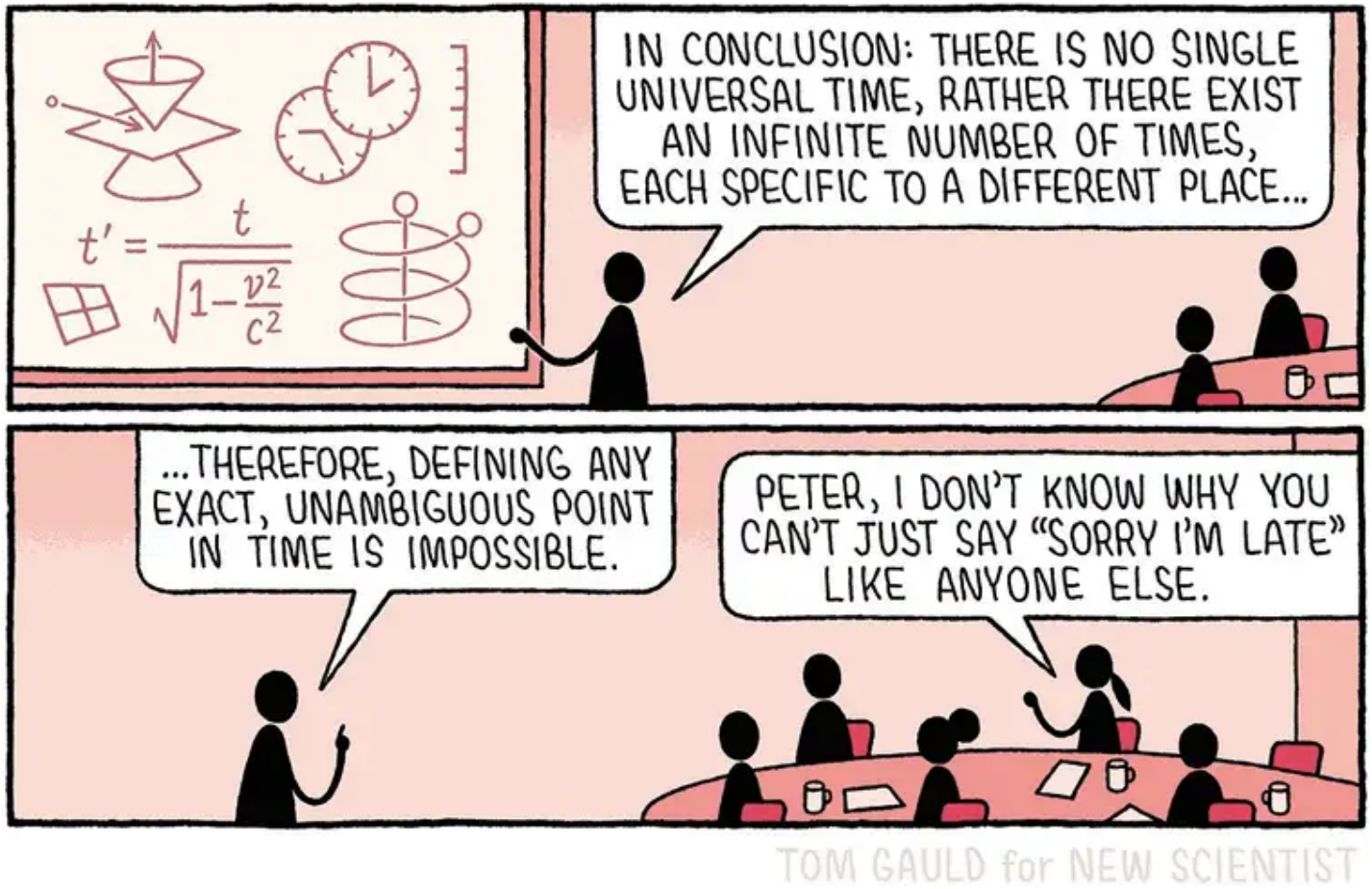
Preamp amplitude for various input charges



Jitter measurement on scope (not measured with TDC)



Conclusion

- Many different architecture and methods for time-to-digital conversion exist.
- Counters are usually employed together with 'fine' measurement techniques to achieve long ranges together with ps-level resolution.
- 'Fine' measurement techniques include:
  - Analog techniques (TAC+ADC; Dual-Slope Pulse Stretching + Counter)
  - Pulse Shrinking
  - Time Amplifiers (SR latch based or Cross-Coupled Delay Line)
  - Delay Line / Multiphase Clocks
  - Delay Interpolation: resistive divider, multipath cells
  - Vernier Delay Lines (cyclic, ring oscillator, 2D, 3D)
  - Linearity improvement: sliding scale, wave union, stochastic
- Delay Elements are usually implemented as Voltage-Controlled Delay Cells (Current-Starved or Shunt-Capacitor) and their delay is stabilized against PVT variations using DLLs or PLLs
- Interfaces between interpolation stages, signal routing, effects of mismatches are critical at ps resolution levels
- TDCs are part of a bigger (HEP) system; performances at the system level are what counts!

*Thank you for your **TIME**!*