Silicon Tracking Detectors

M. Garcia-Sciveres
Lawrence Berkeley National Lab

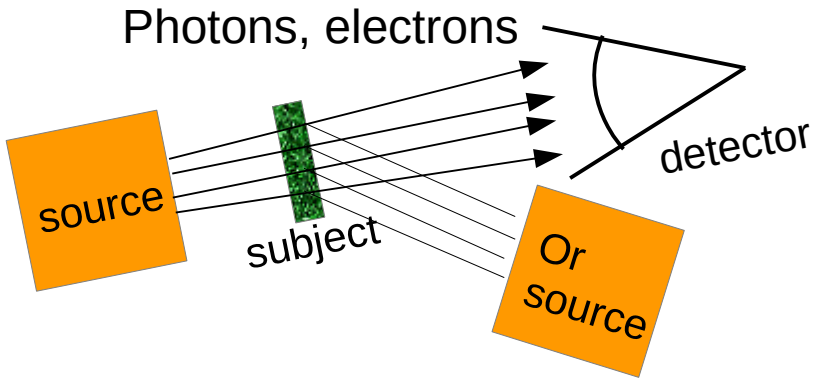
2022 HEPIC Summer Week – SLAC

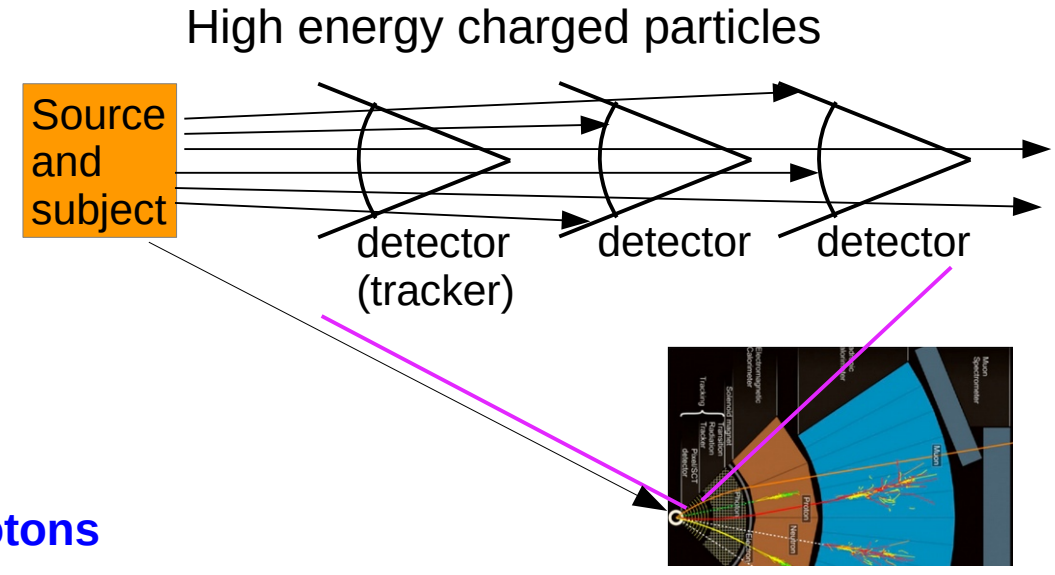
Close-up of ATLAS pixel detector, installed in 2007

Contents

- Imaging particles
- Pixel detector technology
- High rate challenges
- ASIC Radiation damage
- Summary

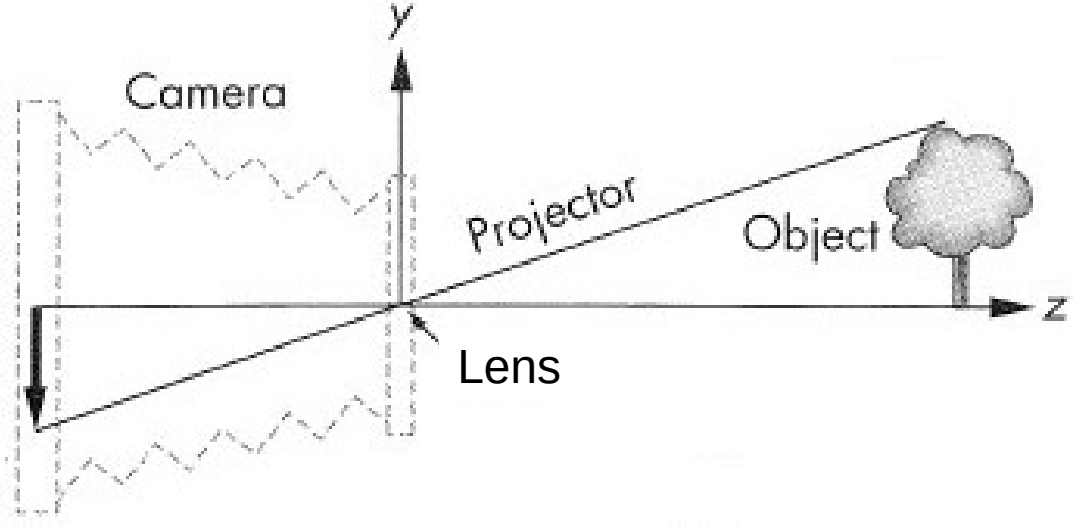
Imaging Particles



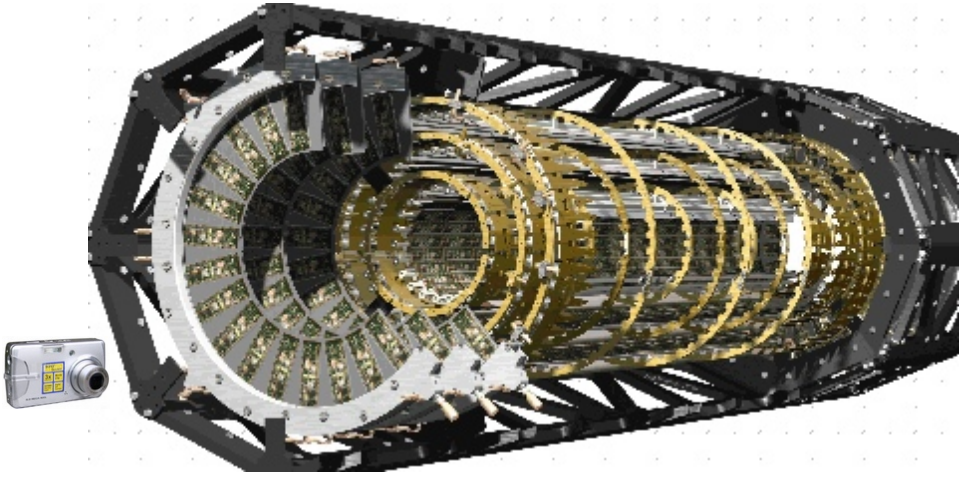


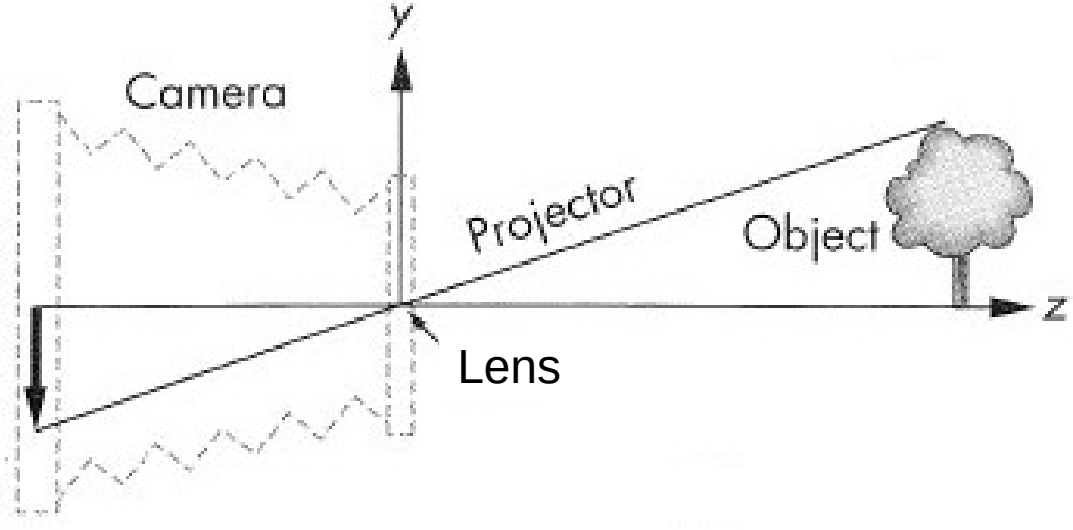
- **What you're used to:**
  - **Detector to completely stops photons**
  - **Lots of photons- every pixel gets some- source intensity limited on purpose**
  - **Integrate or count many photons per channel**
- **Crucial differences for Imaging high energy charged particles**
  - **Want particles to pass thorough imaging detector (aka tracker) as if it was not there. There are other detectors behind it**
  - **There is no sample. We are looking at the quantum vacuum. Want intensity as high as possible.**
  - **Measure every particle individually**

Inverse problem to usual imaging

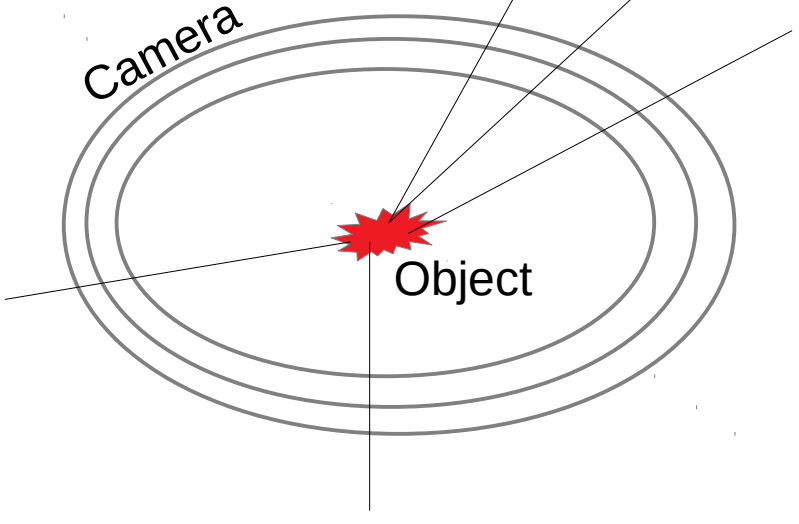


Inverse problem to usual imaging





Particle trajectories are the projectors

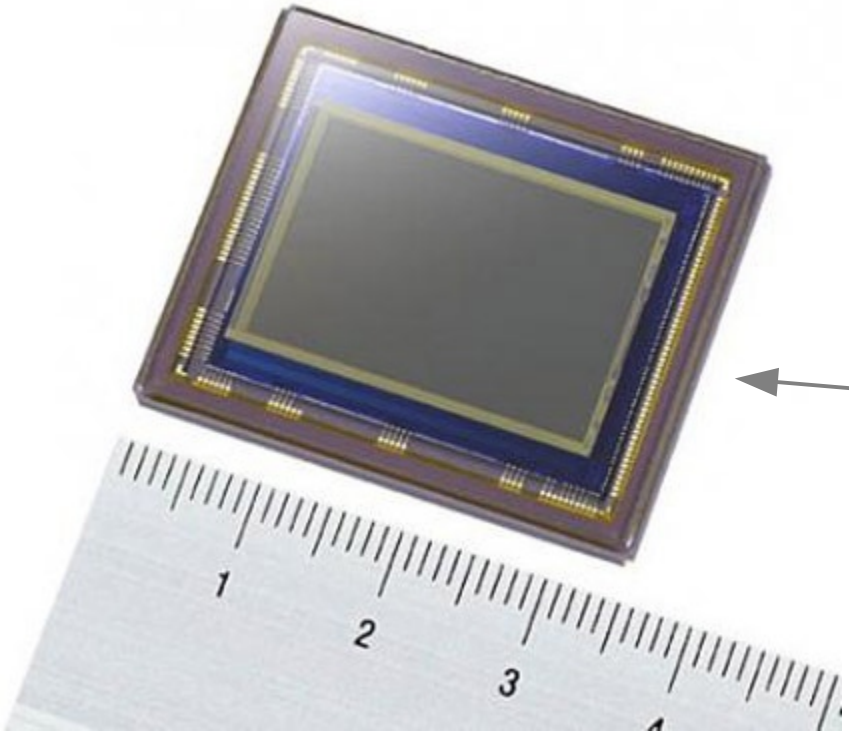


Clear?

Let’s do it

Let’s build ourselves a silicon pixel tracking detector

Let's do it

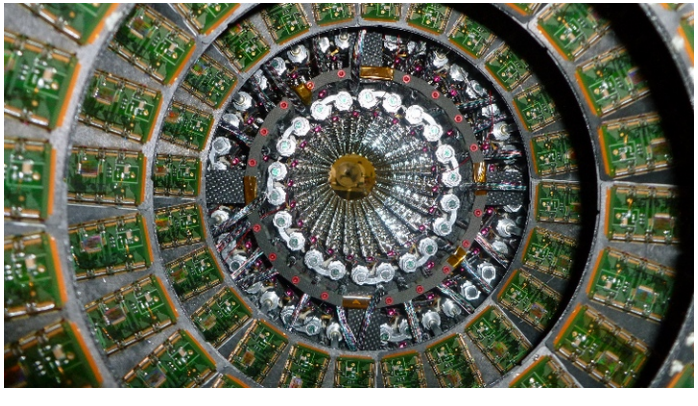


~2 cm^2

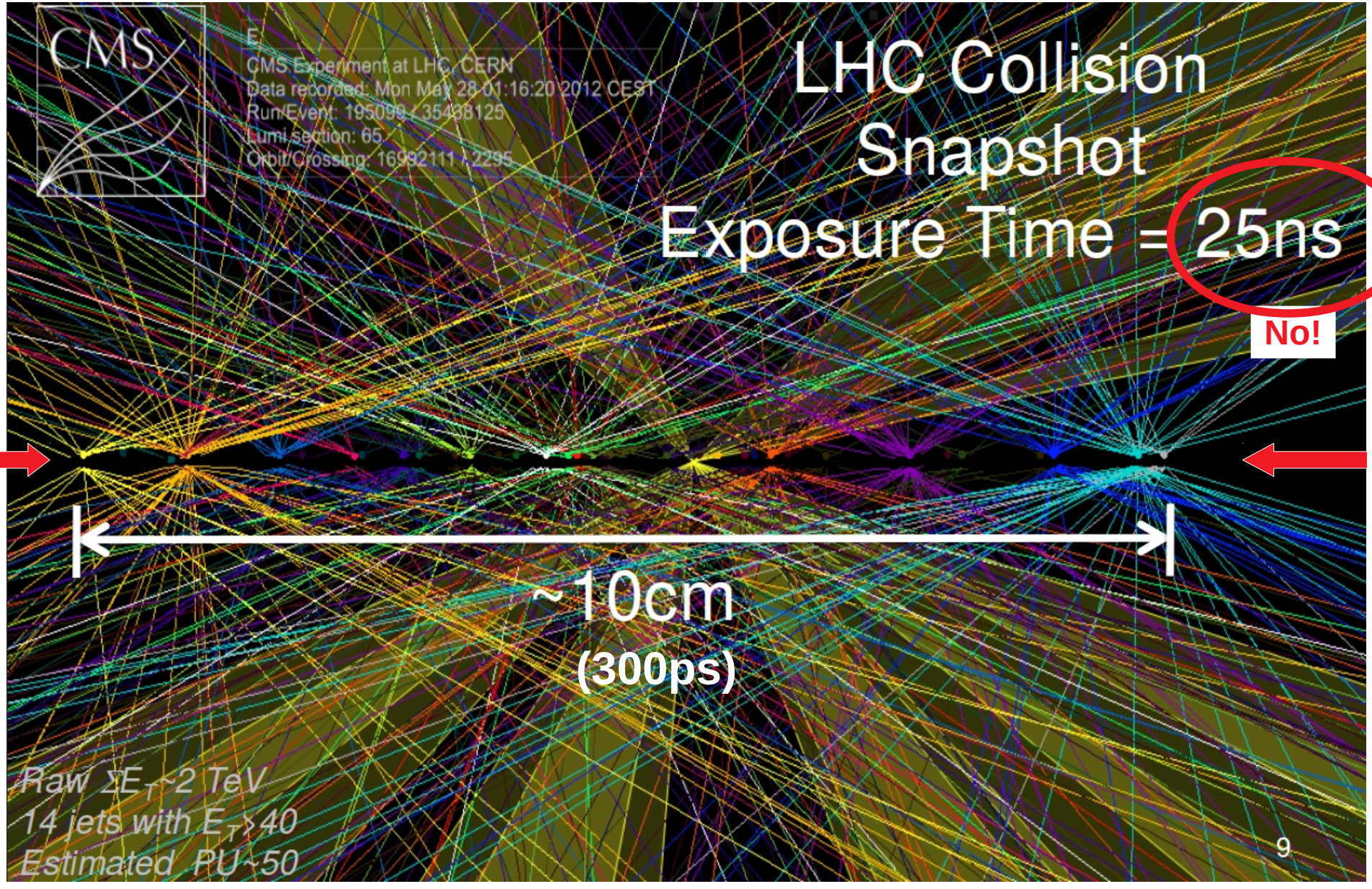
Surround interaction point with few layers of sensors

~100 000 cm^2

($500K plus tax)

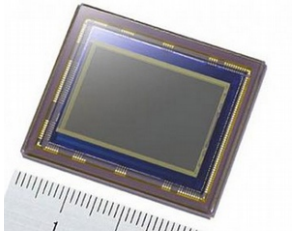


Will it work?


CMS
CMS Experiment at LHC, CERN
Data recorded: Mon May 28 01:16:20 2012 CEST
Run/Event: 195099 / 35438125
Lumi section: 65
Orbit/Crossing: 16992111 / 2295
LHC Collision
Snapshot
Exposure Time = 25ns
No!
p
p
~10cm
(300ps)
Raw ΣE_T~2 TeV
14 jets with E_T>40
Estimated PU~50
9

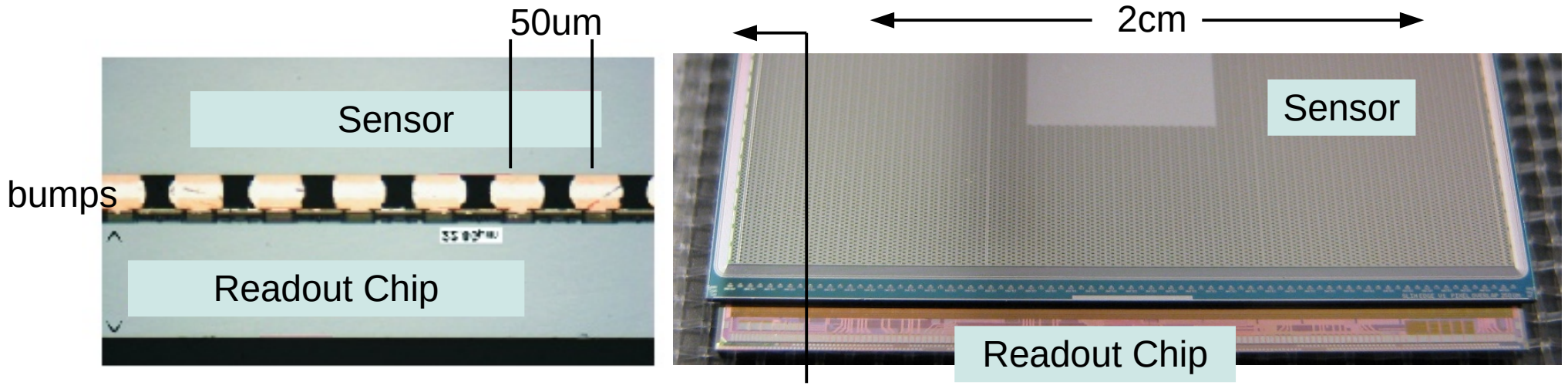
Back to the drawing board

- OK, so this thing can do 30 fps right?

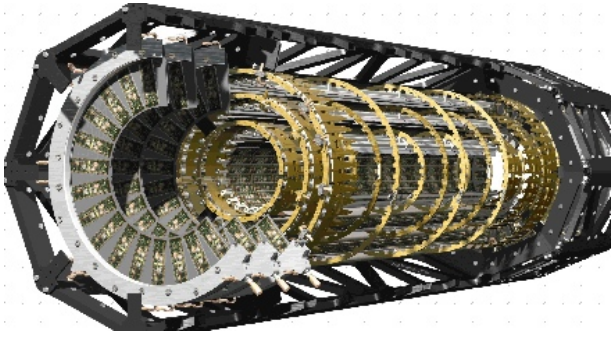


- Then instead of 50,000 sensors we need (40,000,000 / 30) * 50,000 = 65B sensors, which will only cost us $650B. Maybe we can get a volume discount?
-
-
-
- And that’s why we need custom ASICs to make tracking detectors
- Review how they’re actually made next (or just remember the tour)

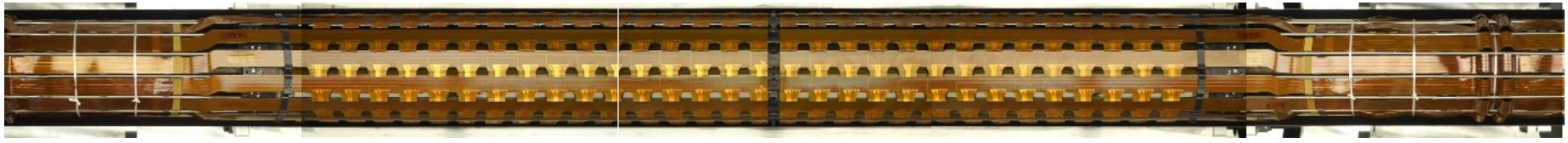
Hybrid Pixel Detector Technology



ATLAS
PIXEL
2007
80M pixels

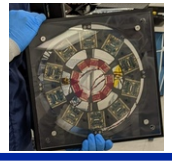


ATLAS
IBL
2014
12M pixels

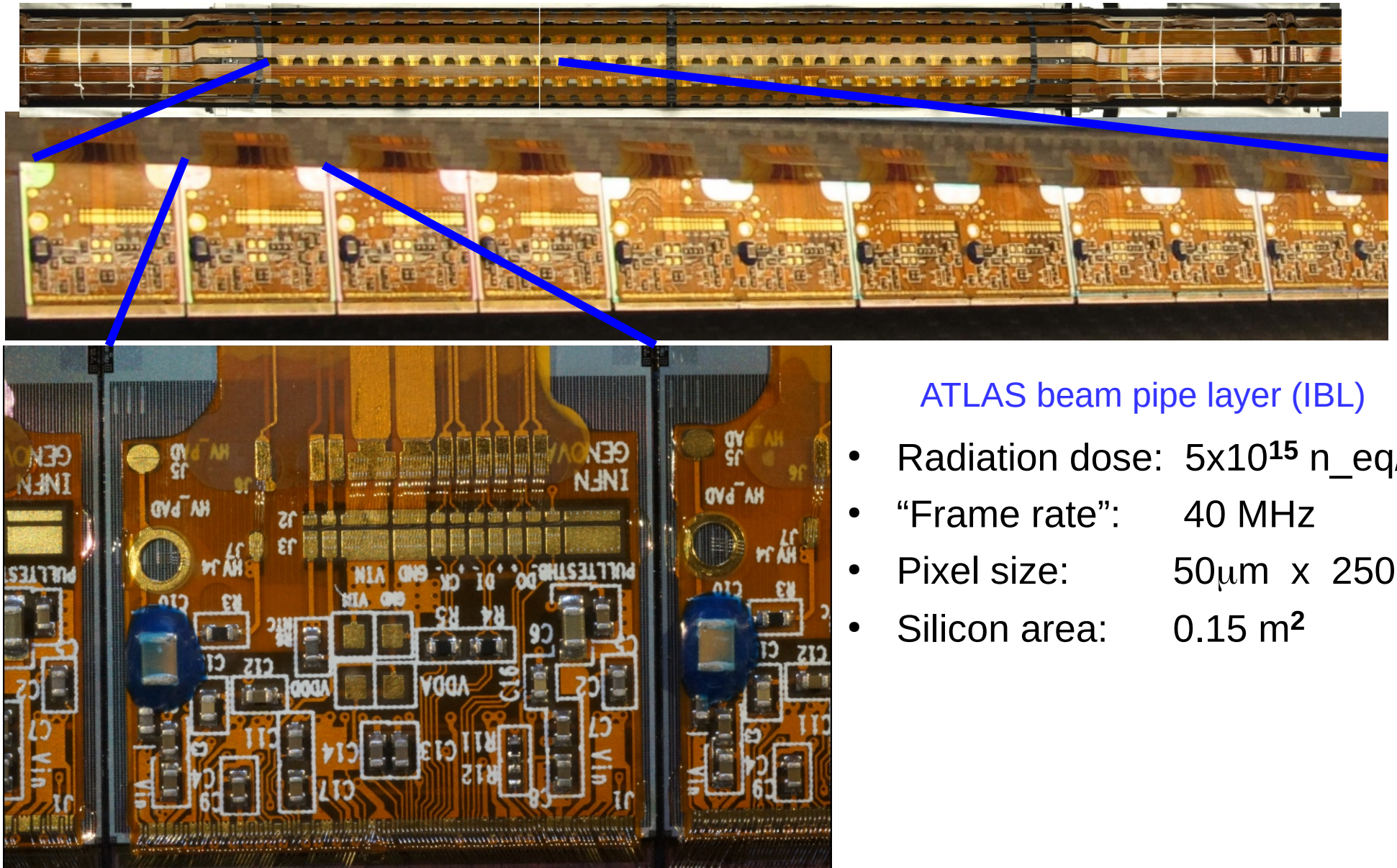


ATLAS ITK 2026, 5G pixels

Remember the tour...



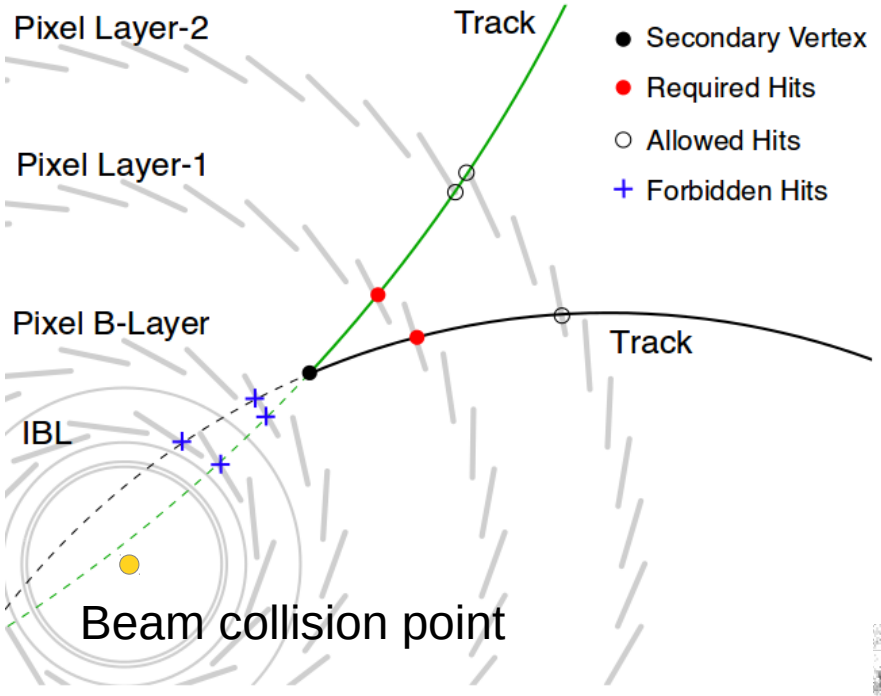
Hybrid Pixel Technology (IBL)

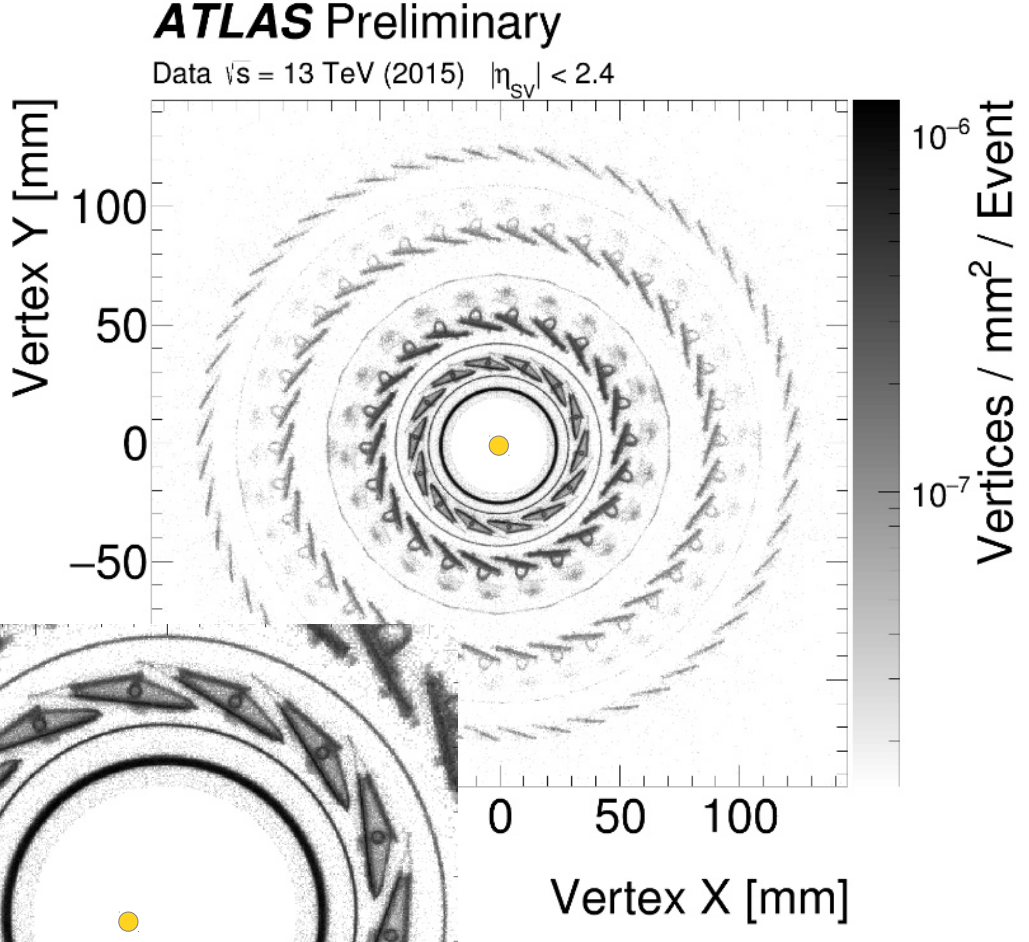


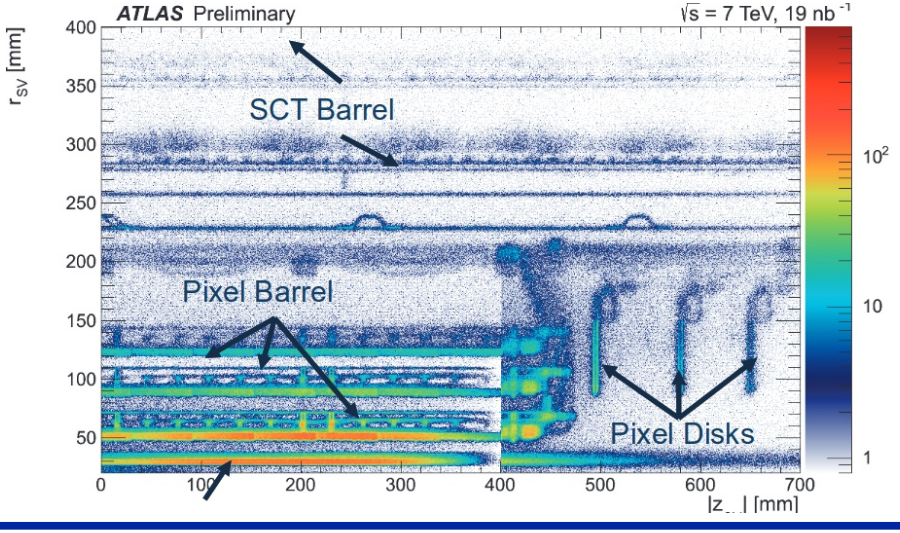
ATLAS beam pipe layer (IBL)

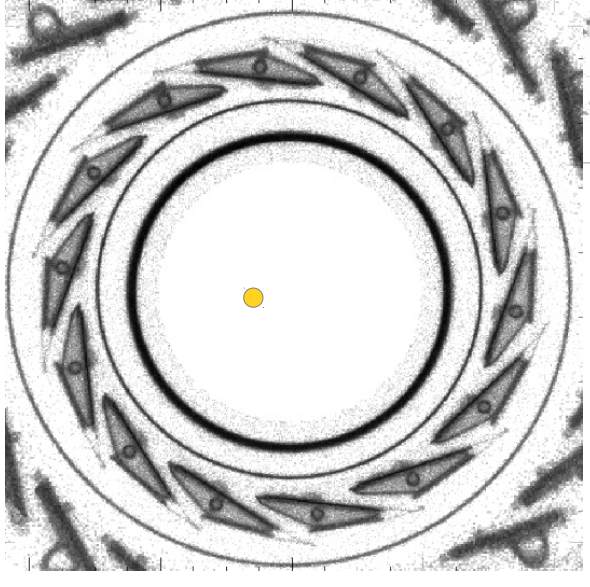
- Radiation dose: 5×10^{15} n_eq/cm^2
- "Frame rate": 40 MHz
- Pixel size: 50μm x 250μm
- Silicon area: 0.15 m^2

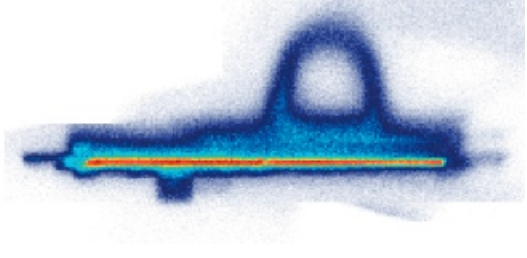
Detector can image itself in 3D



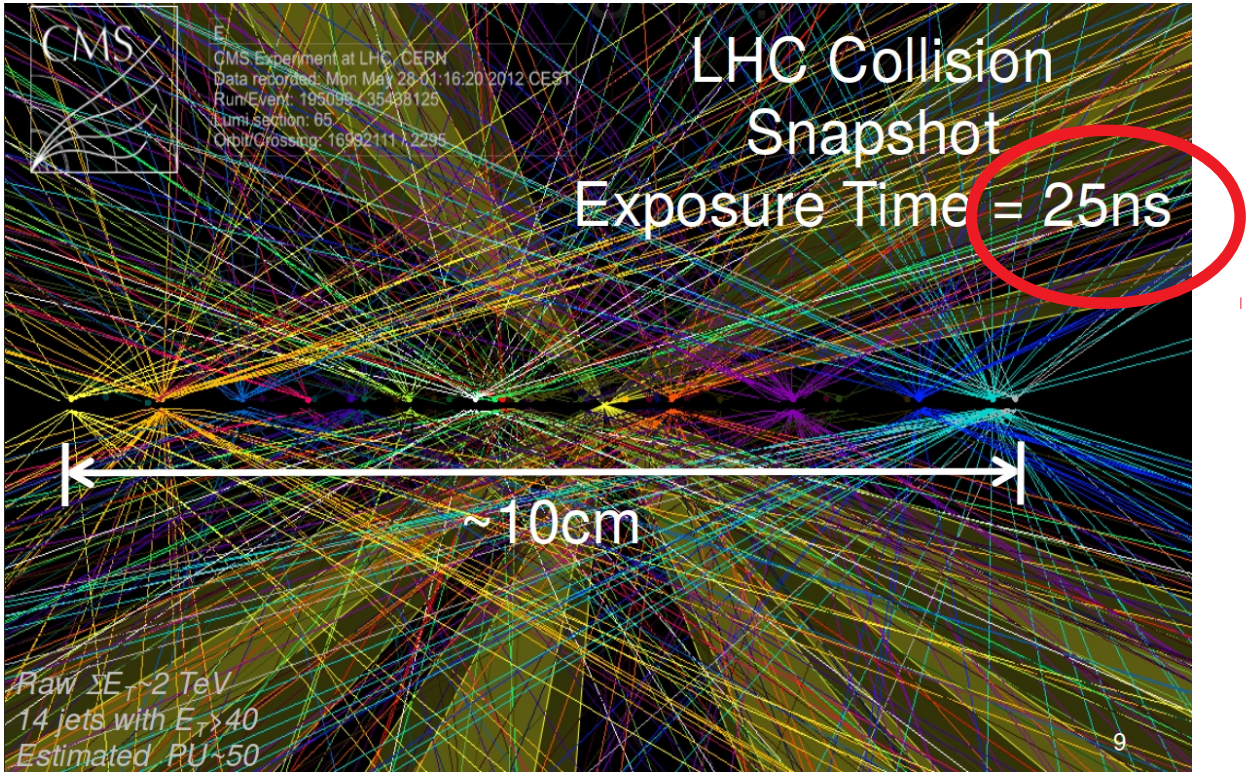








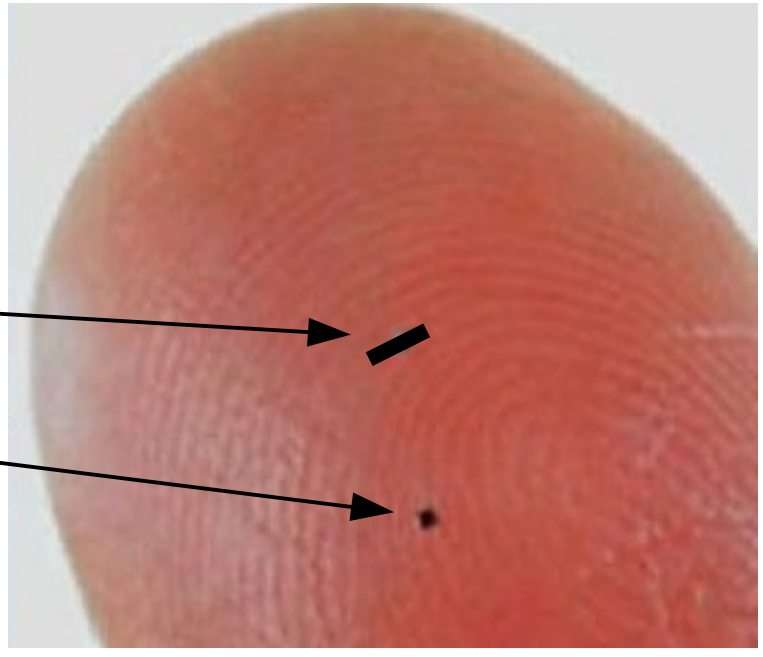
But how do we handle the rate?



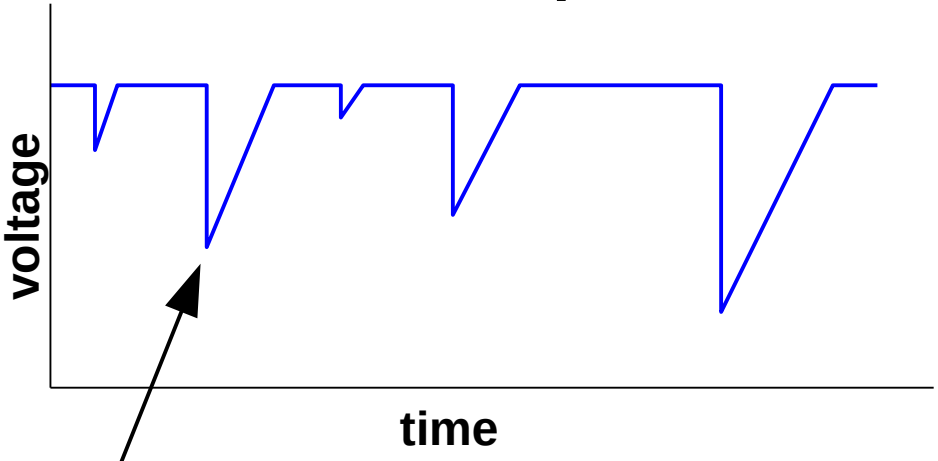
- Capturing 40M 5Gpixel images per second is not feasible.
- Triggering only saves a factor of 40 in readout
  - 1M 5Gpixel images per second is still far from feasible
- A: We do NOT do conventional image capture.
- We treat every pixel as an independent, free-running detector and store it's output (heavily redacted)

Single Pixel Perspective

Pixel size



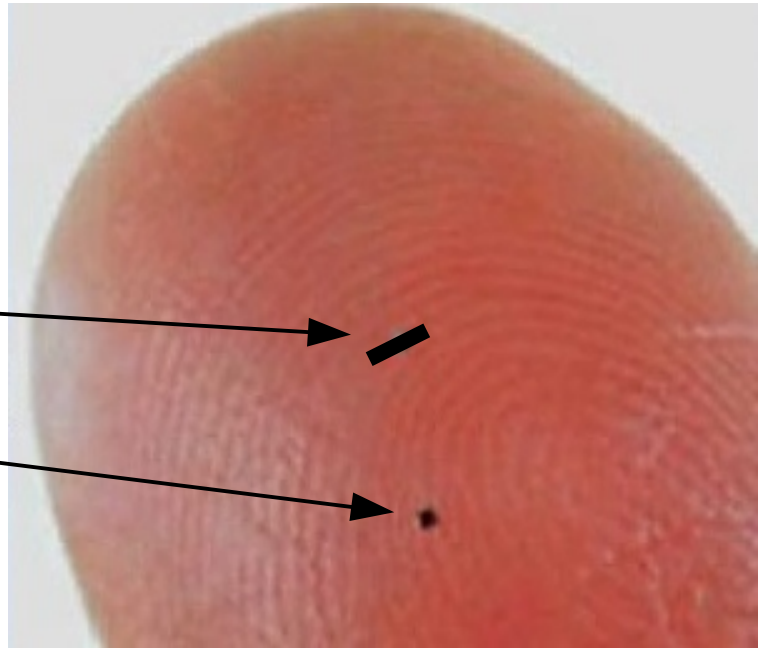
Pixel output



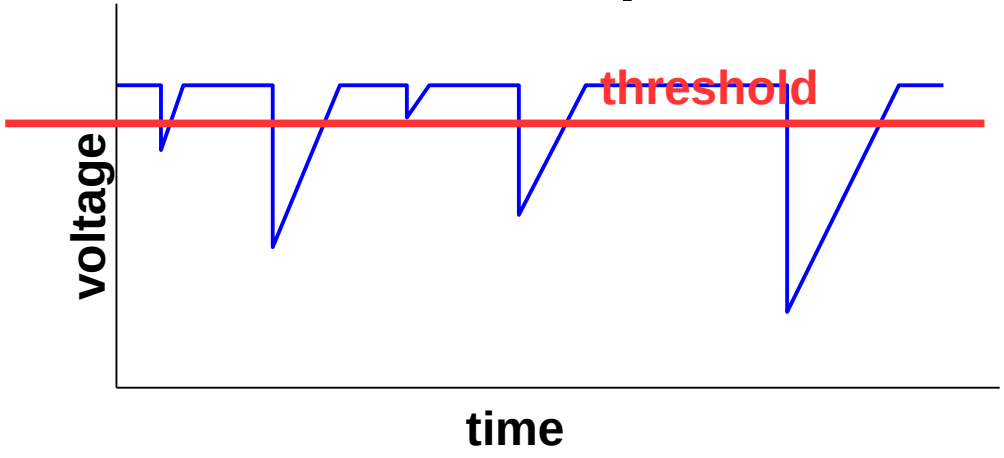
Hits
~50 kHz
(not too bad compared to 40 MHz)

Single Pixel Perspective

Pixel size

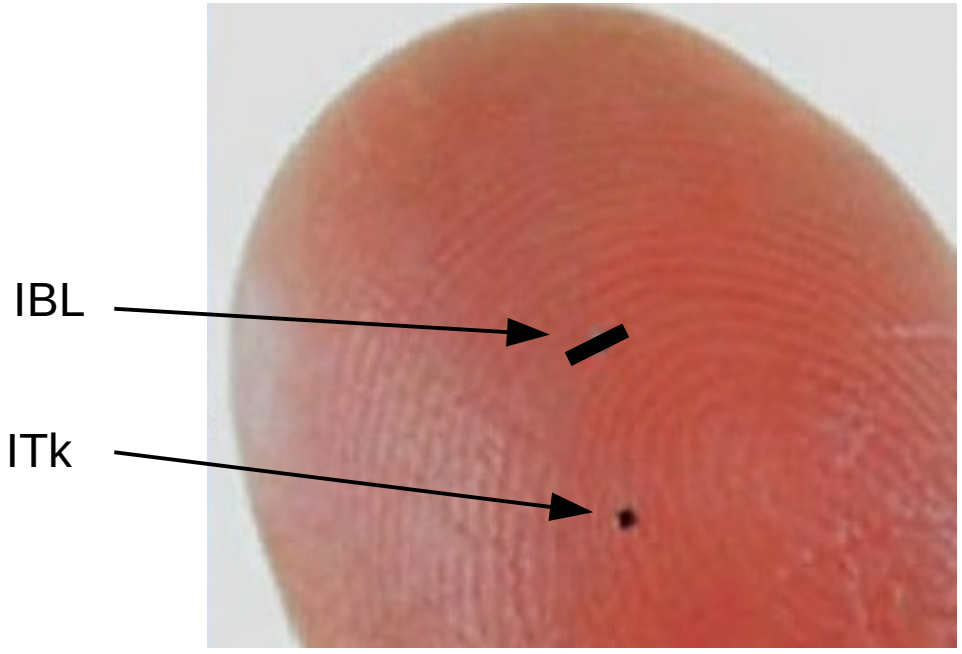


Pixel output

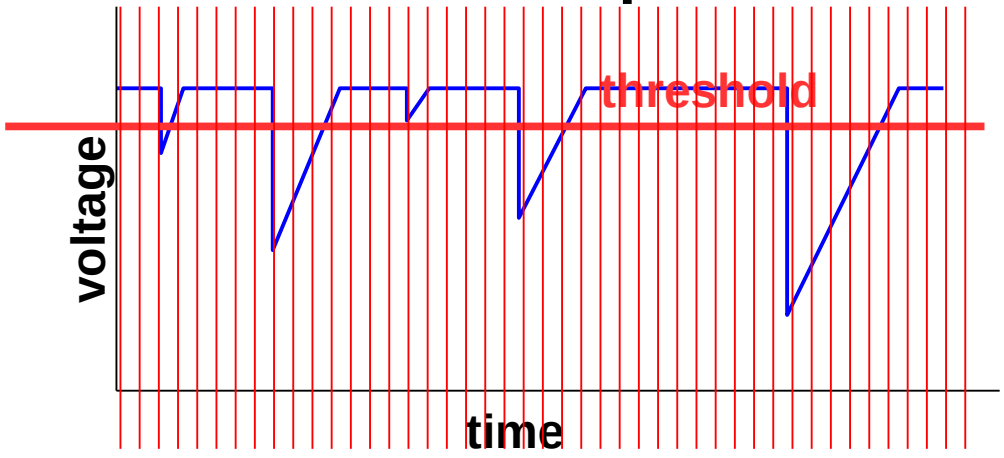


Single Pixel Perspective

Pixel size



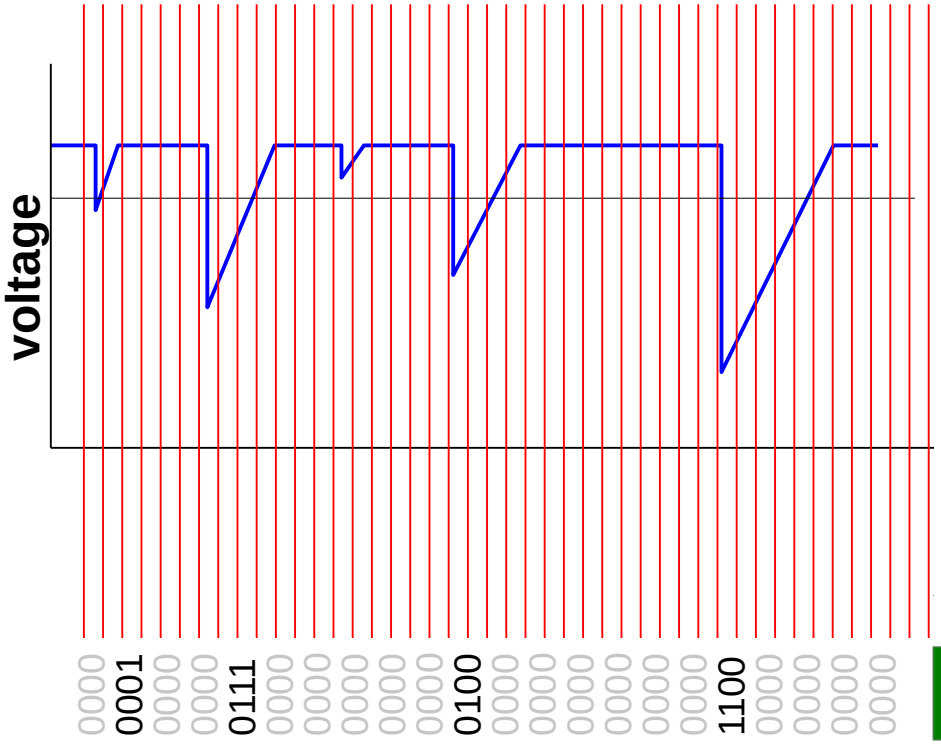
Pixel output



Bunch crossings

Digitize amplitude above threshold in each Bunch Crossing

On-Chip Storage and Trigger



On-chip memory ("FIFO")

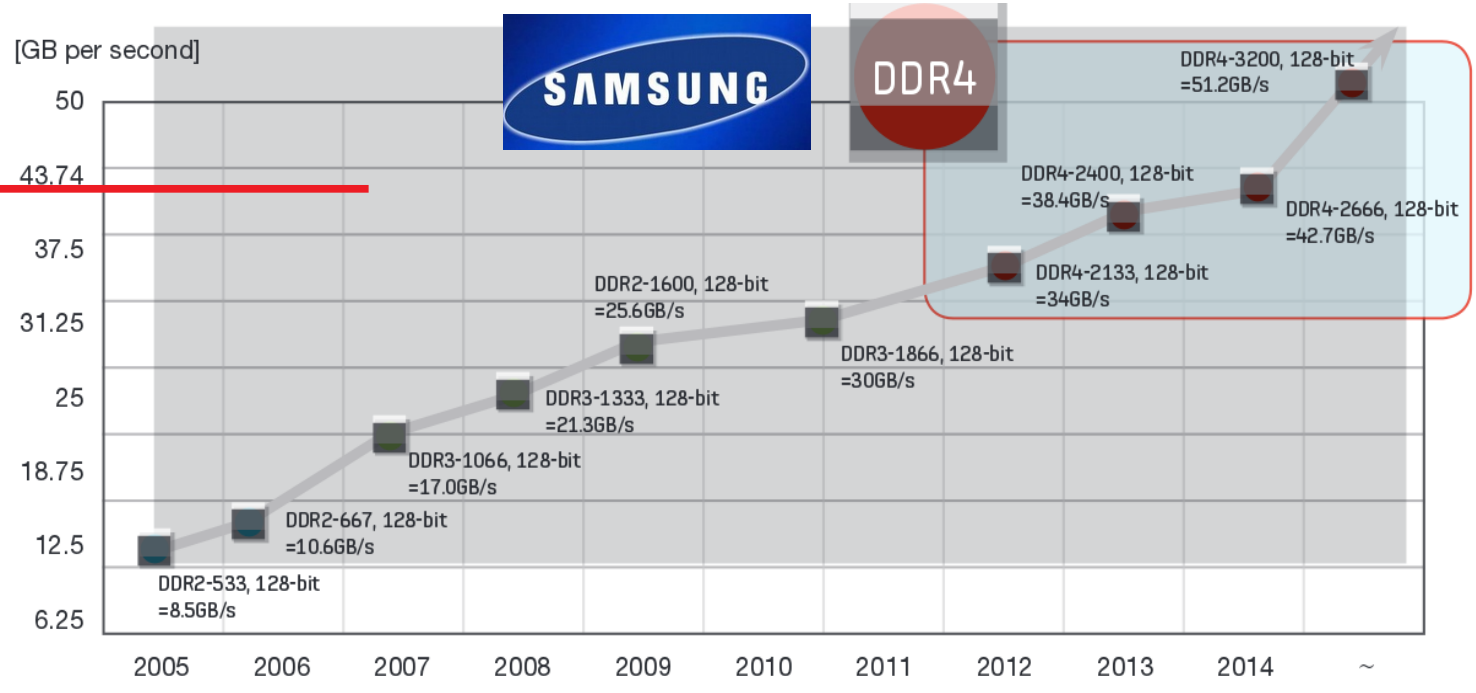
Readout ~Gbps

Storage of all individual hits W/ ADC value (~40 Gbps for a 100Kpx chip)

Triggers (select 1/40 slice times)

Did I just say a chip is storing 40Gbps?

High rate pixel readout chips are memories (in addition to being pixel readout chips)



40

Figure 2. DDR4 higher performance compared with DDR3L and DDR2

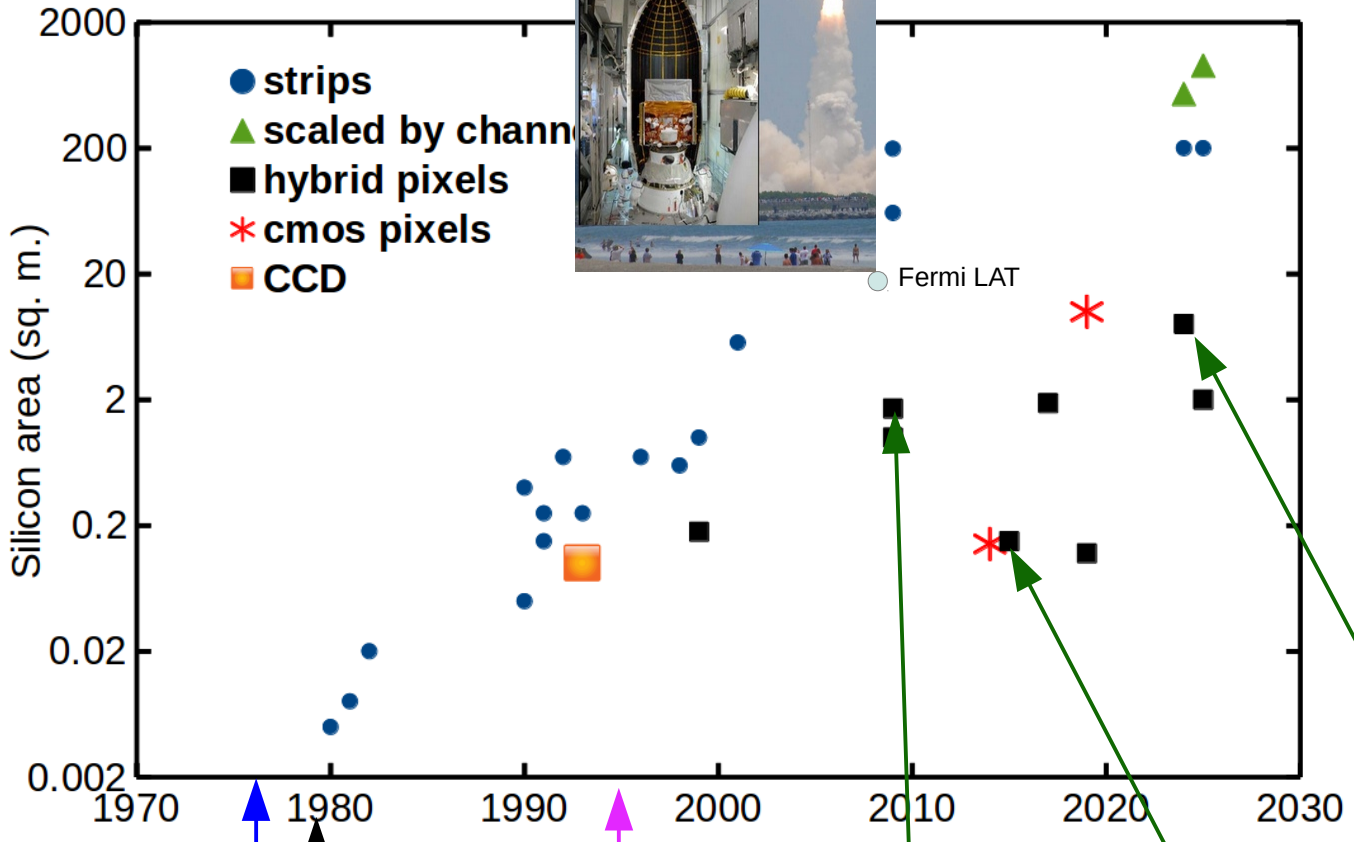
Plot is for a memory module containing 8 silicon chips so B = b

(and this is not rad hard)

Silicon Detectors at Colliders

(and in orbit)

Fermi LAT



Strip Detectors

1980	NA1
1981	NA11
1982	NA14
1990	MarkII
1990	DELPHI
1991	ALEPH
1991	OPAL
1992	CDF SVX
1993	L3
1996	CDF SVX'
1998	CLEO III
1999	BaBar
2001	CDF SVXII+ISL
2009	ATLAS SCT
2009	CMS tracker
2025	ATLAS ITK
2025	CMS upgrade

Hybrid Pixels

1999	Delphi
2009	ATLAS
2009	CMS
2015	ATLAS IBL
2017	CMS
2019	velopix
2025	ATLAS
2025	CMS

CMOS Pixels

2014	STAR
2019	ALICE

CCDs

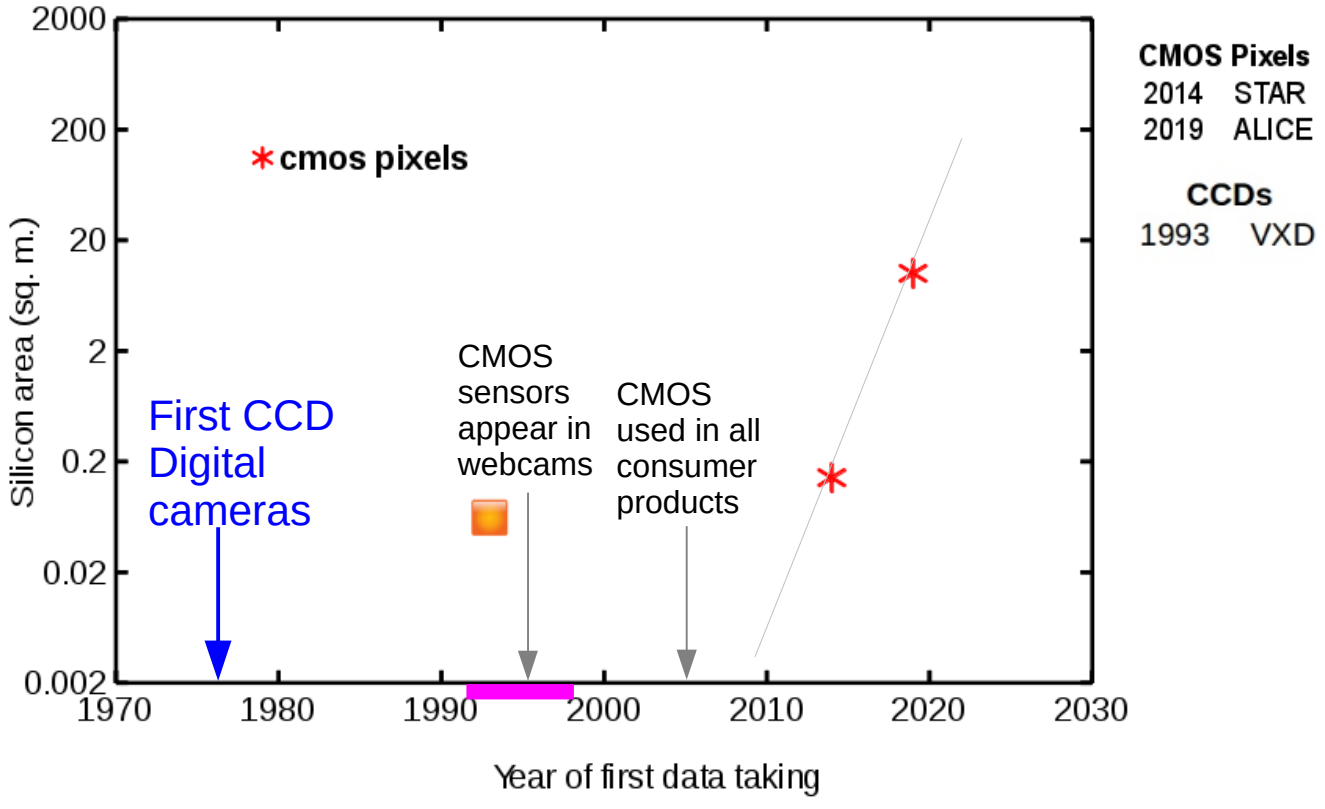
1993	VXD

pixel

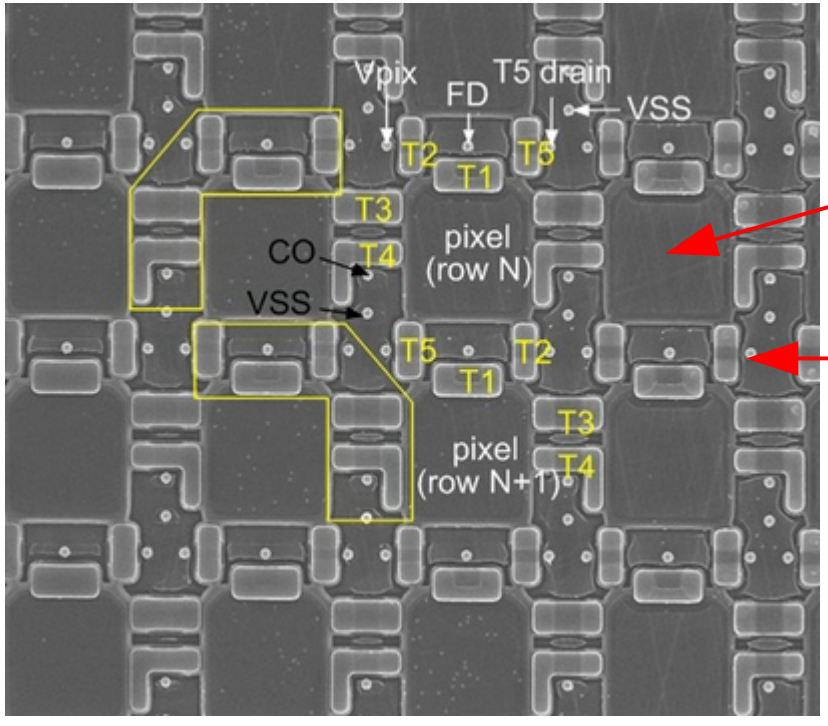
IBL

ITk

Connection to Consumer Electronics



Close-up of CMOS camera sensor



Photodiode covers about half the pixel area in this example

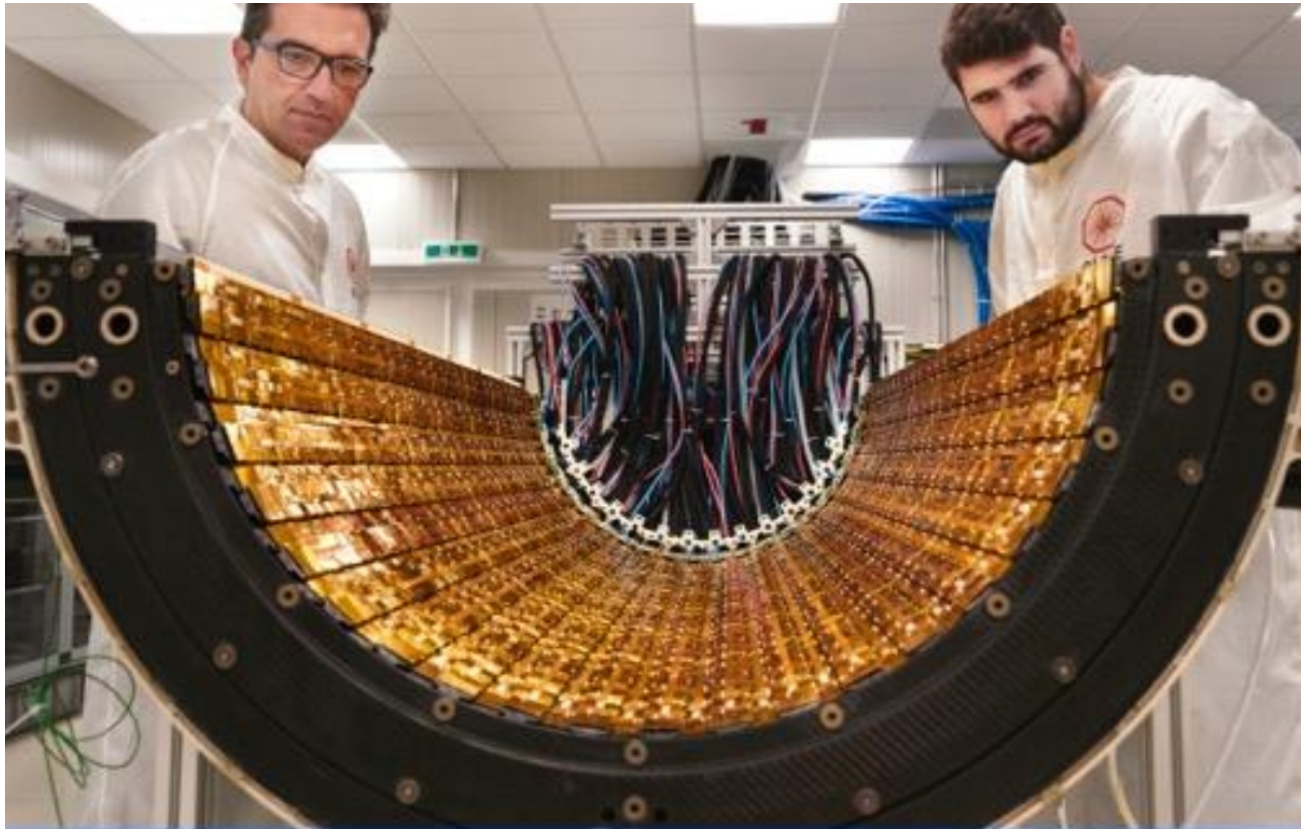
Metal traces have been removed. They run over the transistors leaving photodiode exposed

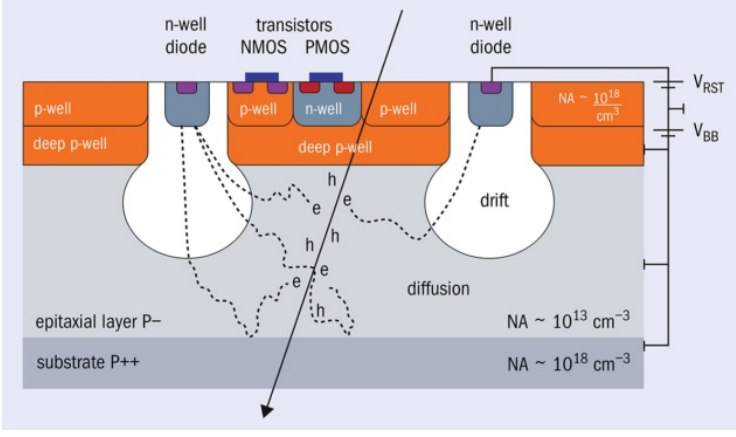
For particle tracking need 100% fill factor

Need low enough noise that can detect a single particle

Need radiation hardness

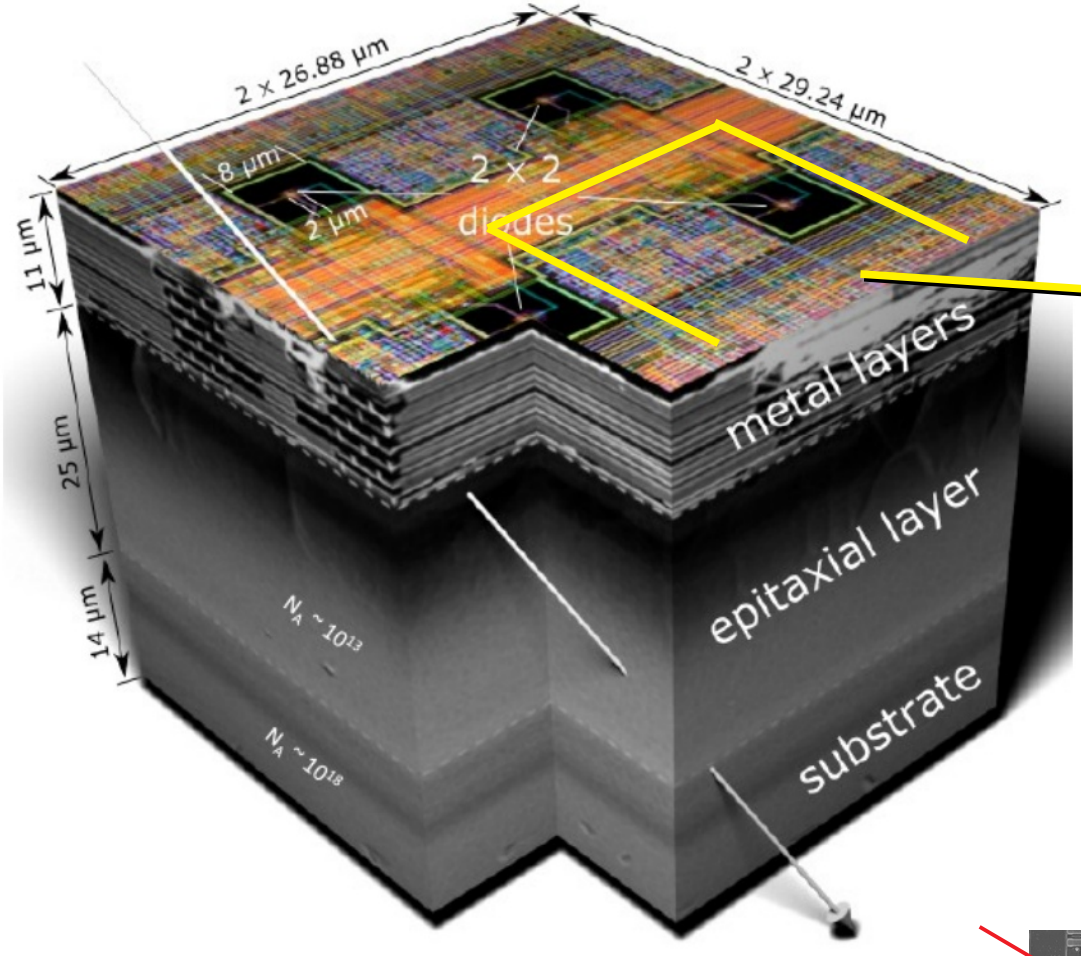
ALICE just installed a 10m^2 tracker made of CMOS sensors

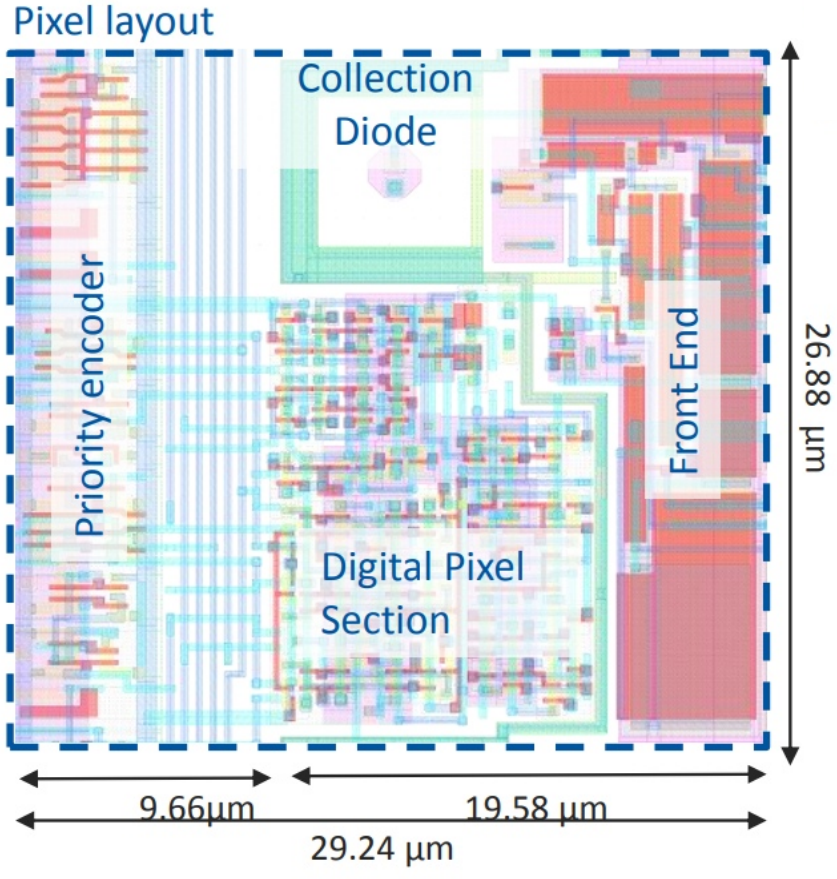


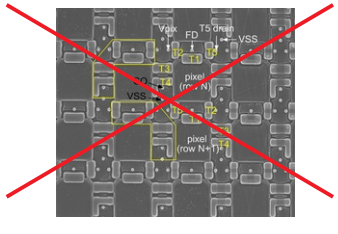


Highly customized CMOS process. Proprietary. Not portable

ALPIDE sensor chip- not a simple 3T pixel







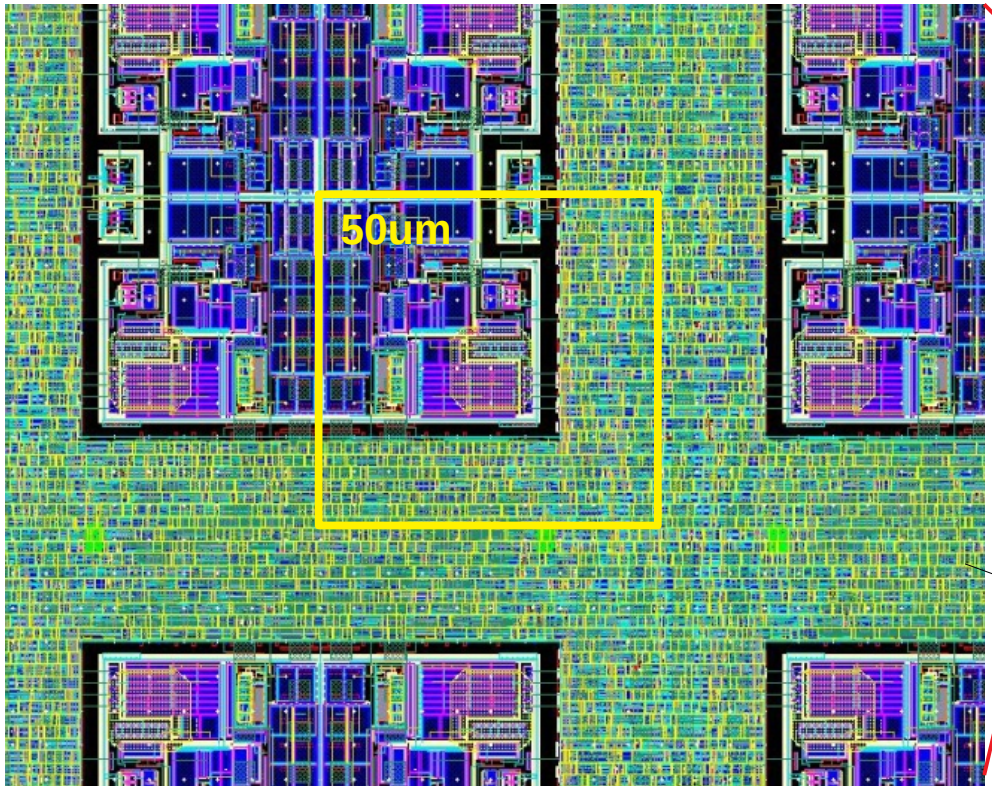
~100 transistors

RD53 Hybrid Pixel Readout
100x higher rate and radiation

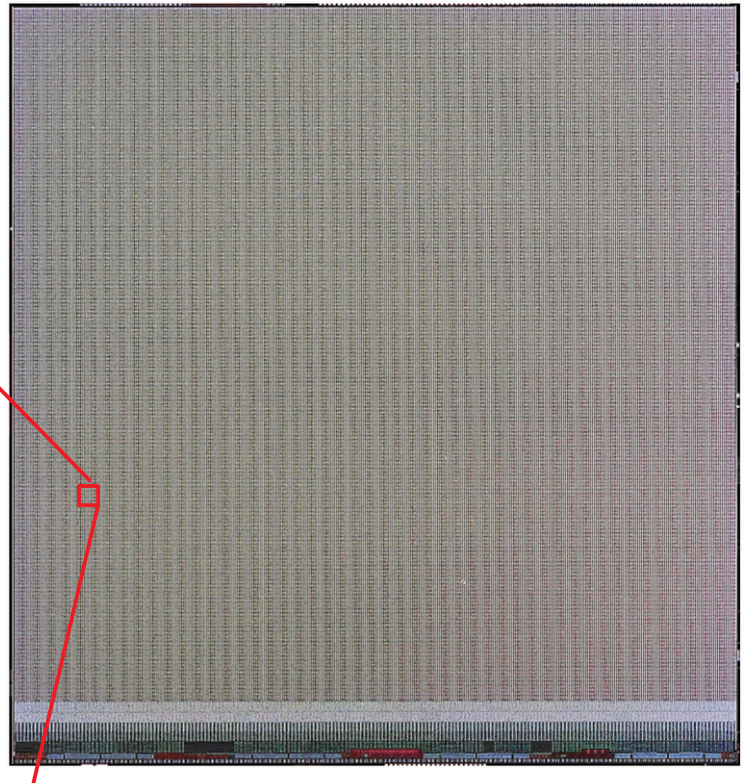
Cern.ch/rd53

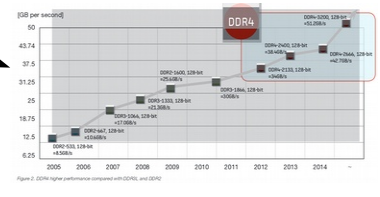
RD-53 Collaboration Home

RD-53 will design and produce the next generation of readout chips for the ATLAS and CMS pixel detector upgrades at the HL-LHC. More details can be found in the 2018 extension proposal and the original collaboration proposal.

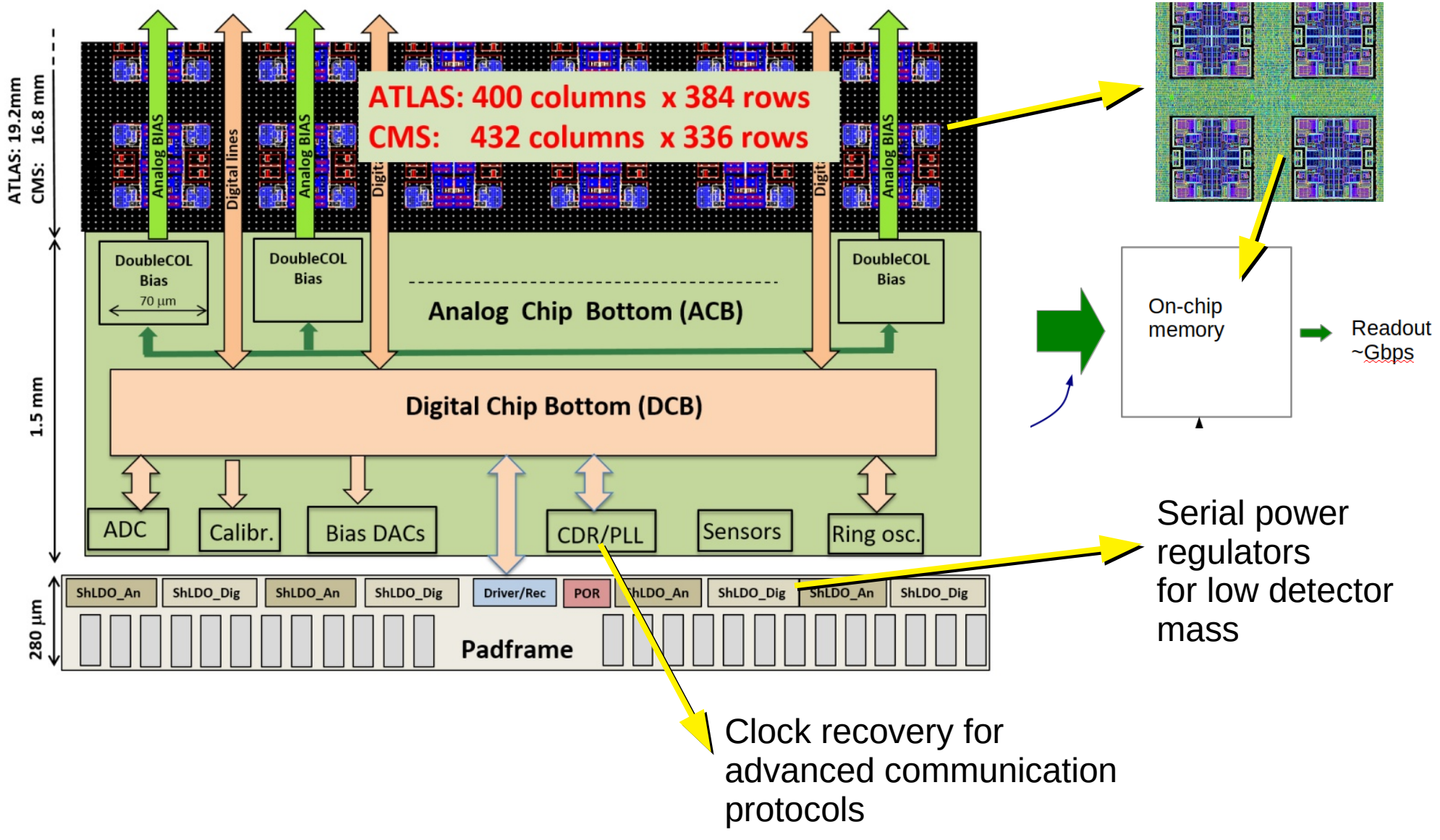


~1000 transistors

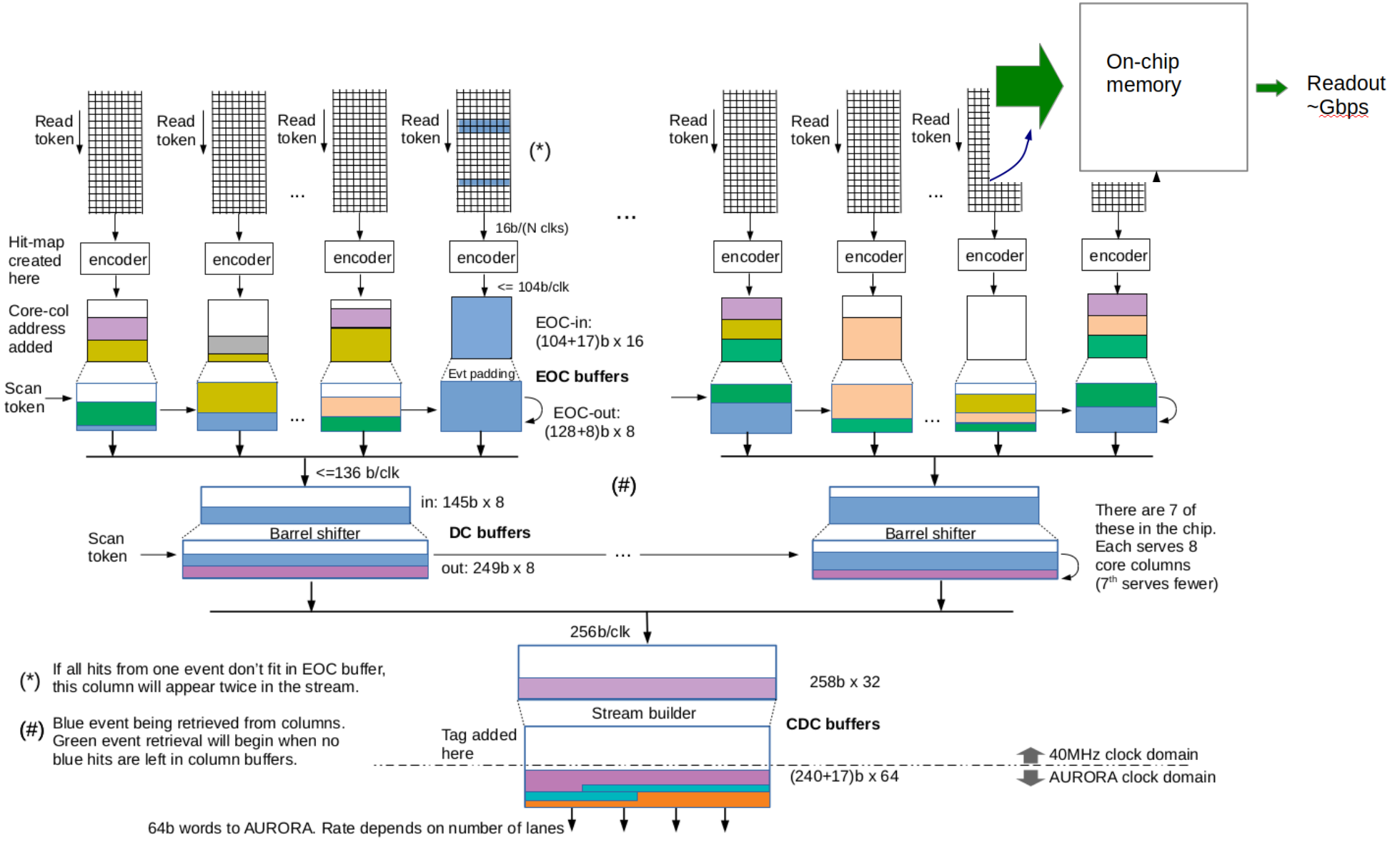




Complex system on chip

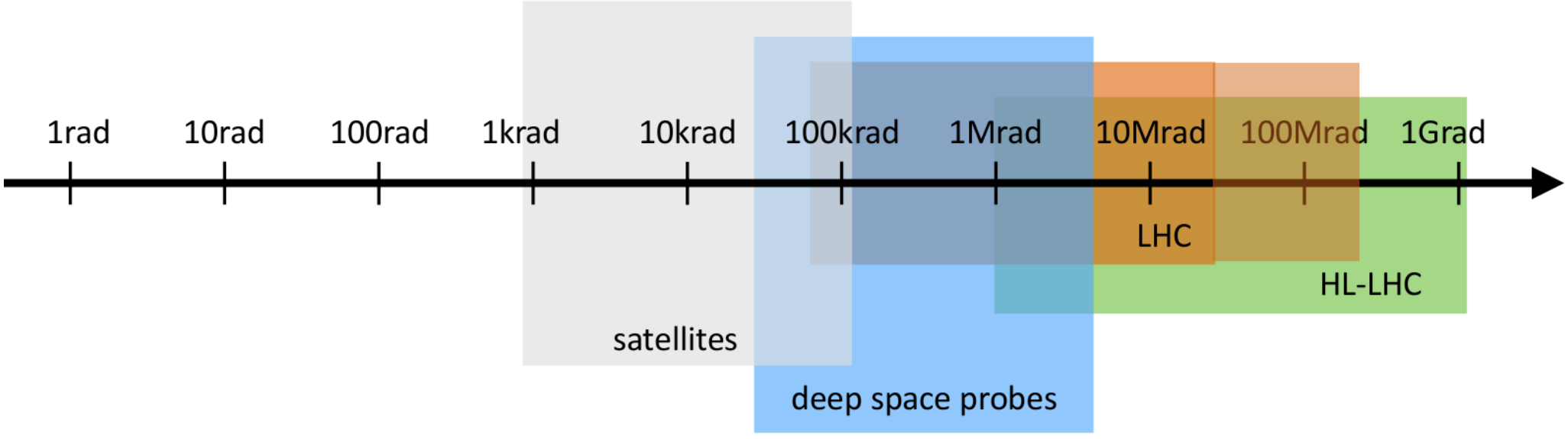


Example of non-trivial processing

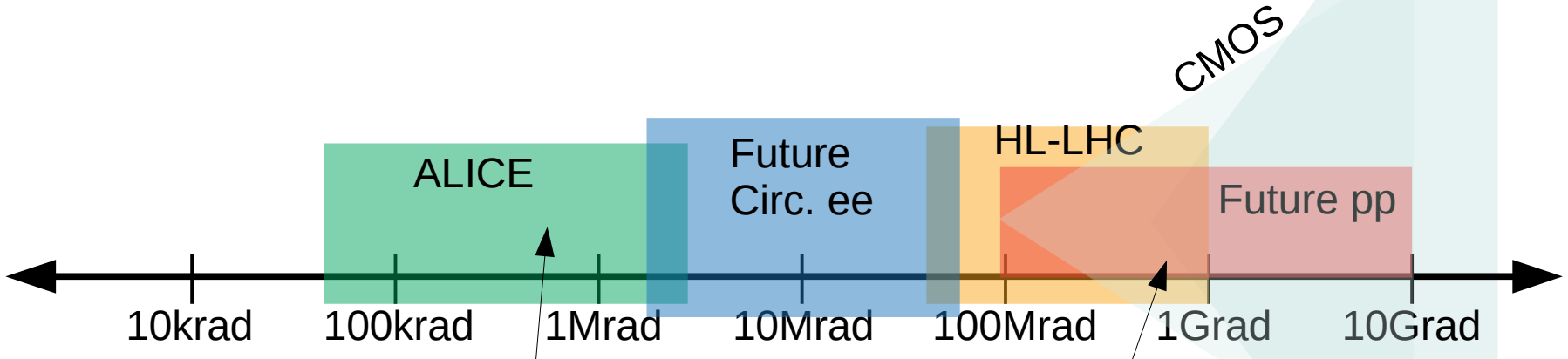


Large design effort
(top end of the scale for HEP)

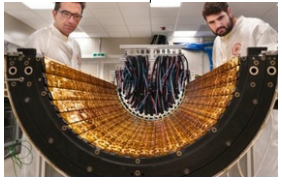
Radiation Environments

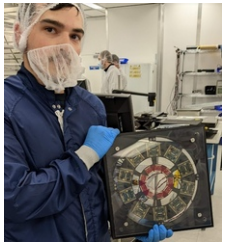


HEP IC Radiation Outlook



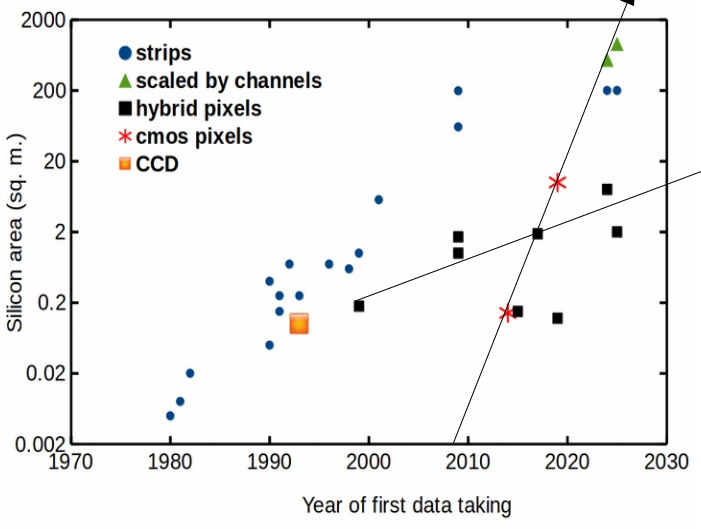
Inner Layer Dose

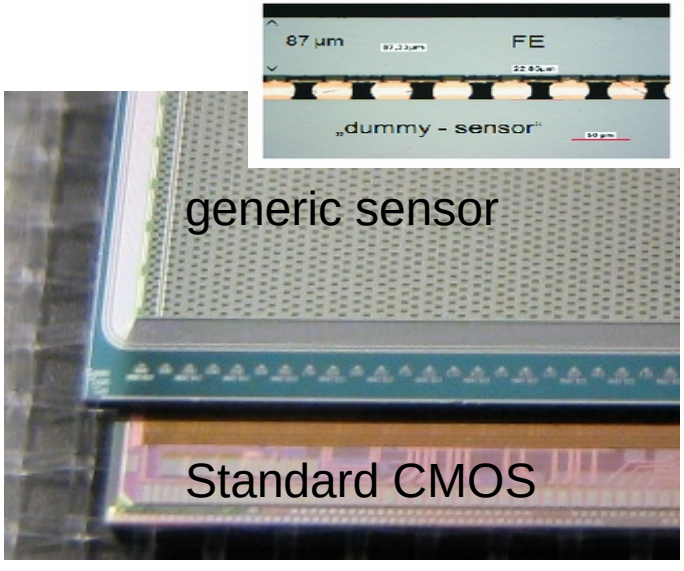


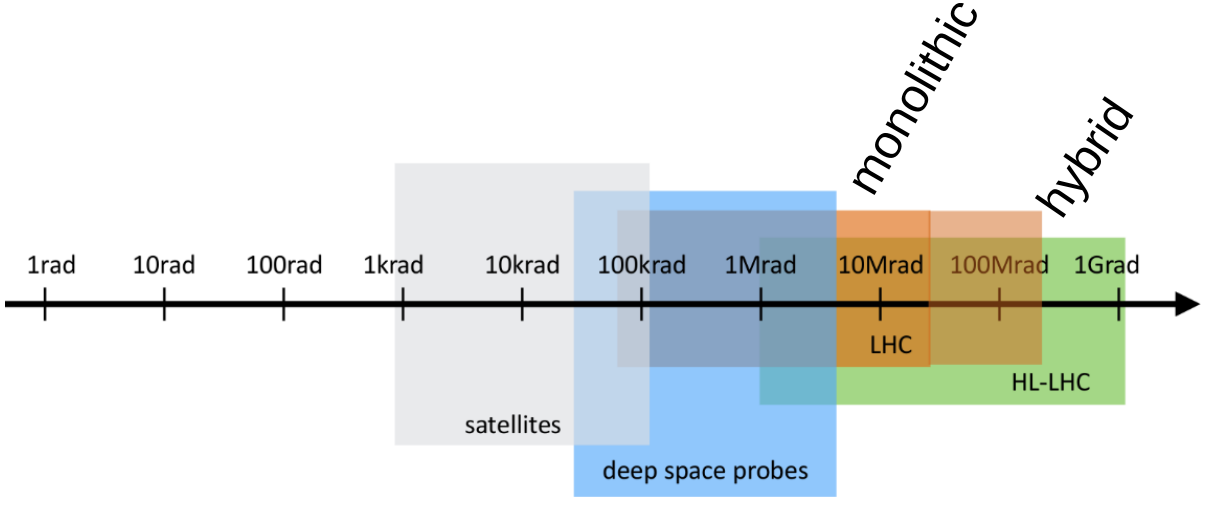


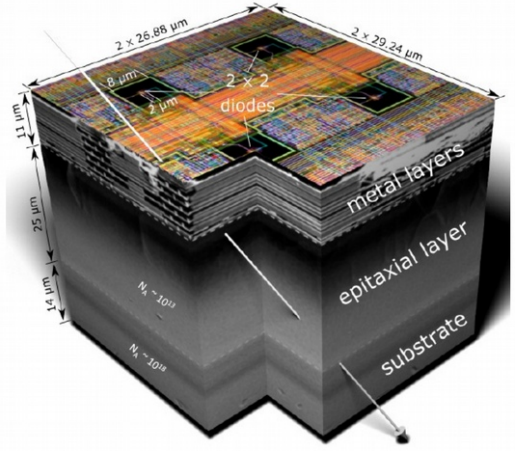
Temperature history
Process details
Dose rate
Dose history
Annealing
…

Trade-offs







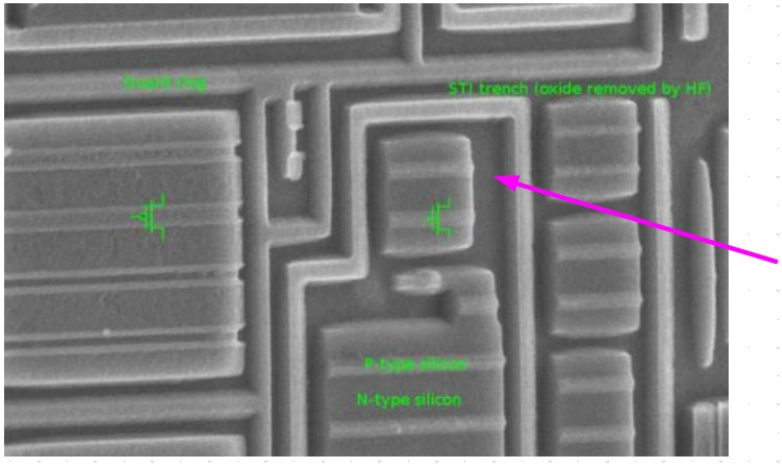


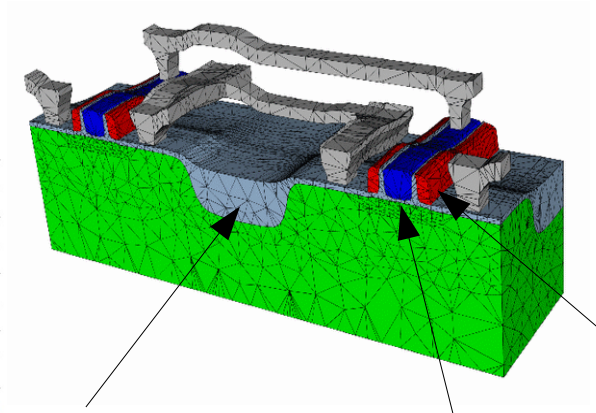
Highly customized non-portable process

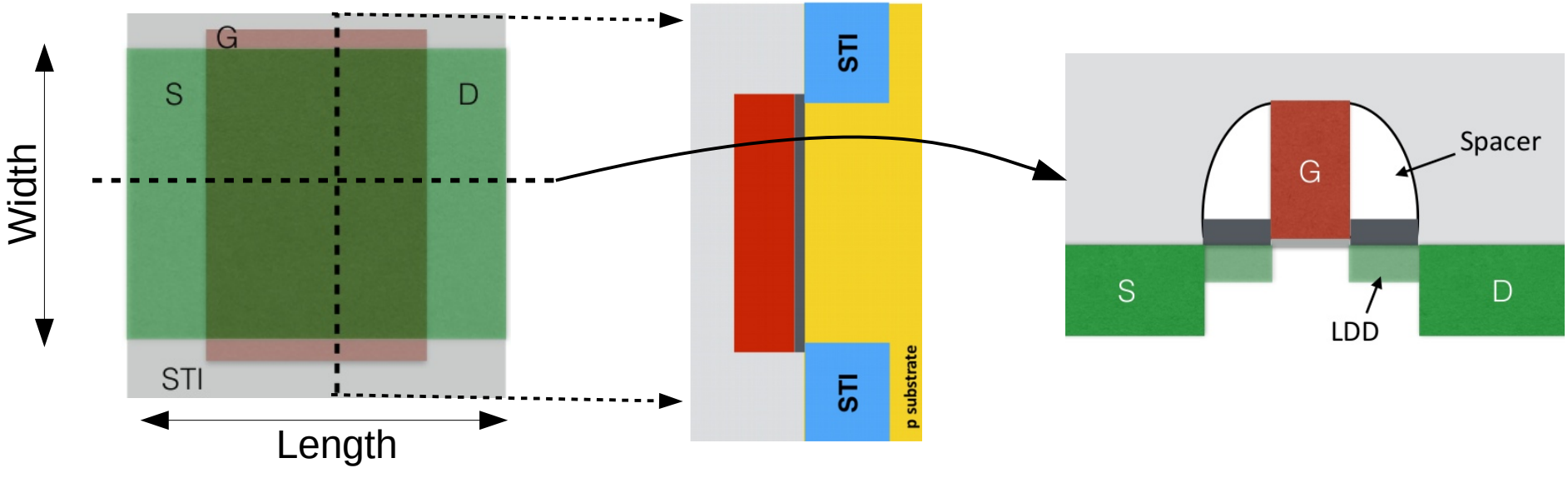
IC Electronics Radiation Damage

- Change in effective doping is insignificant, because doping levels in CMOS transistors are very high.
- All radiation damage effects to CMOS are due to parasitic electric fields form charge trapped in oxides and oxide-silicon interfaces
- Meet the oxides:
  - Gate oxide
  - Field Oxide
  - Buried Oxide (only for SOI)
  - Shallow trench Isolation (STI)
  - Gate Spacer

STI, Gate, Spacer





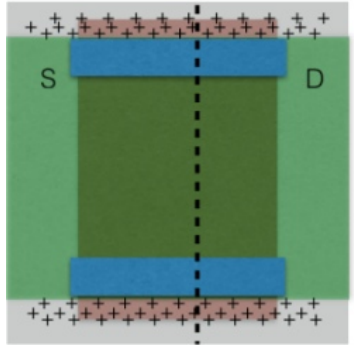


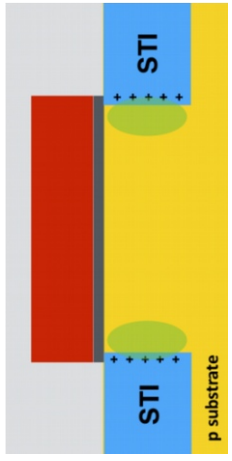
RINCE

Radiation Induced Narrow Channel Effect

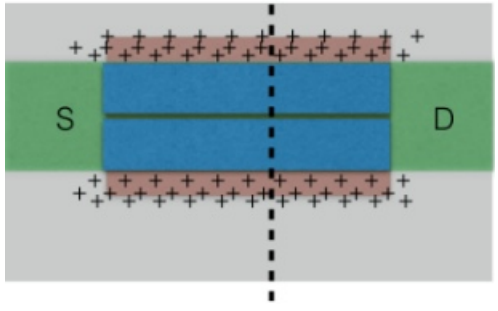
F. Faccio and G.Cervelli, "Radiation induced edge effects in deep submicron CMOS transistors", IEEE Trans. Nucl. Science, Vol.52, N.6 (2005) pp.2413-2420 http://dx.doi.org/10.1109/TNS.2005.860698

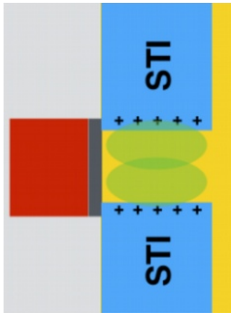
Wide Transistor

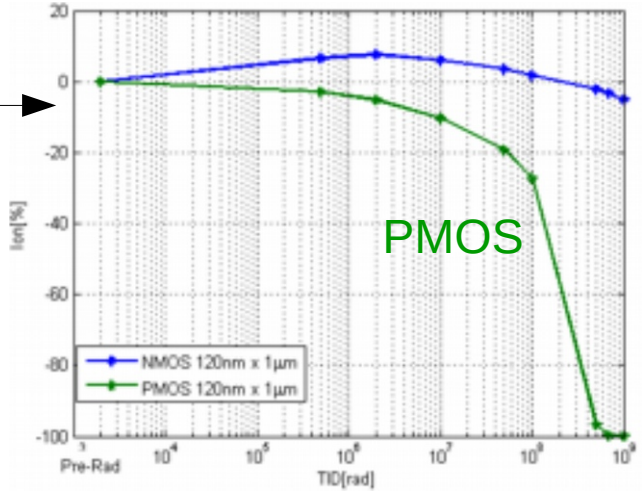




Narrowest Transistor





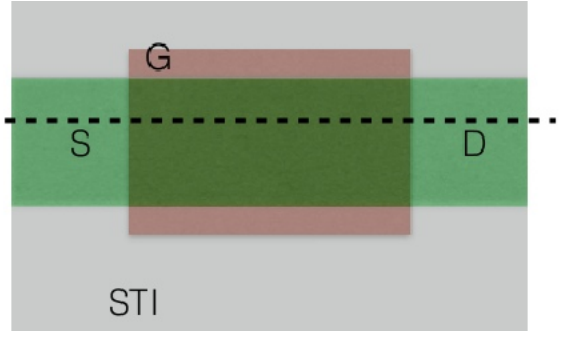


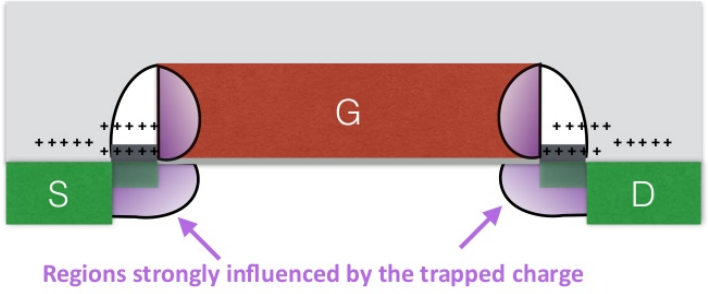
1Grad

Radiation Induced Short Channel Effect

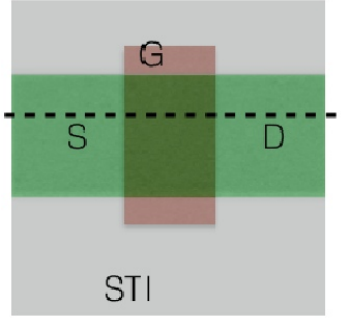
F. Faccio et al., "Radiation-Induced Short Channel (RISCE) and Narrow Channel (RINCE) Effects in 65 and 130 nm MOSFETs," IEEE Trans. Nucl. Science, Vol.62 , N.6 (2015) http://dx.doi.org/10.1109/TNS.2015.2492778

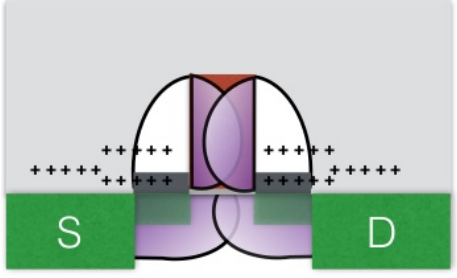
Long Transistor

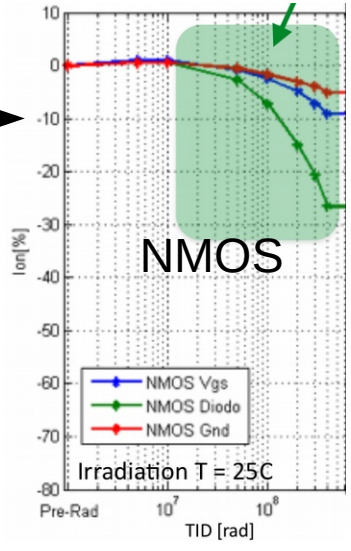


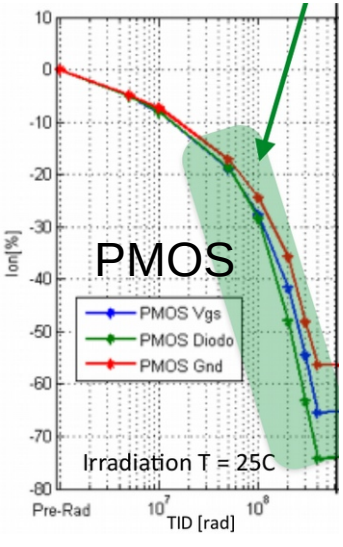


Shortest Transistor





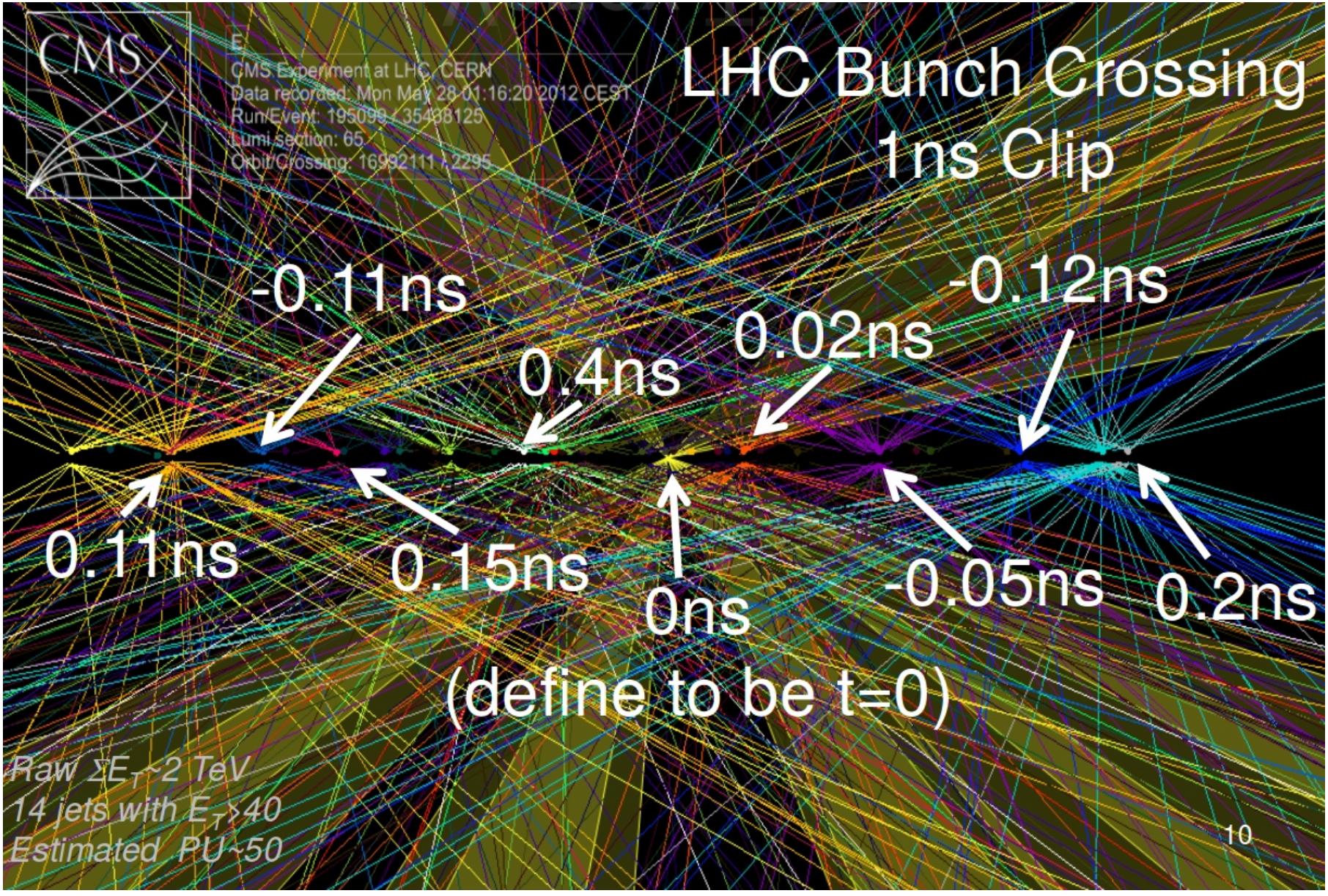




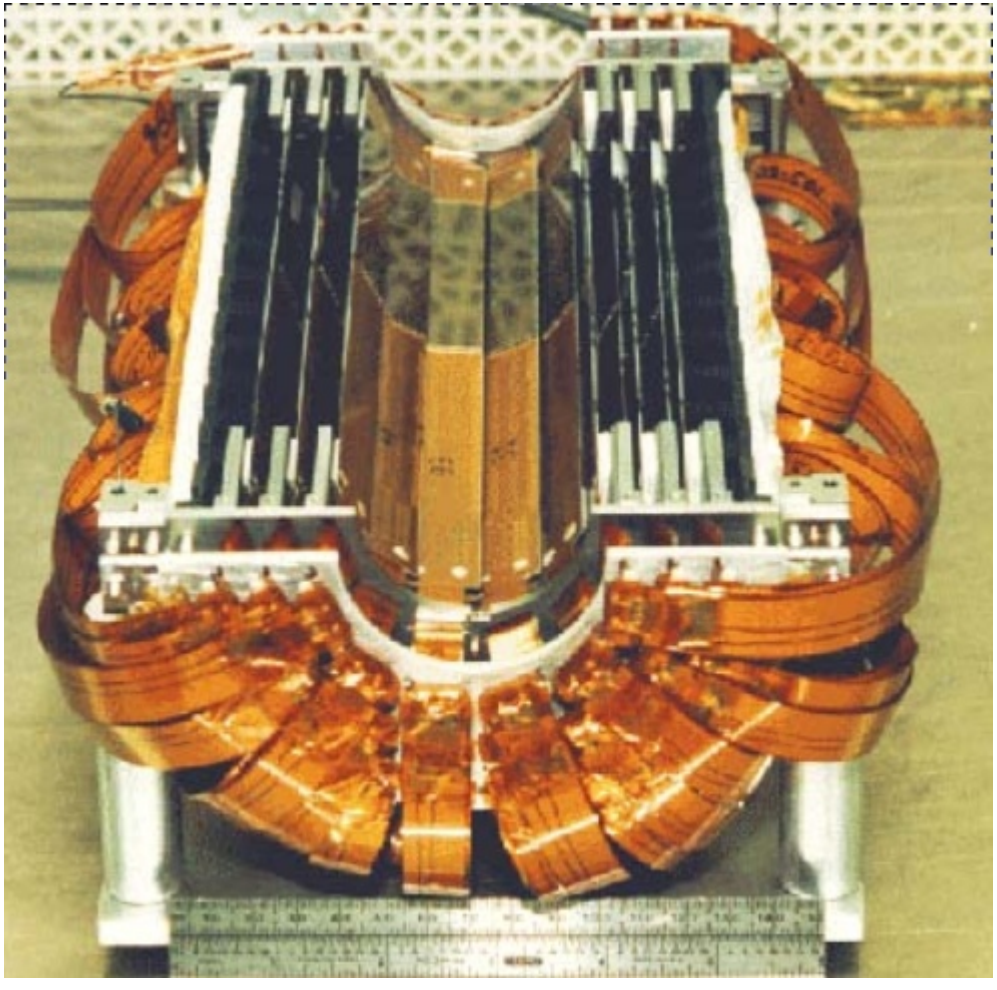
Recap

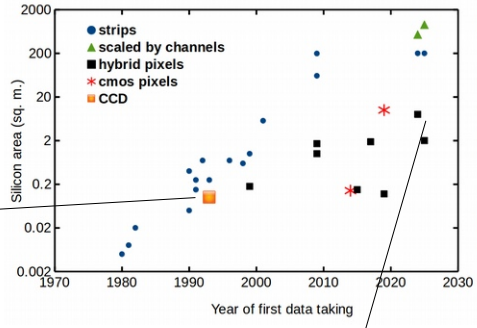
- Imaging particles is an inverse problem to typical imaging
- Need to surround the source of particles with senors – large area of silicon needed
- Plus frame rate is in the MHz
- => Custom ICs needed
- CMOS sensors for particle detection scale better to large areas, but hae limited rate and radiation hardness and need highly customized fabrication process.
- Hybrid detectors can use standard CMOS for readout (custom design but not custom process) and radiation optimized sensors.
- Design of radiation hard ASICs is a cottage industry in HEP

A future direction



The Rate Extremes



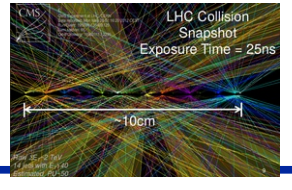


SLD VXD

- Silicon area: 0.12 m²
- 300M pixels (20μm x 20μm)
- But only 350,000 Z decays recorded
- => most pixels were never hit by real collision particle!

HL-LHC

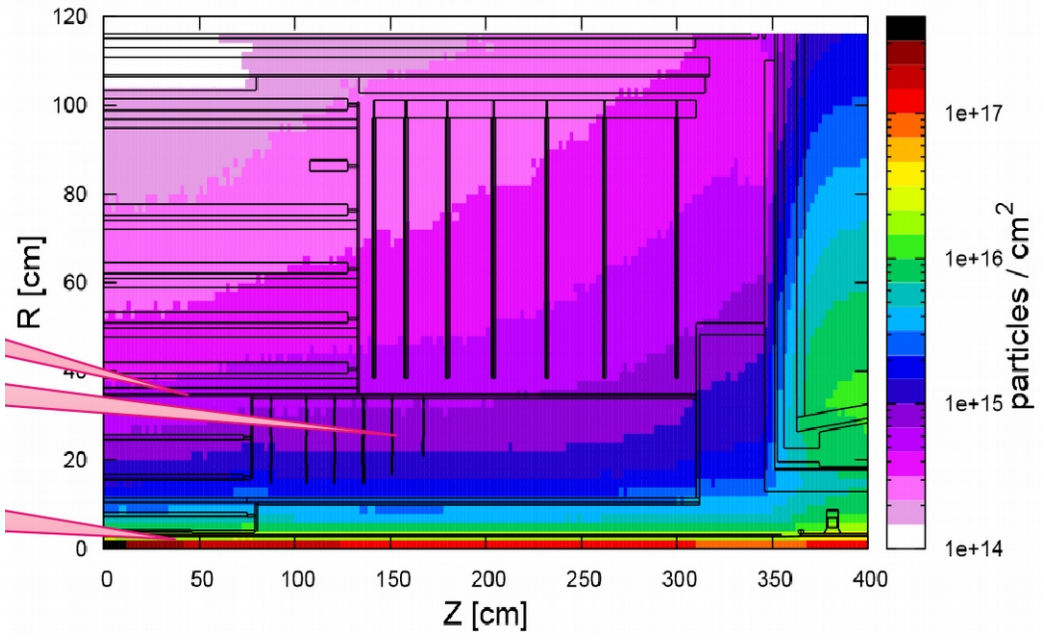
- Inner layers of ATLAS and CMS high luminosity upgrades will see 10 collision particles in every Si atom!



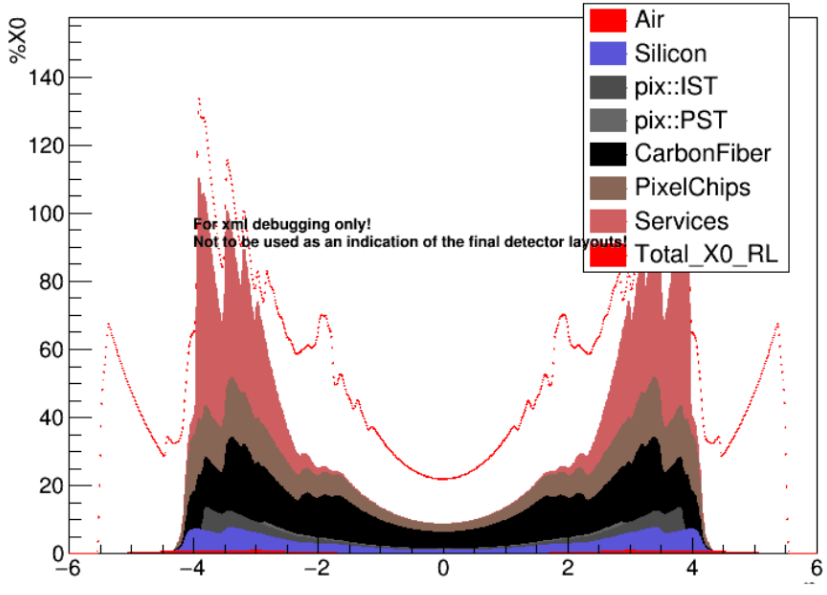
X 10^{16}

B A C K U P

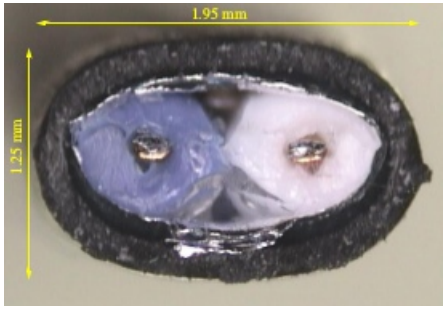
Limited Readout Bandwidth

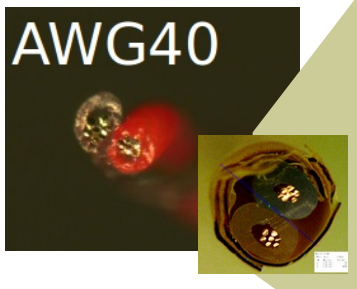


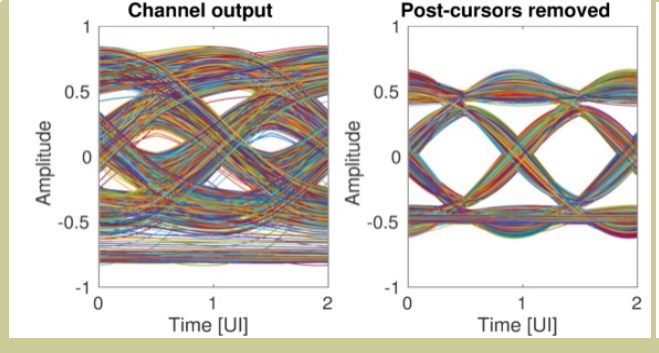
Can’t use optical transmitters

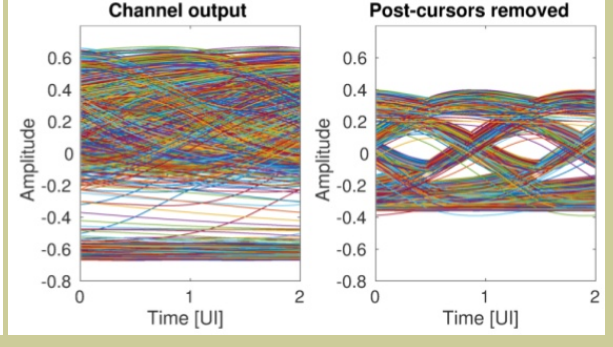


Can’t use heavy shielded cables



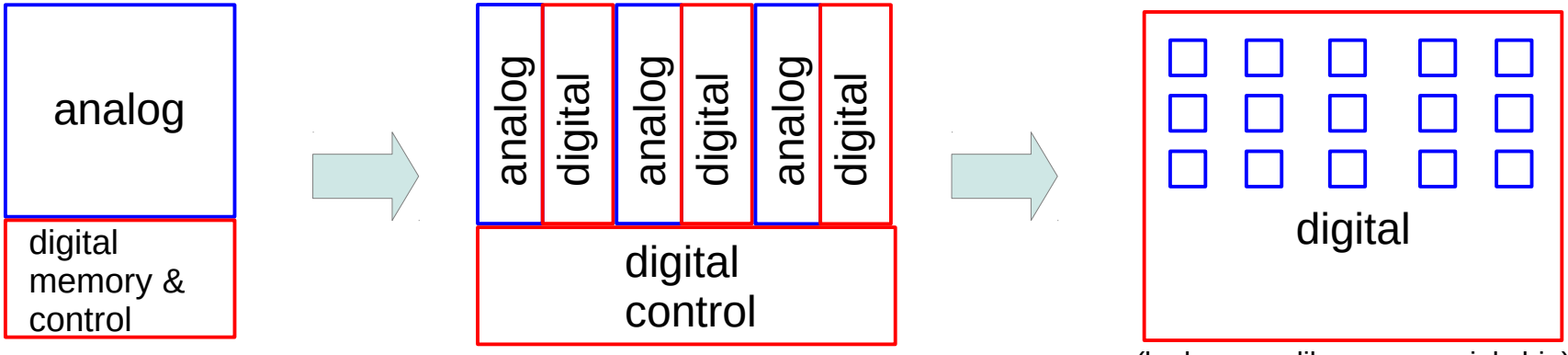






3m **5Gbps Simulation** **5m**

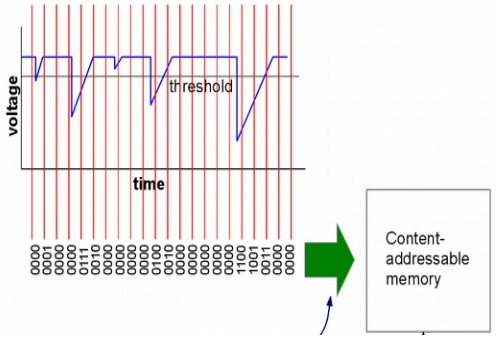
Readout Chip Evolution

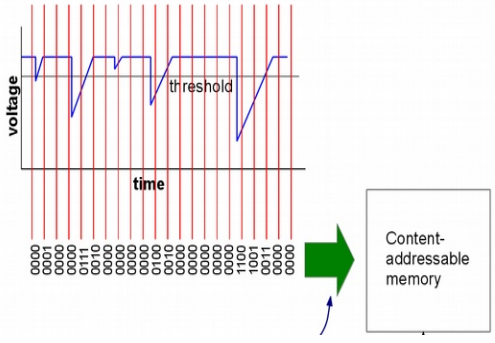


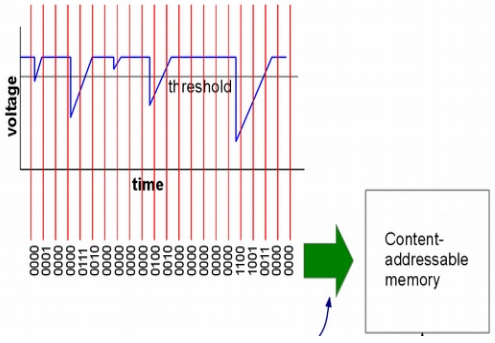
10 yrs ago

today

Future





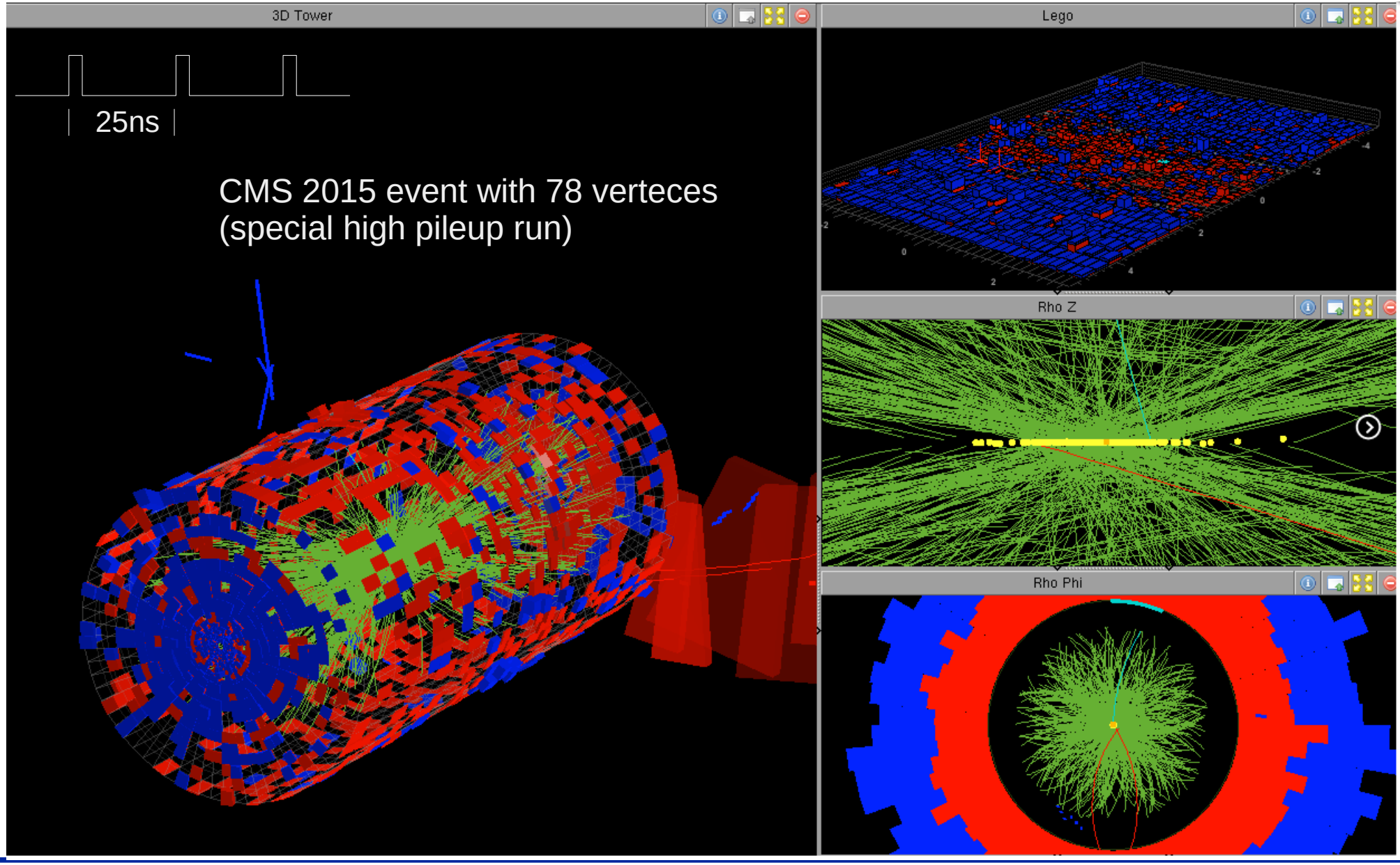


<1Gb/s /cm^2

5Gb/s /cm^2

40Gb/s /cm^2

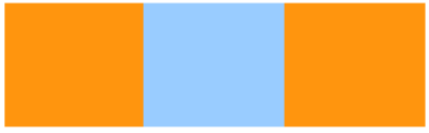
What Images Look Like



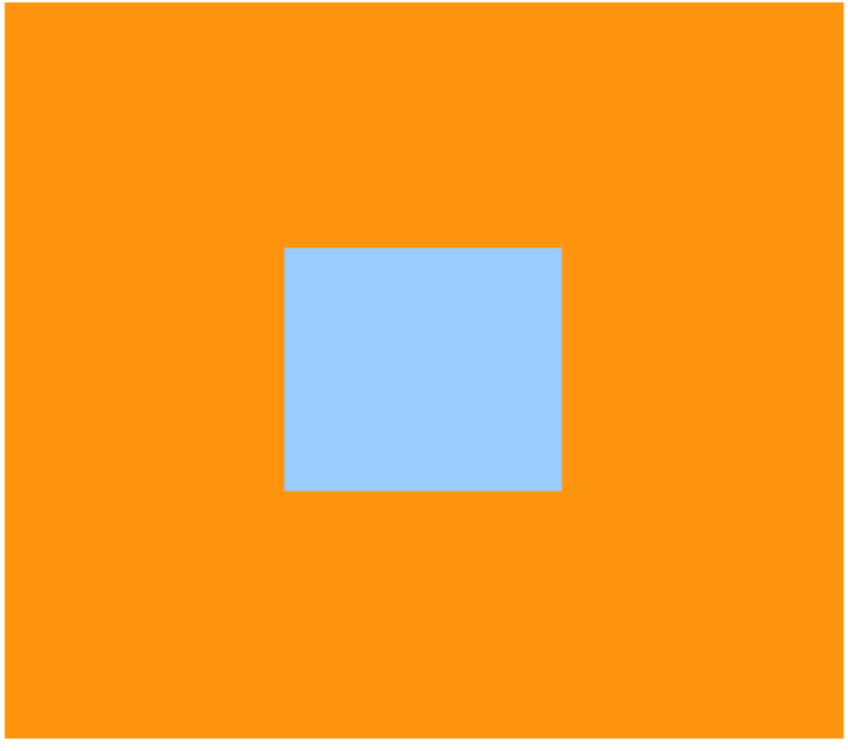
Rad Hard Logic Density Scaling

65nm

130nm

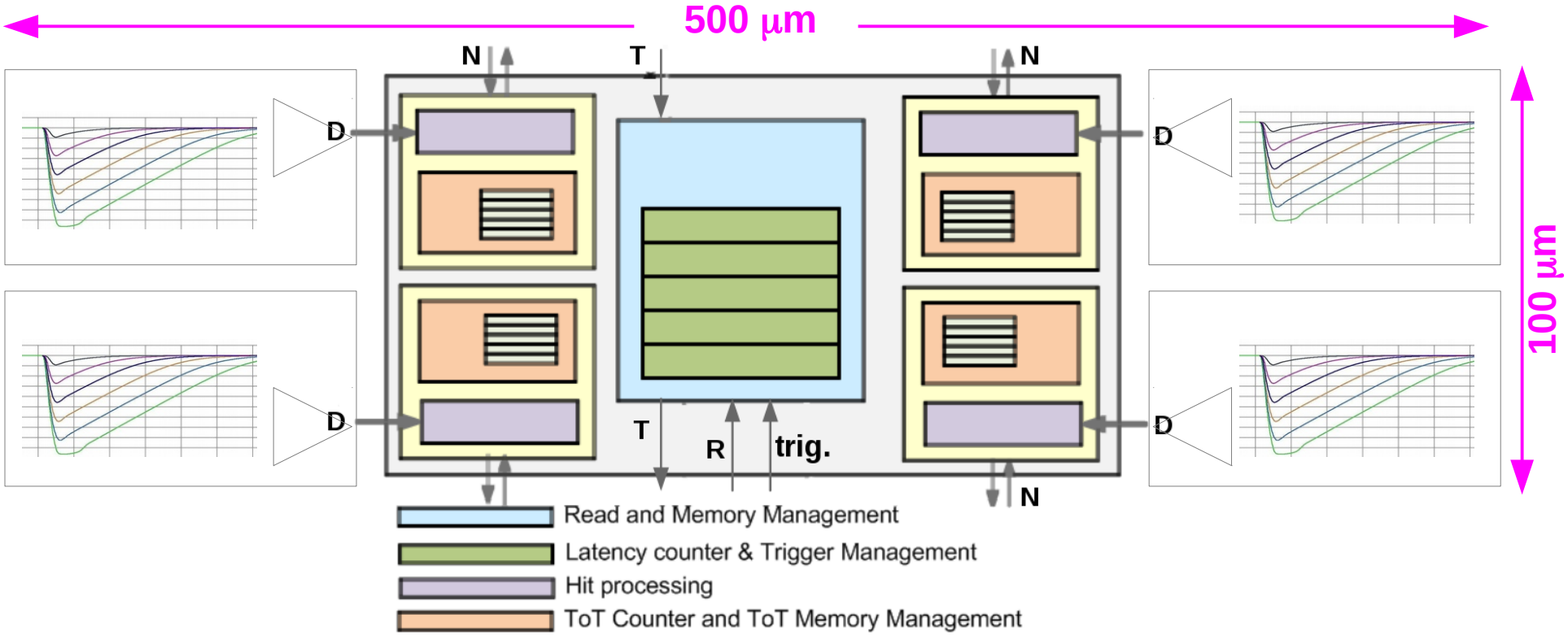


0.25um
ELT



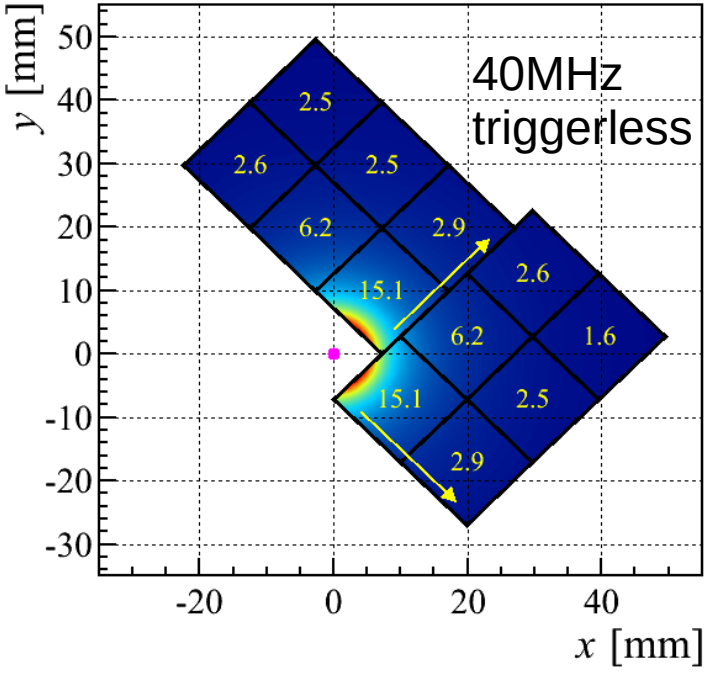
FE-I4 Digital Region

- **Digital block is shared with 4 inputs- each form an identical analog pixel.**

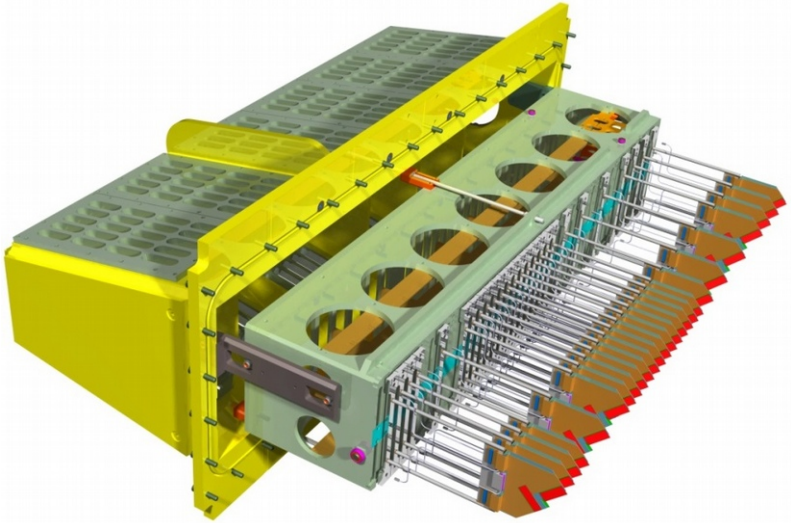


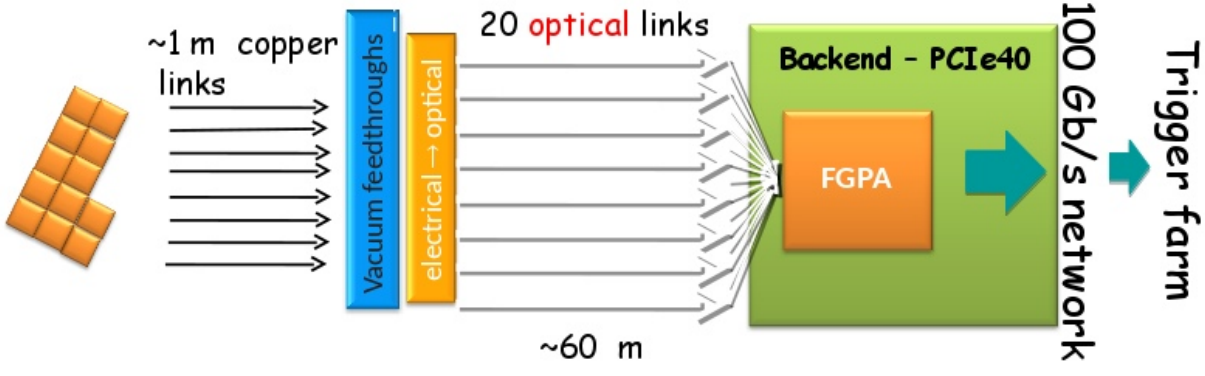
Velopix triggerless readout

Readout chips in LHCb Velopix plane
Output data rate per chip in Gbps



Velopix half with 26 planes





- Geometry looks like data flow diagram
- Lots of room outside physics acceptance
- Can have many cables out of each chip