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HEXITEC *MHz*

A Spectroscopic Imaging Camera with a 1 MHz Frame Rate Continuous Readout

Ben Cline

Detector Development Group, UKRI STFC

Email: ben.cline@stfc.ac.uk

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Detector
Development

Ivan Church
Ben Cline
Matt Hart
Sion Richards
Paul Seller
Dave Sole
Matt Wilson
Rhian Wheeler
Matt Veale

Interconnect

Paul Adkin
Paul Booker
Simon Cross
Navid Ghorbanian
John Lipp
Andreas Schneider

Detector Systems
Software

Christian Angelsen
Victor Bozhinov
Adam Davies
Josh Harris
Ashley Neaves
Tim Nicholls
Joseph Nobes



Funded by the: Centre for Instrumentation (CFI) run by Marcus French

PCB Design Office

Darren Ballard
Dan Becket
Chris Day

ASIC Design

Stephen Bell
Thomas Gardiner
Lawrence Jones
Mark Prydderch

Detector Systems

William Helsby

Electronic Systems
Design

Adam Barcock
Rob Halsall
John Holden
Chris Lyford
Matt Roberts
Maged Sallam

Agenda

1 HEXITEC vs HEXITEC_{MHz}

The next generation of HEXITEC systems

2 HEXITEC_{MHz} Overview

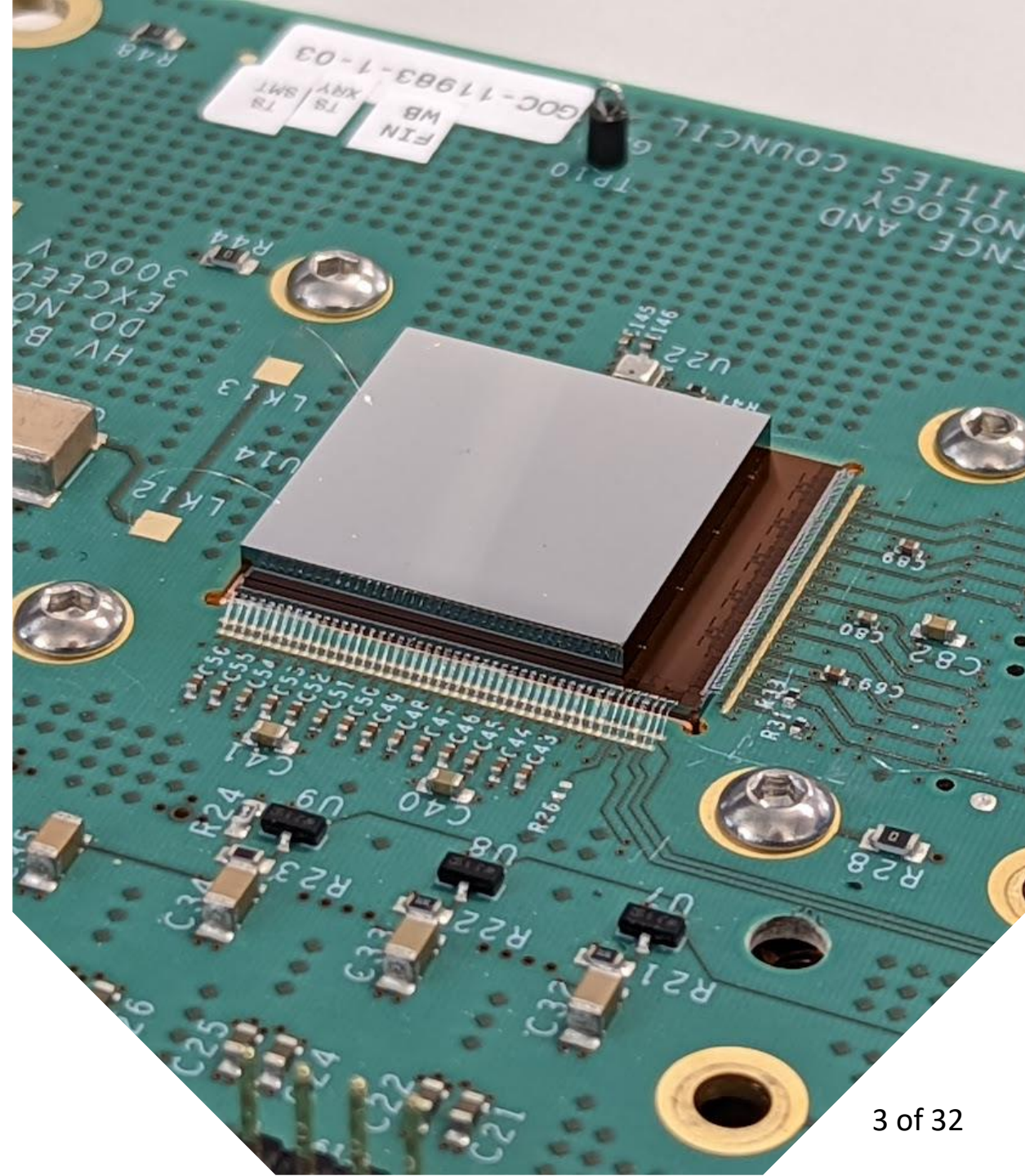
An introduction to our new HEXITEC_{MHz} ASIC including its architecture and specification

3 Test Results

Characterisation of spectroscopic performance using a lab-based X-Ray source and Diamond Light Source synchrotron X-Rays

4 Next Steps

A look to the next 12 months



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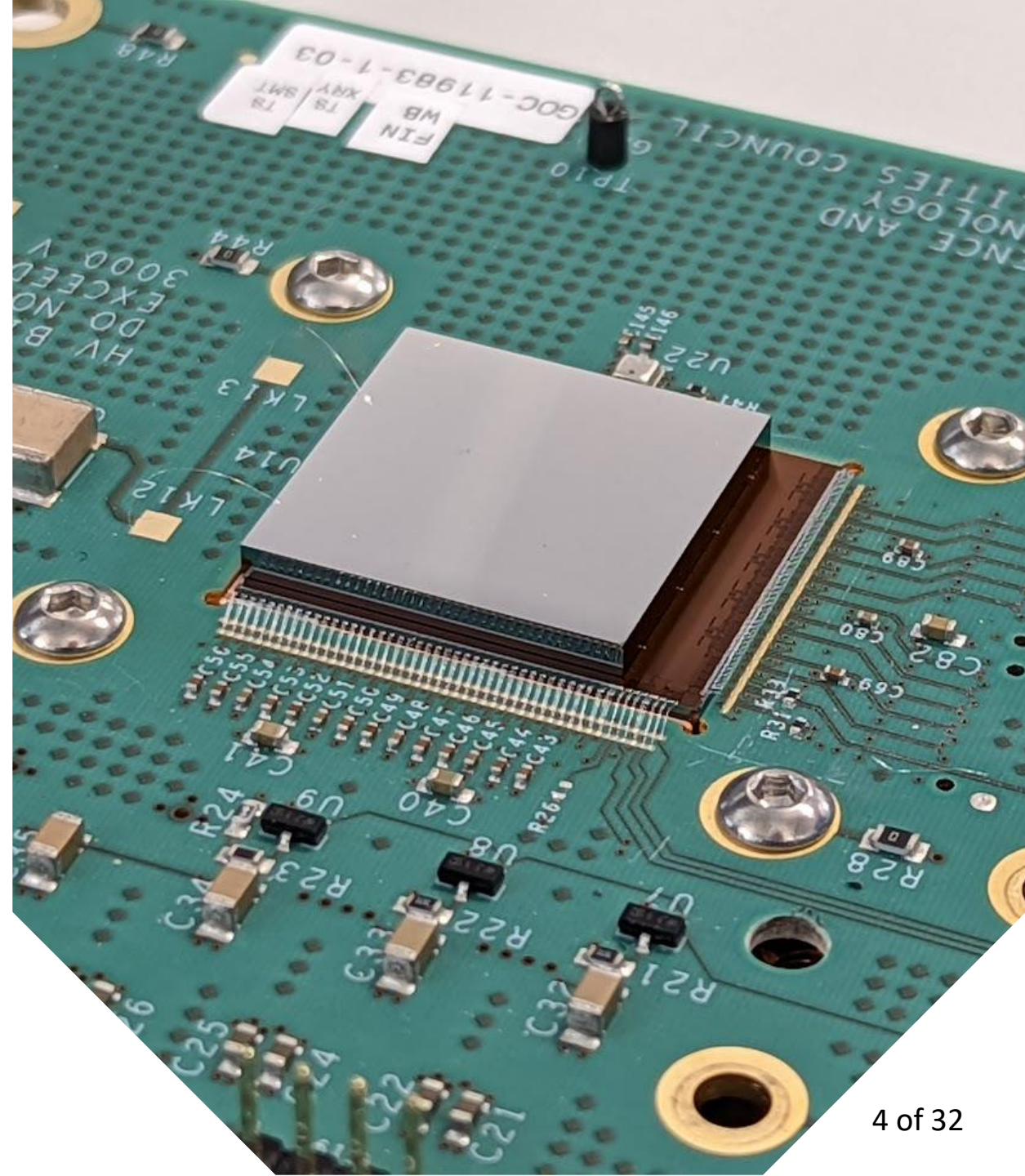
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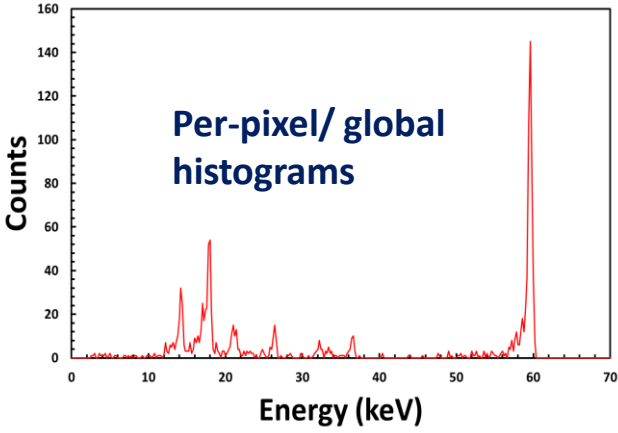
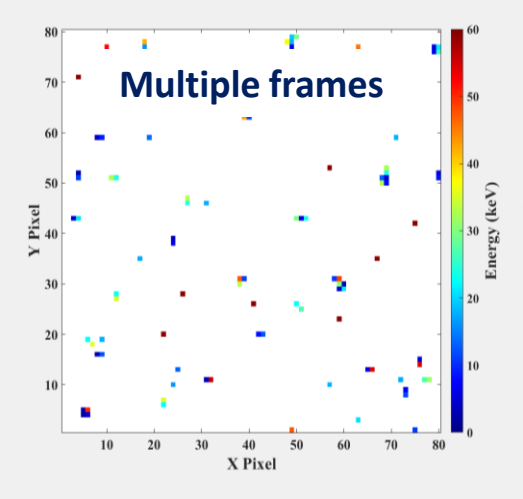
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A look to the next 12 months



- **Fully spectroscopic X-Ray Imaging** with CdTe/ CdZnTe (CZT) detectors
- 80×80 pixel array on a 250 μm pitch
- **Analogue readout** via a rolling shutter to **4 ADCs in the DAQ**
- Maximum ~10 kHz data output (~100 MB s⁻¹)
- AMS 0.35 μm - since 2010



HEXITEC specifications

Parameter	HEXITEC
Pixel Pitch (μm)	250
Array Size	80×80
Max Frame Rate (kHz)	~10
Max Spectroscopic Flux (ph s ⁻¹ mm ⁻²)	~10 ⁴
Digitisation	Off-chip
Detector Type	Peak Track + Hold
Gain stages (keV in CZT)	200
	600
FWHM _{@100keV} (keV in CZT)	< 1 <ul style="list-style-type: none"> • HF-CZT: 0.79 keV @ 59.54 keV [1] • 300-μm thick p-type Si: 0.59 keV @ 59.54 keV [2]

[1] DOI: [10.3390/s20102747](https://doi.org/10.3390/s20102747) [2] DOI: [10.1088/1748-0221/17/05/P05030](https://doi.org/10.1088/1748-0221/17/05/P05030)

- HEXITEC has been used across many applications including:

Compton X-Ray Imaging [3]

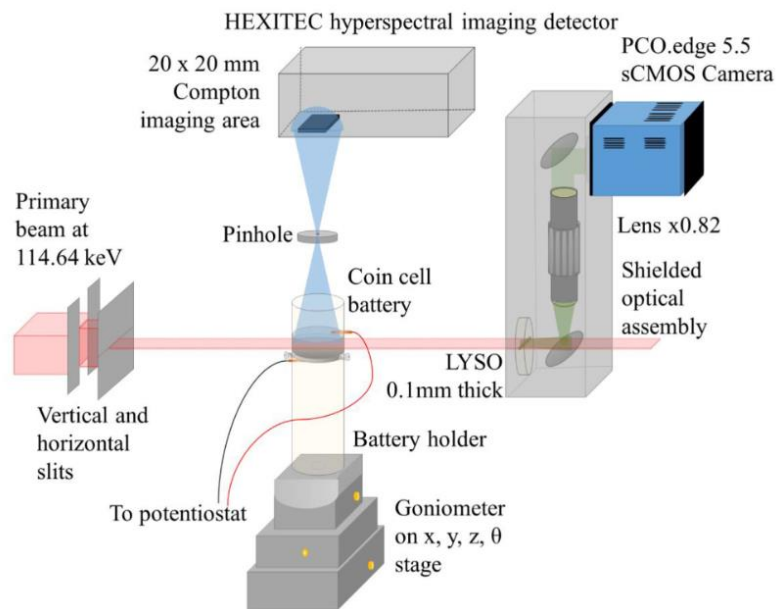


Figure 1. Schematic of the correlative X-Ray Compton scattering imaging (XCS-I) and X-Ray computed tomography (XCT) technique experimental set-up

X-Ray Fluorescence Imaging [4]

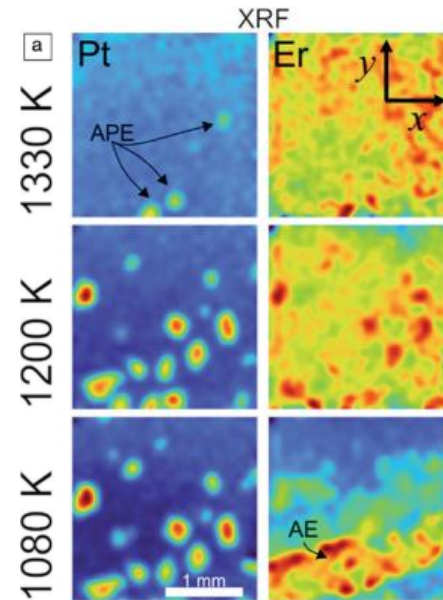


Figure 7. (a) Pt and Er XRF intensity maps as a function of temperature during the solidification of an Al-23Pt-20Er alloy at 0.1 K s^{-1} .

Hyperspectral X-Ray Tomography [5]

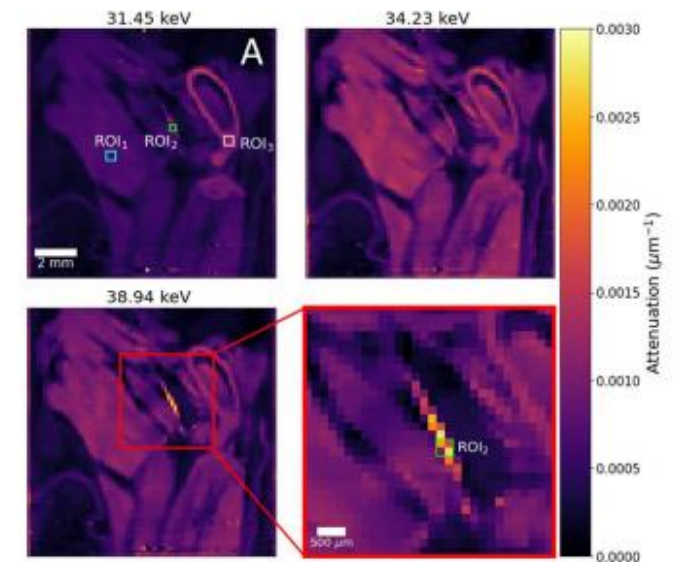


Figure 2. Voxel spectra analysis for double-stained hindlimb specimen. (A) Single image slice in the sagittal plane across three monochromatic energy channels, following iterative reconstruction. A set of three regions-of-interest (ROIs) are highlighted for voxel spectra analysis.

BUT ...

- **HEXITEC is frame-rate and therefore flux limited**
 - Charge-sharing corrections require <10% frame occupancy
 - This limits spectroscopic imaging @10 kHz to a **max X-Ray flux of $\sim 10^4 \text{ ph s}^{-1} \text{ mm}^{-2}$**

→ **There is a need for a continuous spectroscopic X-Ray detector that operates at faster frame rates**

- **Faster (MHz) imaging requires:**
 - In-pixel digitisation
 - High-speed serialisers
 - Dedicated FPGA processing
- **These requirements apply to a large number of STFC's upcoming detector development projects**
 - E.g. DynamiX, C100

A new fully spectroscopic X-Ray imaging detector:

- 80×80 pixels on a 250 μm pitch
- New front-end design – now an **integrating** detector
- **On-chip 12-bit digitisation** (no external ADCs)
 - Data outputted via **20 × 4.1 Gbps serialisers**
- **1 MHz continuous frame rate**
 - Spectroscopic X-Ray fluxes of **>10⁶ ph s⁻¹ mm⁻²**

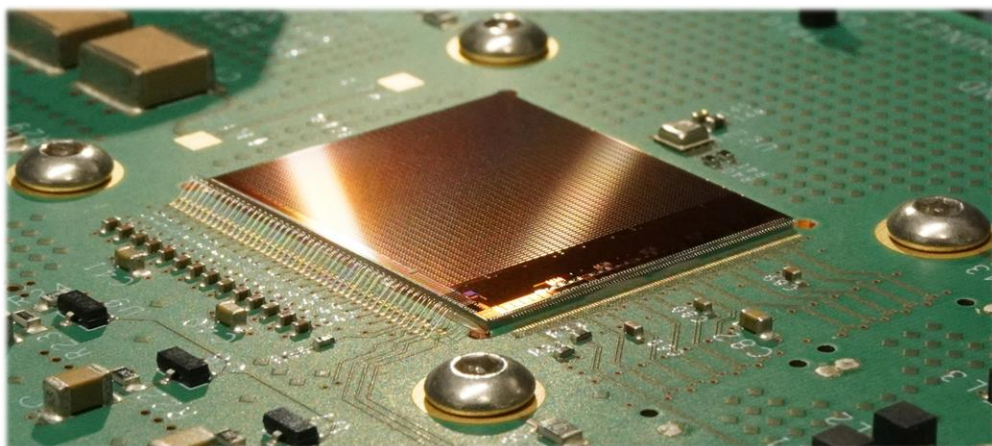
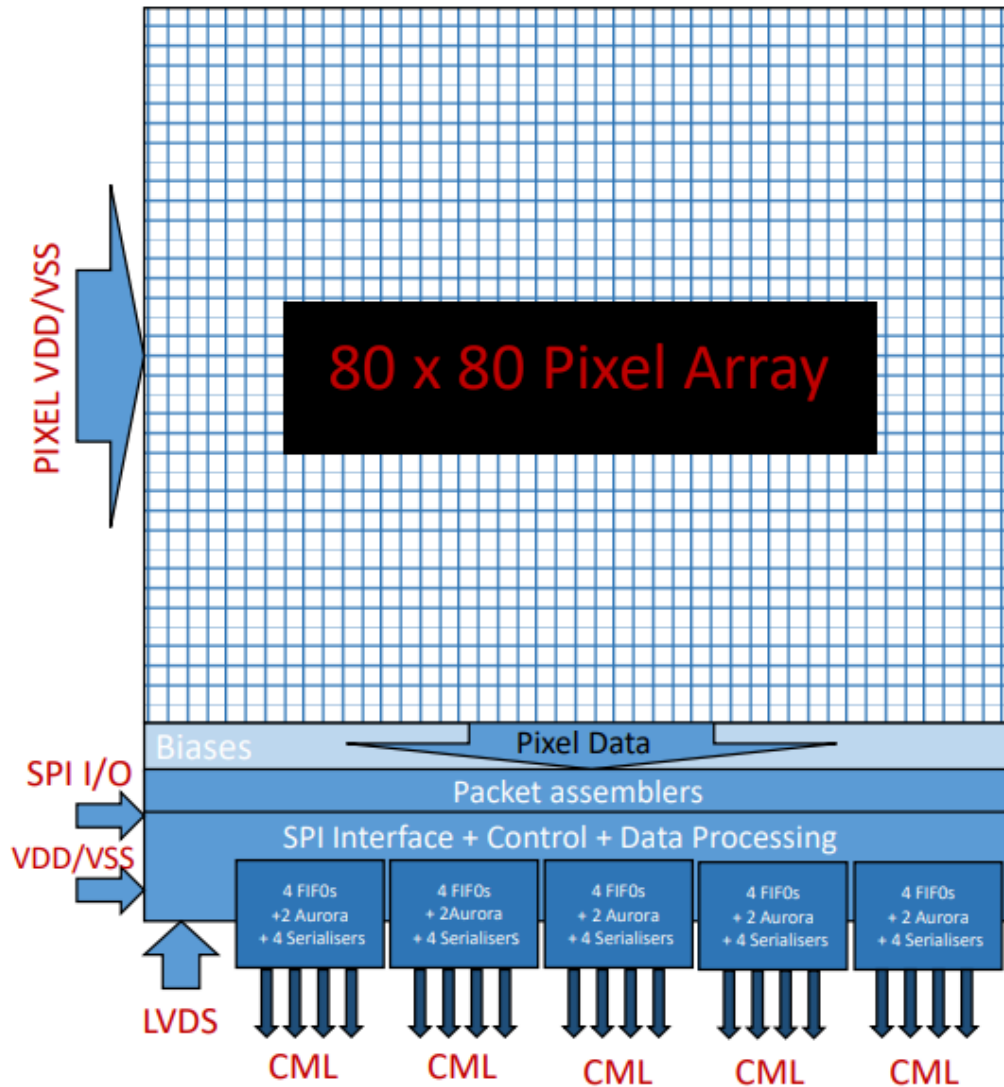


Photo of ASIC

Comparison of HEXITEC and HEXITEC_{MHz} specifications

Parameter	HEXITEC	HEXITEC _{MHz}
Pixel Pitch (μm)	250	250
Array Size	80×80	80×80
Max Frame Rate (kHz)	~10	1000
Max Spectroscopic Flux (ph s ⁻¹ mm ⁻²)	~10 ⁴	>10⁶
Digitisation	Off-chip	On-chip
Detector Type	Track + Hold	Integrating
Gain stages (keV in CZT)	200	100
	600	200
		300
FWHM@100keV (keV in CZT)	< 1	< 1
Power Consumption (W)	1.5	15



ASIC block diagram

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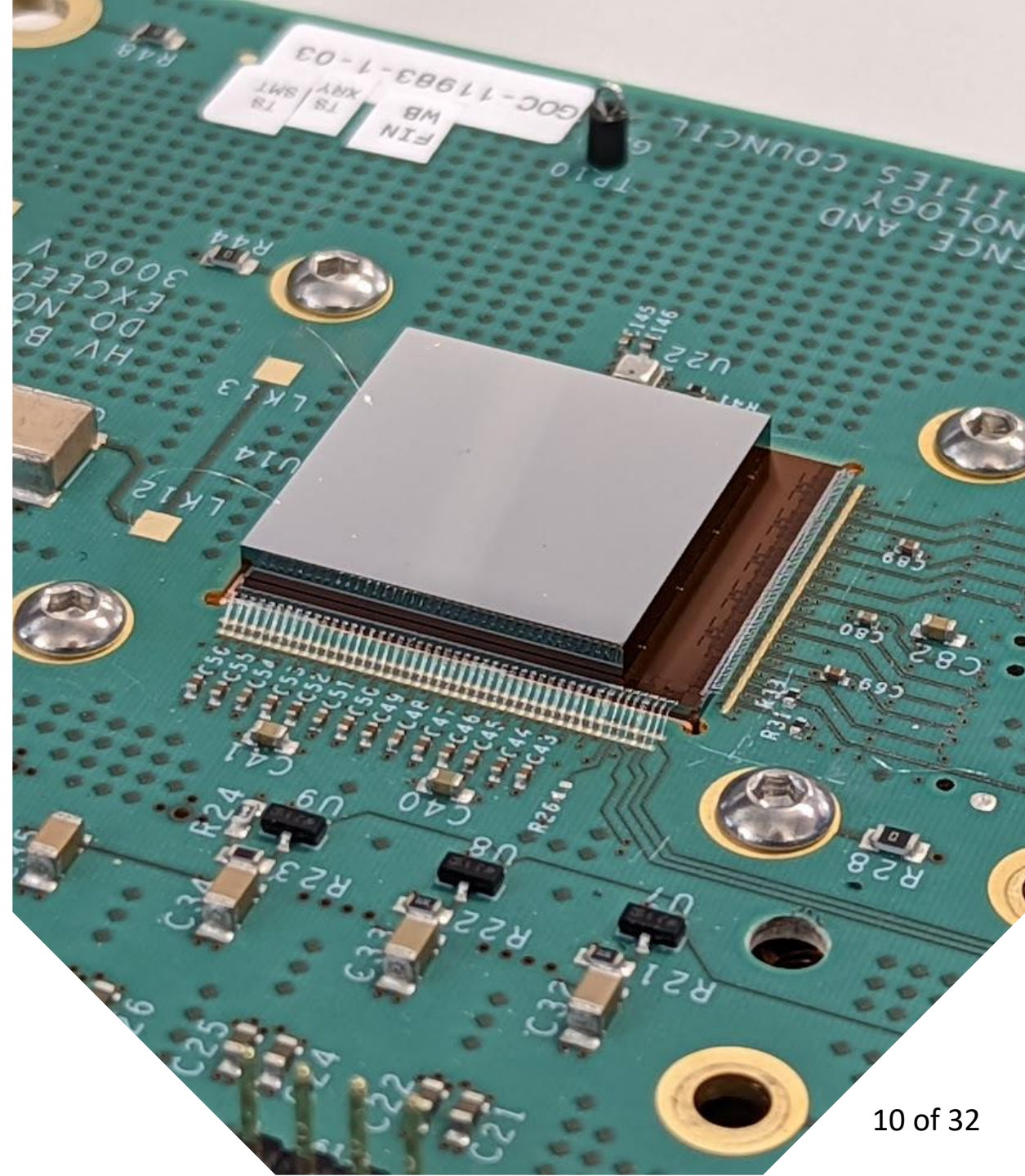
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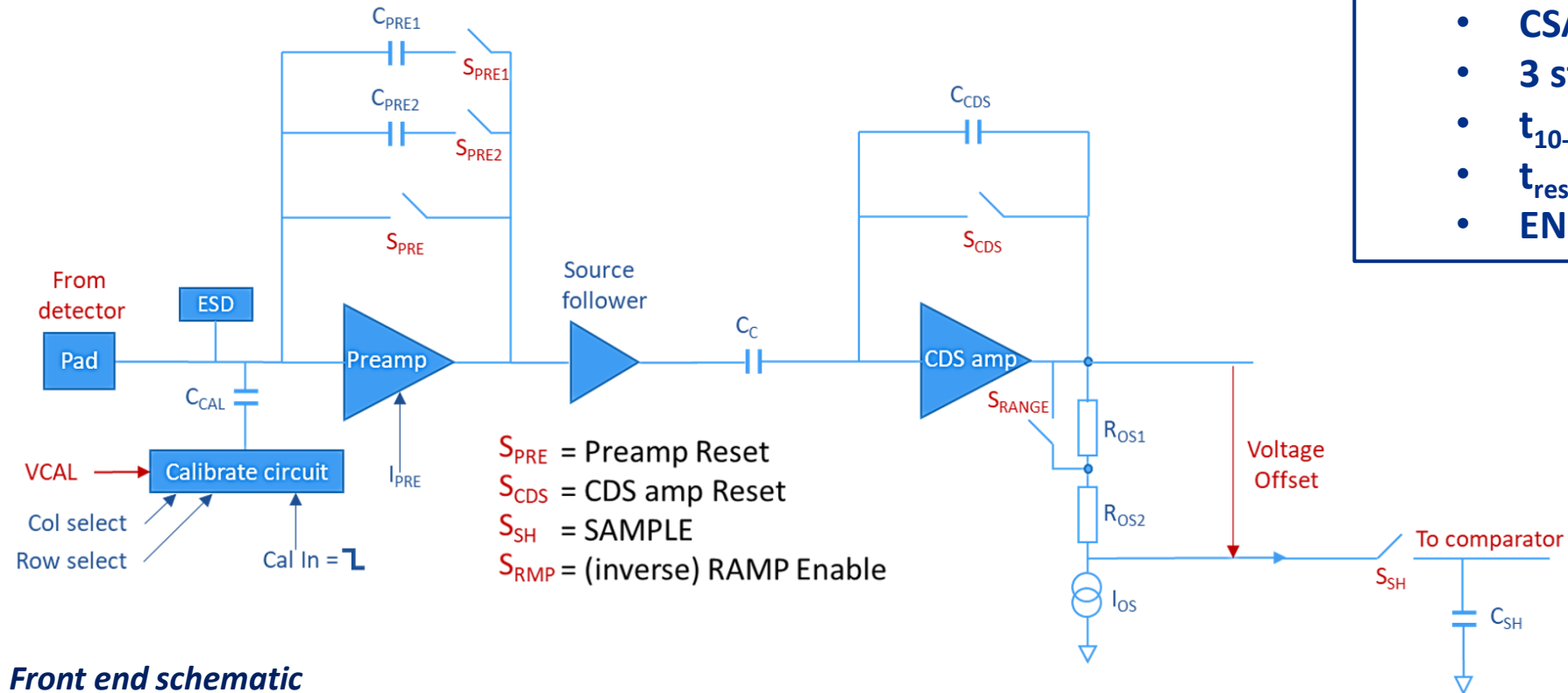
Characterisation of spectroscopic performance using a lab-based X-Ray source and Diamond Light Source synchrotron X-Rays

4 Next Steps

A look to the next 12 months



HEXITEC_{MHz} - Integrating Front End

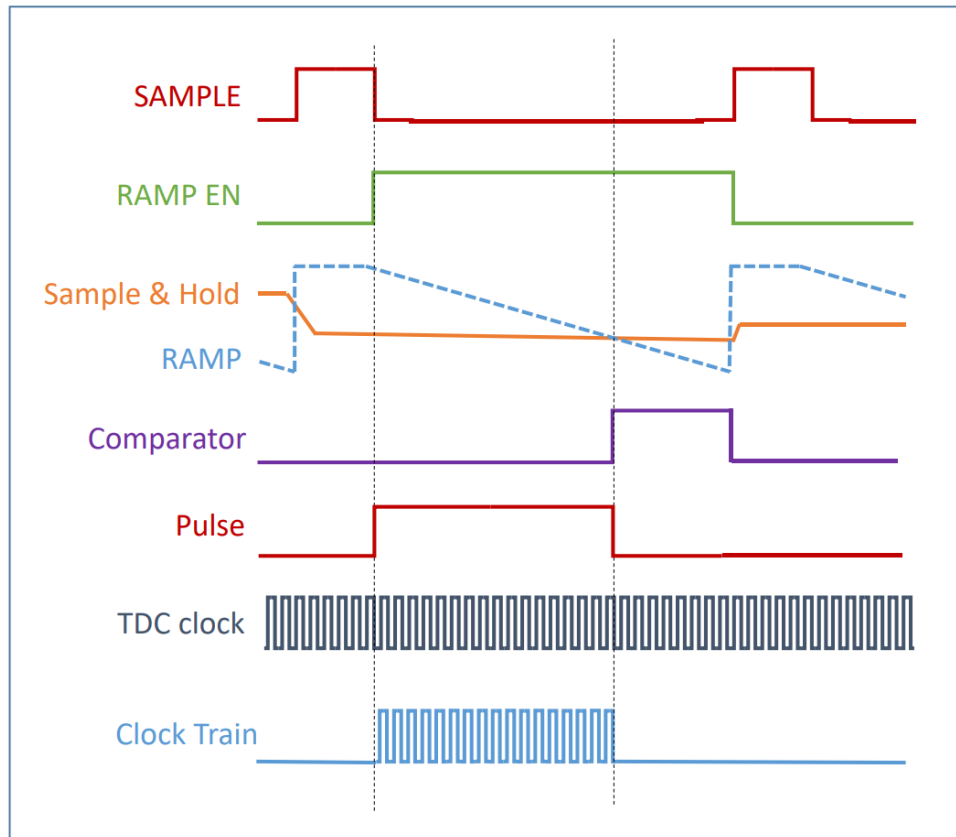


Properties:

- CSA + CDS amplifier
- 3 static dynamic ranges
- t_{10-90} = 50 ns
- t_{reset} \approx 90 ns
- ENC < 60e⁻

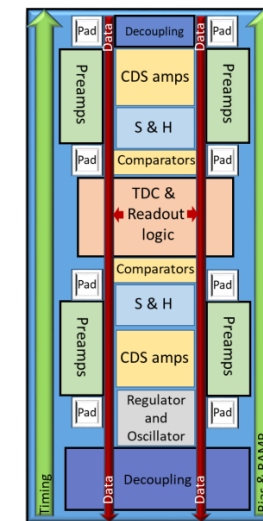
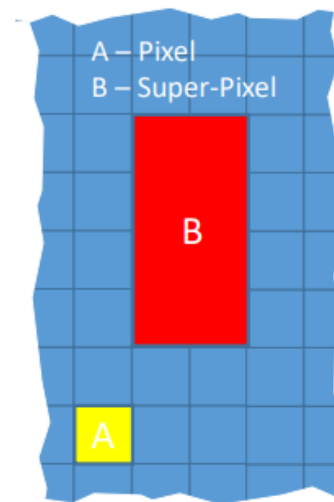
Front end schematic

HEXITEC_{MHz} - In-Pixel TDC



TDC signal timing

- **12-bit** digitisation
 - The Sample & Hold signal is compared with a ramp with a programmable slew
- The ASIC comprises **800 super-pixels of 2×4 pixels**
 - These contain **one TDC block and shared readout logic**



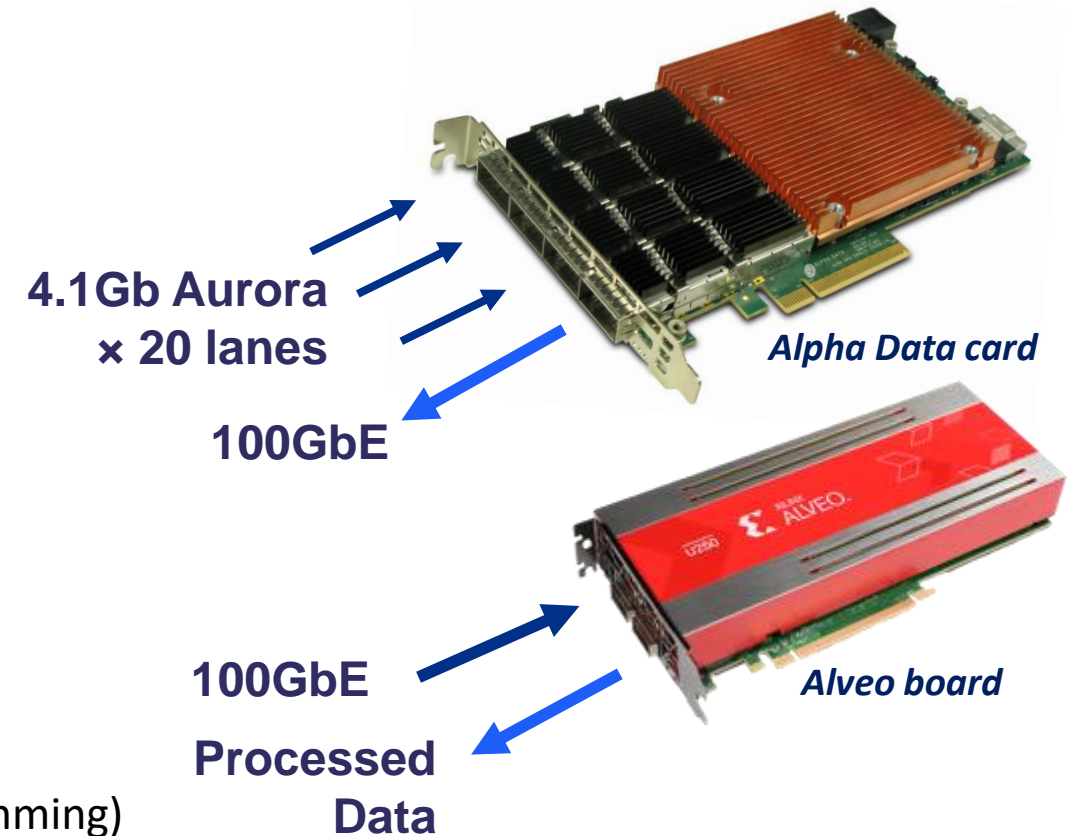
Super-pixel schematics

HEXITEC_{MHZ} - Data Output

- 80×80 array is divided into **divisions of 4 columns**
 - Each division has **packet-assembler** and dedicated **serialiser**
 - Packets constructed using **Xilinx's Aurora 64B/66B protocol**
 - Serialisers operate at **4.1 Gb s⁻¹ (total data rate ≈ 10 GBs⁻¹)**

What to do with all this data?

- Two receiving data planes:
 - **First-stage FPGA – Alpha Data card**
 - Recovers and reorders the received optical data
 - **Second-stage FPGA – Xilinx Alveo U50 board**
 - Data corrections (darks, energy calibration)
 - Data reduction (charge-sharing discrimination, histogramming)
- Then received by **ODIN Data, a scalable data-processing and acquisition network**



HEXITEC_{MHz} - Data Output

- 80×80 array is divided into 16 divisions of 5×5 pixels
- Each division has its own serialiser
- Packets contain 5×5 pixel data
- Serialisers output data to Alpha Data card

What to do with data

- Two receiving data cards
 - **First-stage** data card
 - Recover data from Alpha Data card
 - **Second-stage** data card
 - Data compression
 - Data reduction

- Then received by **ODIN Data**, a scalable data-processing and acquisition network

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Journal of Instrumentation

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Spectroscopic X-ray imaging at MHz frame rates — the HEXITEC_{MHz} ASIC

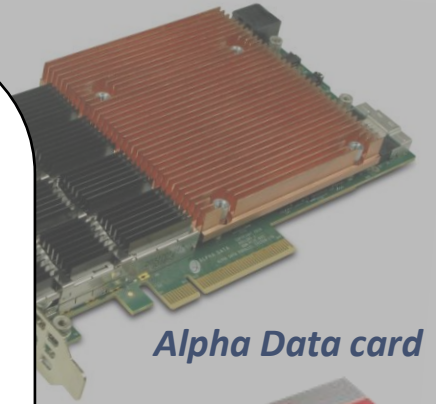
L. Jones^{2,1}, S. Bell¹, B. Cline¹, T. Gardiner¹, M. Hart¹, M. Prydderch¹, P. Seller¹, M. Veale¹ and M. Wilson¹

Published 11 October 2022 • © 2022 The Author(s). Published by IOP Publishing Ltd on behalf of Sissa Medialab.

[Journal of Instrumentation](#), Volume 17, October 2022

Citation L. Jones *et al* 2022 *JINST* 17 C10012

DOI: 10.1088/1748-0221/17/10/C10012



Alpha Data card



Alveo board

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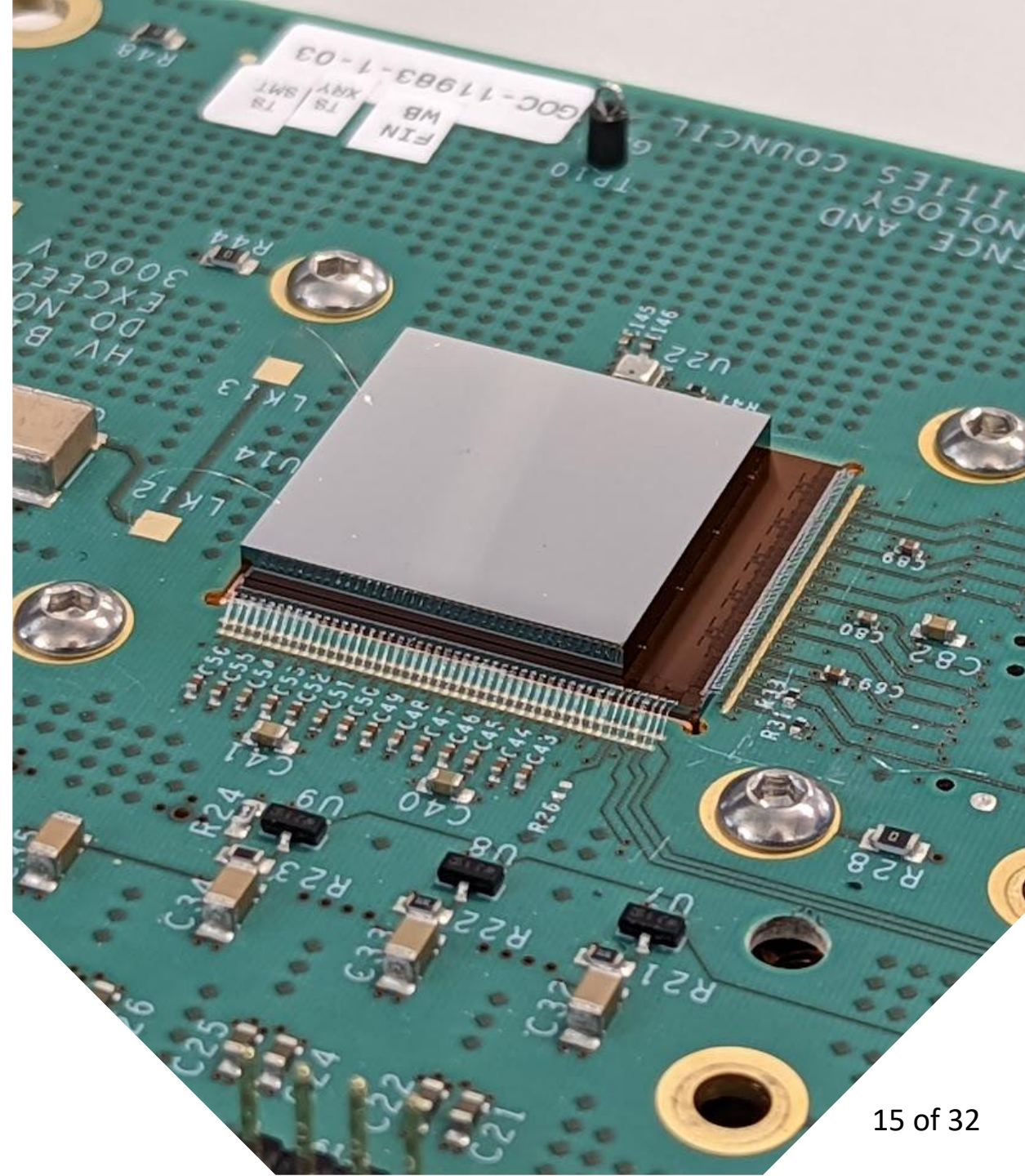
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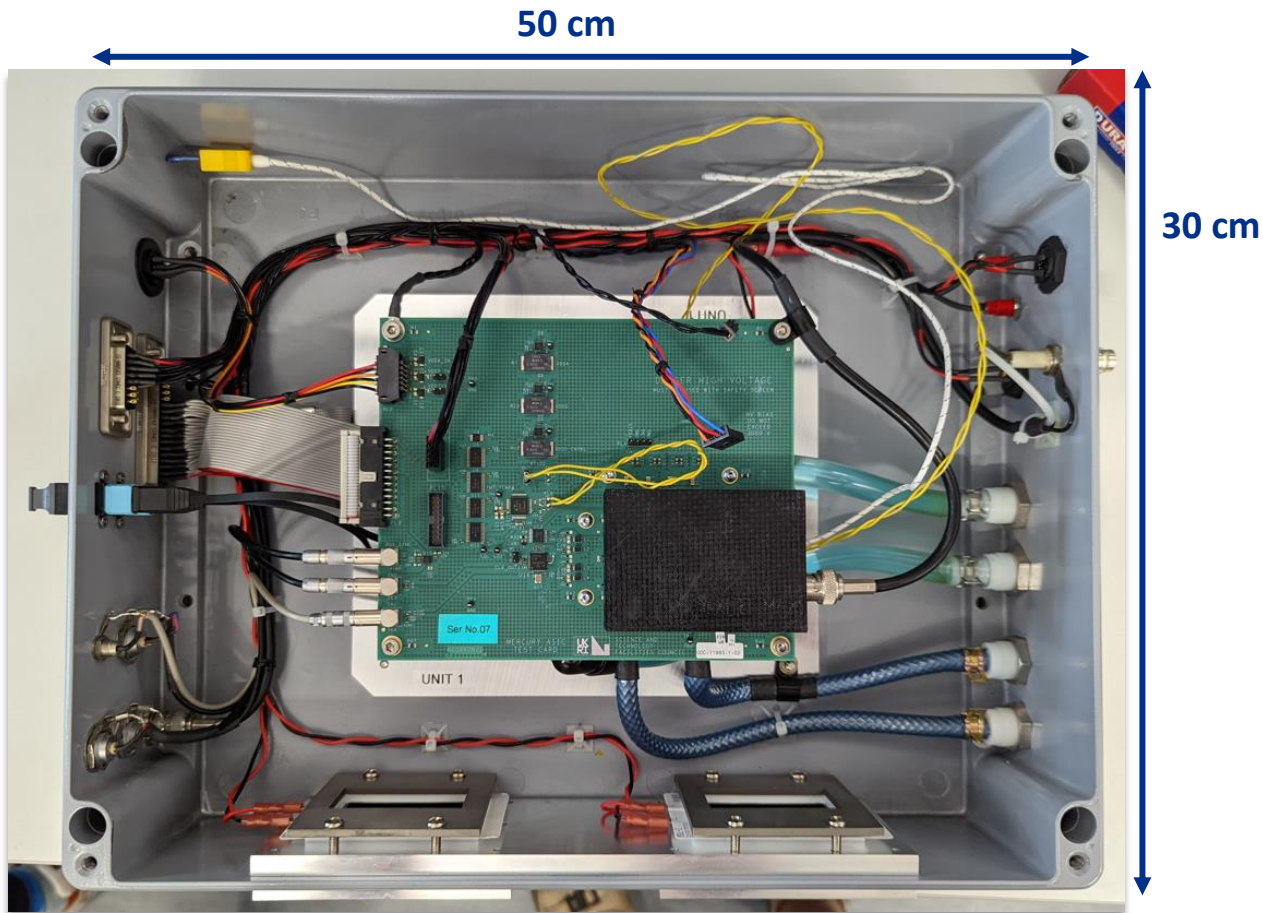
Characterisation of spectroscopic performance using a lab-based X-Ray source and Diamond Light Source synchrotron X-Rays

4 Next Steps

A look to the next 12 months



Current Status

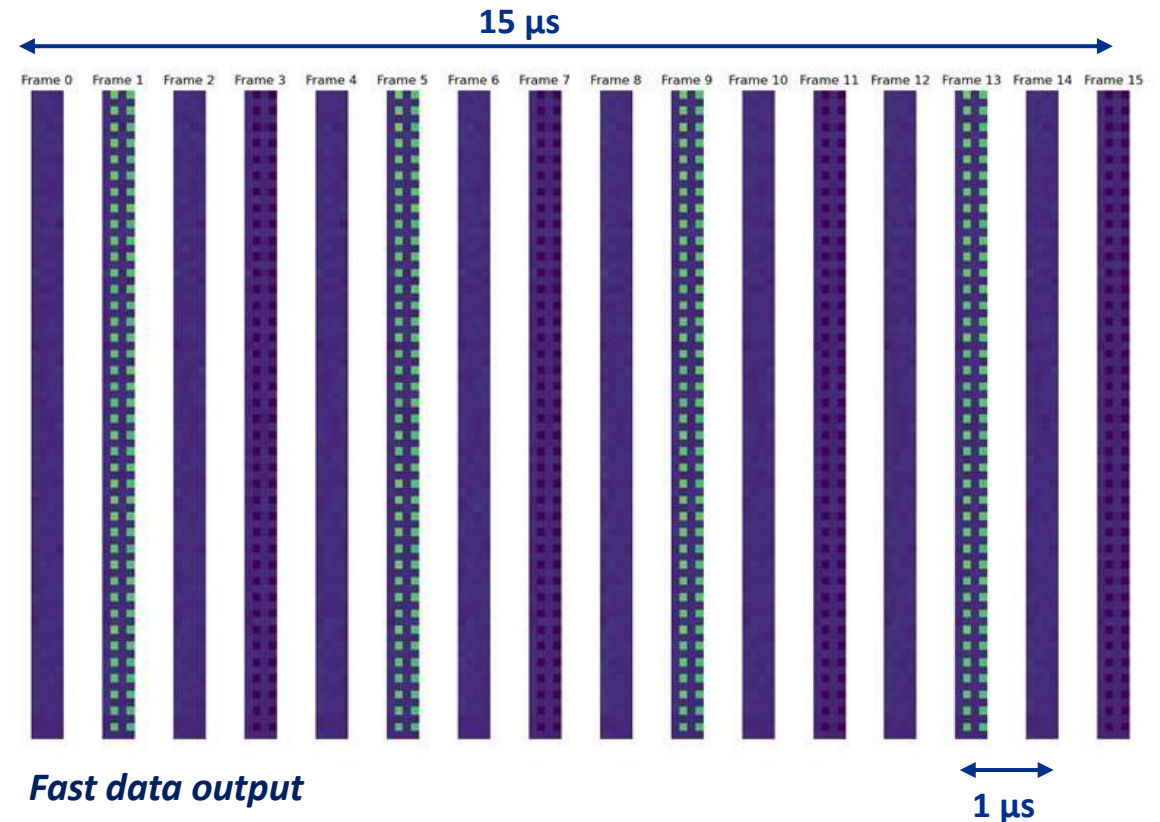


HEXITEC_{MHz} test enclosure

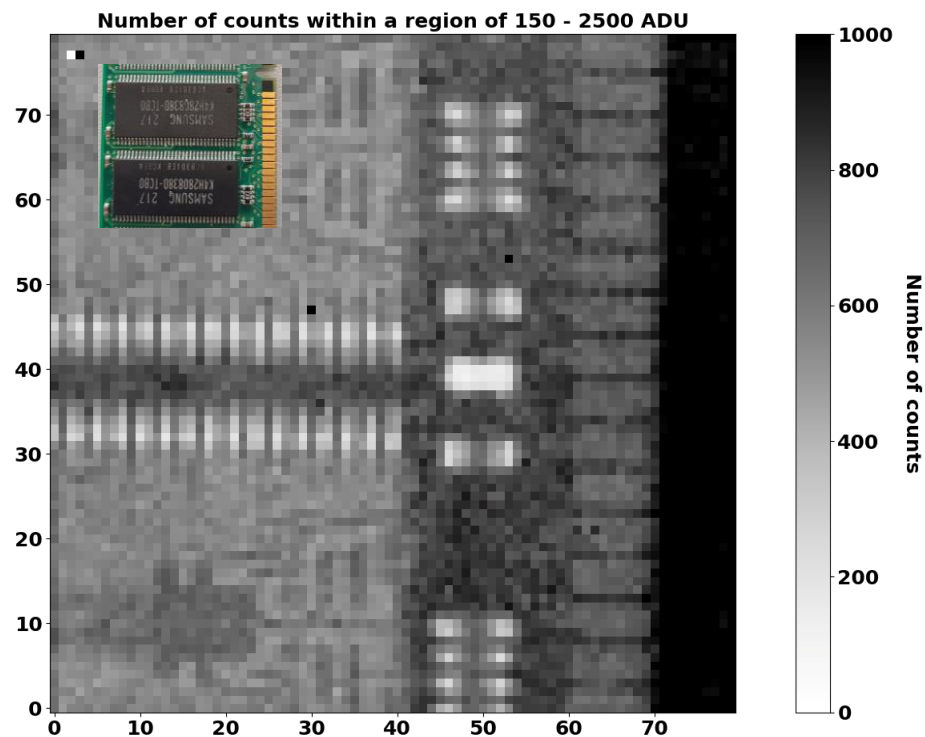


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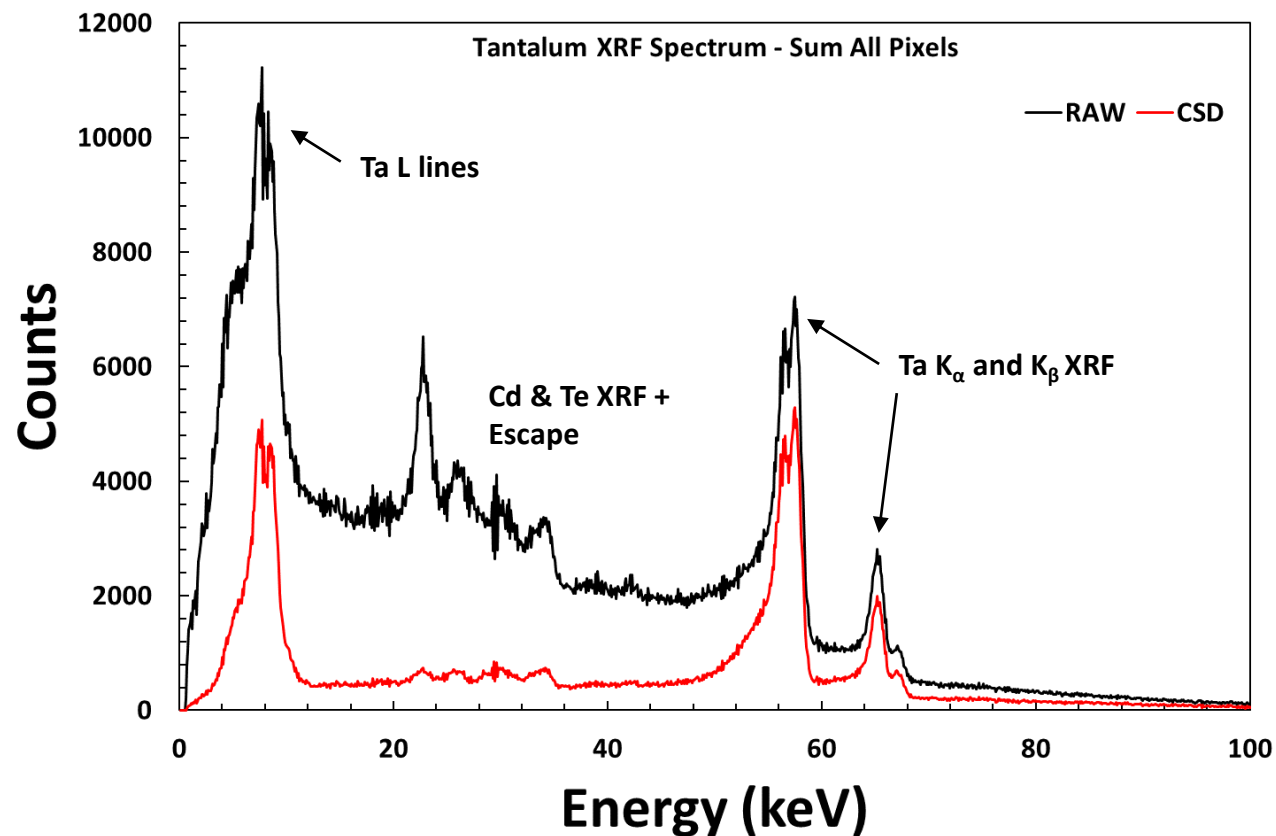
- ASIC is fully functioning
- Using **test enclosure**
- FPGA firmware in development – at present, **1 channel (4×80 pixels) over fast data**



Testing – Initial X-Ray Tests



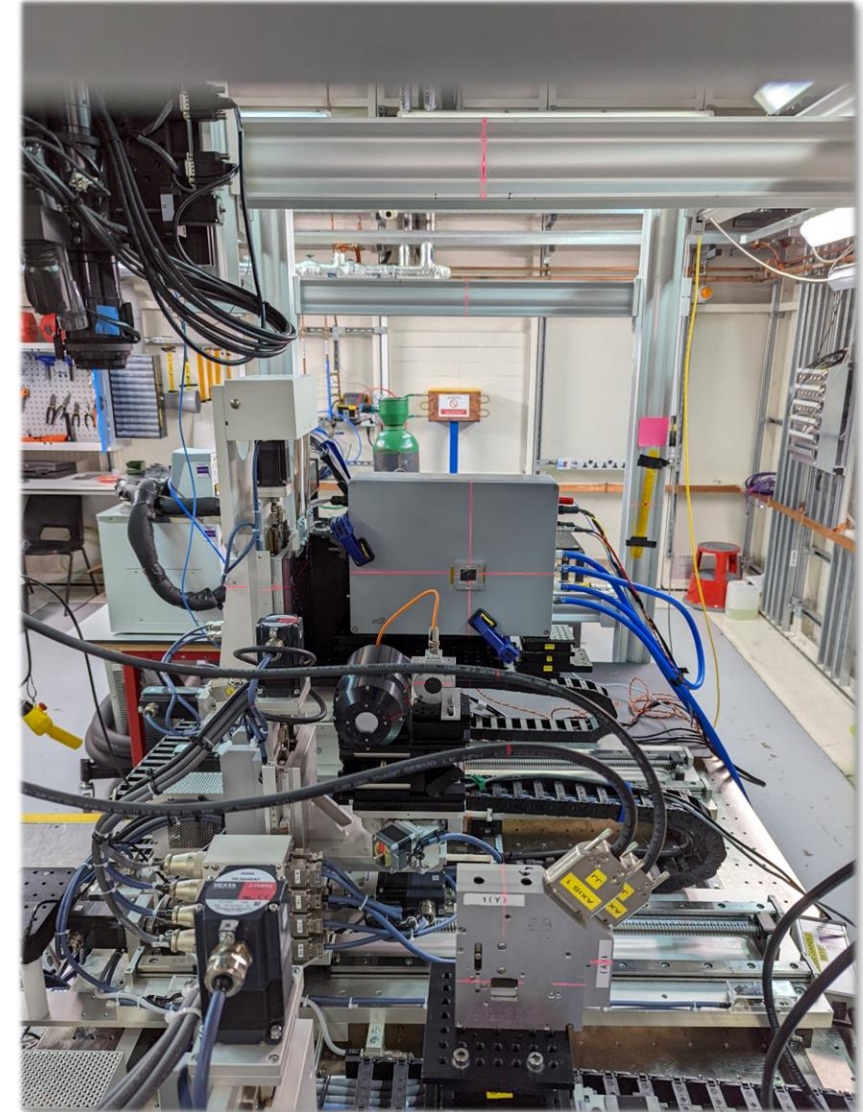
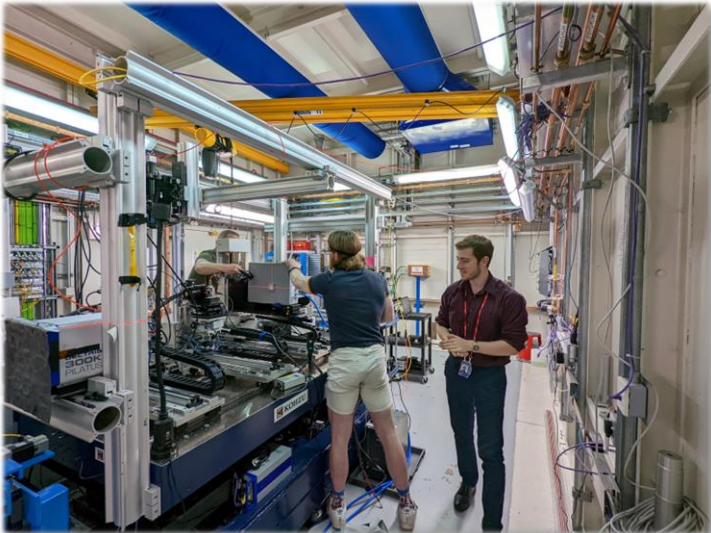
X-Ray transmission measurements of a DDR Ram Card using a HEXITEC_{MHz} HF-CZT sensor



X-Ray Fluorescence (XRF) measurements of Ta foil using a HEXITEC_{MHz} HF-CZT sensor in medium-gain mode

Experimentation at diamond

- **B16 Beamline: August and December 2022**
 - Monochromatic X-Rays: 10 – 20 keV
 - Photon fluxes: $10^5 - 10^8 \text{ ph s}^{-1} \text{ mm}^{-2}$
 - 1 MHz data stream on one fast-data channel
 - Tested **p-type Si (300 μm)**, **HF-CZT (2 mm)**, **GaAs (500 μm)** devices
- Beamline scientists: Vishal Dhamgaye, Oliver Fox, Kawal Sawhney

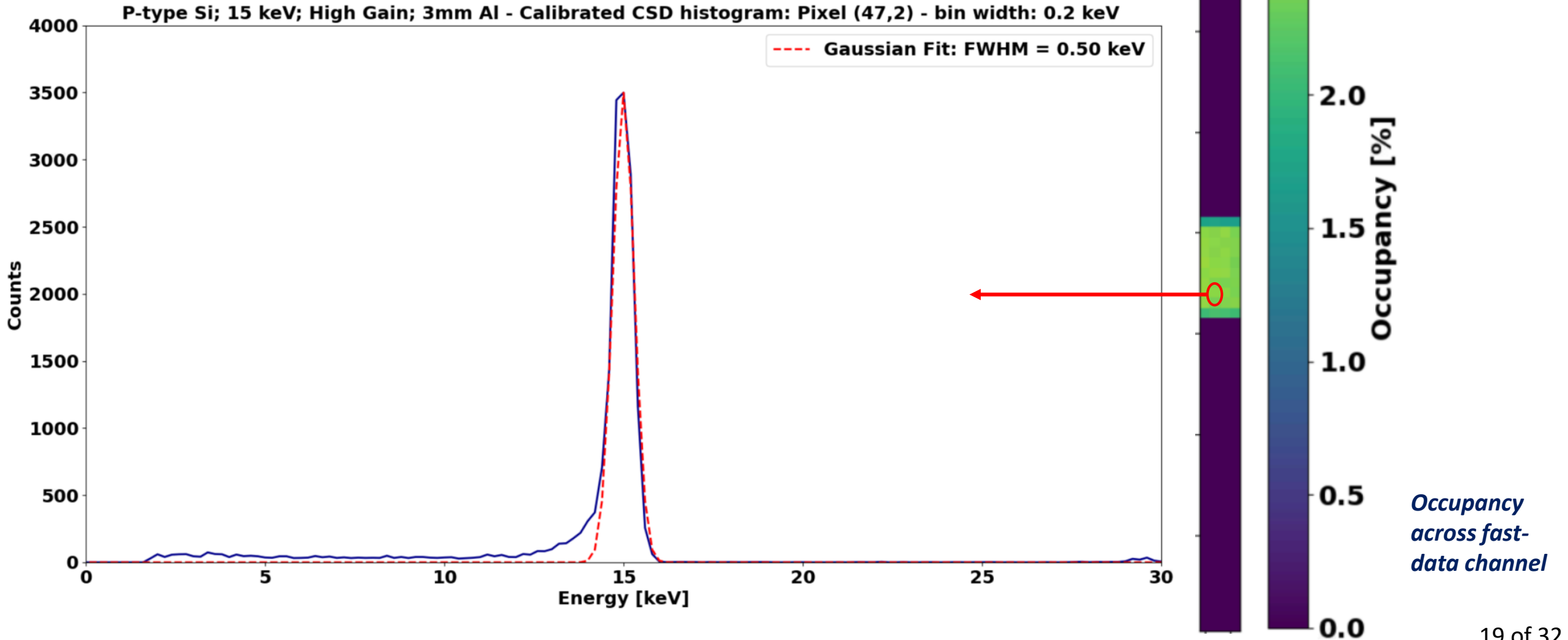


B16 setup photos



diamond – Characterisation

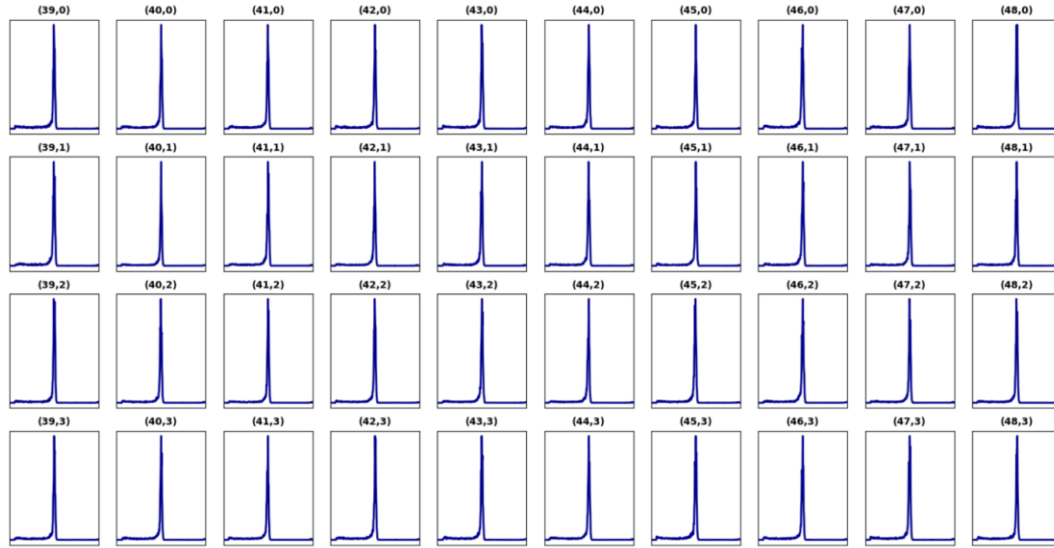
P-type Si; 15 keV; High Gain; 3 mm Al



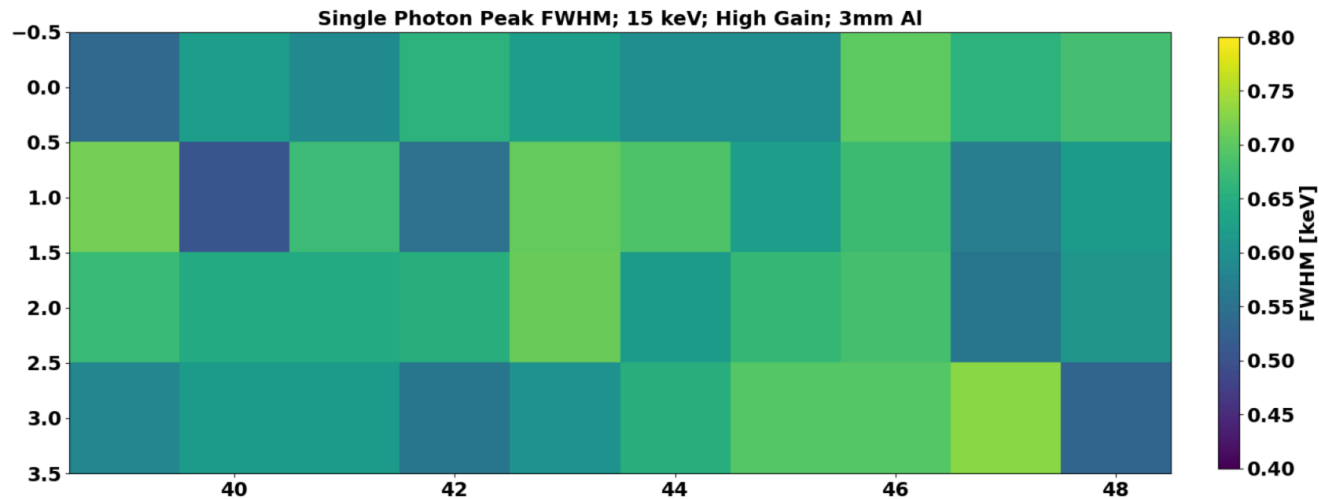


diamond – Characterisation

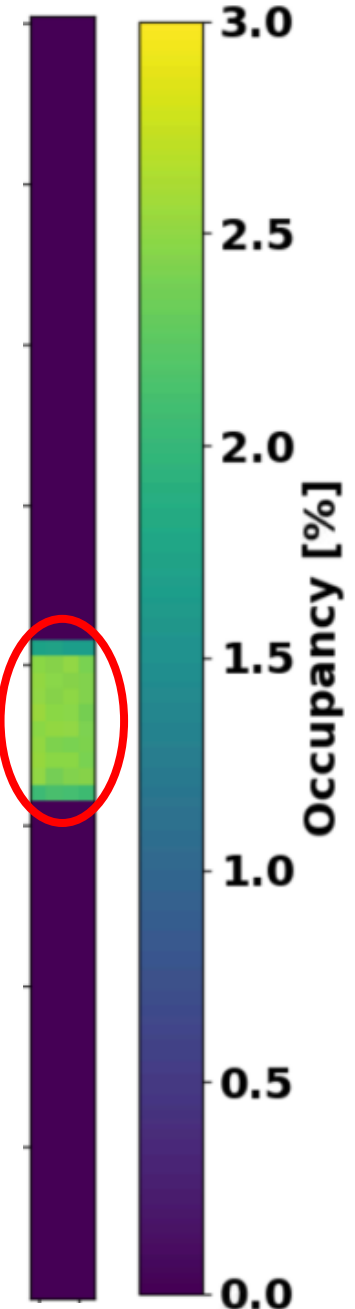
P-type Si; 15 keV; High Gain; 3 mm Al



*Calibrated histograms
in beam area*



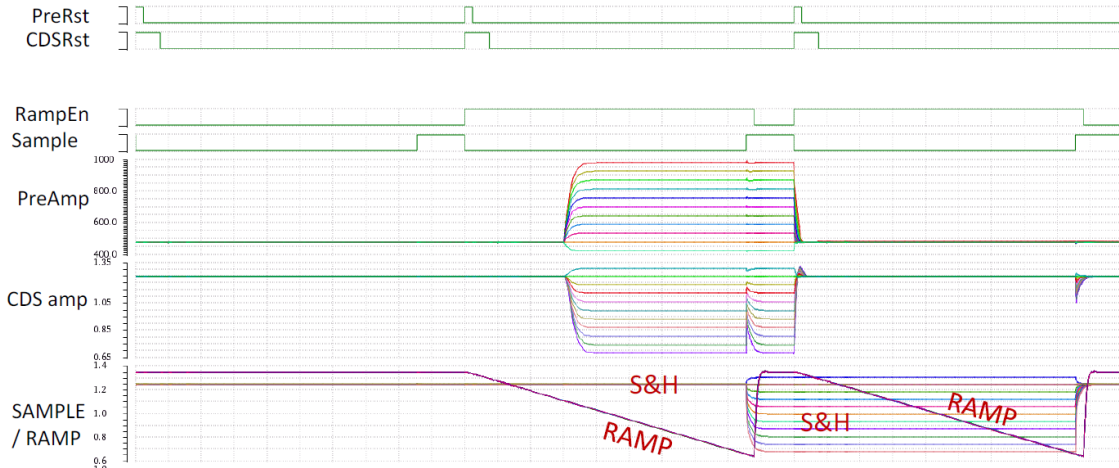
*Single photon
FWHM in beam area*



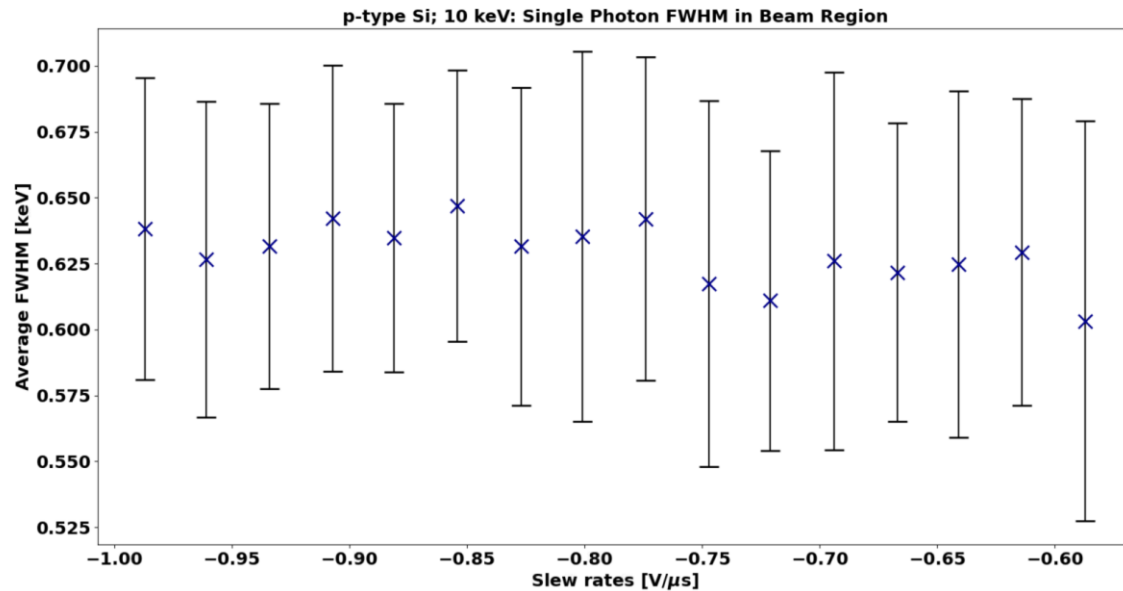
*Occupancy
across fast-
data channel*



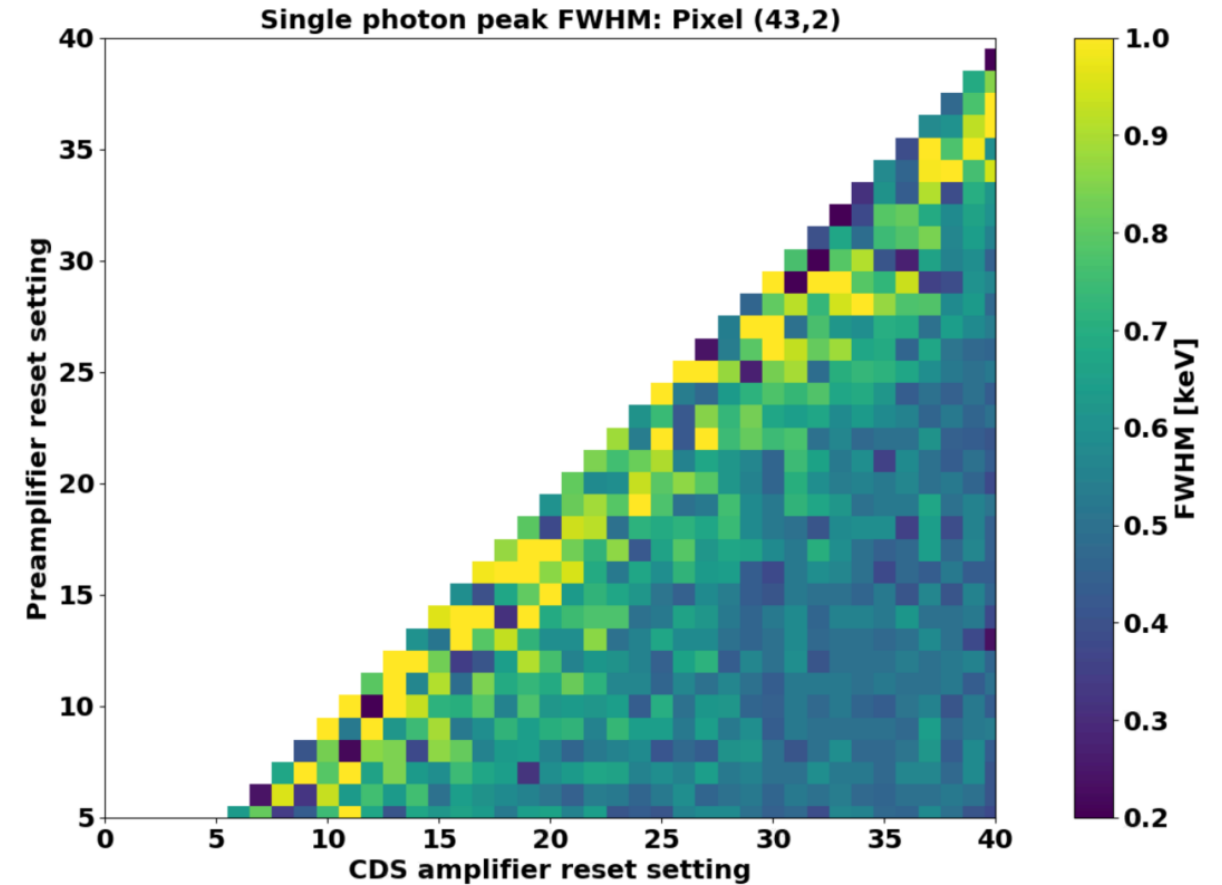
diamond – Optimisation



Timing signals schematic



Optimising ramp slew rate

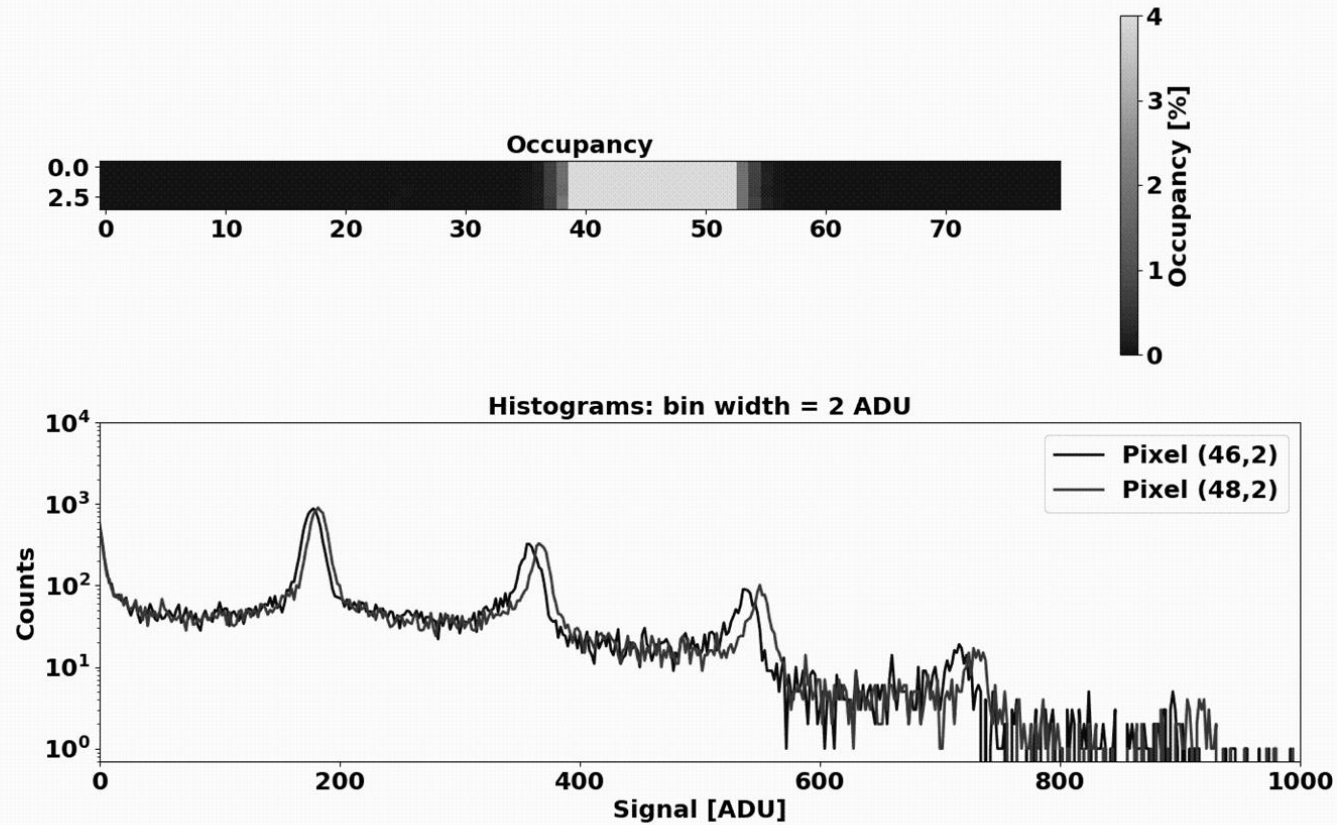


Optimising preamplifier and CDS amplifier timings



diamond – Dynamic Measurements

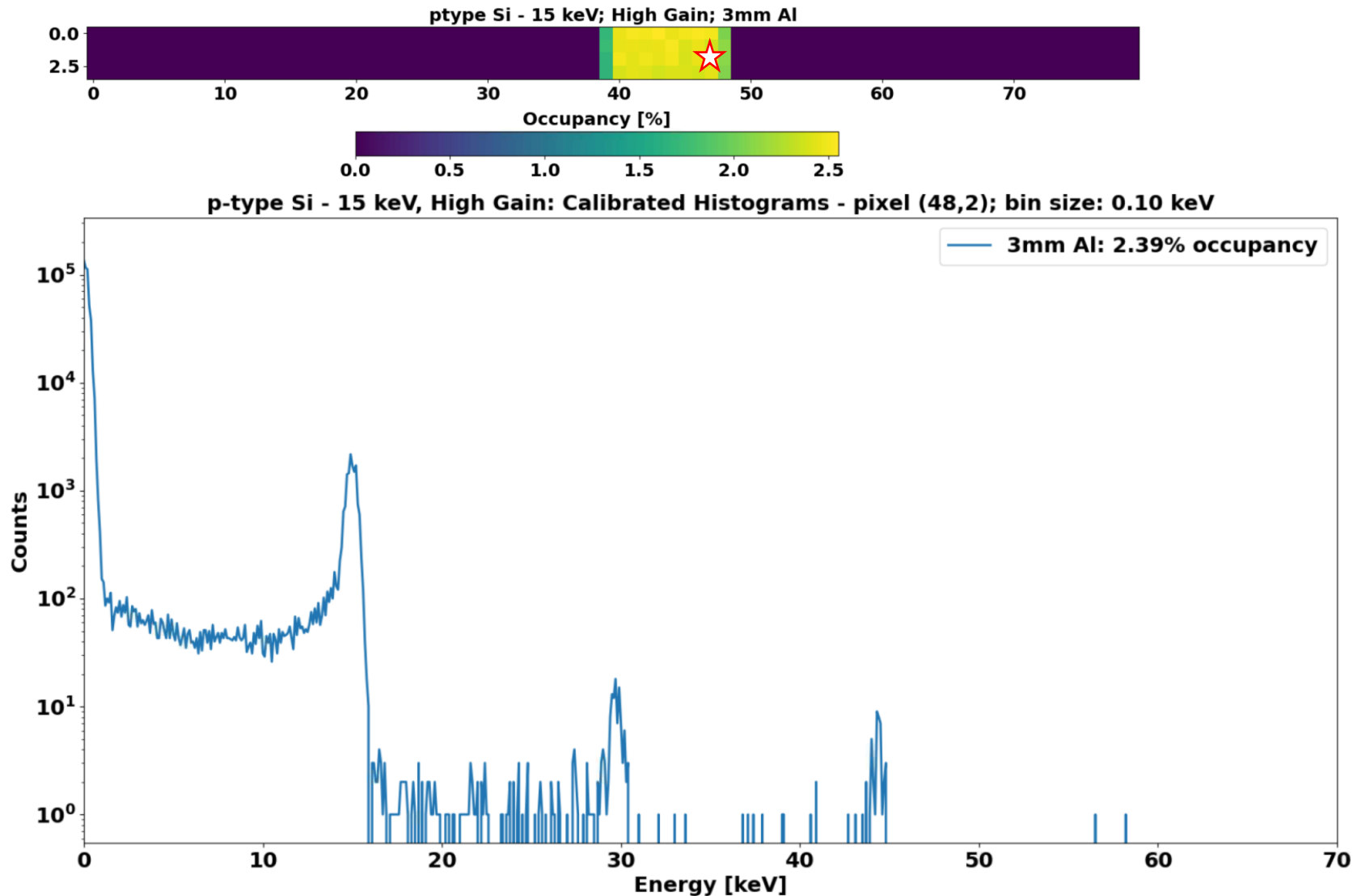
P-type Si: Changing slit size over 60 seconds (30 ms/video frame)





diamond – Integrating Measurements

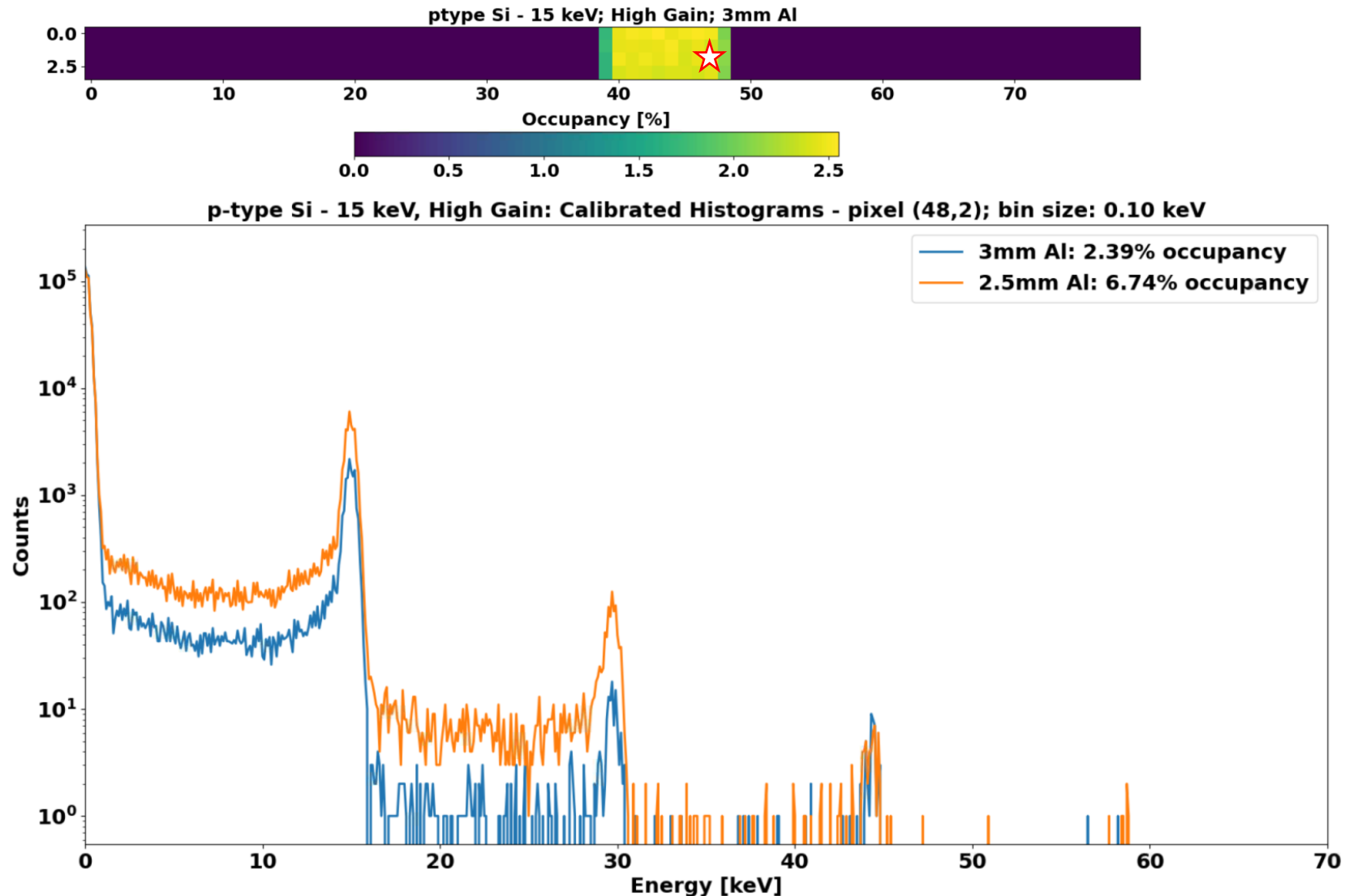
P-type Si; 15 keV; High Gain; 3 mm Al – 0 mm Al





diamond – Integrating Measurements

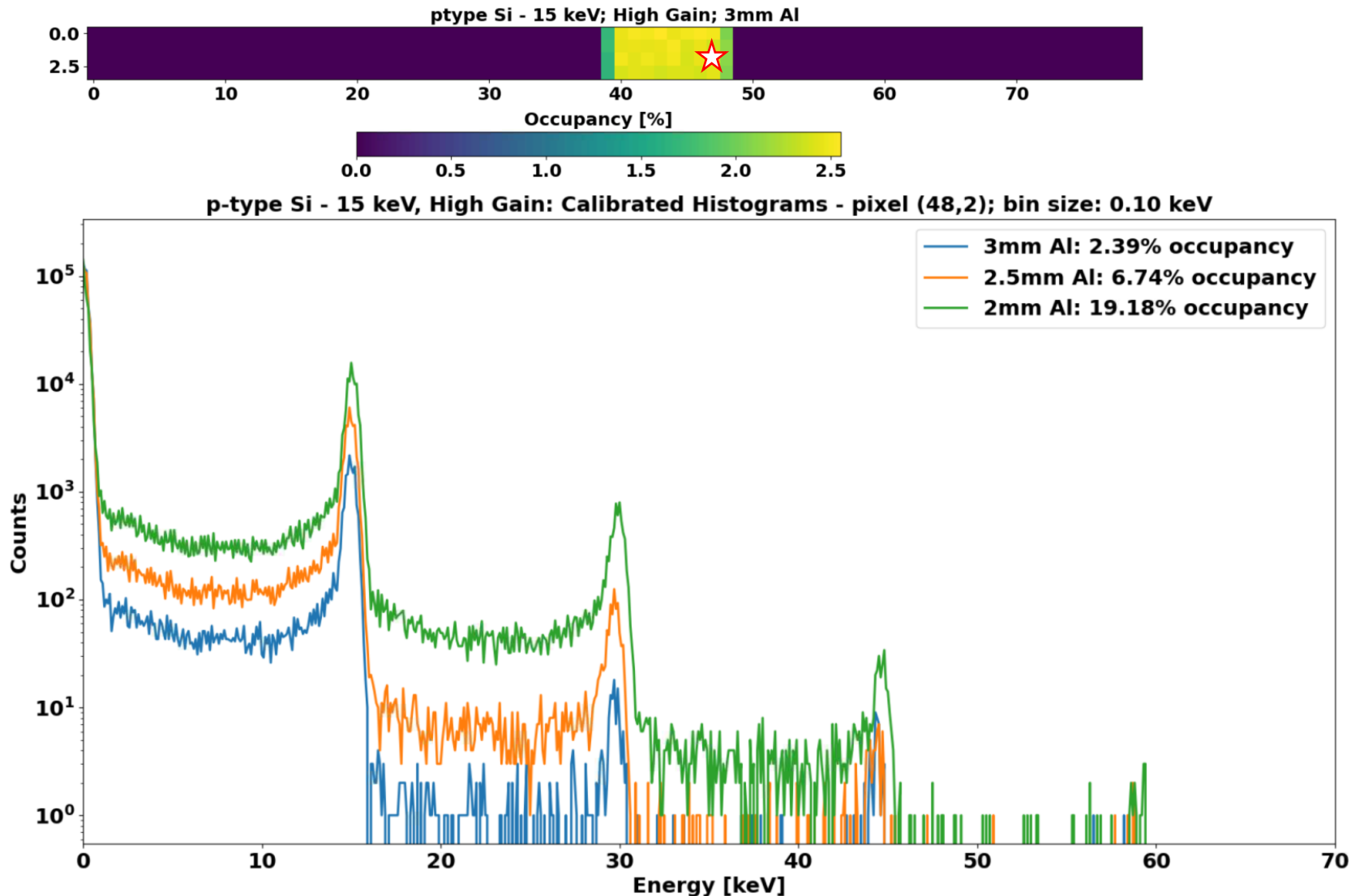
P-type Si; 15 keV; High Gain; 3 mm Al – 0 mm Al





diamond – Integrating Measurements

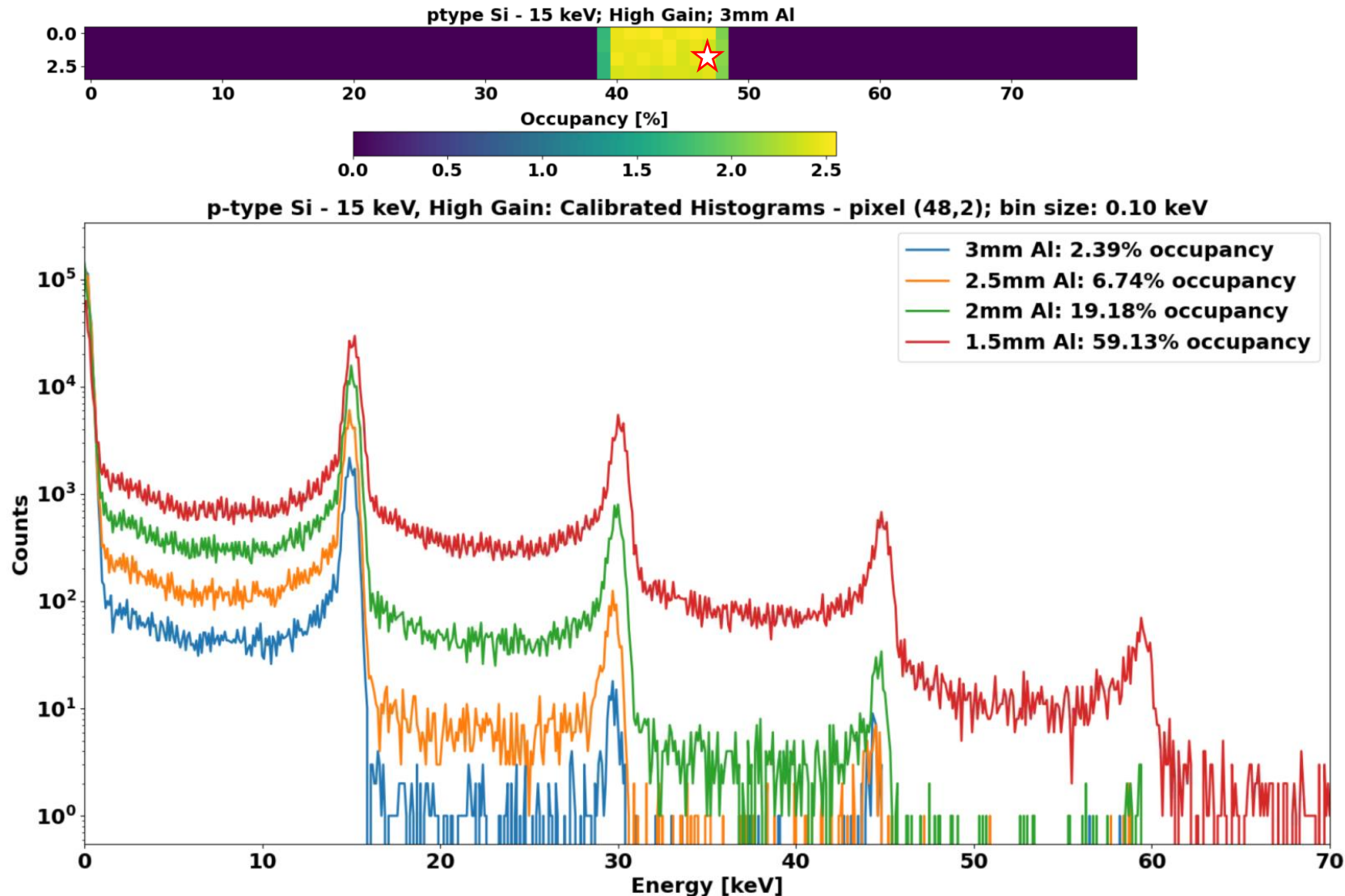
P-type Si; 15 keV; High Gain; 3 mm Al – 0 mm Al





diamond – Integrating Measurements

P-type Si; 15 keV; High Gain; 3 mm Al – 0 mm Al

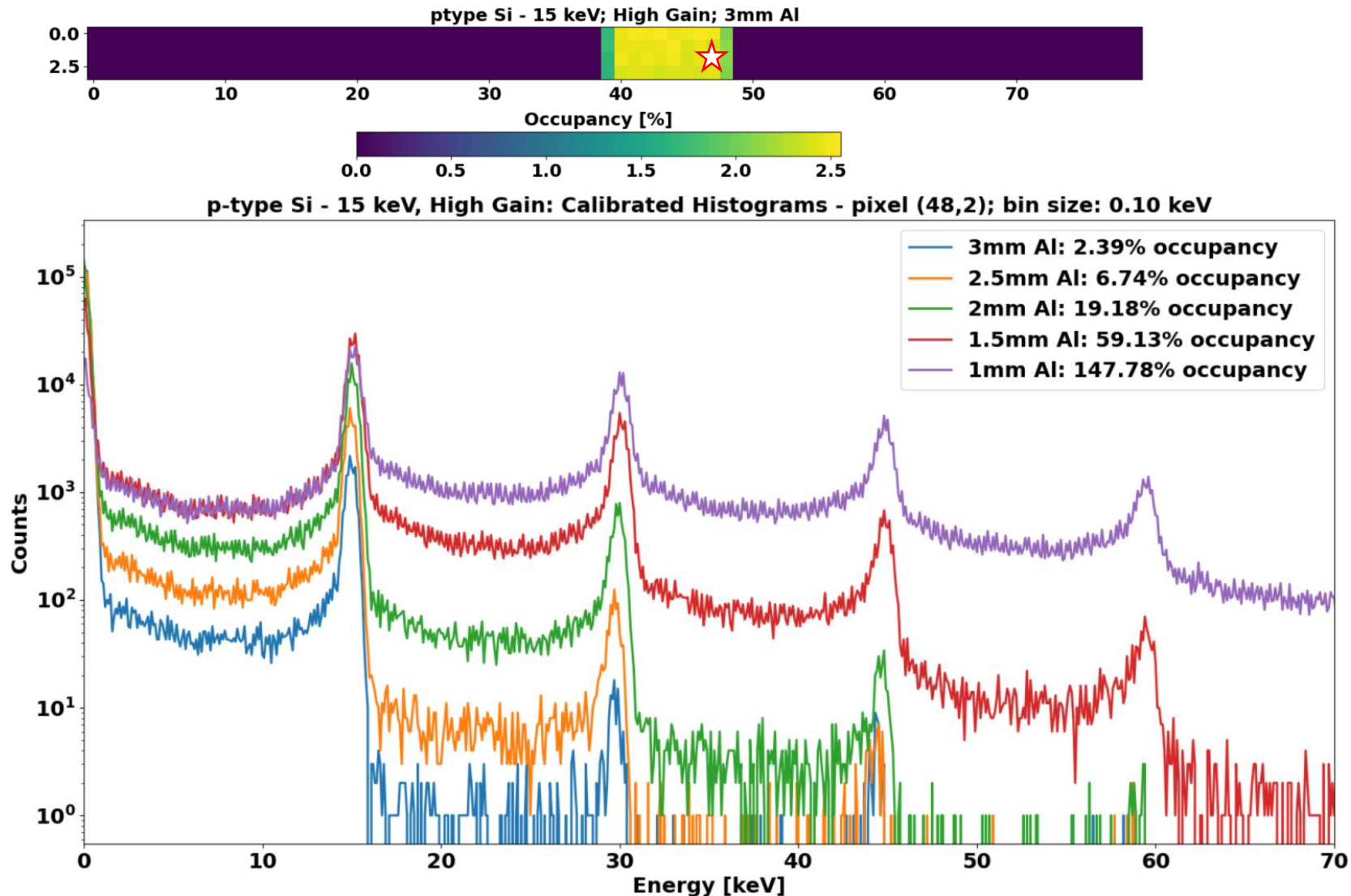


*Calibrated histograms of
pixel (48,2)*



diamond – Integrating Measurements

P-type Si; 15 keV; High Gain; 3 mm Al – 0 mm Al

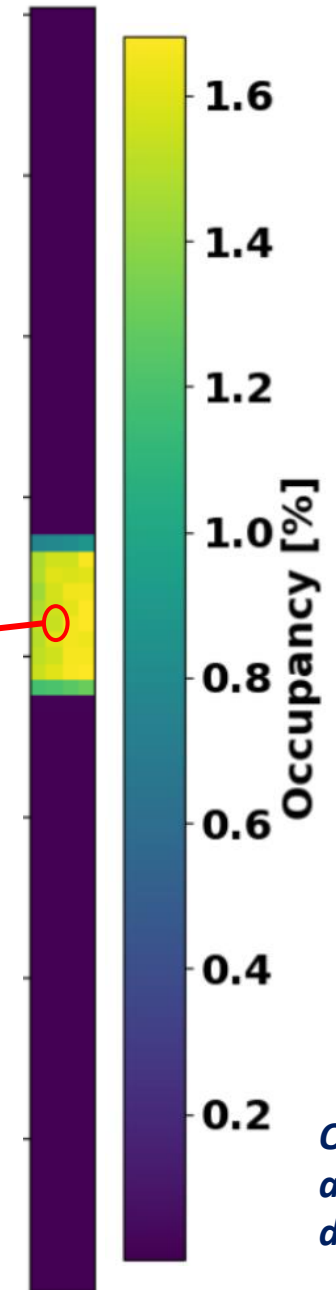
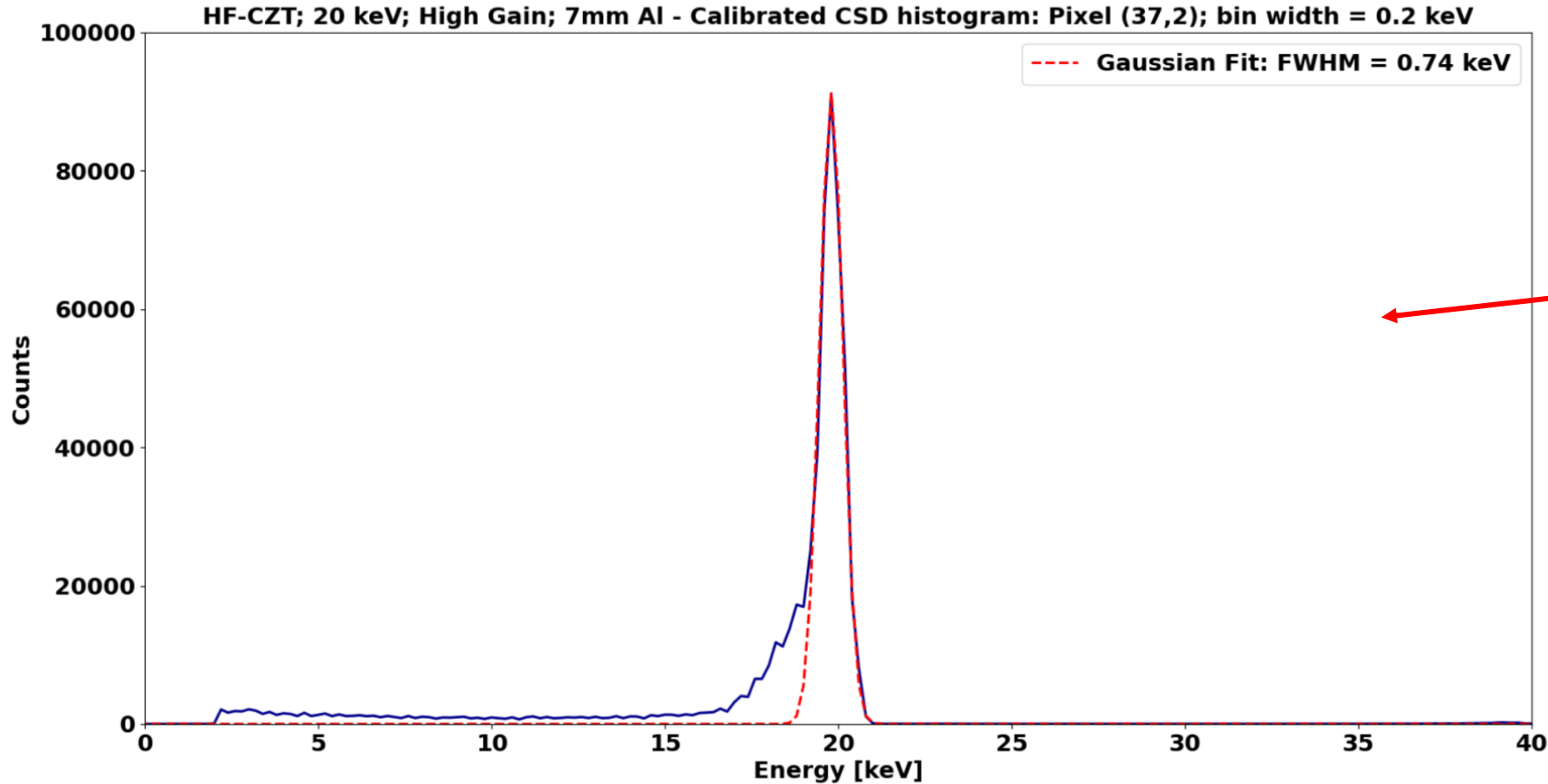


*Calibrated histograms of
pixel (48,2)*



diamond – HF-CZT Characterisation

HF-CZT; 20 keV; High Gain; 7 mm Al

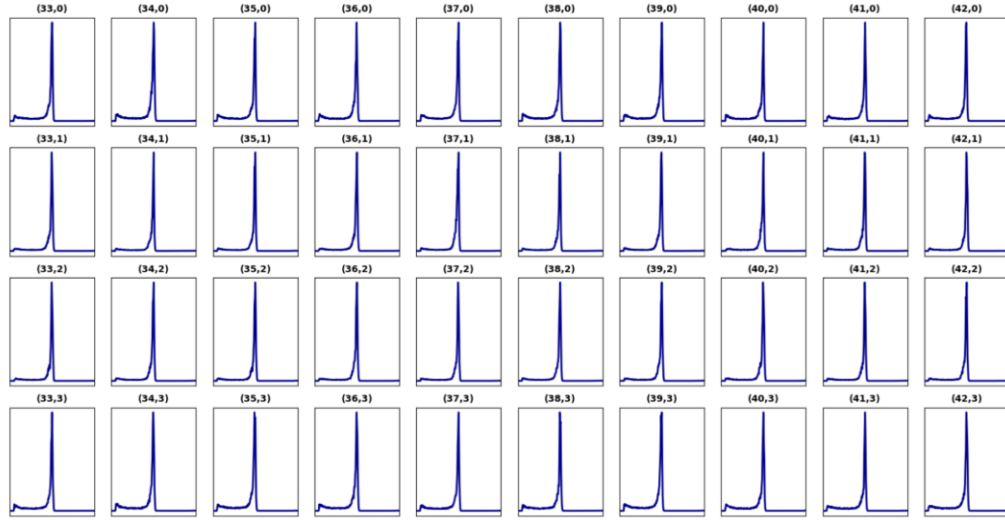


*Occupancy
across fast-
data channel*

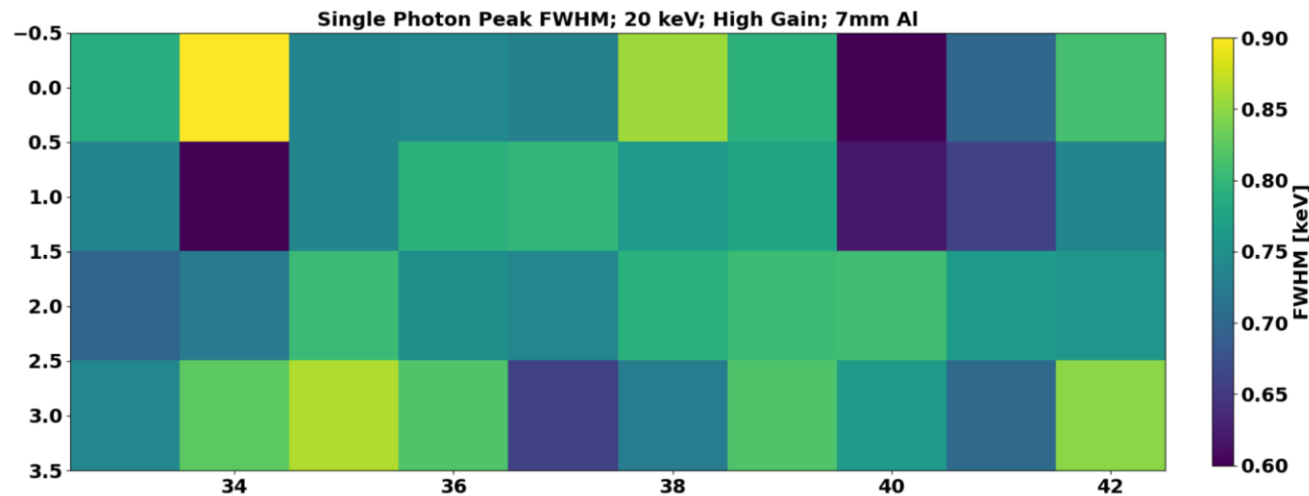


diamond – HF-CZT Characterisation

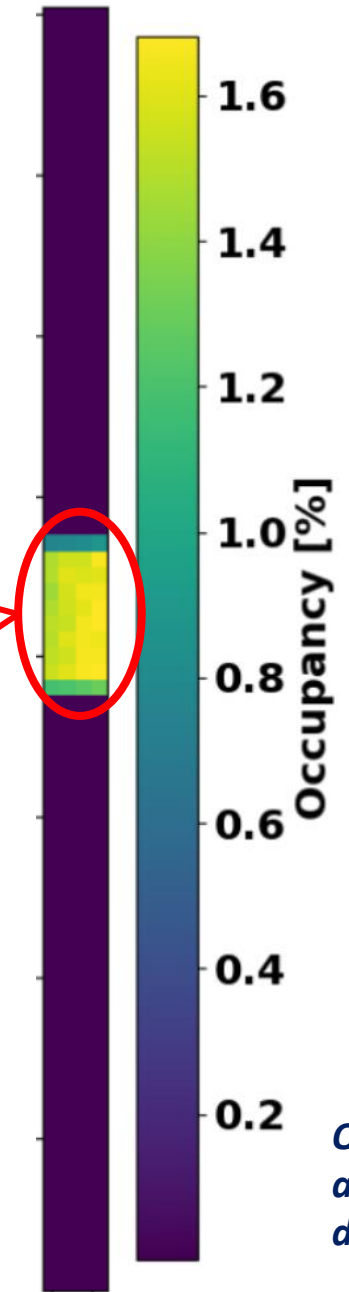
HF-CZT; 20 keV; High Gain; 7 mm Al



*Calibrated CSD
histograms in beam area*



*Single photon
FWHM in beam area*



*Occupancy
across fast-
data channel*

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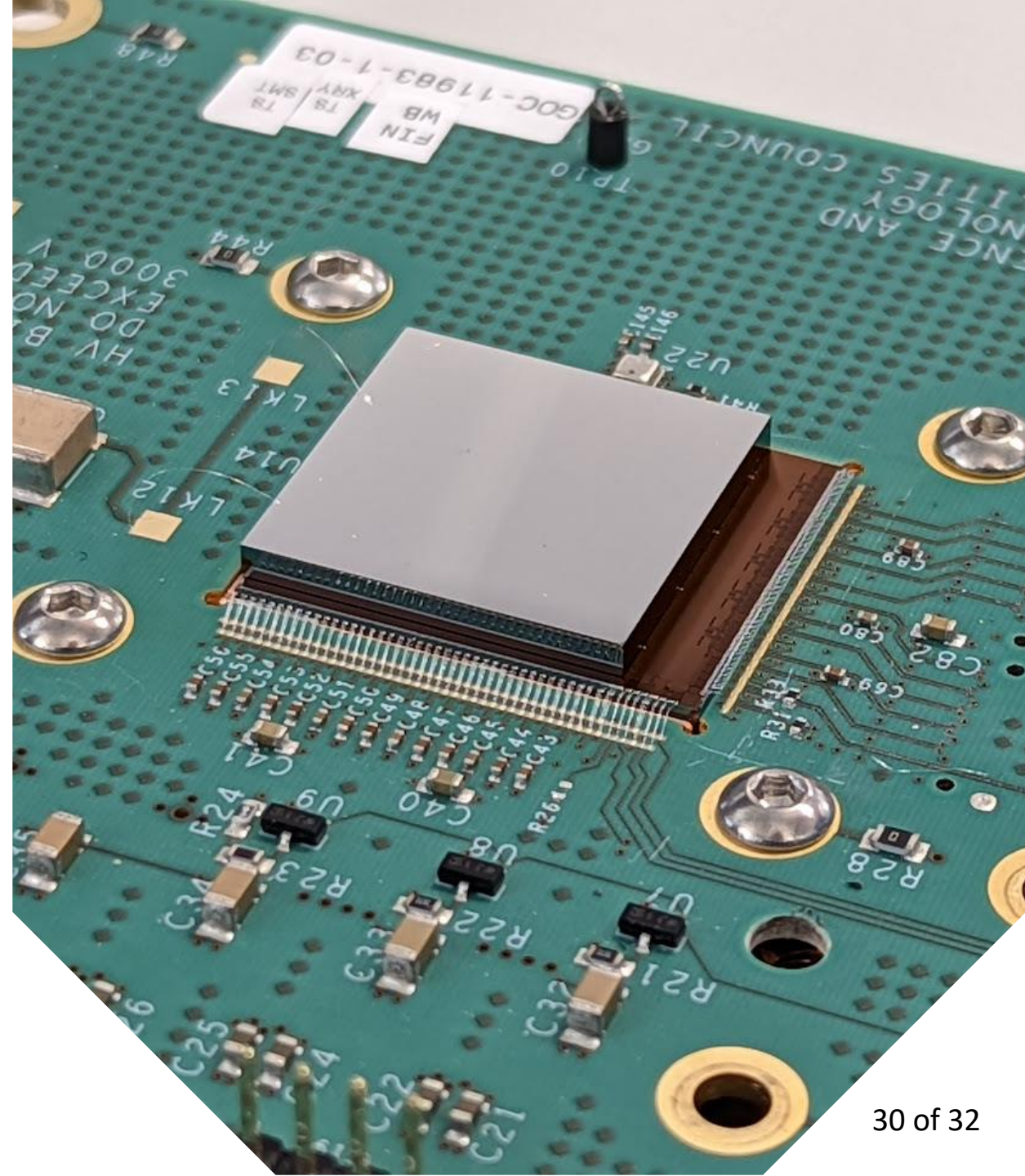
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Next Steps

Achieving a 20-channel fast data output

- Reading out the full 80×80 array using the fast data

Further lab-based ASIC and sensor characterisation

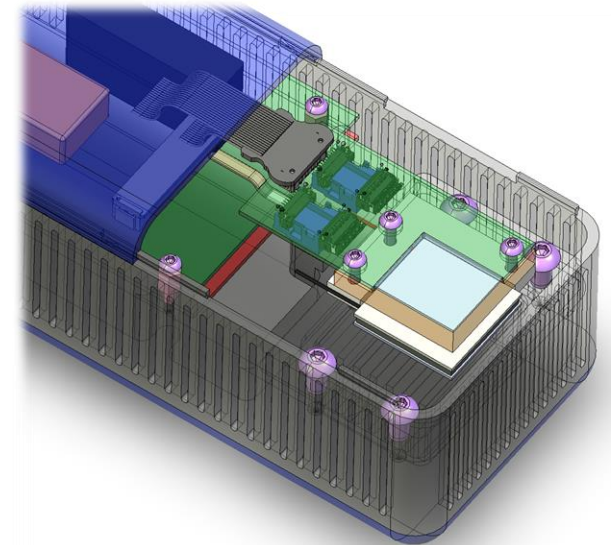
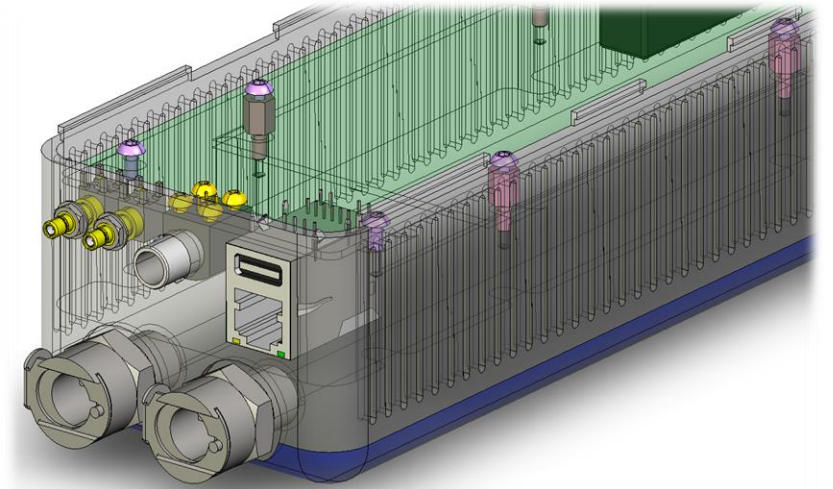
Implementation of in-FPGA histogramming

Delivery of HEXITEC_{MHz} detector system

- Smaller, form factor production-grade system

Delivering Science

- 5D-CT for Materials Science – University of Manchester
- Mammography – Institute of Cancer Research, UK
- Security imaging – Nottingham-Trent University



Possible designs for HEXITEC_{MHz} detector system

Summary

- HEXITEC_{MHz} is a fully-spectroscopic X-Ray detector capable of operating continuously at 1 MHz

Parameter	HEXITEC _{MHz}
Max Frame Rate (MHz)	1
Max Spectroscopic Flux (ph s ⁻¹ mm ⁻²)	>10 ⁶
Digitisation	On-chip
Detector Type	Integrating
Measured FWHM	0.50 keV @ 15 keV in p-type Si 0.74 keV @ 20 keV in HF-CZT

- Testing underway to characterise the ASIC and optimise register settings
- The next year will include delivery of a full 80×80 pixel readout and a new smaller form-factor system

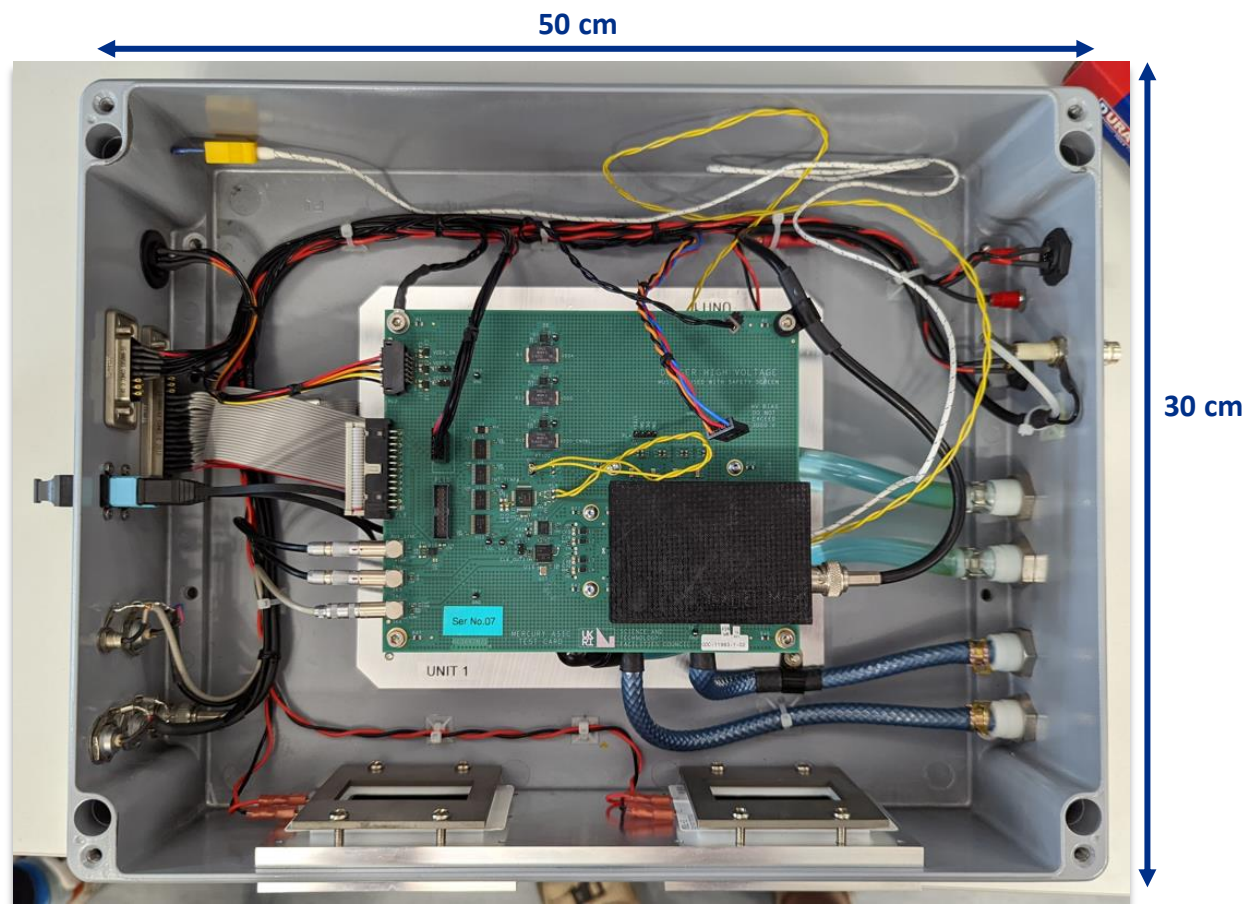


HEXITEC_{MHz} testing in February 2022

Backup Slides



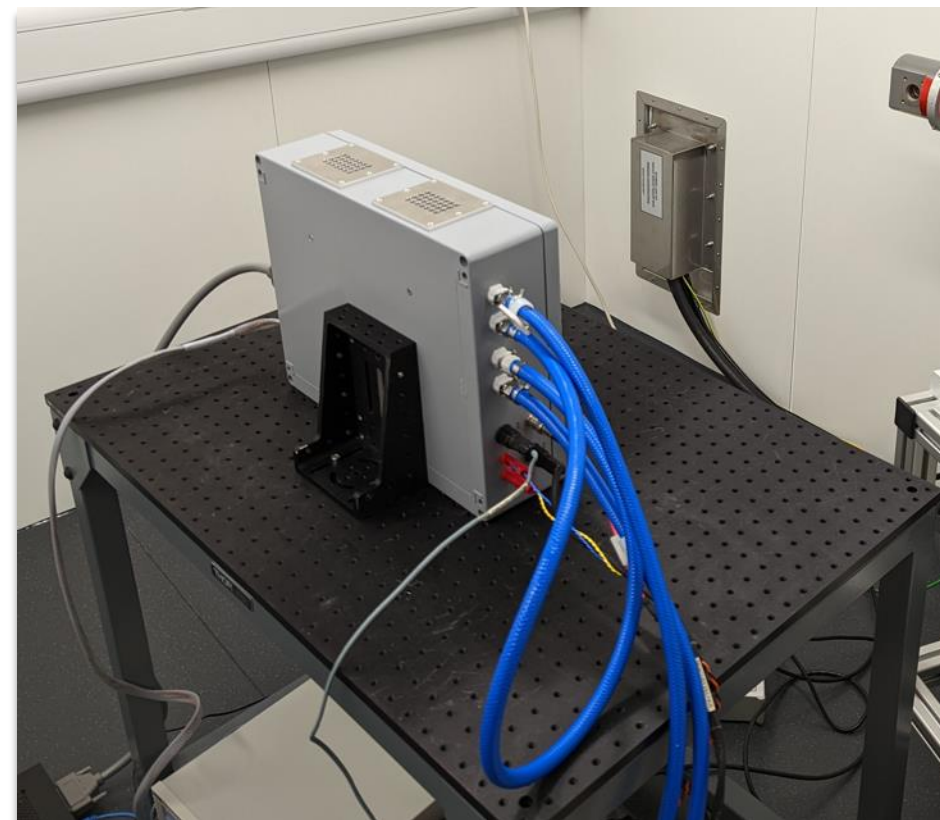
Testing – Test Setup



HEXITEC_{MHz} test enclosure (interior)



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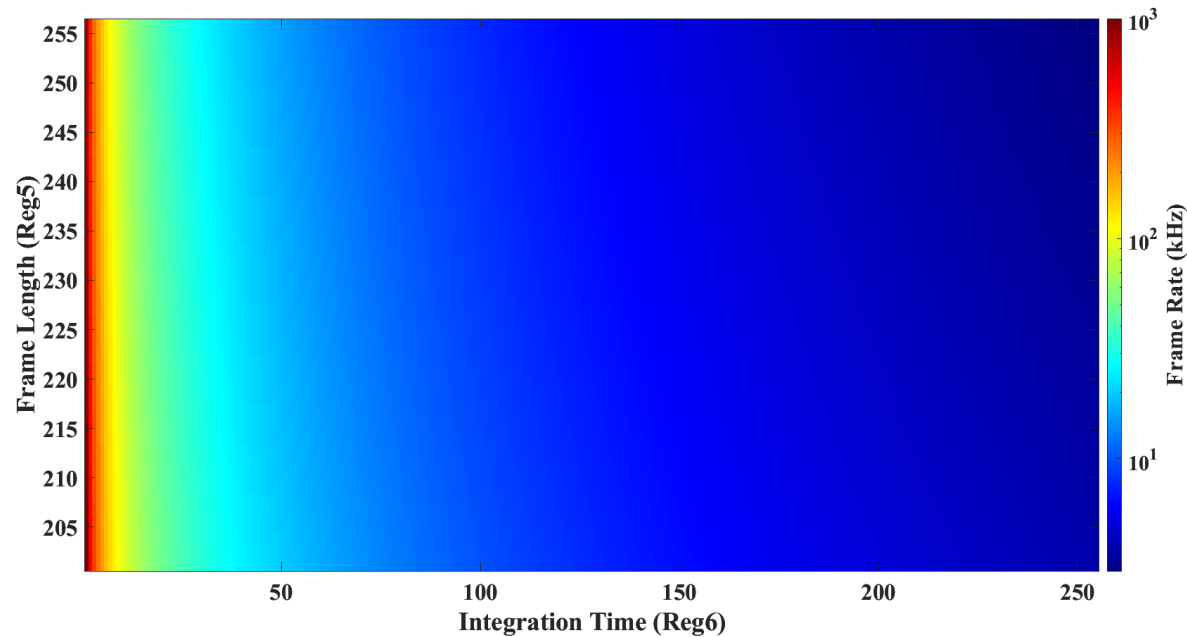


HEXITEC_{MHz} test enclosure (exterior)

Available Frame Rates

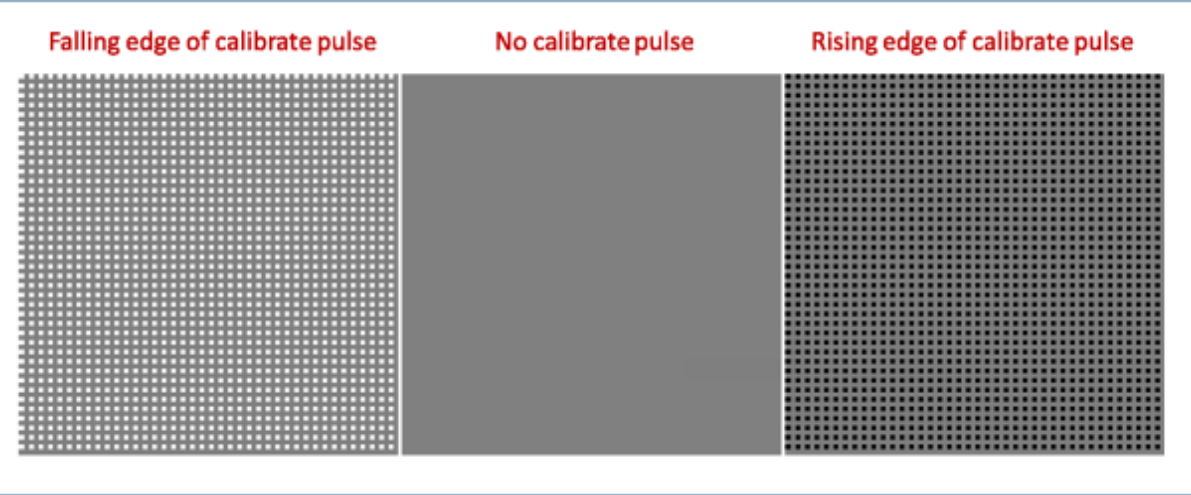
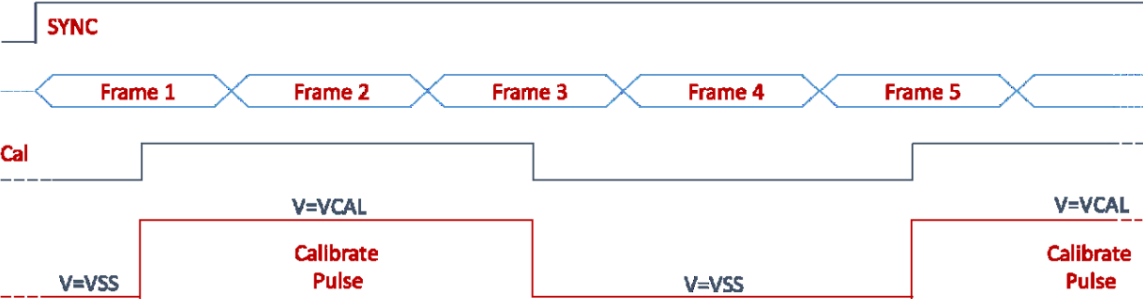
- Two chip registers can be altered:
 - Frame Time: 200 → 255 clocks frame⁻¹
 - Integration Length: 1 → 255 frames

■ Default values

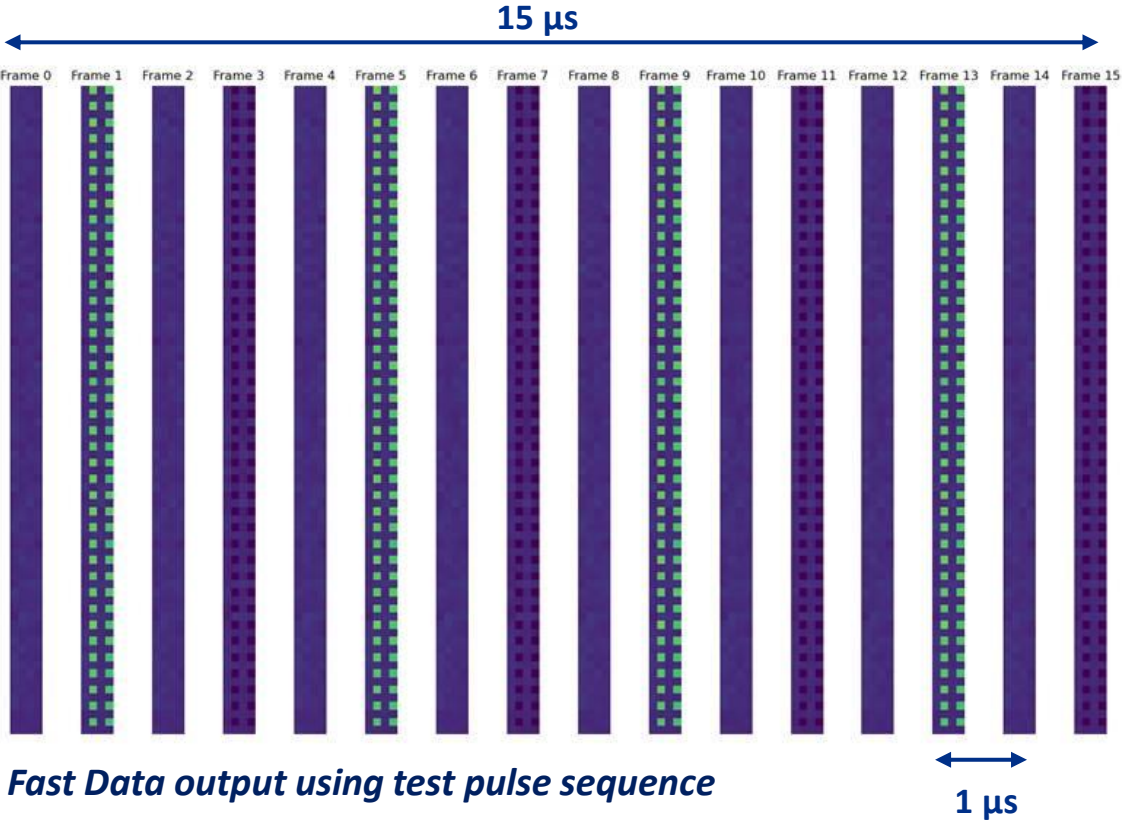


Available Frame Rates

Test Pulse Sequence

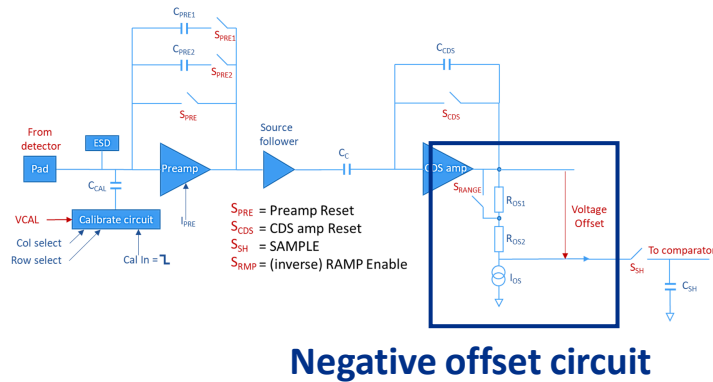


Test pulse sequence



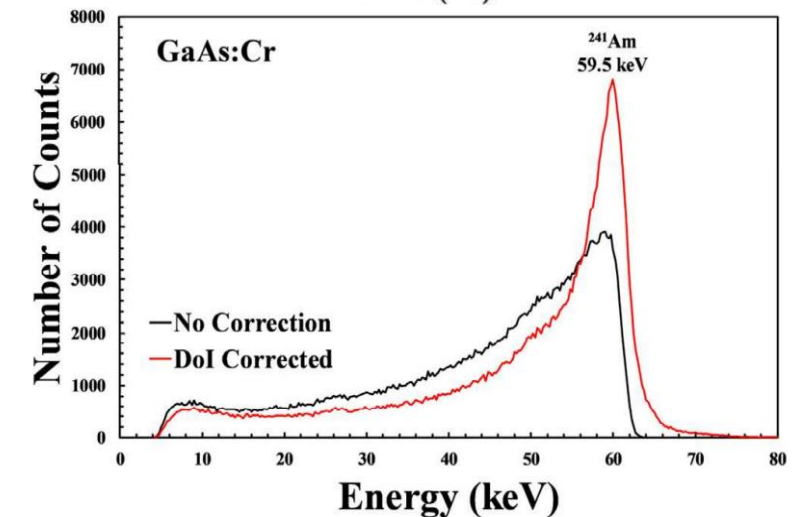
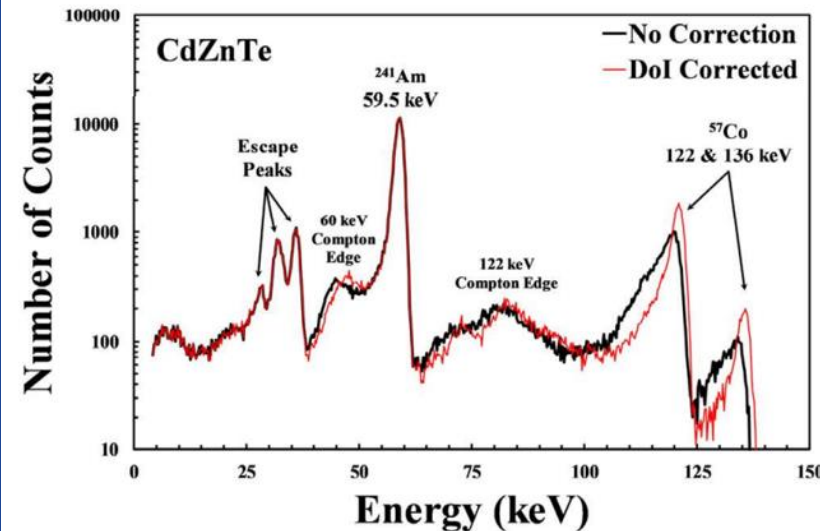
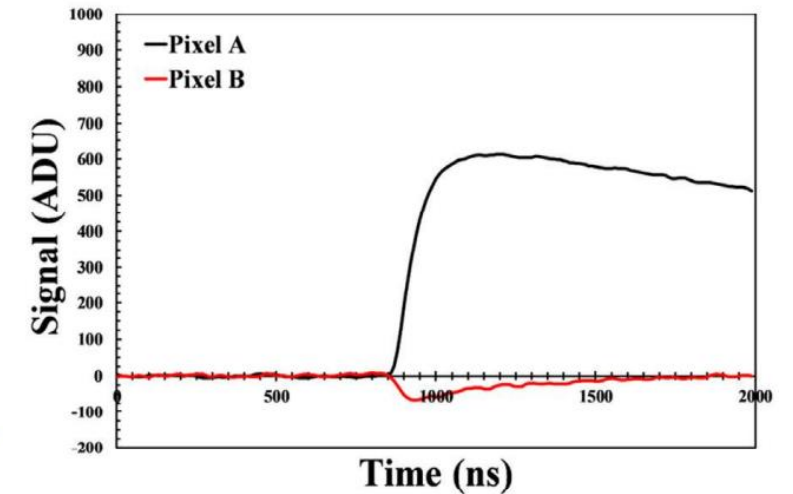
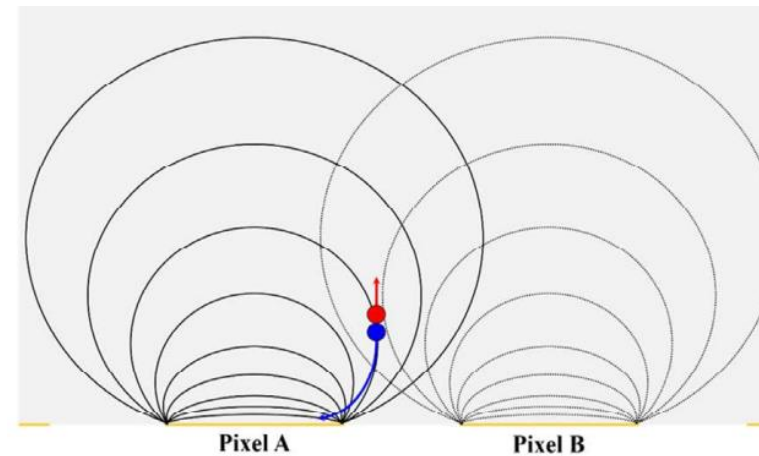
Fast Data output using test pulse sequence

Front End – Negative Offset Circuit

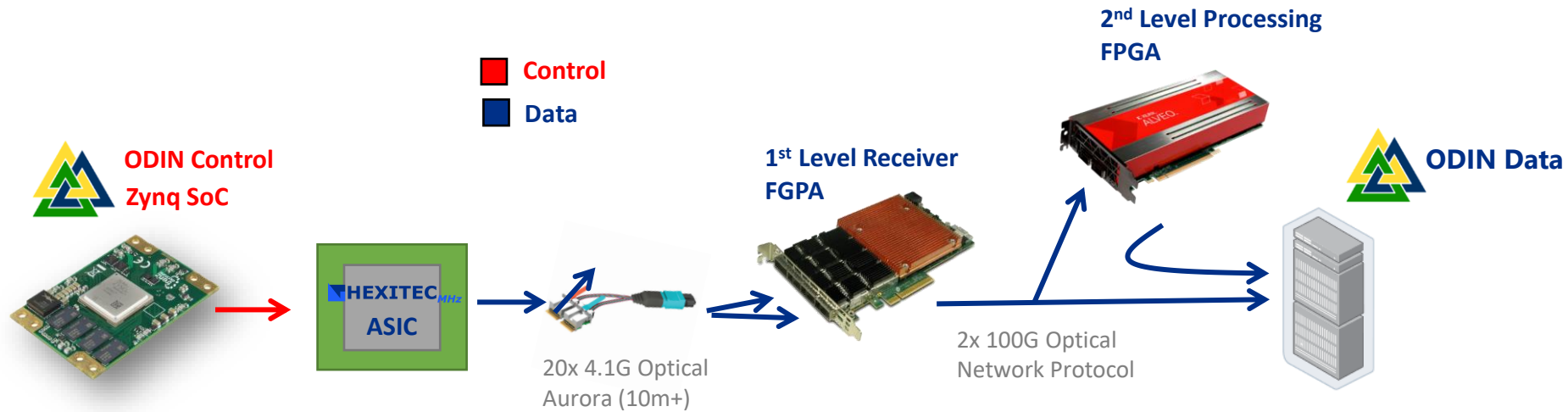


Potential application - Results from Veale et al., 2019;

- Data collected with STFC's PIXIE ASIC ([DOI: 10.1016/j.nima.2019.01.045](https://doi.org/10.1016/j.nima.2019.01.045))

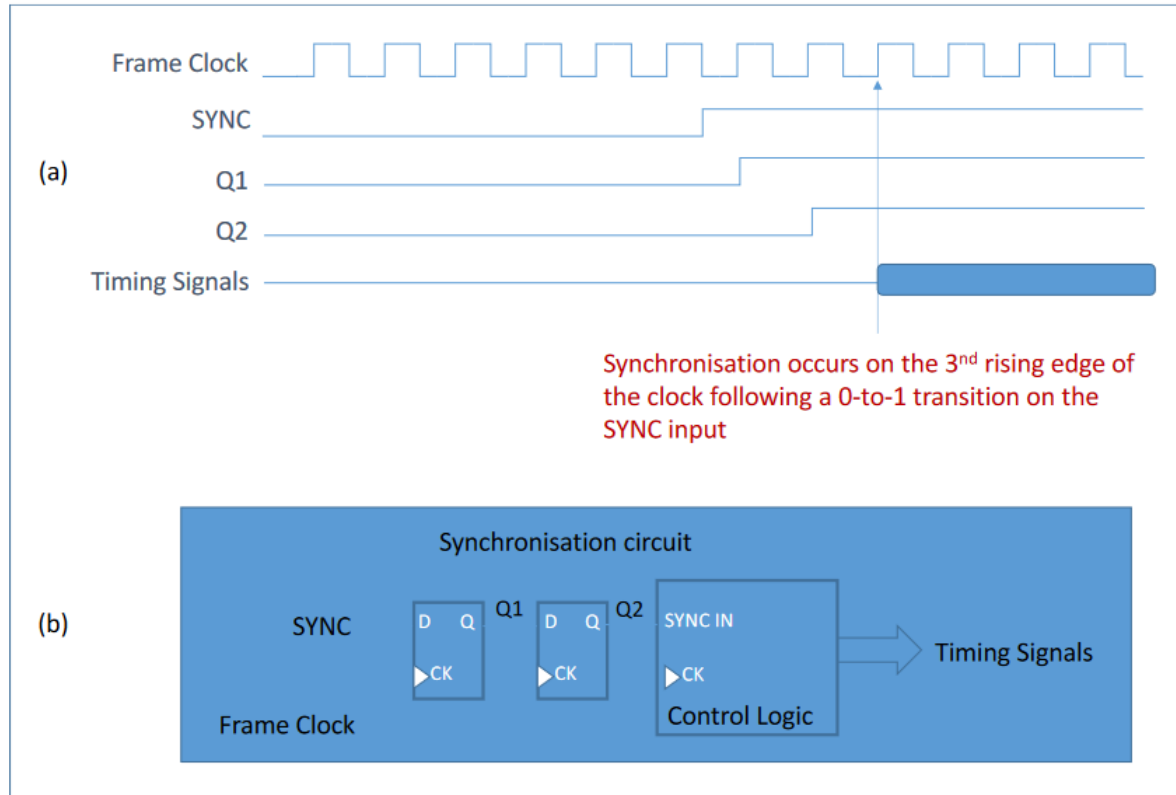


Data Output Plane



Data output path schematic

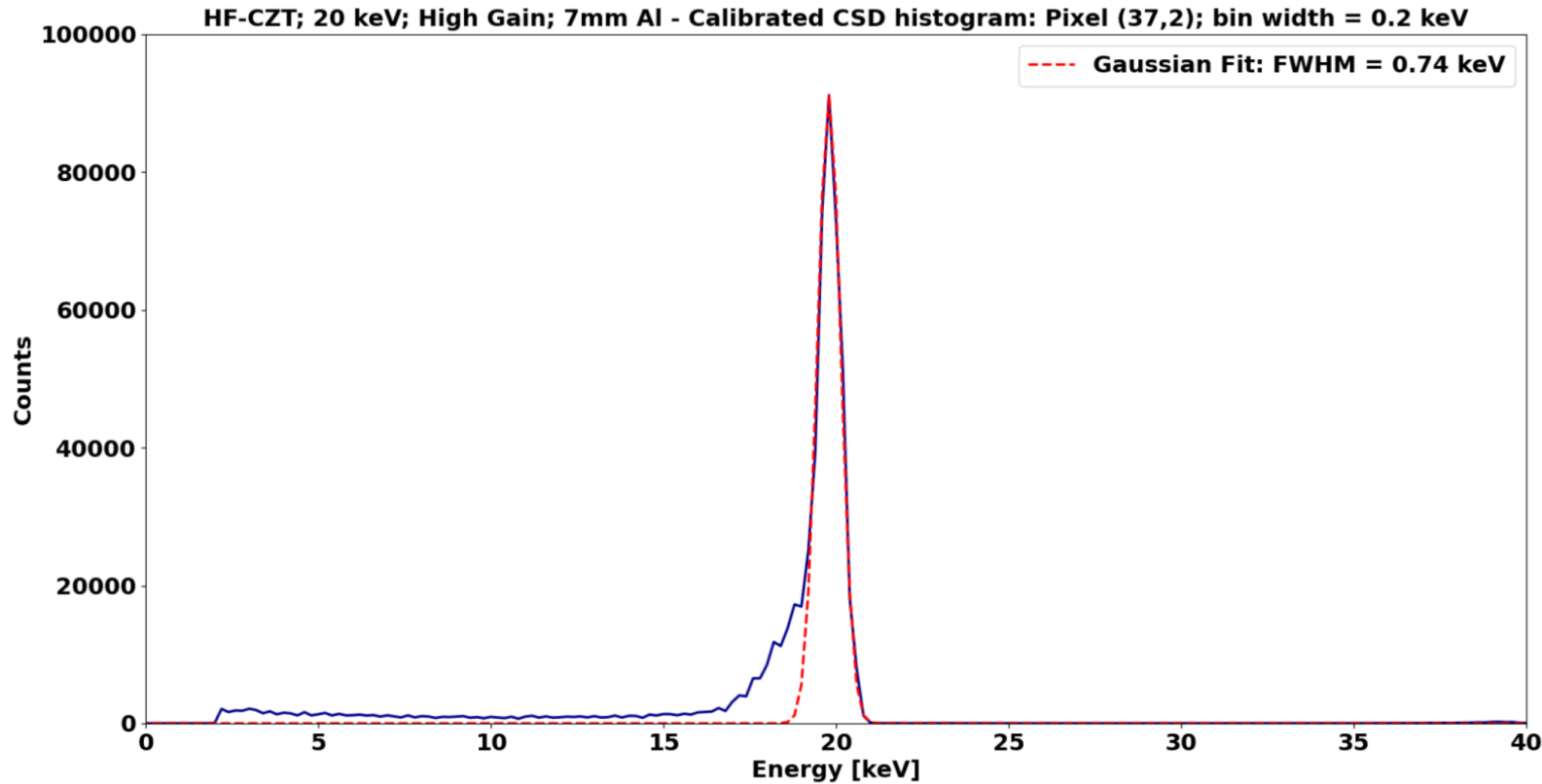
Synchronising the ASIC



- ASIC synchronised by **controlling transition of SYNC input**
 - Logic 0 → logic 1
 - Synchronisation occurs on 3rd subsequent rising clock edge
- Used for external synchronisation and multi-ASIC systems

Synchronisation circuit

Electronic Noise Contribution

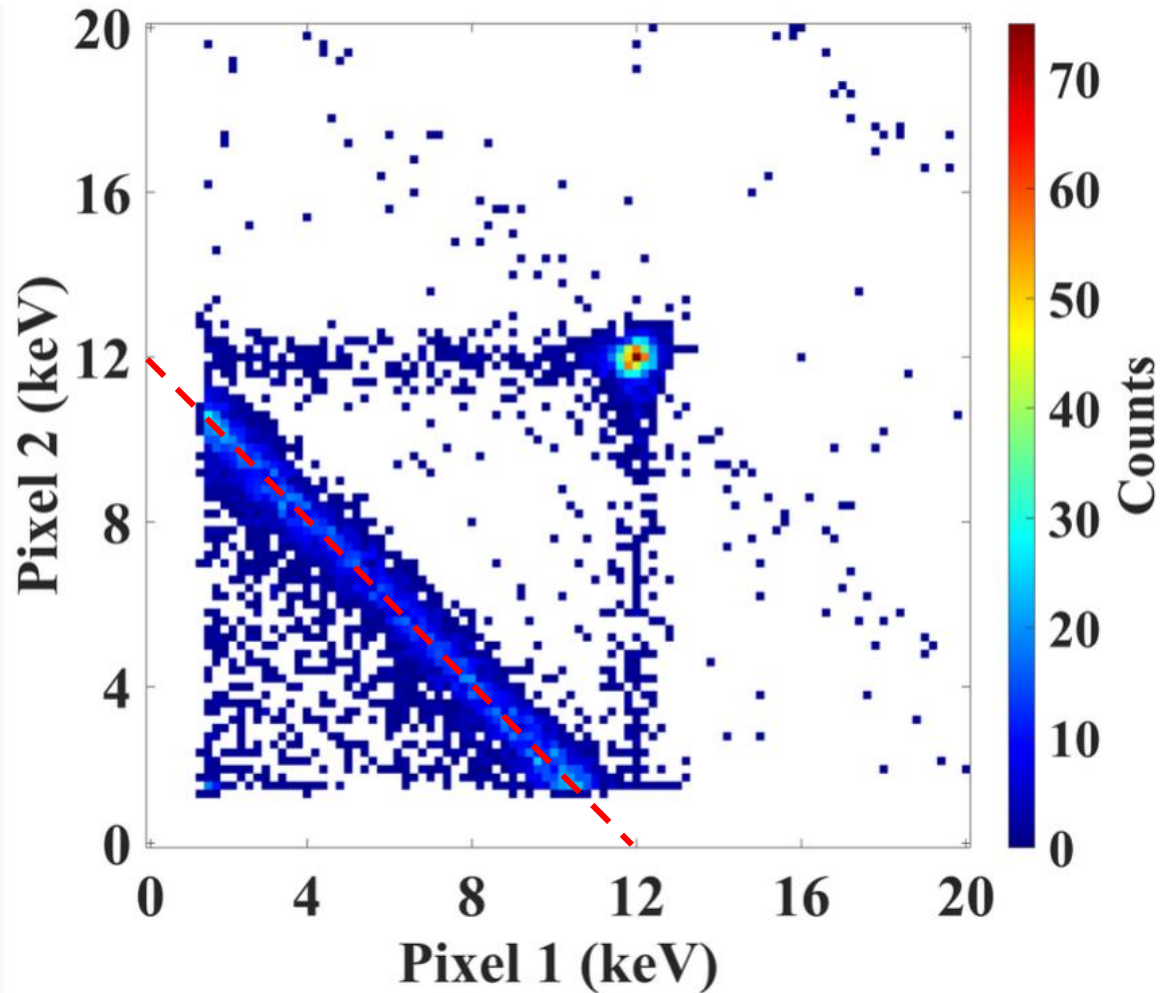


- HF-CZT FWHM @ 20 keV ≈ 0.7 keV
- HF-CZT w factor = 4.67 eV
- $\rightarrow \text{ENC} = \sqrt{700 \times 4.67} \approx 57 \text{ e}^-$



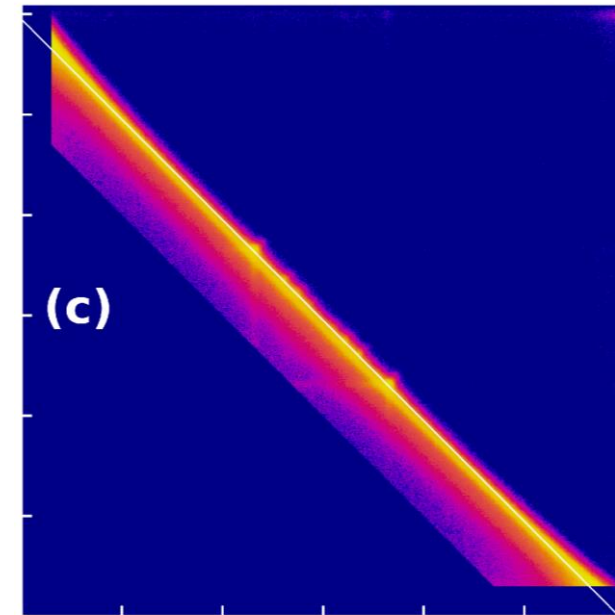
diamond – Charge Sharing

P-type Si; 12 keV; High Gain; 1.5mm Al



Energy-components of two-pixel charge-shared events at 12 keV

HF – CdZnTe
Frame occupancy : 0.4%



Open Access Article

Charge Sharing and Charge Loss in High-Flux Capable Pixelated CdZnTe Detectors

by Kjell A. L. Koch-Mehrin ^{1,*}, Sarah L. Bugby ², John E. Lees ¹,
Matthew C. Veale ³ and Matthew D. Wilson ³

¹ Space Research Centre, Department of Physics & Astronomy, University of Leicester, Leicester LE1 7RH, UK

² Centre for Imaging Science, Department of Physics, Loughborough University, Loughborough LE11 3TU, UK

³ STFC Rutherford Appleton Laboratory, Harwell Campus, Didcot OX11 0QX, UK

* Author to whom correspondence should be addressed.

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TSVs on HEXITEC

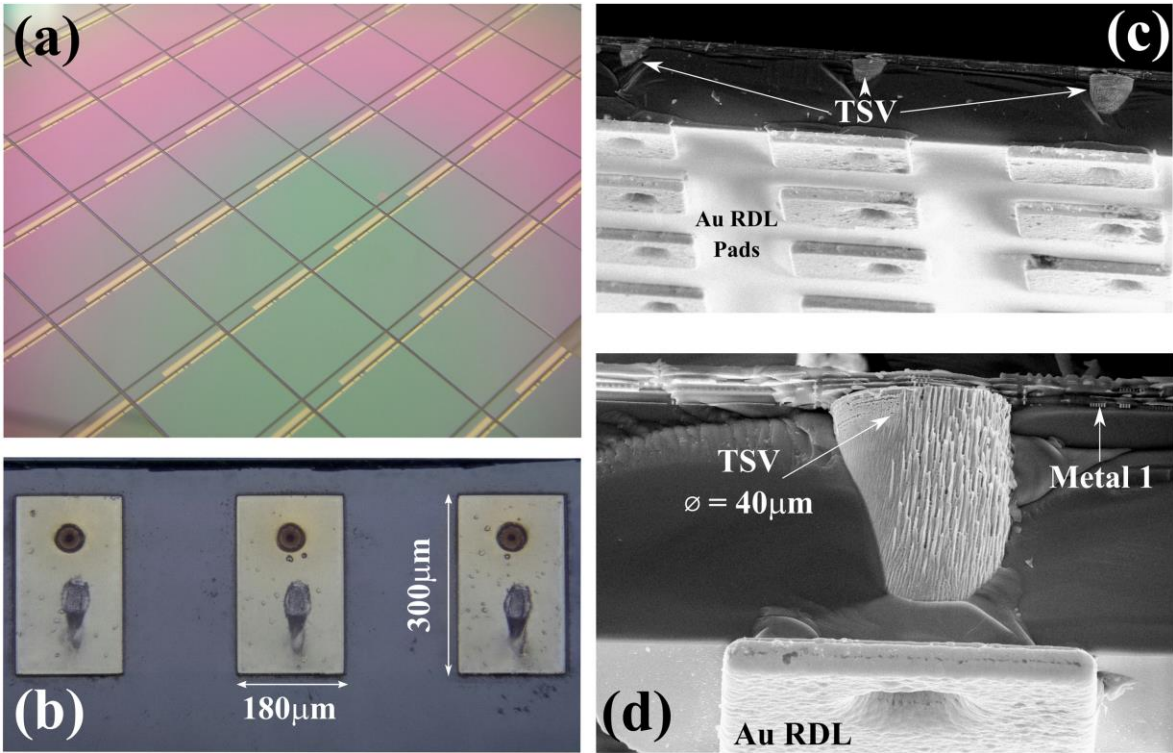


Fig. 2. (a) I/O pads on reverse of the 200 mm HEXITEC4S wafer post-TSV-last processing (b) RDL pads dimensions on ASIC's reverse. (c) SEM micrograph of exposed TSVs in cleaved test chip. (d) SEM micrograph showing contact between TSV and ASIC's bottom metal layer.



Characterisation of the HEXITEC_{4S} X-ray spectroscopic imaging detector incorporating through-silicon via (TSV) technology

M.C. Veale^a, P. Booker^a, I. Church^a, L.L. Jones^a, J. Lipp^a, A. Schneider^a, P. Seller^a,
M.D. Wilson^a, I. Chsherbakov^b, I. Kolesnikova^b, A. Lozinskaya^b, V. Novikov^b, O. Tolbanov^b,
A. Tyazhev^b, A. Zarubin^b

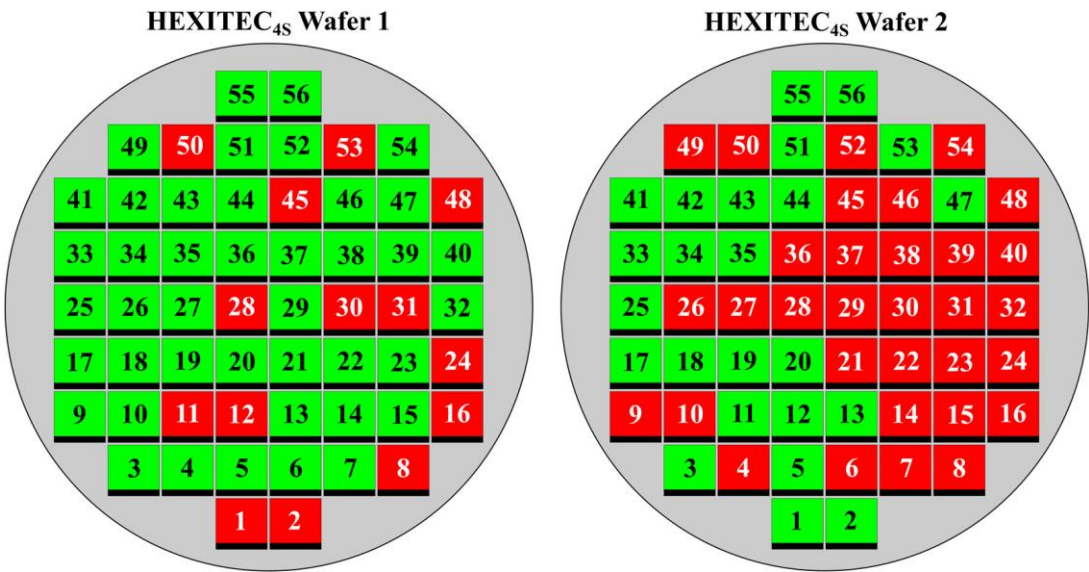
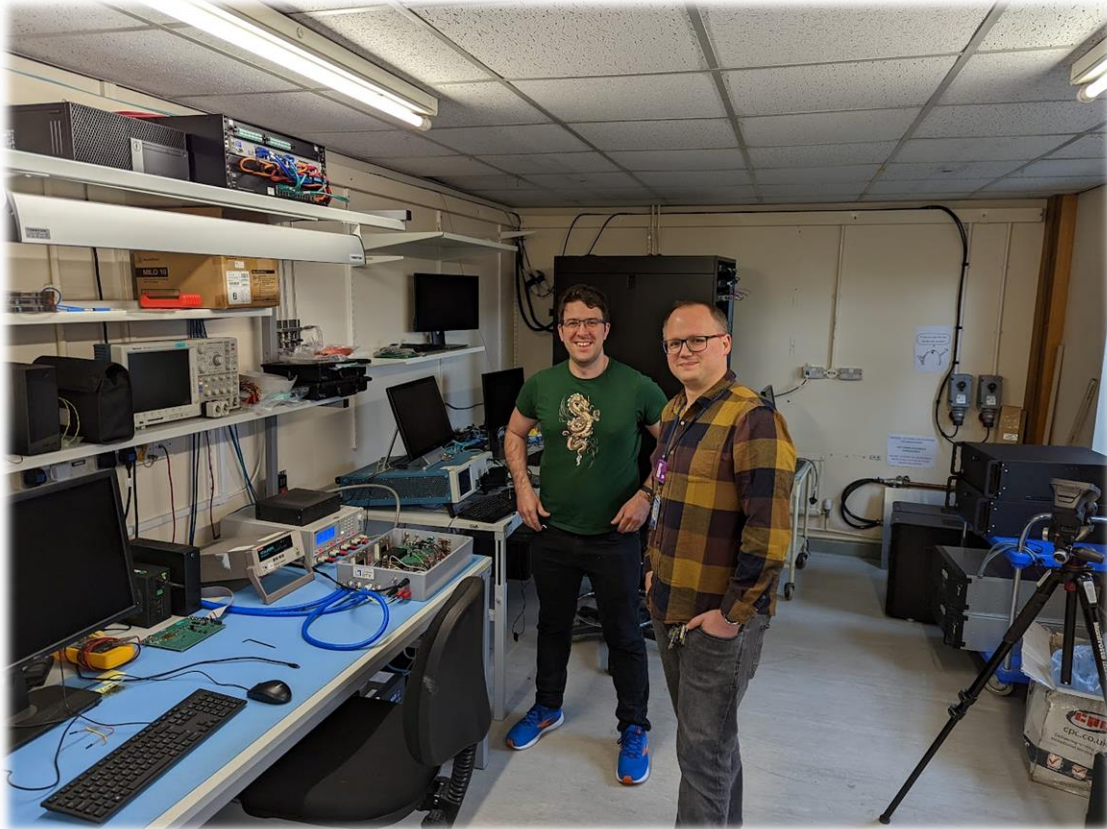


Fig. 4. Wafer maps showing results of probe testing. Green – functioning; Red – non functioning

Next steps – Current Applications

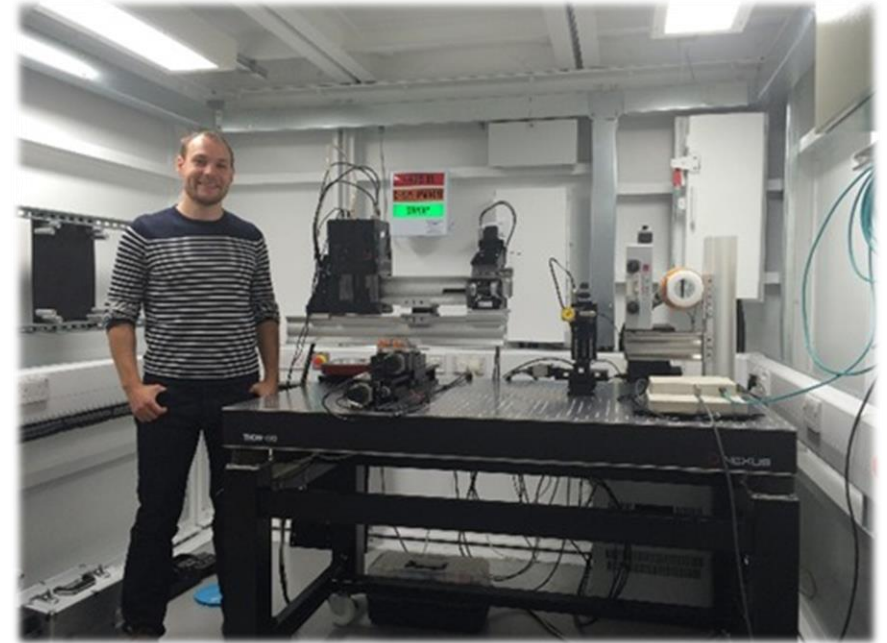
MIC-12-434: *On the feasibility of using HEXITEC_{MHZ} and fully-spectral x-ray imaging to detect breast tumours: an in-silico study*



The **ROYAL MARSDEN**
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ICR The Institute of
Cancer Research

New Project: 5DCT – *Dynamic Colour X-ray
Computed Tomography*



NXCT | National X-Ray
Computed
Tomography

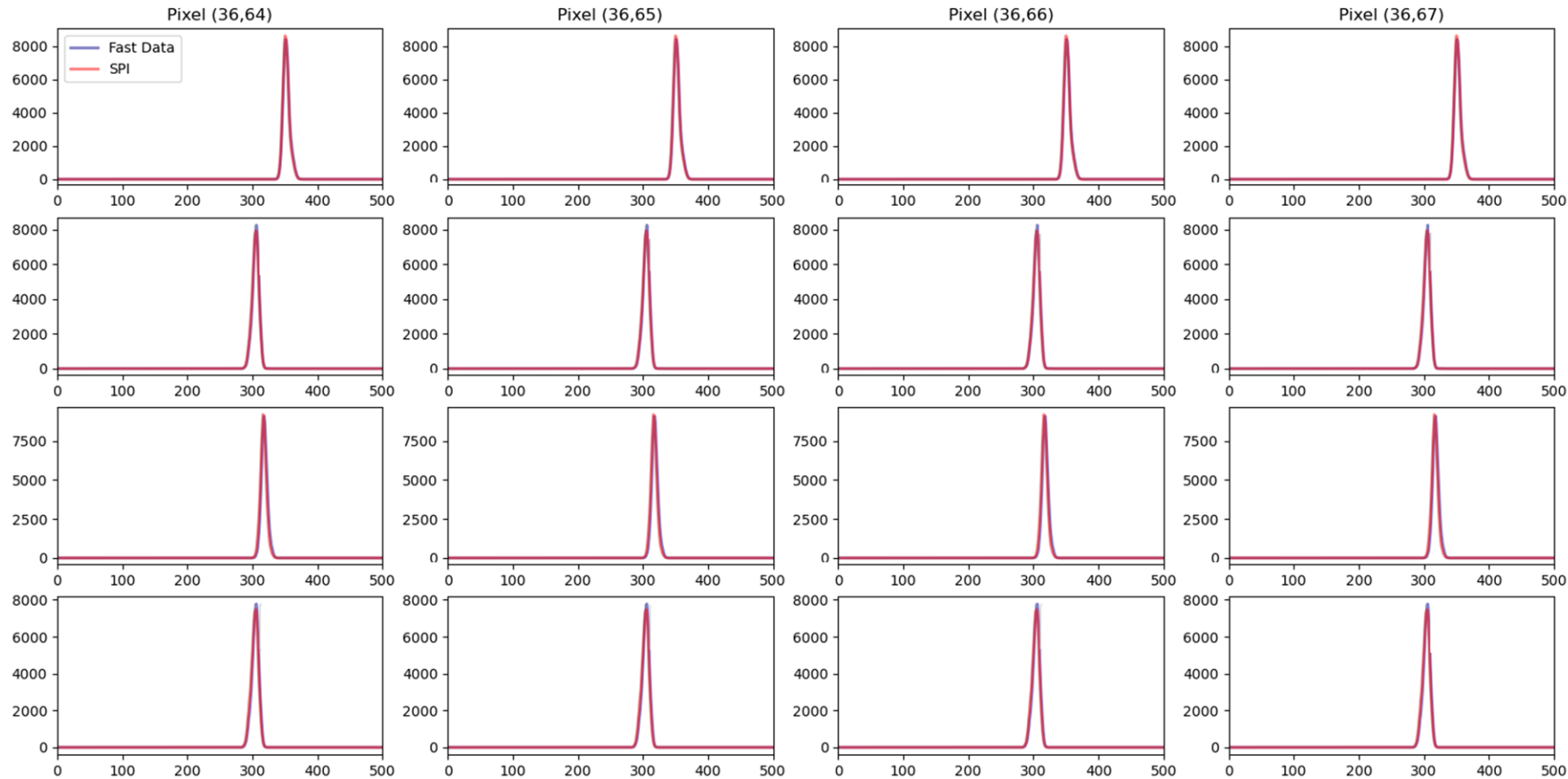


Department for
Business, Energy
& Industrial Strategy



Biotechnology and
Biological Sciences
Research Council

Testing – SPI vs Fast Data Comparison



Comparison of fast data and SPI measurements using test pulse

Fast data matches SPI output 😊