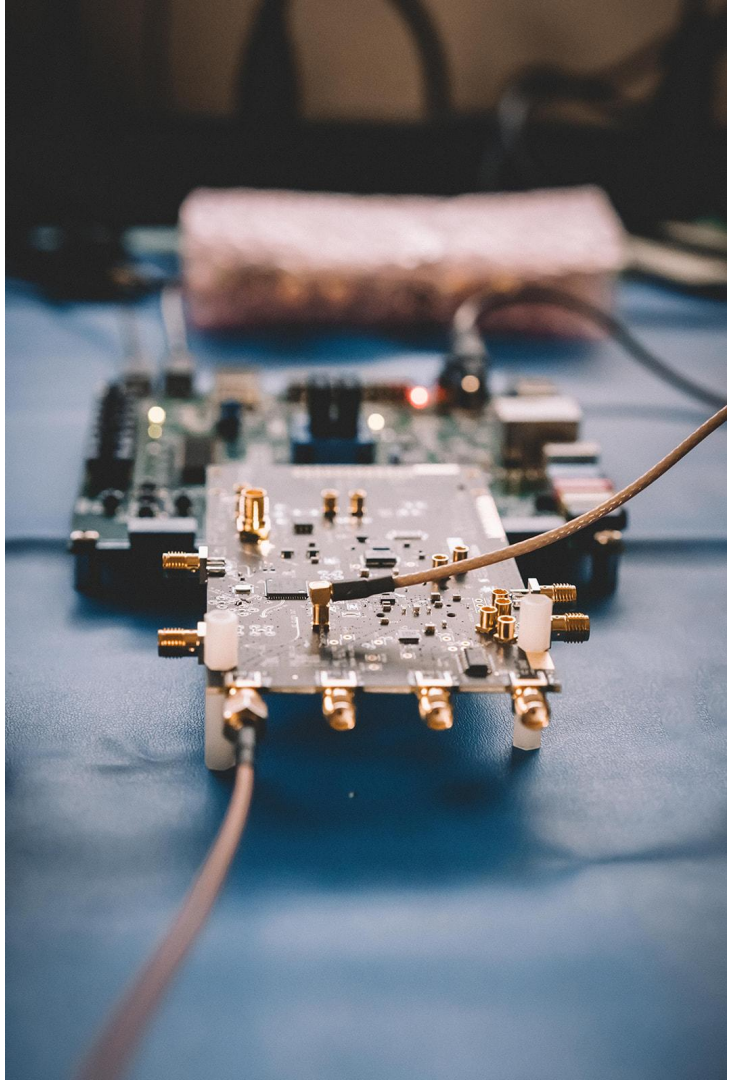

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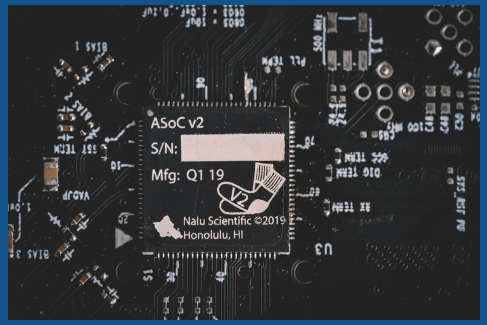
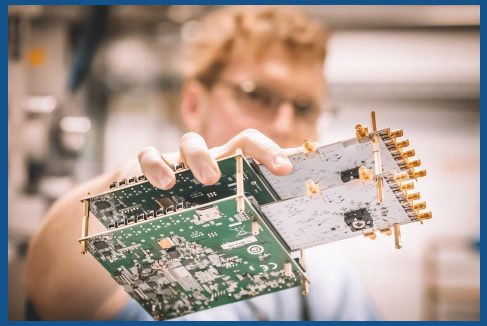
Test and qualification of the UDC: a 10 GSa/s, 16 channel digitizer system on a chip for fast plasma imaging applications

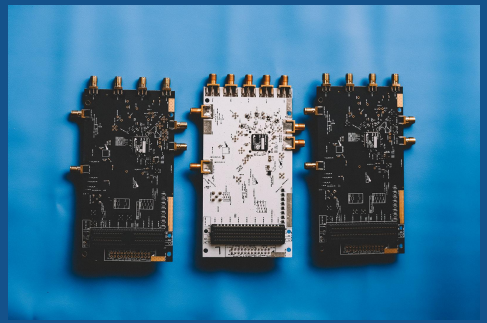
Isar Mostafanezhad
Founder and CEO
isar@naluscientific.com
Ulitimia 2023 - SLAC

Acknowledgements: US DOE, UCSC, UH, Sandia

Work partially funded under DOE DE-SC0019790, DE-SC0021785 SBIR awards.







ABOUT NALU SCIENTIFIC

Agile Small Business in Honolulu, Hawai'i

- Located at the Manoa Innovation Center near U. of Hawaii
- 20 staff members: 7 PhDs, 5 MSc, 8 BSc
- Access to advanced design tools
- Rapid design, prototyping and testing

Technical Team:

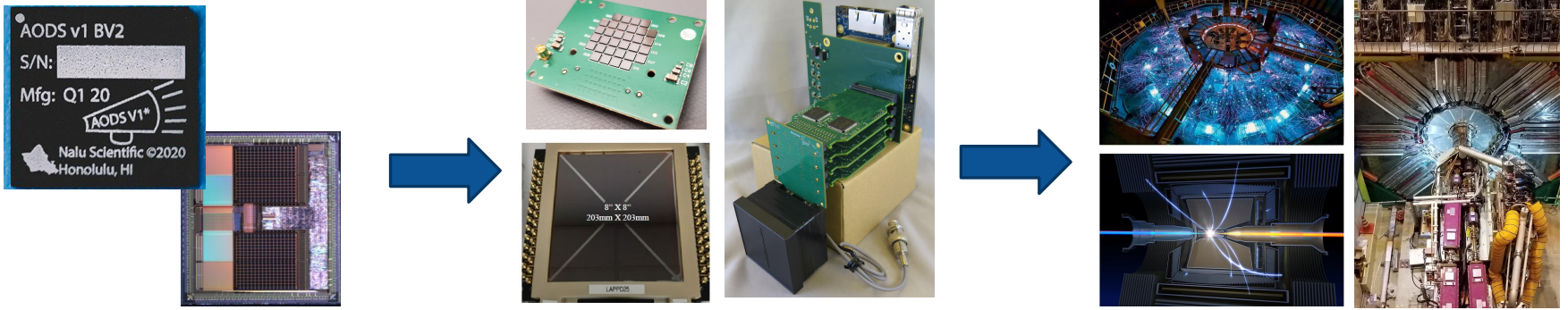
Microelectronics	Analog + digital System-on-Chip (SoC)
Hardware	Complex multi-layer PCBs
Firmware	FPGAs, CPUs, Embedded
Software	Data science, GUI, documentation
Scientific	Plasma, medical, physicists, space

Exclusive Distributor Agreement for North America CAEN Technologies Inc.

- Sales of ASICs, eval boards
- Enhanced OEM opportunities

Nalu = 'wave' in native Hawaiian language

WAVEFORM DIGITIZER SoCs
For Precision Fast Timing Applications



1. Front-end Chips:

- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP-C
- User friendly: FW/SW tools

2. Integration:

- SiPM
- PMT
- LAPPD
- Detector arrays

3. Applications:

- NP/HEP experiments
- Astro particle physics
- Beam Diagnostics
- Plasma/fusion diagnostics
- Lidar
- PET imaging

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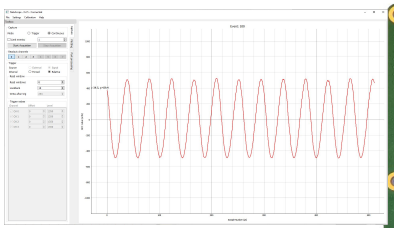
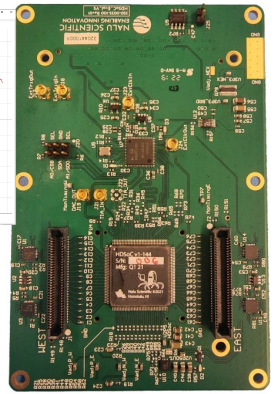
Current ASIC Projects

Project	Sampling (GHz)	BW (GHz)	Buffer (Samples)	Number of Channels	Timing Res. (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoC	1-3	0.6	2k	64	80-120	Rev 1 avail
AARDVARC	8-14	2.2	16k	8	10	Rev 4 avail
AODS	1-2	1	8k	1-4	100-200	Rev 2 avail
UDC	8-10	1.5	4k	16	10	Rev 1 avail

- DOE Phase I/II SBIRs
- Low SWaP-C specialty digitizers for
  - Radiation detection
  - Photonic sensors
  - Time of Flight (ToF)
  - Medical imaging
  - Space
  - Rad hard and harsh
- Evaluation PCBs available
- Extensive suite of software tools
- All microchips and tools available through CAEN Technologies USA

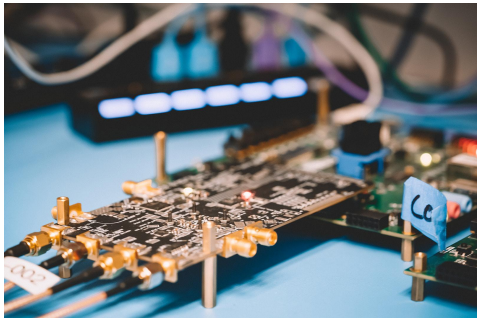


Software



Eval PCB

Microchips

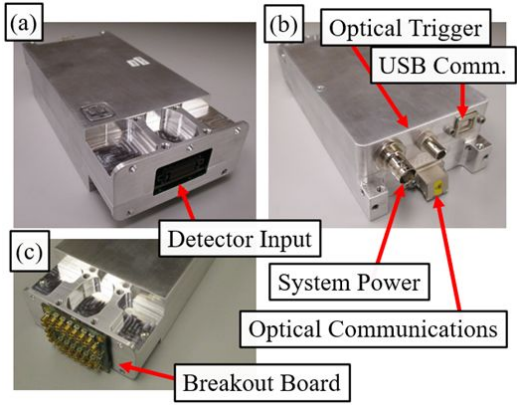


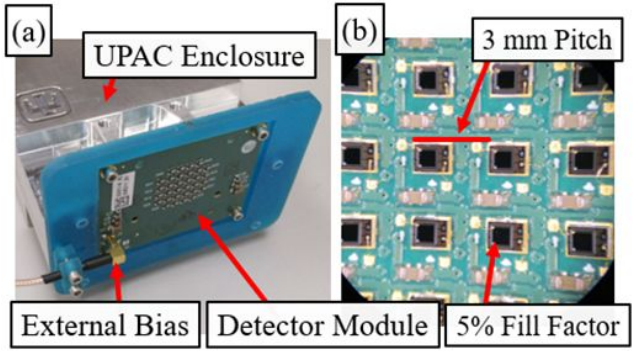
Motivation

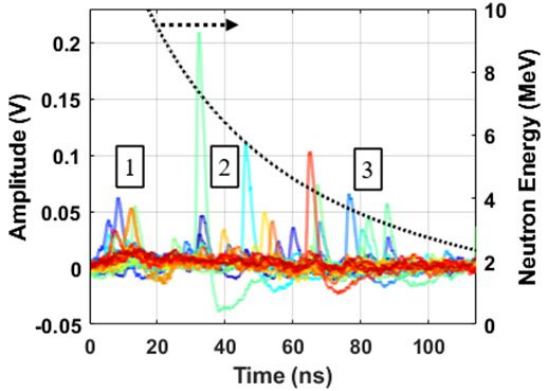
- High-Energy-Density Laboratory Plasma (HEDLP) science: understanding high-density plasma general science and Inertial Fusion Energy
- Benefit of high-channel count solid-state detector arrays for plasma diagnostics.
- Available waveform digitizers @ speed: large physical size, high cost, and difficulty in integrating into existing facilities.
- Detector signals are fast analog pulses: <1ns rise time and duration of 50ps-1ns.
  - sampling at over 10GSa/s,
  - analog bandwidth of over 2.5GHz
  - record length in the order of 100s of nanoseconds.
- Many channels (100s to 1000s)
  - Compact
  - Low cost

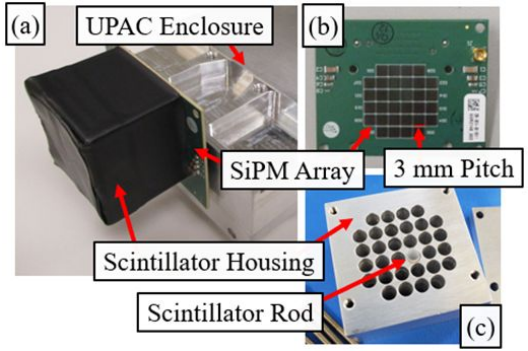
Ultrafast Pixel Array Camera (UPAC)

- UPAC 32: 32 channel 10 GSa/s compact DAQ based on **PSEC4A**
- Applications:
  - Solid-state streak camera,
  - Ultrafast imaging array
  - Neutron time-of-flight spectrometer
- Under test at Sandia
- Next generation:
  - Must be based on commercially available chips: **UDC**
  - 100-400 channels
  - Same form factor









Quinn Looker, et al: The Ultrafast Pixel Array Camera System and its Applications in High Energy Density Physics Review of Scientific Instruments 93, 074702 (2022); https://doi.org/10.1063/5.0091824 (**Editor's Pick**)

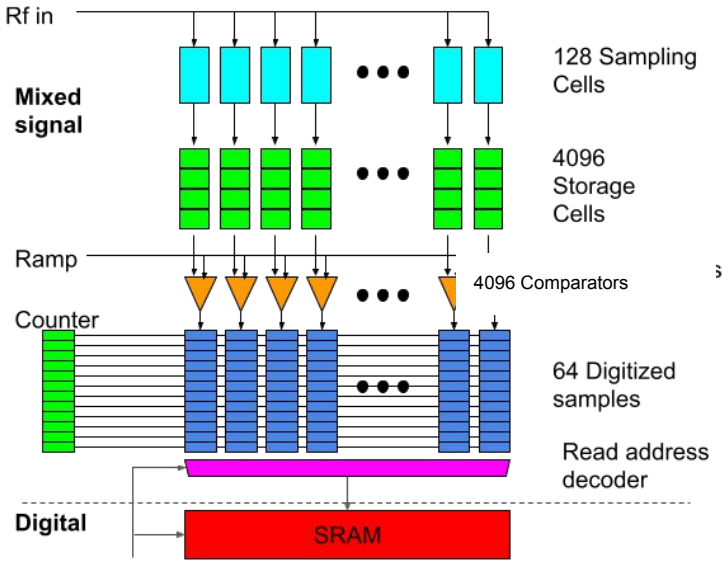
UPAC Digitizer Chip (UDC) concept and design specs

- Custom asic to cover the requirements:
  - Cannot use traditional continuous ultra-high-speed ADC due to power/density/cost requirements
  - "On demand" digitization - stores full waveform in analog form (using switched-capacitor (S-C) arrays and converts only after trigger - ideal for "one-shot" or relatively low rate experiments
- General features
  - Digitization of 16 channels
  - Sampling rates up to 10 Gsps
  - Relatively mature technology (reasonable prototyping costs): standard 130 nm CMOS
  - Long recording length per channel (4096 samples)
  - On-chip digitization
  - Internal storage of full digitized signal
  - Simple serial interfaces for configuration and readout
  - Derived from chip (AARDVARC) on smaller channels and higher record length developed for HEP applications (proven components)

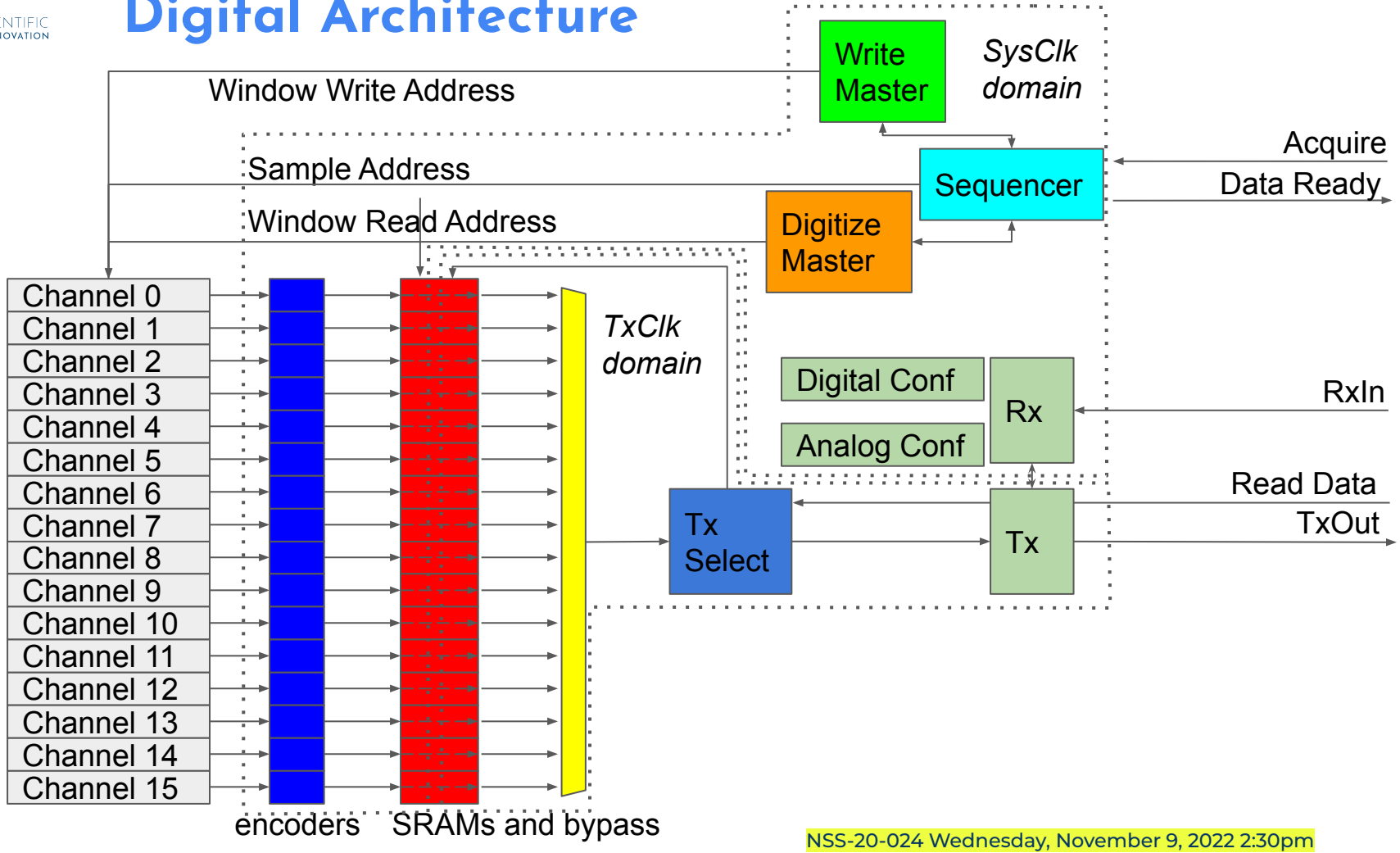
Parameter	UDC
Channels	16
Sampling Rate	Dual: ● <1 Gsps ● 7-11 Gsps
ABW	1-2 GHz (under evaluation)
Samples/channel	4096
On-chip digital storage	Yes
ADC bits (not ENOB)	10
Die size	~6.4mm x ~4.5mm = 28.8 mm^2
Package	QFN64 (9x9)
Output IF	Serial or parallel, polled or streaming
Trigger out	Yes
Self Triggering	No
Input amplifier/buffer	No

Channel structure and operation

- Channel operation:
  - **Sampling**: continuously at 10GSa/s rate,
  - **Storing**: keeping a buffer of 4096 samples;
  - **Triggering**: stops sampling, and digitizes
  - **Transmitting**: the data is packetized and sent via (selectable) parallel or serial interface.
- Channel architecture
  - **Sampling array :** 128-cell S-C that continuously samples at 10GSa/s,
  - **Storage array:** 4096 S-C array where samples are copied in groups of 64
  - **Timing generator** providing all strobes for sampling and transfer
  - **Wilkinson ADC:** composed of:
    - *Comparator* (in storage cells)
    - *Ramp generator* and *counter* (shared)
    - *Converted sample registers* (64)



Digital Architecture



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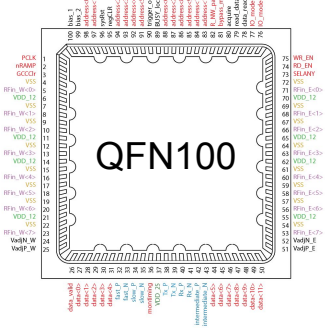
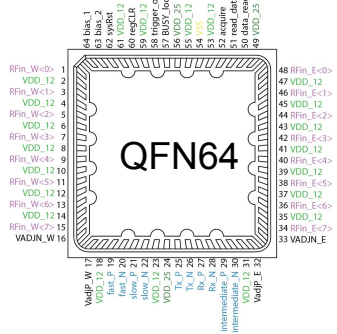
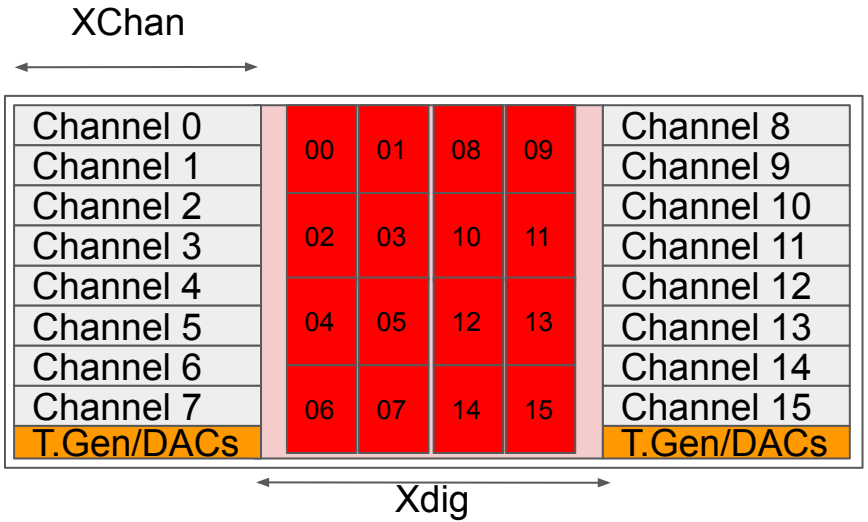
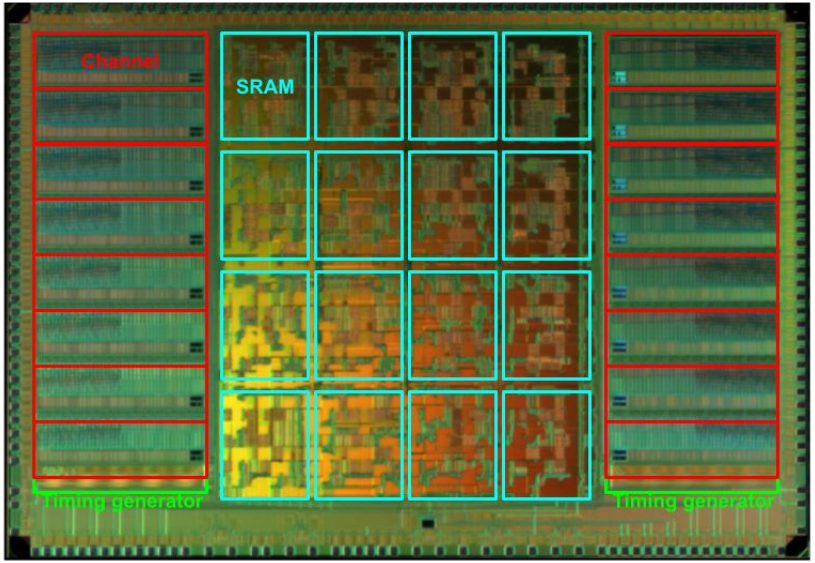
UDC Floorplan and Size

- X values:
  - Xchan: ~1.5mm (x2)
  - Xdig = ~3.0 mm - most space on SRAMs!
- Ydie = 4.3 mm
- Xdie = 6.2 mm
- Total area: 26.6mm^2









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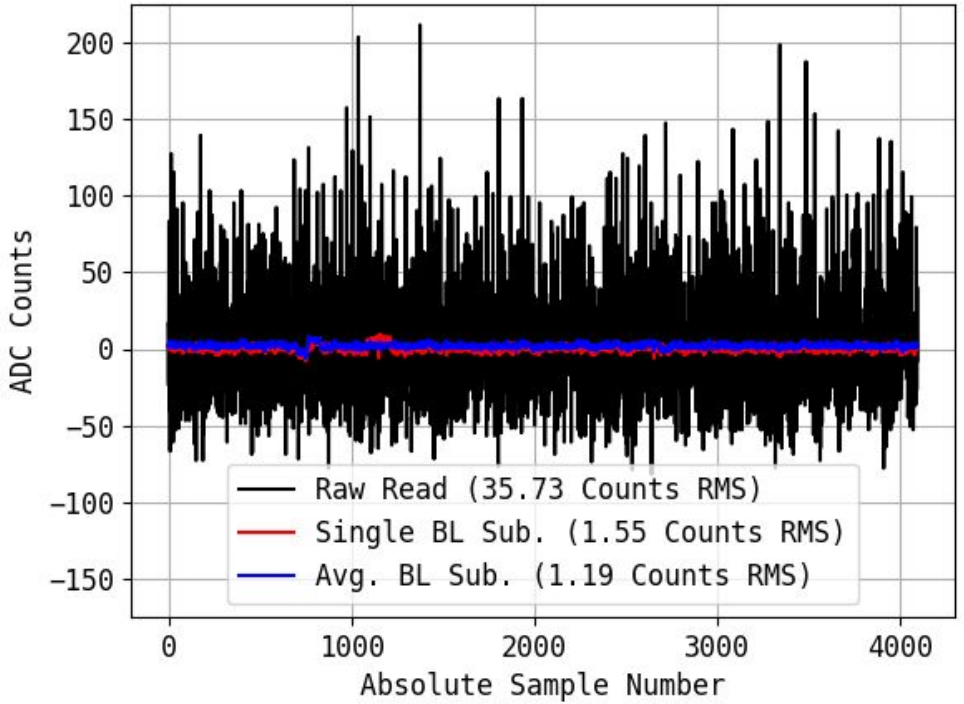
DC calibration - pedestals

- Due to the non idealities among the different sample circuits (especially comparator offsets), digitized values require voltage calibration:
- After calibration a residual of **1.19 ADC counts** remains (in this example) Using slope from DAC sweep - see later - average baseline subtraction yields **~0.84mV RMS**



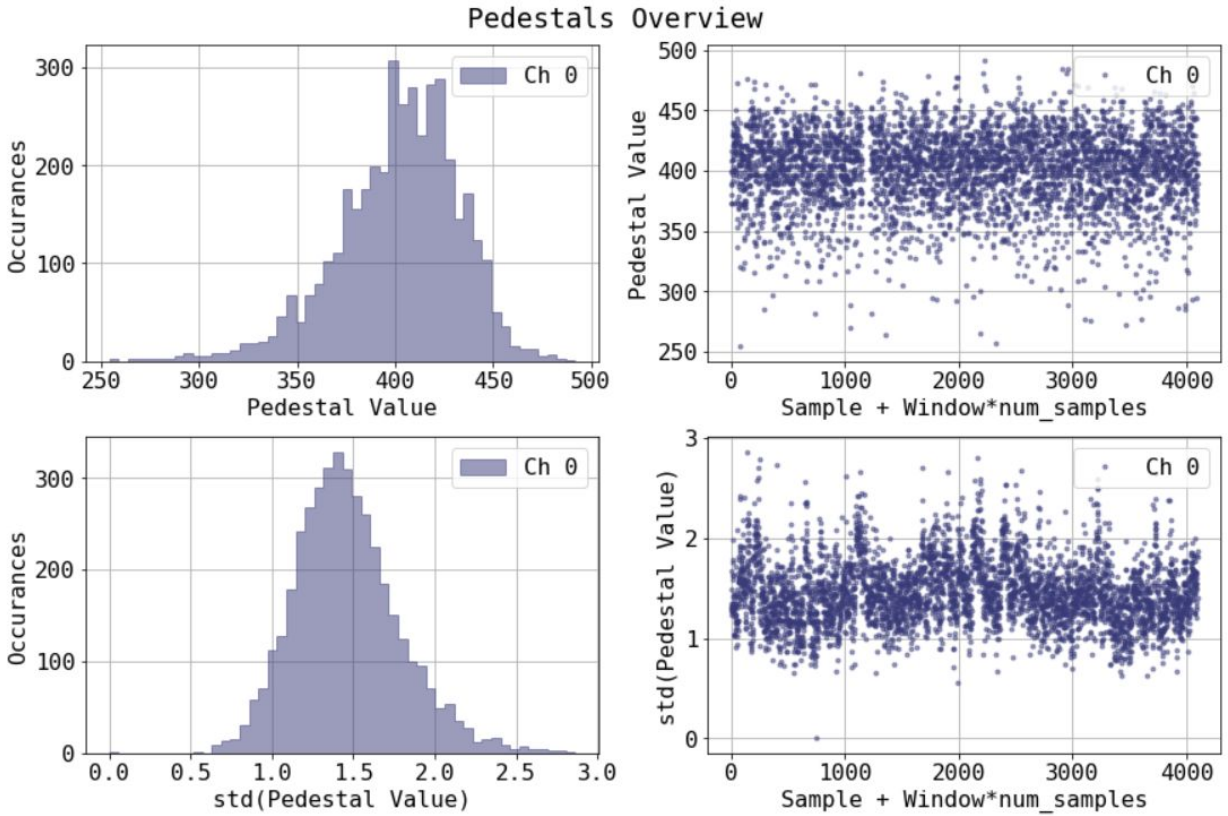
Raw read: pedestal variation of a single capture; common DC subtracted

Single subtraction: another capture subtracted from original capture

Average subtraction: average of remaining (19) captures subtracted

Pedestal statistics

Typical single channel pedestal distribution and standard deviation
Note that the average RMS error is less than **1.5 counts** - resulting in around **8.5 bits** accuracy in DC.



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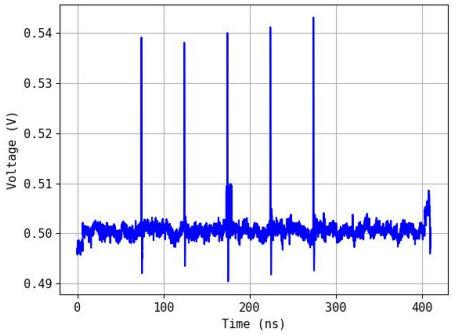
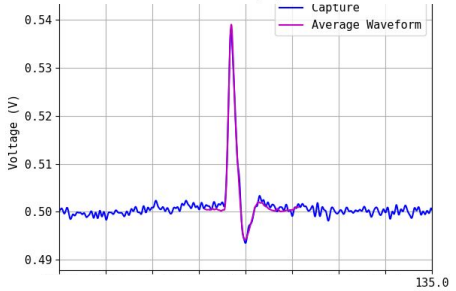
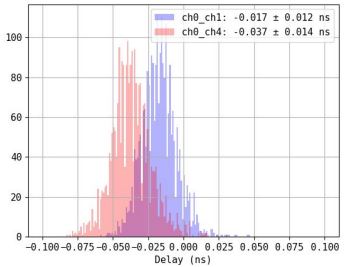
Channel timing evaluation

Multiple pulsed are generated to estimate timing accuracy:

- Interval between pulses is defined by passive delay.
- Interchannel and intra-channel timing between channels and/or different pulse used to estimate timing RMS without and with calibration.
- Average waveform collected by averaging 5ns region around 500 first waveforms (upsampled by factor of 100)
- Average waveform correlated with each capture and maximum correlation around waveform regions used to find a delay ch0 delay subtracted from comparison channel (ch1/4) to get inter-channel delay
- Channel pairs should low time jitter (A little over **10ps)**
- We expect these numbers to be confirmed or improved in all conditions after timing calibration

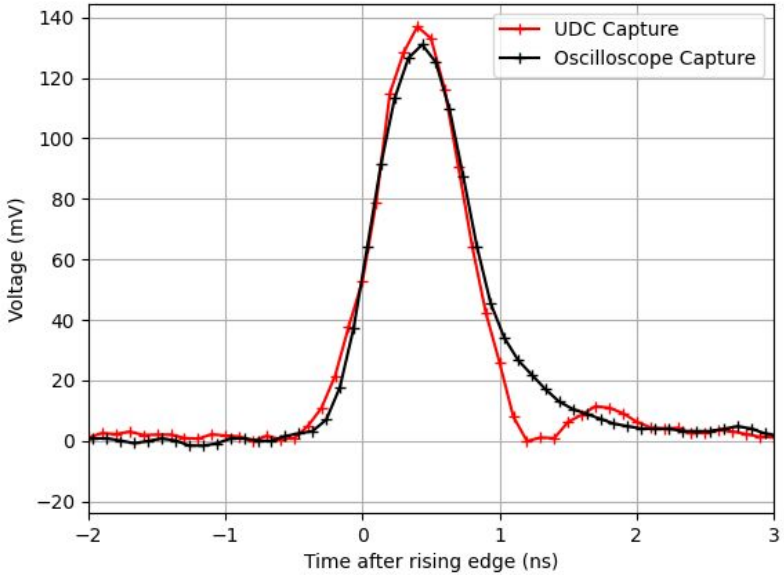






NSS-20-024 Wednesday, November 9, 2022 2:30pm

Example of sensor acquisition



Fast laser-excited photo-diode signal captured by the UDC microchip (red) and fast oscilloscope (Tektronix 2 GHz, 10 GSa/s, DPO 5204B oscilloscope) showing good match on the overall shape and rising edge of the pulse.

UDC v1 issues and plans for v2

UDC v1 was primarily designed for function hence some performance issues:

- Power Consumption:
  - 35mW/ch
  - Complete power consumption model is being developed.
- Bandwidth
  - Initial design for 2 GHz, but measured ~1GHz.
  - Input buffer, better packaging in V2
- Modulation effect on continuous waveforms
  - Freq. dependent amplitude modulation observed on pure tones
  - Converging on an explanation and a fix for V2
- Switched-cap kick-back effect (well known)
  - Older samples are affecting new samples due to on-off switching on sampling array - Shows as a signal dependent step error
  - Solution: Add a buffer at chip input in V2
- ADC Code nonuniformity
  - Caused by crosstalk of clock signals
  - Better digital and mixed signal isolation in V2

UPAC96: Ultrafast Pixel Array Camera

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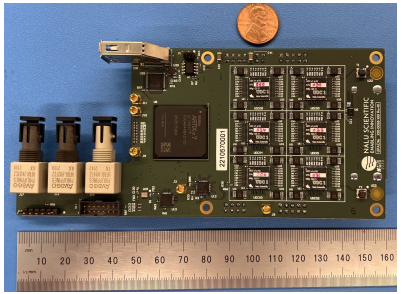
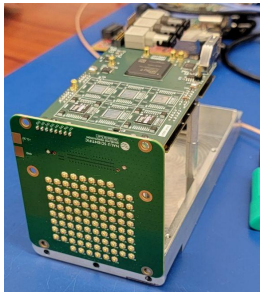
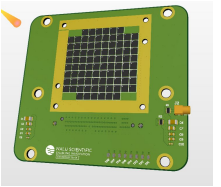
Product Name: **DSA E10-96**
Product Description: 96 channel, 10 GSa/s digitizer, 10b
Dimensions: ~ 12” x 4” x 1”
Bandwidth: ~1.2 GHz
Interface: USB 3/UART
Integration: chip, FPGA, clock, regulators, comm, FW, SW
Software: GUI, script, Python, analysis
Sensor (separate): Fast xray, SiPMs, fast diodes



UPAC 96 PCB



UFL breakout

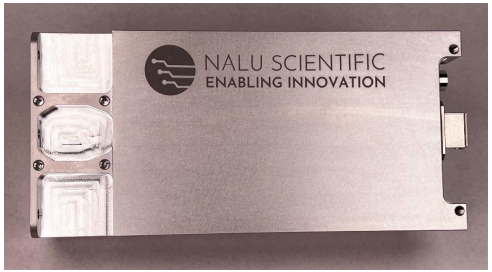


SiPM array

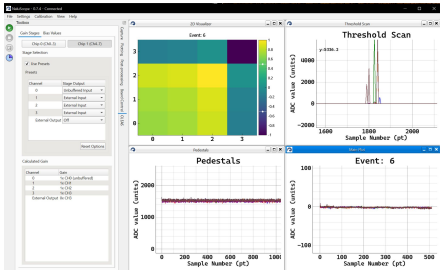
Designed and vertically integrated at Nalu Scientific

Under evaluation at Sandia

Main user: Fusion Energy Research at Sandia National Laboratory



Enclosure for harsh environments

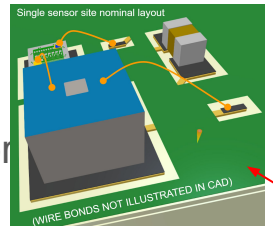


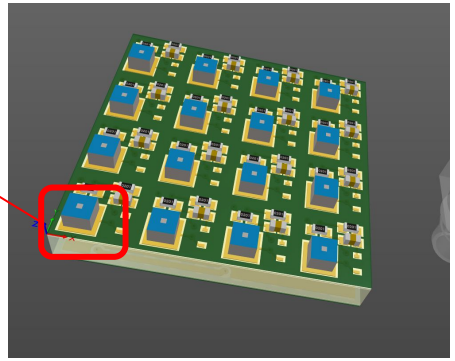
Software and analysis

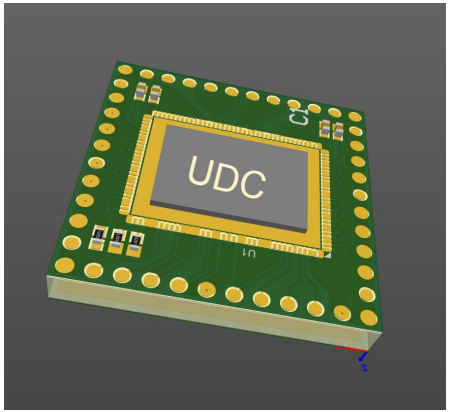
Funded by DOE Phase I/II SBIRs

WURP: Wideband Ultrafast Recorder for Plasma science

- WURP 1k:
  - ~1k pixels+readout in 10cm x 10cm x 3cm form factor
  - UDC: 10 GSa/s, 4k sample depth per pixel (400 ns recor length), 130nm CMOS, 5x5mm die size
  - Mini tile: 4x4 =16 pixels in 12mm x 12mm
  - Full tile: 8 x 8 mini tiles installed on a passive ridge type backplane PCB
  - Backplane: power, data, clock, trig
  - WURP 1k-v: more clearance on mini-tile sides for vacuum sealing
  - All standard COTS fabrication, bonding steps at reasonable cost.
  - Feasibility study: Mini Tile design final
- Next steps
  - Fabricate mini tile
  - Design and fab backplane
  - Test

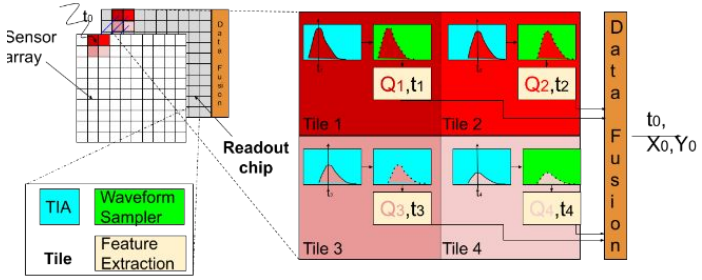


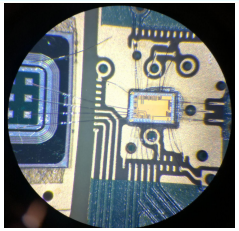


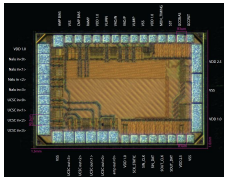


HPSoC: Fast Waveform Digitizer for Readout of Dense Sensor Arrays

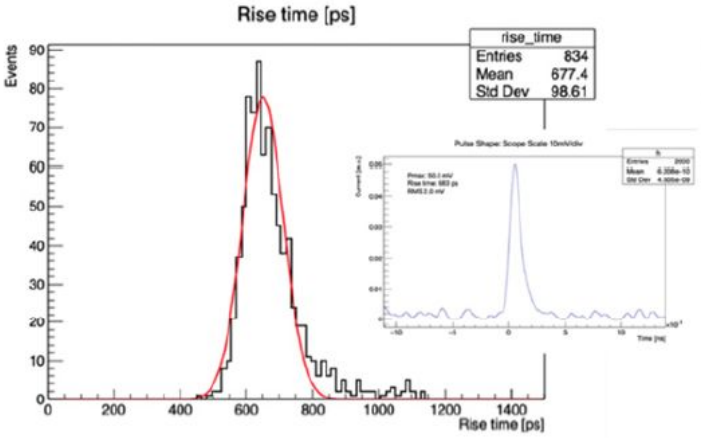
- 10 GSa/s Waveform Acquisition for Dense AC-LGADs
- Feasibility study:
  - Designed and fabbed 65nm test chip
  - TIA tested
  - Digitizer under test
- Collaboration with UCSC

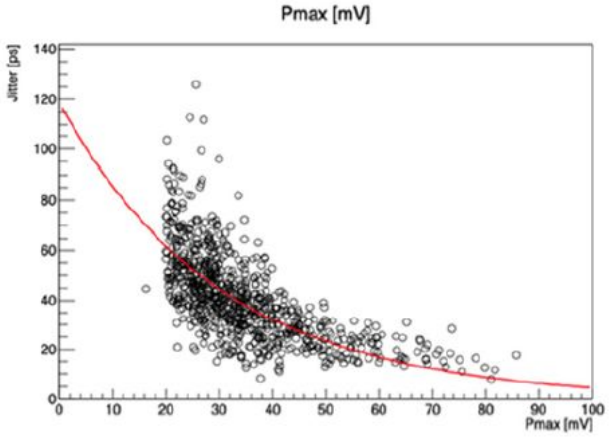






Parameter	Specification
Title Channel no.	100+ (pitch 300-500 µm)
Process	65nm CMOS
Sample rate	10 GSa/s
Bandwidth	2 GHz
No. bits	10
Supply Voltage	1.0V (2.5V for digital I/O)
Timing accuracy	5ps
Front-End stage	Embedded TIA
Buffer length/channel	256 samples
Power/channel	<2mW
On-chip integration	Sampling, Digitization, Calibration, Feature Extraction, Data Fusion





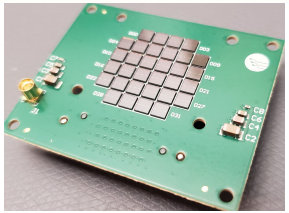
Chock - et al, First Test Results of the Trans-Impedance Amplifier Stage of the Ultra-fast HPSoC ASIC: https://arxiv.org/ftp/arxiv/papers/2210/2210.09555.pdf

Conclusions

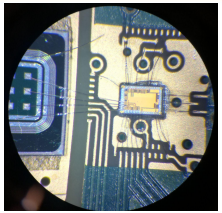
- UDC chip functional and satisfying most specifications
  - Sampling Rate
  - Timing accuracy
  - Negligible leakage effects
  - Reliable readout through serial interface
  - Small packaging possible
- A few limitations and anomalous effects investigated
- Multichip operation on 96 channel board demonstrated
- Preliminary analysis of potential re-design for performance enhancements:
  - Power reduction mechanisms (transfer control, digital SRAM clock gating)
  - Linearity improvements (error, range)
  - Input buffering for BW increase, kickback reduction.
  - Internal generation of all required clocks off single reference clock
  - Added flexibility in control (programmable sample readout, self triggering)

Summary

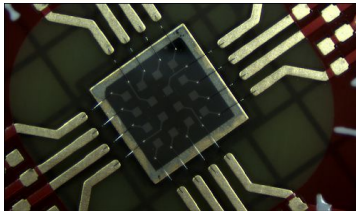
- **Products:**
  - Digitizer microchips
  - Hardware integration
  - Firmware and software
- **Services:**
  - Custom chip/HW design
  - Software and firmware design
  - Custom readout system development
  - Prototyping
- **Expertise:**
  - Electronics engineering
  - Radiation detection
  - Integration and testing
- **Collaborations:**
  - National Labs/ FFRDCs
  - Universities
  - Large Scientific Experiments



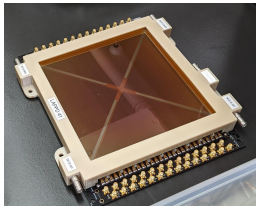
SiPM Arrays

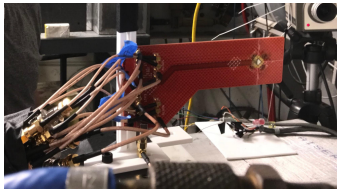


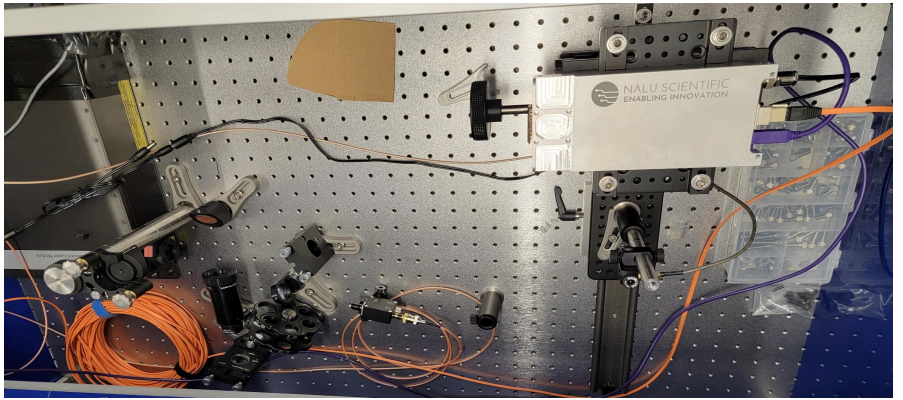
AC-LGAD readout



Diamond detector







UXI electronics production for Sandia