The monolithic ASIC for the high precision preshower detector of the FASER experiment at the LHC

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CERN - UniGe
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Outline

- The FASER Experiment
- The New Preshower Detector
- Detector ASIC
- Final Chip
- Tests & Results of the Preproduction Chip
- Conclusions
The FASER experiment at the LHC

- First operation Run 3!
- Location: 480 m from the ATLAS Experiment
- Designed to search for long-lived particles (LLP) produced at the LHC
- LLPs pass through the LHC infrastructure/rock without interacting and will decay into visible Standard Model particles, detected in ForwArd Search ExpeRiment (FASER)
- Energy scale 100 GeV until few TeV
The current preshower detector

Two Fermion signal

Two Photon signal

NO XY granularity
The new preshower detector

Independent measurement of two very collimated photons

Technical proposal of the new preshower detector of FASER
The goal of the new preshower detector

Our signal: 2 photons with 200 μm separation
- High granularity preshower
- Sample and reconstruct EM shower

- 6 Layers of silicon planes with tungsten layers in between
- Each silicon plane is divided by 12 modules
- Targeting data taking in 2024/25, during LHC run 3 and during HL-LHC
The new preshower detector: Simulation

Tungsten + Aluminum + Modules + Hexagonal Pixels
The new preshower detector: Simulation

PLANE 3

E1 = 1 TeV
E2 = 1 TeV
d = 500 μm

High dynamic range for charge measurement
The new preshower detector: Simulation

PLANE 4

E1 = 1 TeV
E2 = 1 TeV
d = 500 μm
The new preshower detector: Simulation

PLANE 5

E1 = 1 TeV
E2 = 1 TeV
d = 500 μm

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The new preshower detector: Simulation

PLANE 6

E1 = 1 TeV
E2 = 1 TeV
d = 500 μm
The new preshower detector: Simulation

PLANE 6

Why 6 planes? Why pixelated sensors?

Fake cores from low energy electrons

Very large occupancy
Monolithic ASIC architecture
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- First large-area monolithic detector in SiGe BiCMOS
- Chip size of 2.2 x 1.5 cm², with matrix of 208 x 128 pixels (26,624 total pixels)
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- Each SC has 8 Superpixels (SP)
- Each SP has 16x16 pixels
- 1 Digital Line in the middle of each SC

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- 1 Digital Line in the middle of each SC, in the middle (40 µm width), which is inactive
- Dead are in the periphery:
  - 720 µm on the readout side
  - 270 µm on the guard ring sides

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Monolithic ASIC: Sensor

- Monolithic ASIC in 130 nm SiGe BiCMOS technology from IHP microelectronics (design in collaboration between CERN, University of Geneva and KIT)
- The charge needs to be measured for each pixel: acts as an imaging device
- High-resistivity \( (220 \, \Omega \cdot \text{cm}) \) substrate, about 130 \( \mu \text{m} \) thickness
- Hexagonal pixels integrated as triple wells, pixel capacitance of 80 fF

<table>
<thead>
<tr>
<th>Main specifications</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel Size</td>
<td>65 ( \mu \text{m} ) side (hexagonal)</td>
</tr>
<tr>
<td>Pixel dynamic range</td>
<td>( 0.5 \div 65 , \text{fC} )</td>
</tr>
<tr>
<td>Cluster size</td>
<td>( O(1000) ) pixels</td>
</tr>
<tr>
<td>Readout time</td>
<td>(&lt; 200 , \mu \text{s} )</td>
</tr>
<tr>
<td>Power consumption</td>
<td>(&lt; 150 , \text{mW/cm}^2 )</td>
</tr>
<tr>
<td>Time resolution</td>
<td>(&lt; 300 , \text{ps} )</td>
</tr>
</tbody>
</table>
Monolithic ASIC architecture: Periphery and I/O

- The periphery interrogates the super-columns from left to right, and handles the chip I/O
- Two clock domains: 50 MHz (programming phase) and 200 MHz (readout phase)
- **Super-column level frame-based** solution for readout logic in the periphery
- Data are not stored in the chip, but they are sent out on the fly at 200 Mbit/s
Free running ring oscillator, measuring the period of the clock for every event to calibrate it!
Monolithic ASIC architecture: Super-columns

- All the logic is in the supercolumn!
  - Super-column logic: it **masks the pixels**, generates **the test-pulses**, drives the analog **MUX**, handles **readout** and **communication with periphery**
- Unusual aspect ratio digital line: 1.4 cm by 40 µm
Monolithic ASIC architecture: Super-pixel

- Data is stored on the capacitor in each pixel and **converted on the fly** with a flash ADC. 256-to-1 MUX
- The capacitor is charged with a constant current during the TOT
- The same ADC will poll all the pixels in a superpixel and convert them as needed
Monolithic ASIC architecture: Pixel

- **Analog memory** in pixel
- Low-power discriminator (inside the pixel area)
- **Memory control circuit** outside pixel
- Discriminator output activates the charging of the MIM capacitor
Pre-production prototypes

- Large area, fully functional prototype
- Three alternatives test layouts submitted
  - V1
    - 128 x 64 pixels, 4 supercolumns
    - In pixel pre-amp and driver
    - Discriminator outside
  - V2
    - 128 x 48 pixels, 3 supercolumns
    - In pixel pre-amp, driver and discriminator
  - V3
    - 128 x 48 pixels, 3 supercolumns
    - No analog memories
    - Counter for charge measurement

Tests started in June 2022!!
Pre-production prototypes

Pre-production wafers have arrived
• 3 standard wafers
• 53 chips / layout / wafer
Test on board & Design considerations

V2 first prototypes were bonded and are currently under test - they work!
Test with FAST-OR circuits: TOT mismatch

Analog: 0.7 µA / pixel

Analog: 2.3 µA / pixel
Simulation: TOT mismatch

Some mismatch observed from amplifier response: increase the size of preamplifier transistors
Test with FAST–OR circuits

Excellent timing performance for the entire range under test!

Analog: 0.7 µA / pixel

Analog: 2.3 µA / pixel

Preliminary
Test with Readout: testpulse calibration

Before calibration

After calibration

Injected charge

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Test with Readout: Calibrated laser response

The pixels were selected due to their large mismatch!
Conclusions

- A **new preshower detector** is being developed for the **FASER experiment** at the LHC
  - Enabling discrimination of ultra-collimated multi-TeV diphoton events from LLP decays
  - Chosen technology: 130nm SiGe BiCMOS MAPS designed and developed at UniGe
  - Installation in 2024, data taking during LHC Run 3 and High-Luminosity LHC
- **Preproduction chips delivered in June 2022**
  - Everything is working fine with lab characterization
  - Minor bugs have been identified and they are corrected
  - First assembled modules currently ongoing
- **Submission of final chip May 2023!**
The development and construction of the W-Si pre-shower of the FASER experiment was funded by the Swiss National Science Foundation (SNSF) under the FLARE grant 20FL21-201474 at the University of Geneva. Additional financial contributions from KEK, Kyushu University, Mainz University, Tsinghua University and the Heising-Simons Foundation are also acknowledged.
Thank you for your attention...!
Front-end & Memory control
The pedestal is time dependent and it disappears at low temperature, suggesting the presence of a current leakage. Moreover, the independence from the memory load current allowed to identify the issue as due to the leakage through the gates of the analog MUX.

A solution to this issue has been already implemented in the final chip.
HV test on probe station

Standard wafer

Internal ring not referred to ground

Scratch with needle

Epi wafer
The Detector effects code

Import and fit the Monte Carlo data from Cadence:

Sets of \((Q,V)\) pairs

\[ y = a + b(1 - e^{(x-d)}) \]

Apply random \(f_i\) to \(Q_s\):

\[ f_i(Q_s) = V_s \]

Add gaussian noise

\[ V_s \Rightarrow V_{sn} \]

16 equal bins in the range of \(V\)

\[ V_{sn} \Rightarrow V_f \]

\[ f_i^{-1}(V_f) = Q_{meas} \]

\[ Q_{meas_s}(x, y) \]
One Event - Hitmap - Chip 405 - 2 photons - 1 Tev each - 500 μm Distance - After the Detector Effects

Before the Detector Effects

After the Detector Effects
Readout information
Laser setup
One Event - Hitmap - Plane 6 - After Detector Effects - 2 photons - 2 TeV each
Simulation Software update – Neutrino Studies

Occupancy plot neutrinos

Plane 6
Neutrino interactions
GENIE file
0.5 fc thr

Occupancy plot photons

Plane 6
0.5 fc thr
2 photons
1 Tev each
Muons 1 TeV - Single chip - Threshold 0.5 fC

Occupancy Plot - Chip 405 on Plane 6

<table>
<thead>
<tr>
<th>Entries</th>
<th>1000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean</td>
<td>2.035</td>
</tr>
<tr>
<td>Std Dev</td>
<td>6.479</td>
</tr>
</tbody>
</table>
Motivations for the new preshower detector

- **Enables measurement:**
  - Axion-Like Particles (ALP) produced via $aWW$ coupling.
  - LLP with neutral pions in the final state.
  - Neutrino background suppression.

- **Reinforces measurement:**
  - Dark photon and other LLPs decaying into charged fermions.
  - LLP with charged and neutral pions in the final state.

Detector requirement: Discriminate photons with 200 µm separation to exploit the full potential of the experiment.