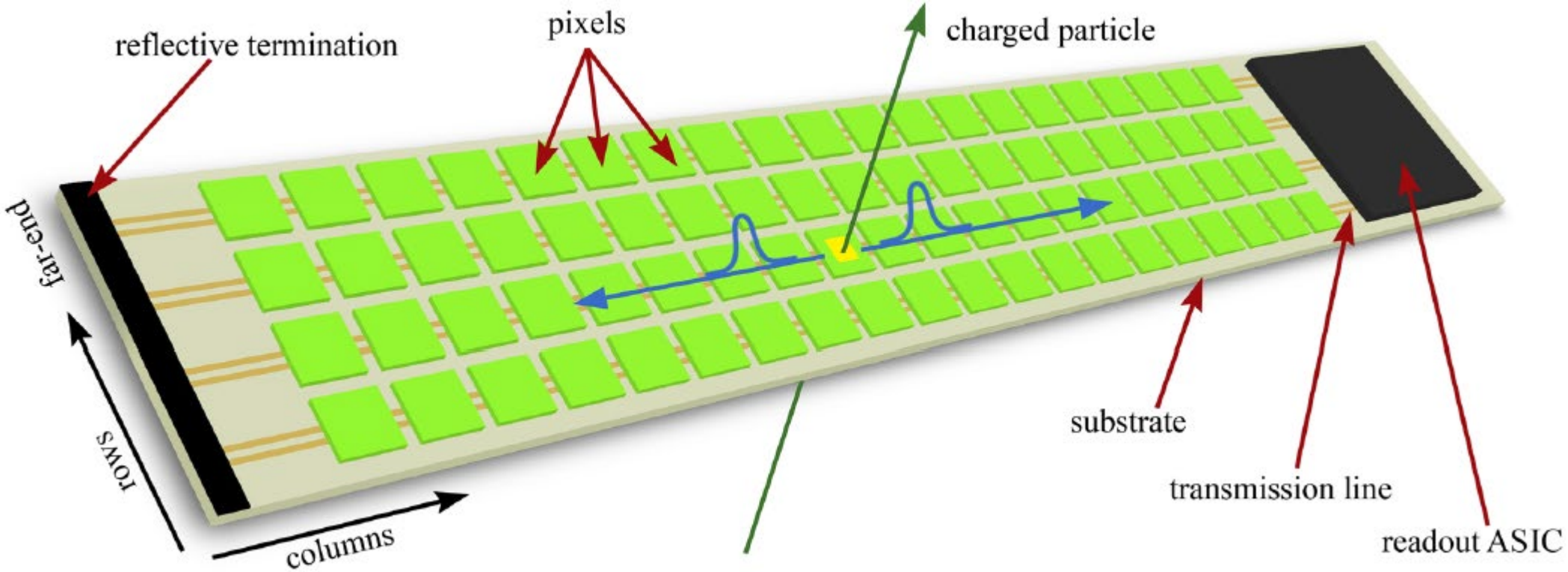
RadioFrequency Pixel (RFpix) Design Considerations for 65nm



Gary S. Varner

ULTIMA 2023
SLAC
14-MAY-2022

Peter Orel

Motivation

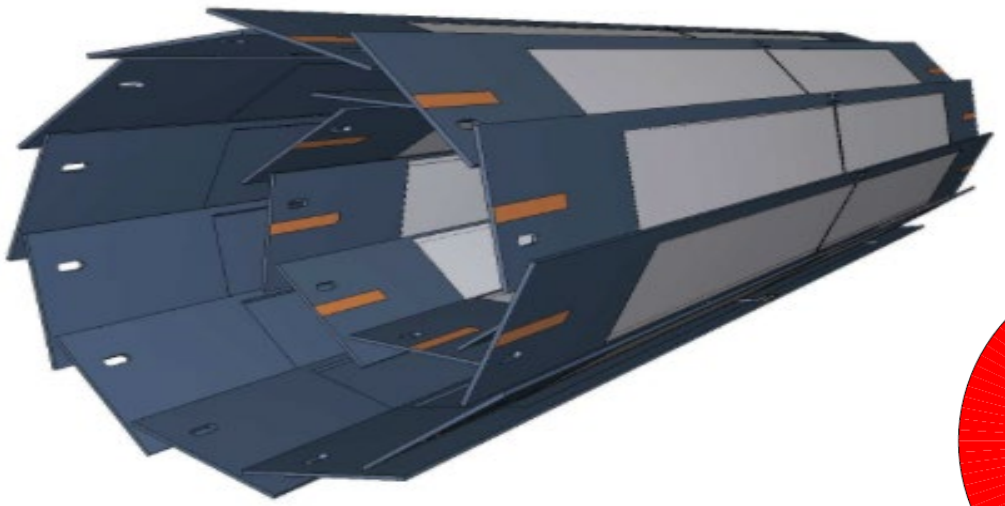
1. **Original studies in 130nm CMOS looked very promising**

2. **<u>Right at the margin</u> of what could be achieved in that process**

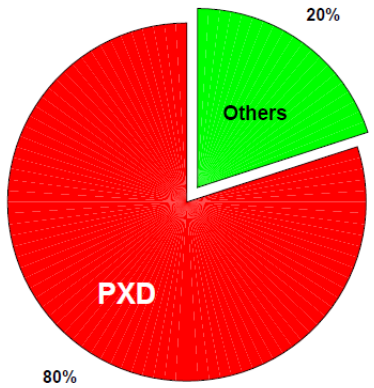
3. **Subsequently have learned some limitations in earlier modeling, interest in 65nm process**

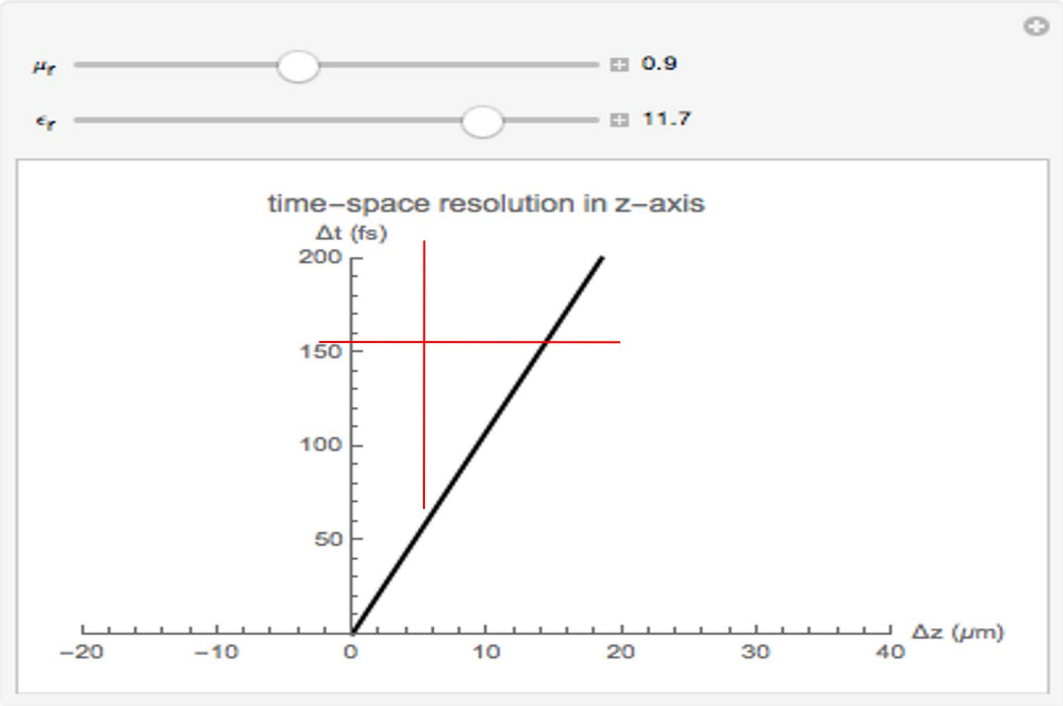
- 1. P. Orel, P. Niknejadi, G.S. Varner, "Exploratory study of a novel low occupancy vertex detector architecture based on high precision timing for high luminosity particle colliders," *Nucl. Instr. Meth.* **A857** (2017) 31-41.
- 2. P. Orel, G.S. Varner, "Femtosecond Resolution Timing in Multi-GS/s Waveform Digitizing ASICs," *IEEE Trans. Nucl. Sci.* **64** (2017) 1950 - 1962.

Context



DEPFET-based Pixel detector (PDX) for Belle II (SuperKEKB)





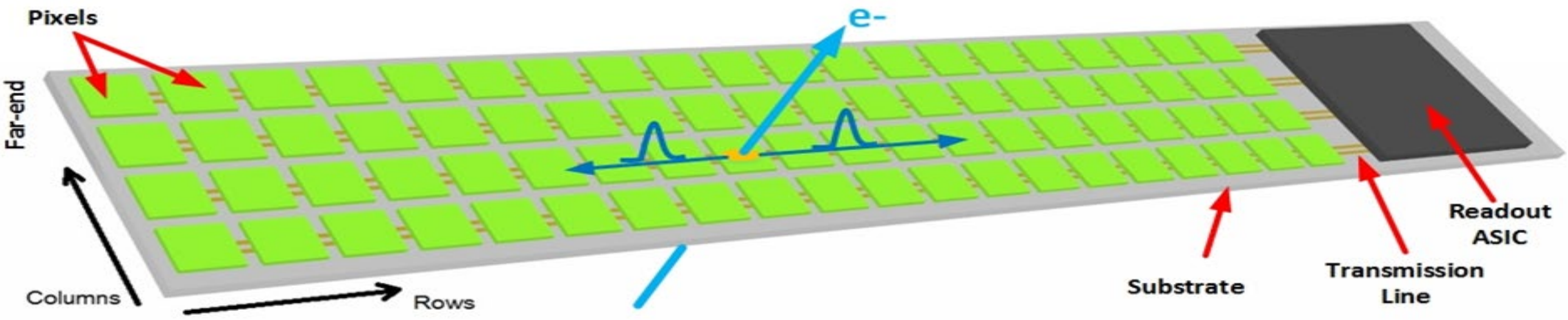
1. **Original motivation was to save a few M$/year in storage for Belle II (as largest component of event size is DEPFET pixels)**

2. **A *more generalized concept* is to use sub-picosecond timing to exchange one (or more) of the spatial dimensions at the *micron level* for timing**

What would it take?

3 key elements:

1) **Avalanche sensor element**
2) **Transmission (delay) line**
3) **Waveform sampling ASIC**

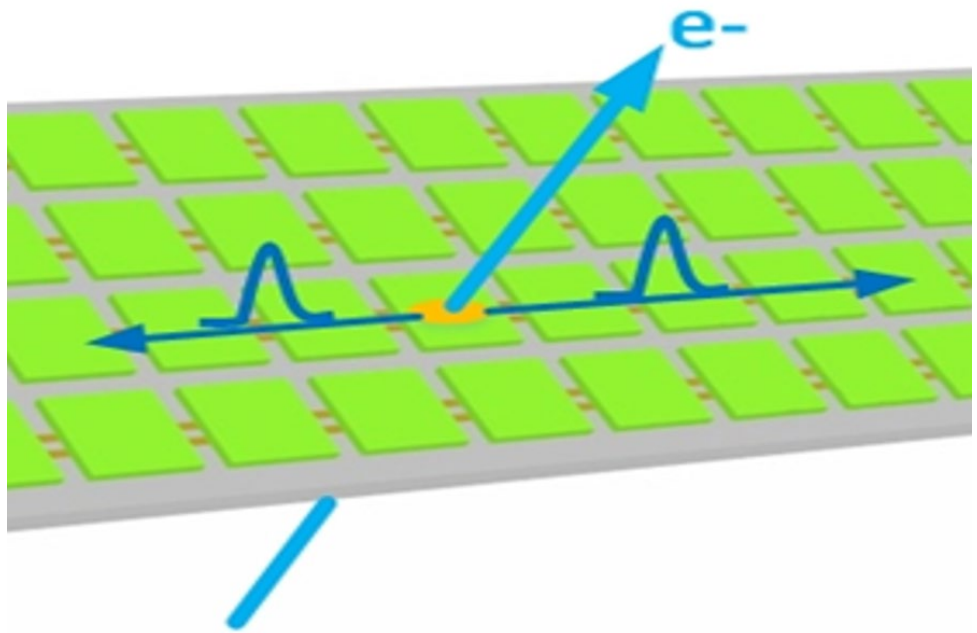


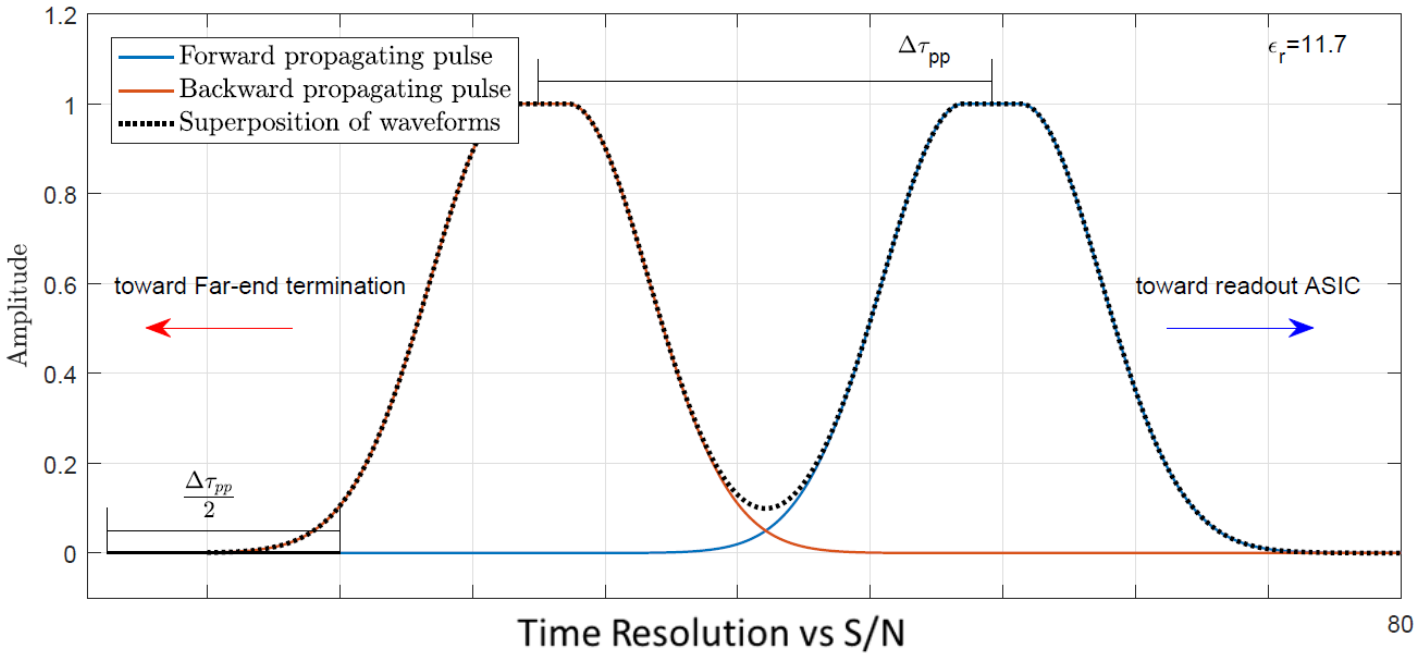
- Micron spatial pixel resolution (using timing)

→ Fast timing brings many benefits:

- *Minimal pile-up (fast clearing)*
- *Improved event timing (direct T0 for TOF/TOP measurements)*

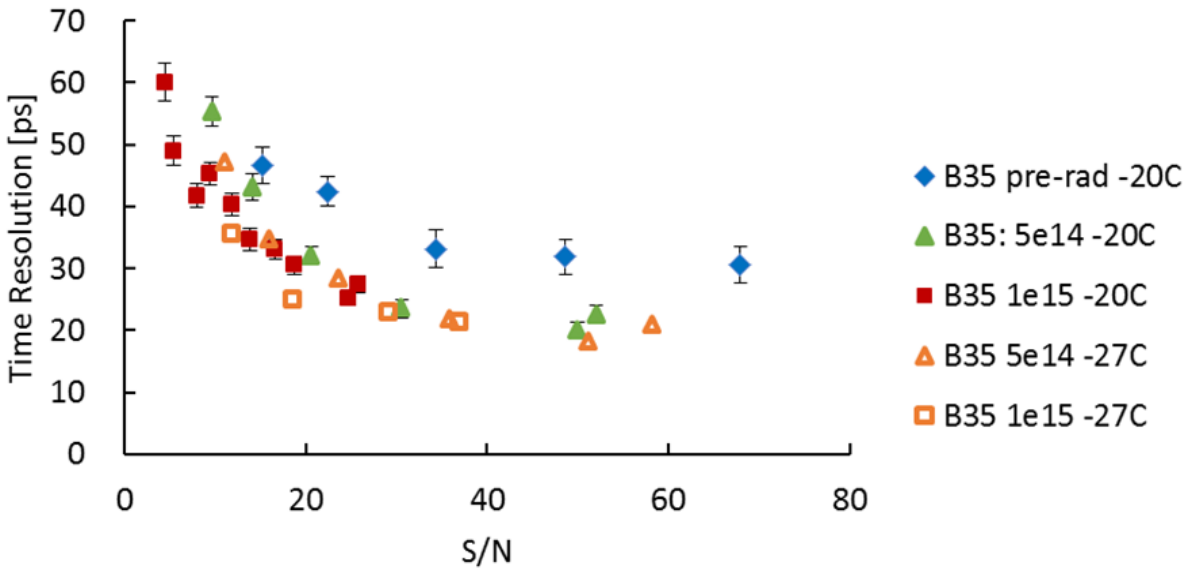
1) Signal Generation – coincident Geiger mode-devices? LGADs?



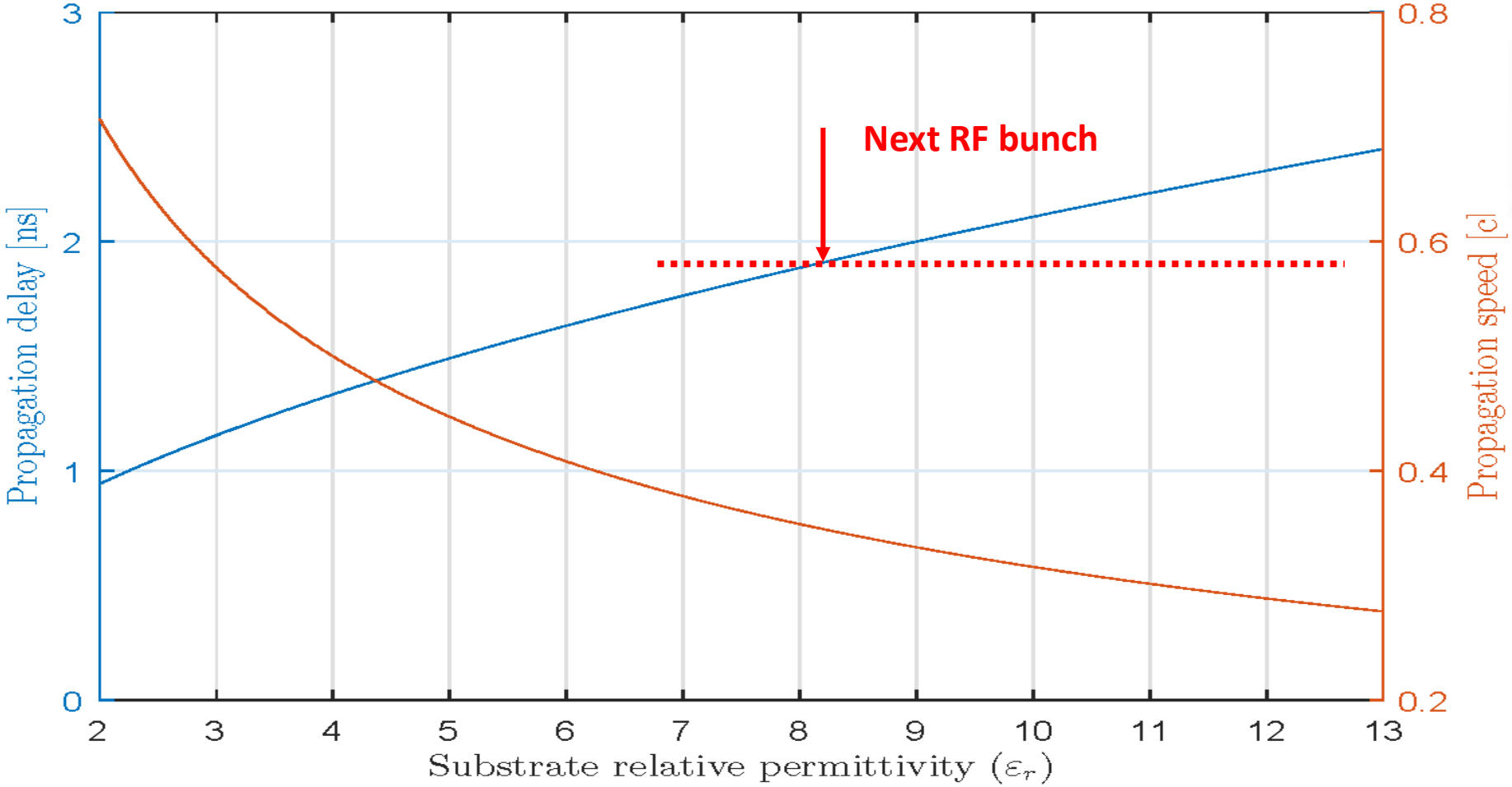


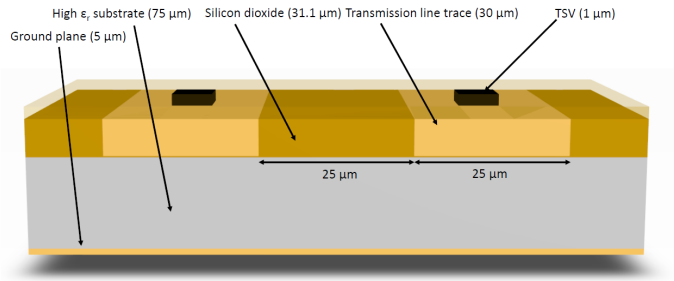
- **Mean time provides TOF**
  (perhaps **10's of ps**)
- **Time difference provides position**
  (**sub-ps** for micron-scale spatial)

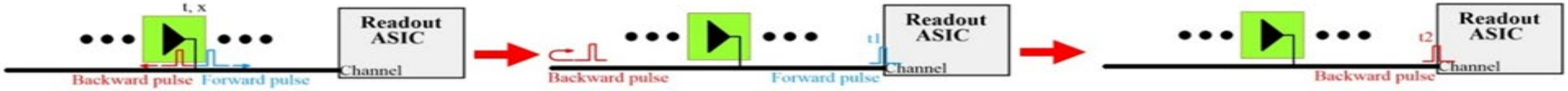
- **"initiator" circuit for clean signal launch**



2) Signal Propagation – tune transmission (delay) line

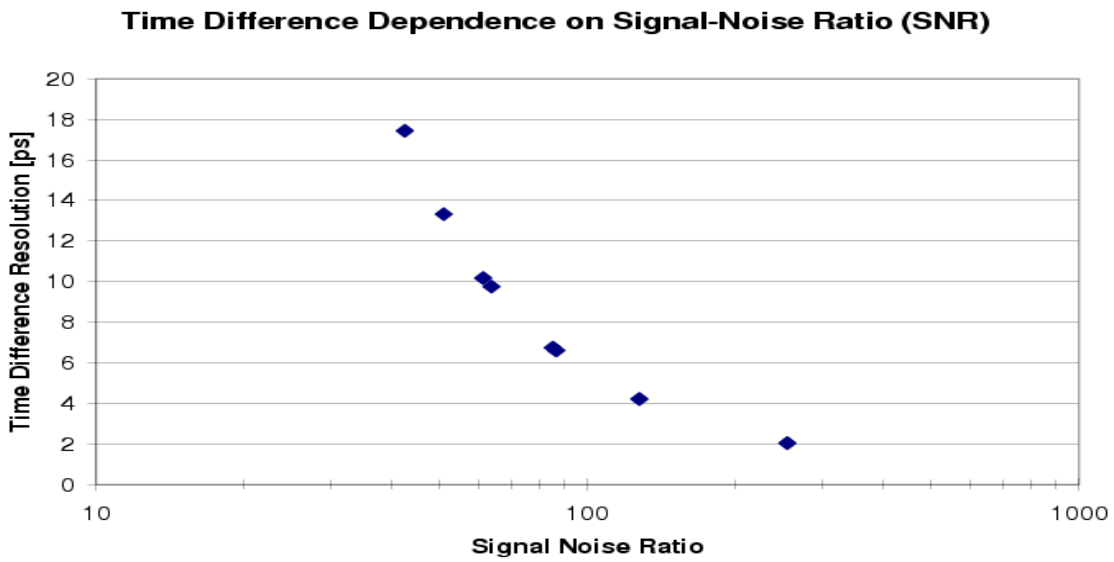






3) Waveform sampling electronics (limits)

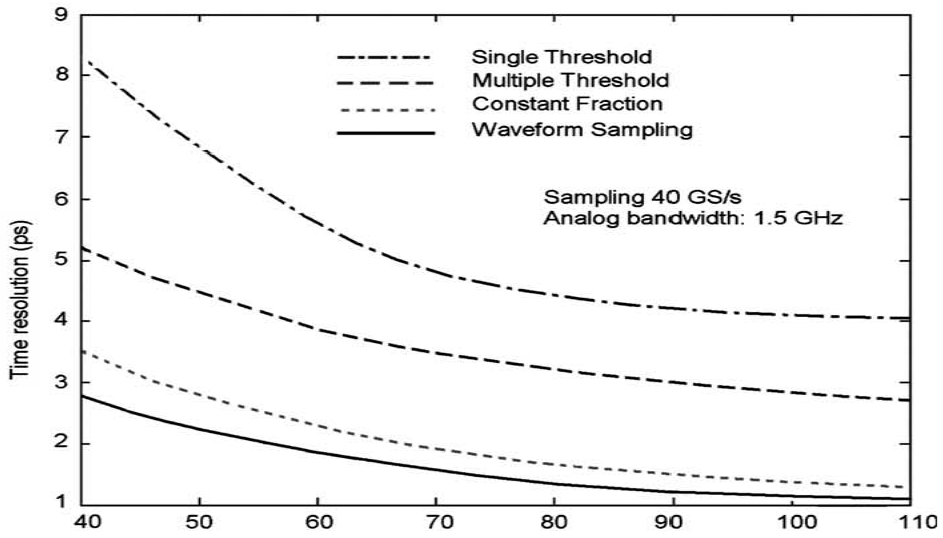
1GHz analog bandwidth, 5GSa/s



G. Varner and L. Ruckman

NIM A**602 (2009) 438-445**.

Simulation includes detector response

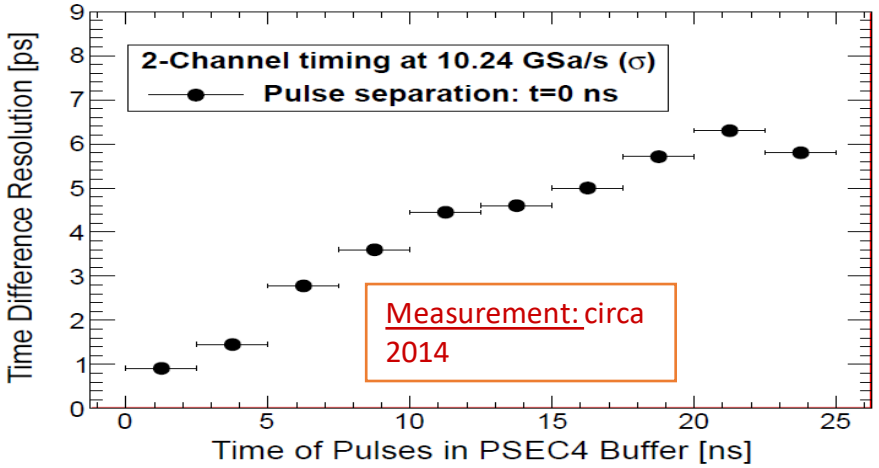


J-F Genat, G. Varner, F. Tang, H. Frisch

NIM A**607 (2009) 387-393**.

E. Oberla, J-F Genat, H. Grabas, H. Frisch, K. Nishimura, G. Varner

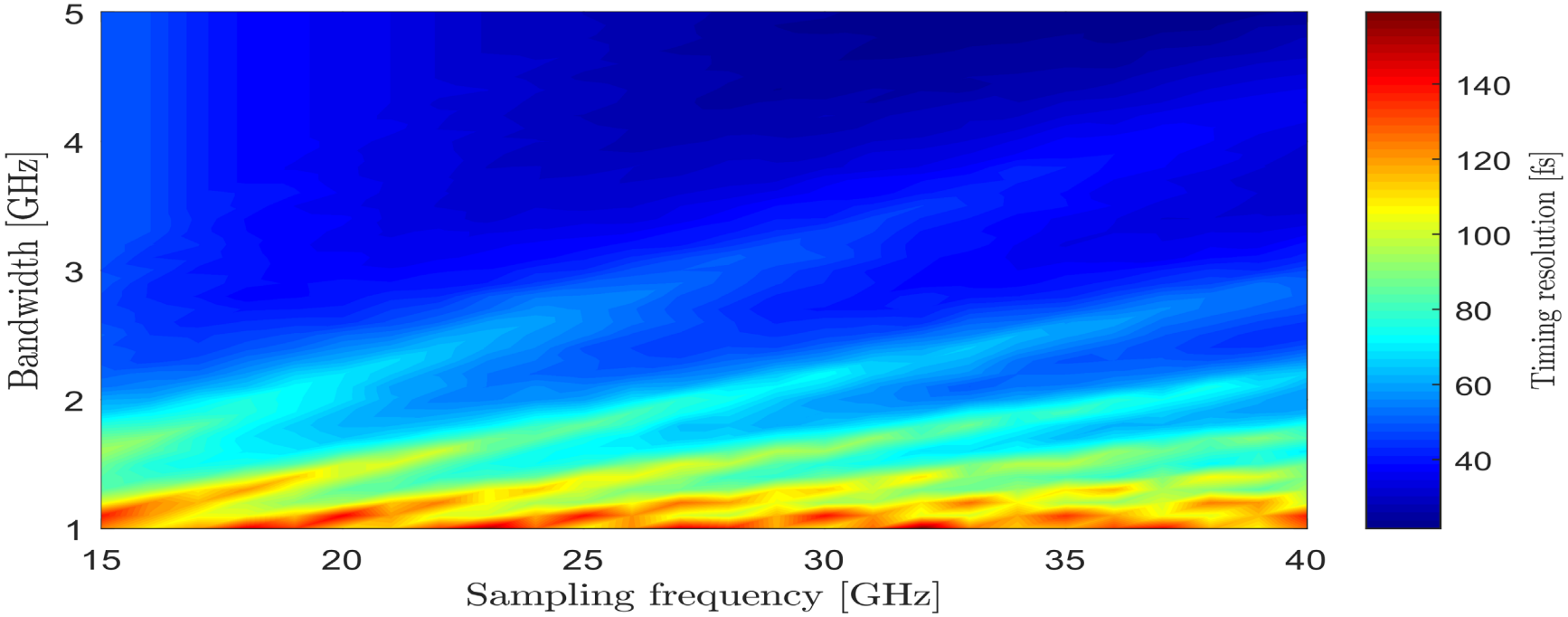
NIM A**735 (2014) 452-461**.



Extending to 1ps and lower, with advanced calibration techniques

Pushing into the femtosecond regime

Pushing sampling speed and analog bandwidth

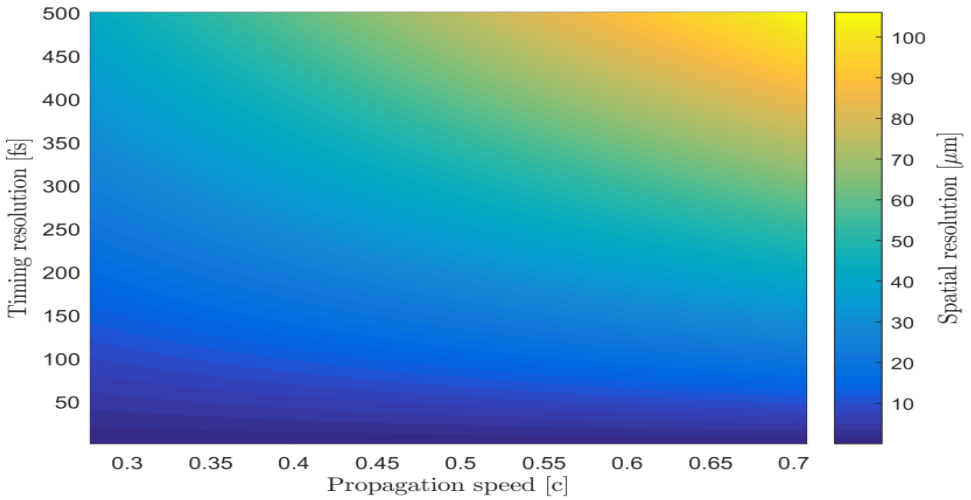


P. Orel, G. Varner
and P. Niknejadi
NIM A**857 (2017) 31-41**.

And pushing the **space-time limit**
(new type of PID or DIRC devices?)

P. Orel and G. Varner

IEEE Trans. Nucl. Sci. **64 (2017) 1950-1962**.

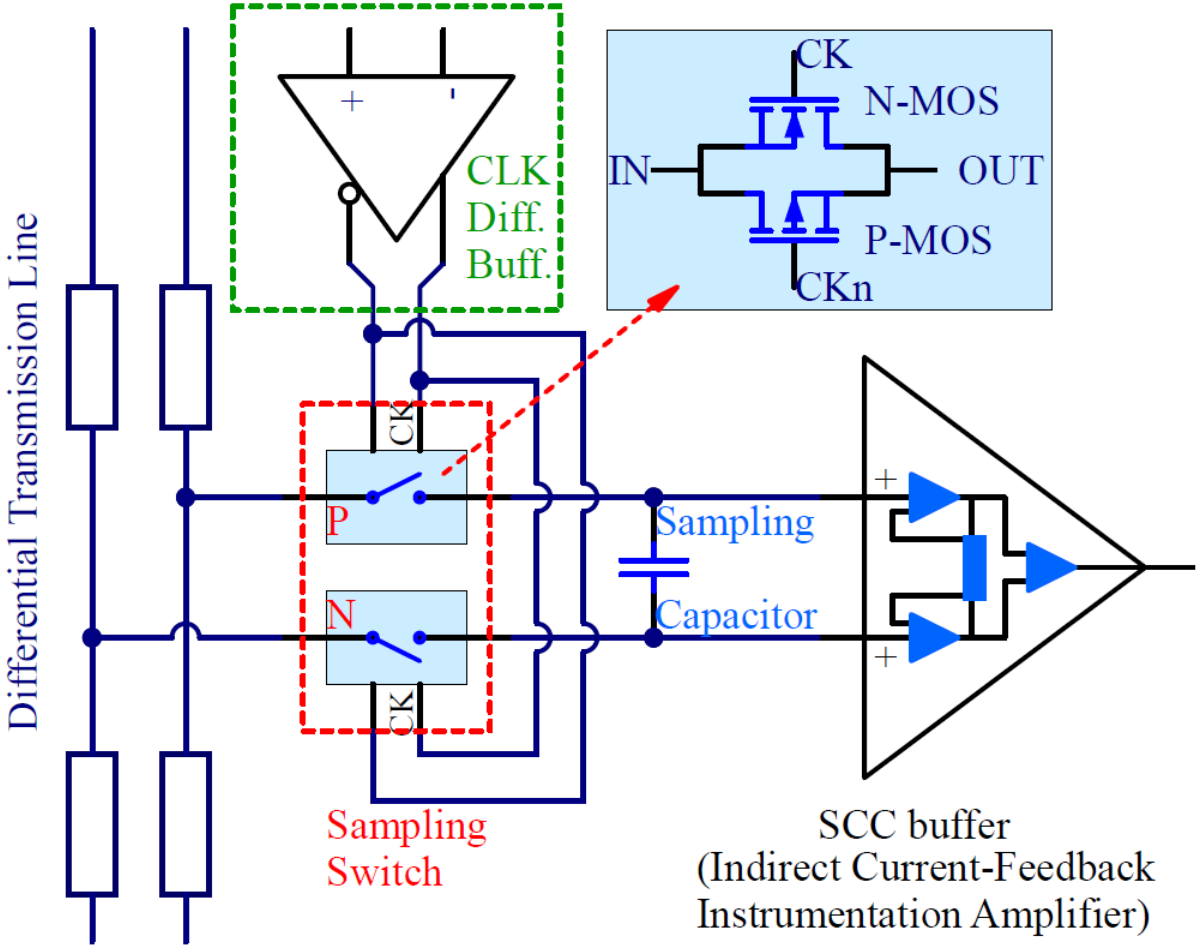


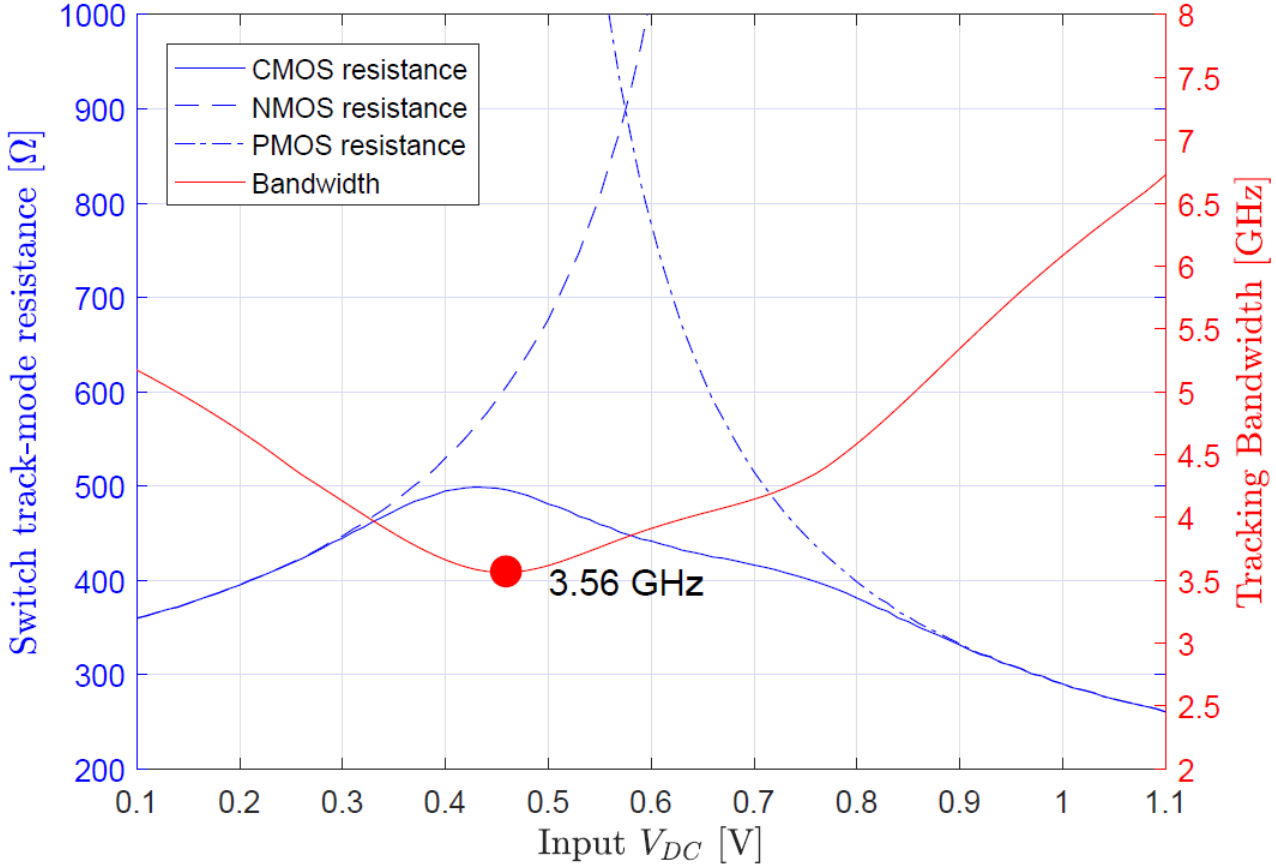
130nm Target Specifications

Parameter	Minimum desired value
Sampling frequency (ASIC)	20 GHz
Bandwidth (Detector and ASIC)	3 GHz
Signal to Noise Ratio (Detector and ASIC)	58dB (V_{signal}=1 Volt)
Velocity of Propagation (Transmission Line/ strip line)	0.35c
Number of Bits of Resolution	9.4 bit

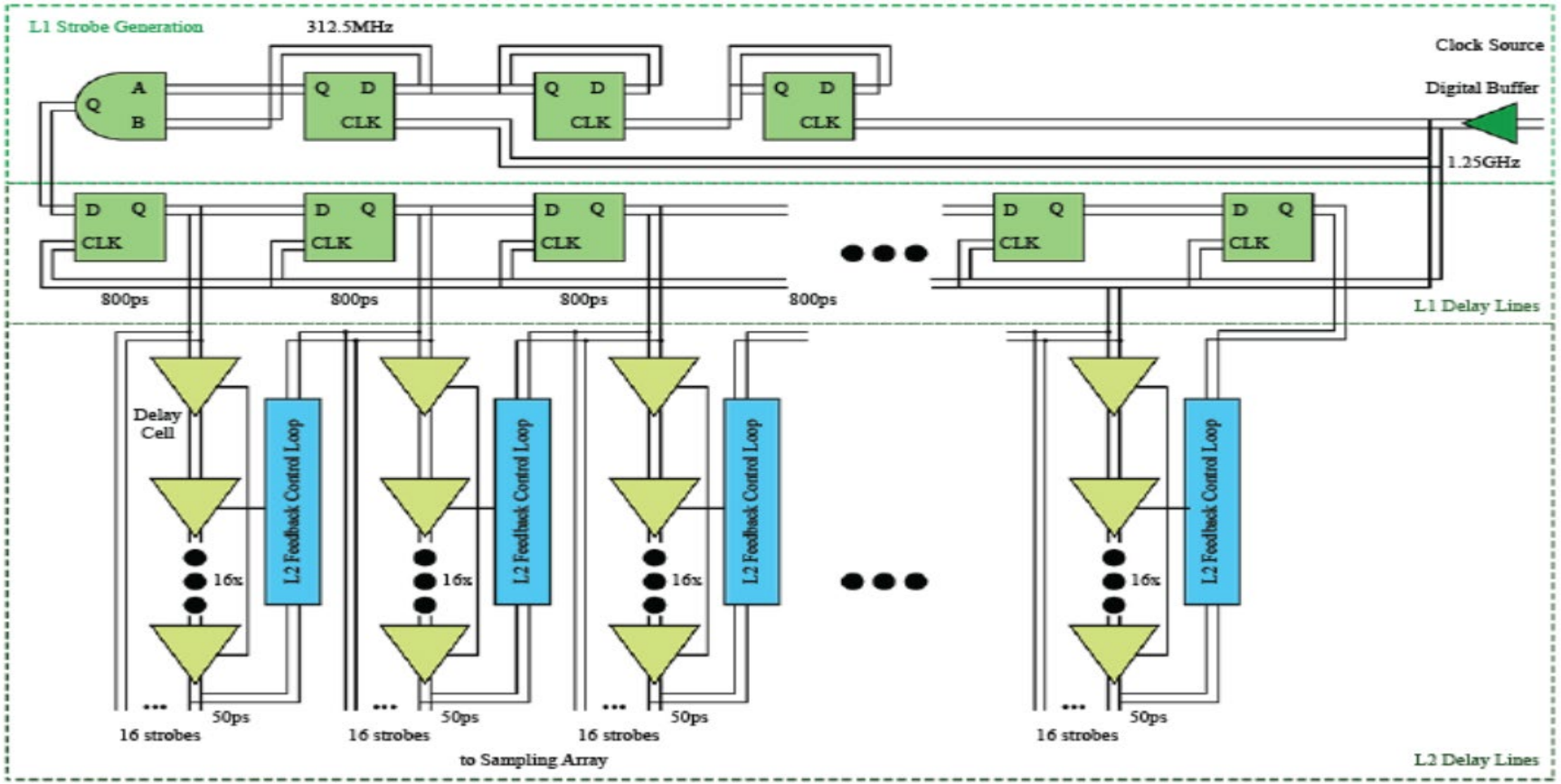
Getting to < 200fs very challenging, but a device with <=1ps (independent of aperture) interesting

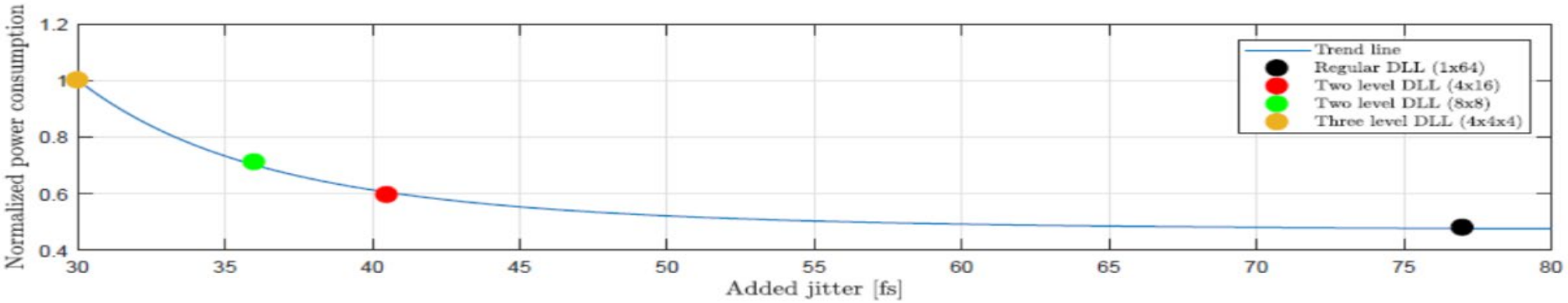
To achieve these specs, SNR and ABW are critical



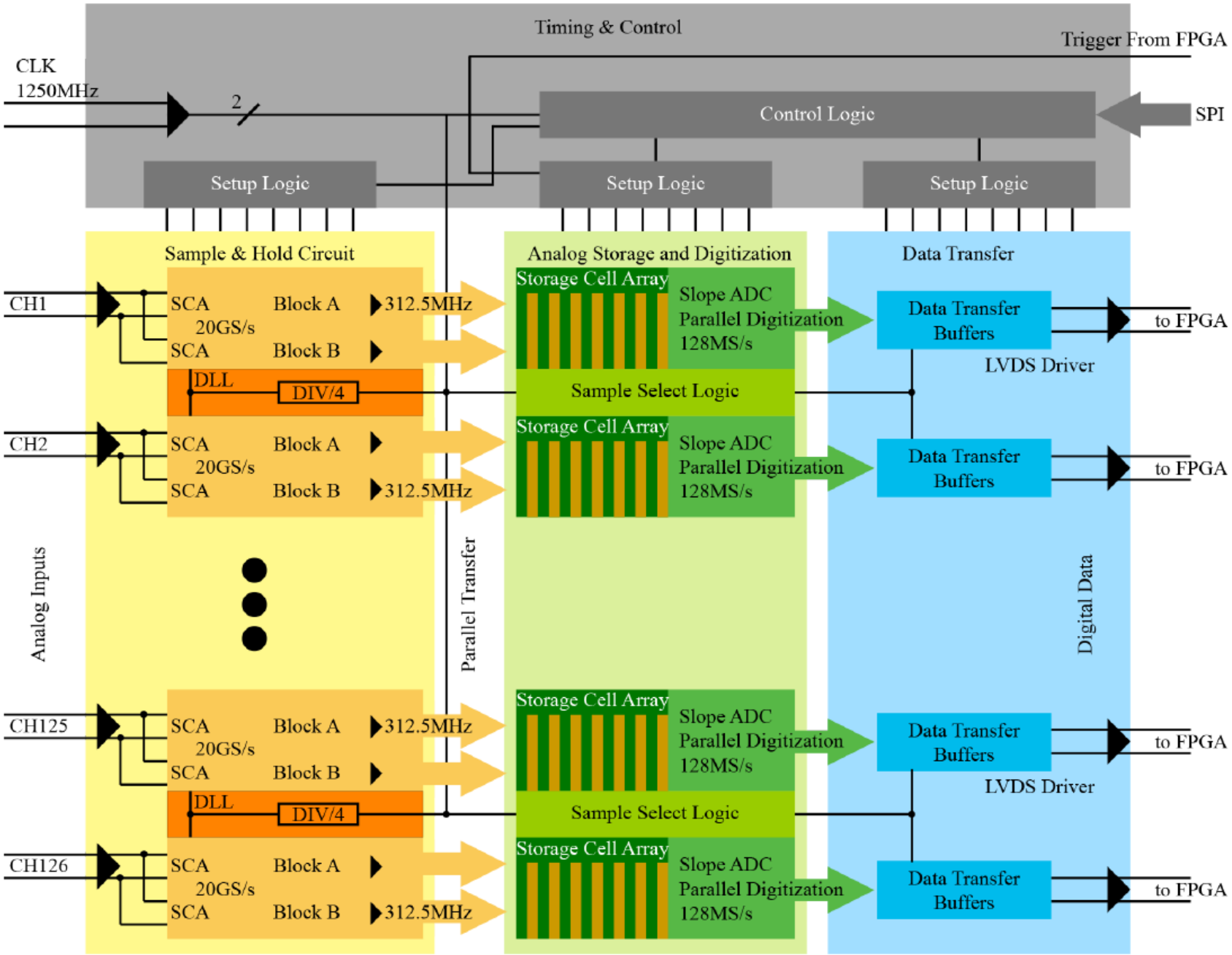


Example of a critical component

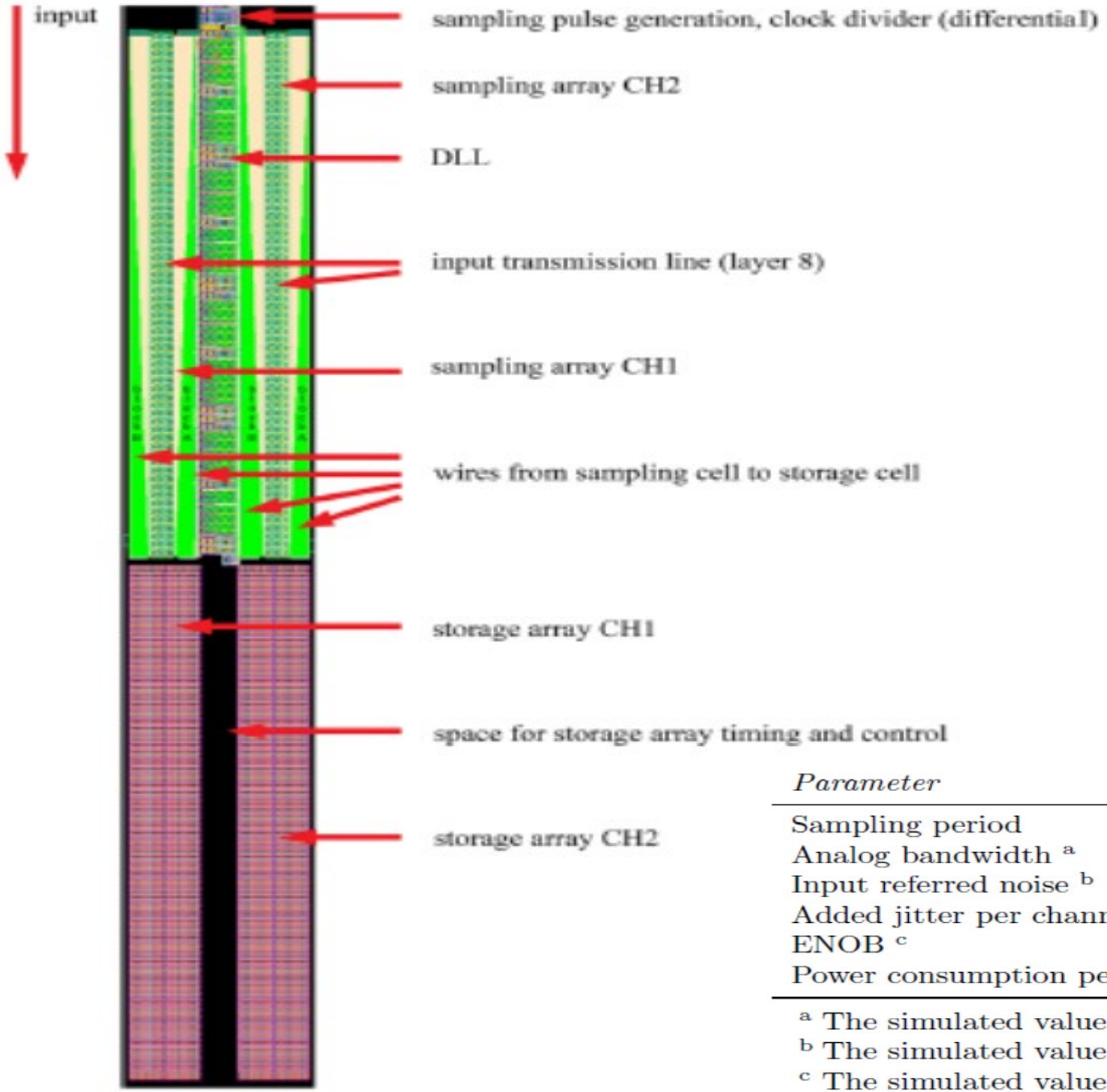




RFPix1 overall architecture



RFpix1 ASIC Design Summary



Key Design components verified

Work still needed on the digital control/address decoding

Moved on to other projects, consideration of <u>other technology nodes</u>

Parameter	*Desired value*	*Simulated value*
Sampling period	$50\ ps$ @$20\ GS/s$	$50\ ps$ @$20\ GS/s$
Analog bandwidth [a]	$\approx 3\ GHz$	$\approx 3.56\ GHz$
Input referred noise [b]	$\leq 0.5\ mV_{RMS}$	$\approx 1.05\ mV_{RMS}$
Added jitter per channel	$\approx 40\ fs$	$\approx 29\ fs$
ENOB [c]	≥ 10	≈ 9.6
Power consumption per channel [b]	$40\ mA$	$41.71\ mA$

[a] The simulated value is the tracking bandwidth of the SCA.
[b] The simulated value does not take into account the input buffer.
[c] The simulated value does not take into account distortion.

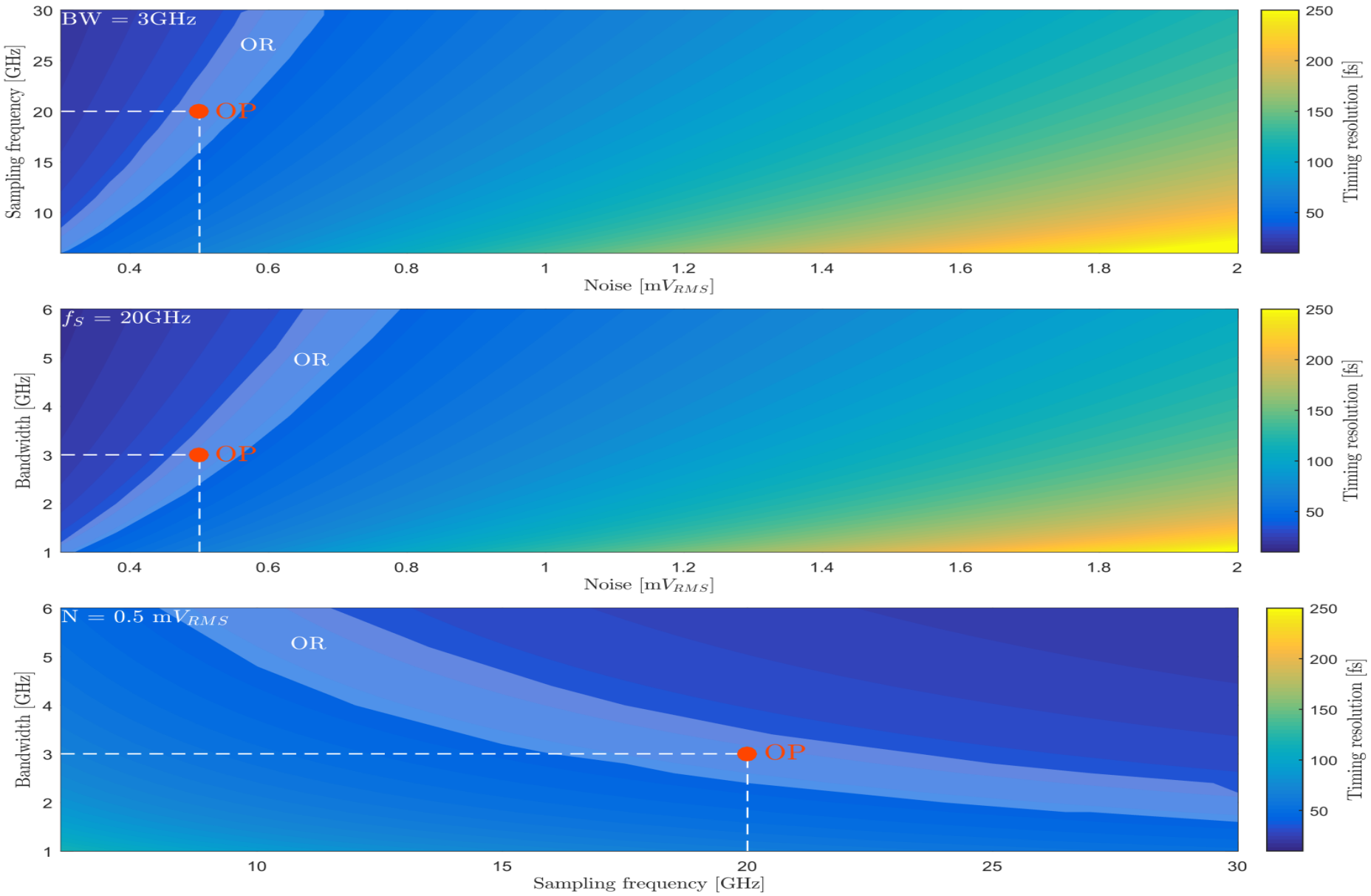
Comparing with the 65nm technology node

- **Sub-ps timing interesting on its own**

- **RFPix is somewhat of a concept study**
  - **However exchanging a spatial dimension (or more) for time, can have significant benefits in Giga-channel count systems**

- **Cost is an issue, however some key benefits:**
  - **Faster (20GSa/s was at limit for 130ns)**
  - **Can fit a lot more stuff (digital processing)**
  - **More radiation hard**

Performance Parameter Space -- comparison



- **RFPix1 → RFPix2**

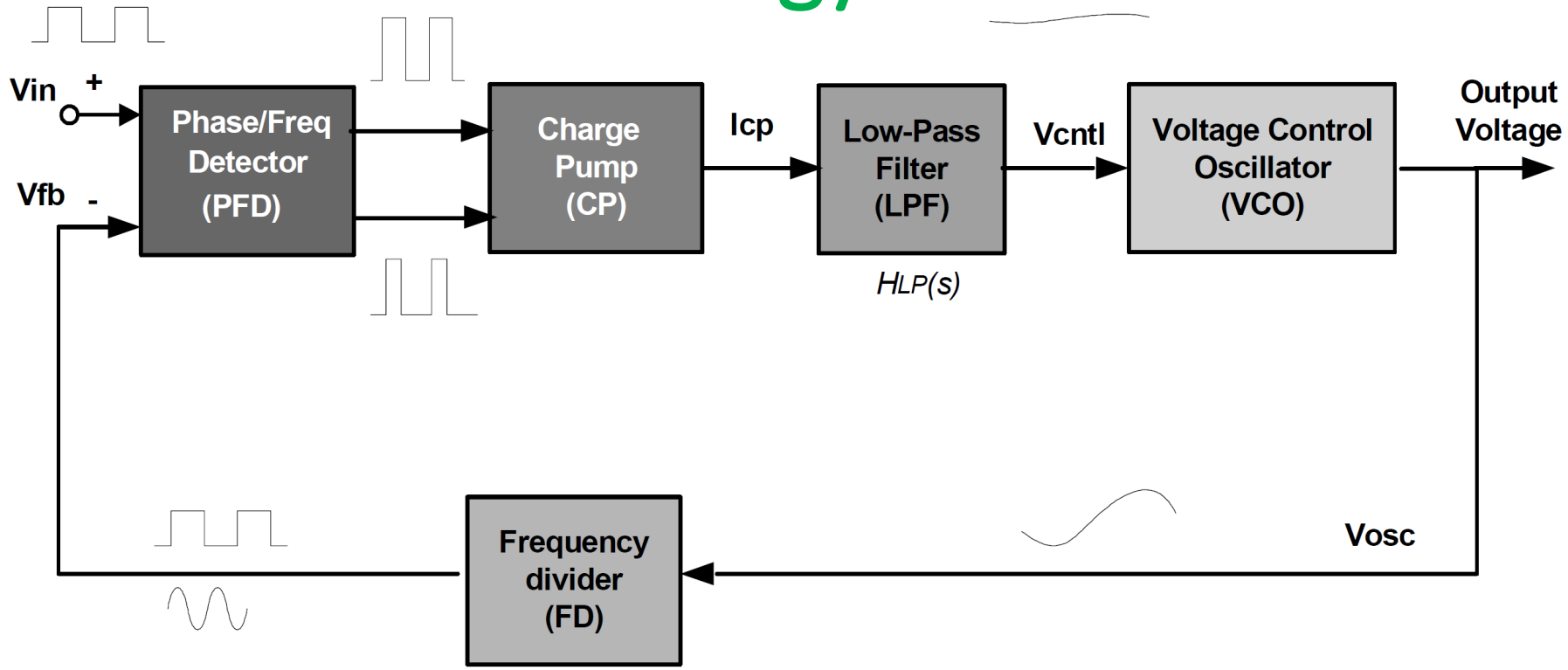
Scaling to 40GSa/s?

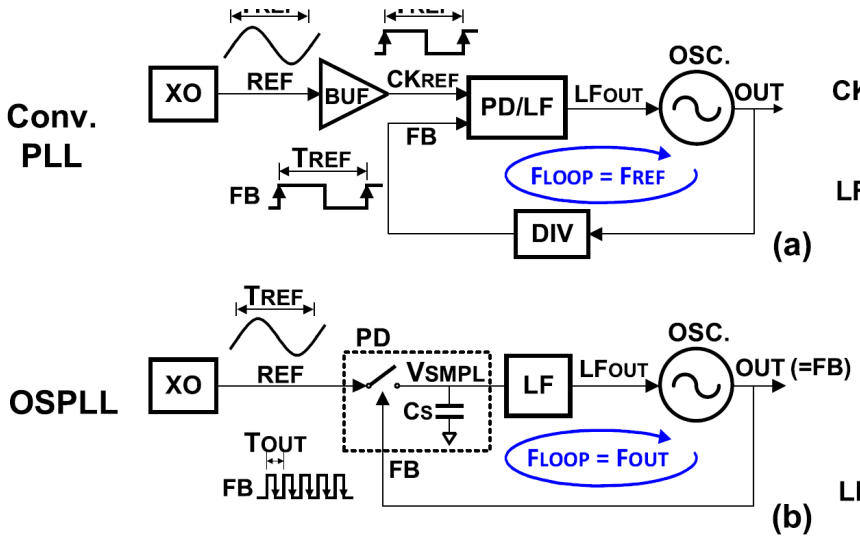
Dynamic range reduced ~20%

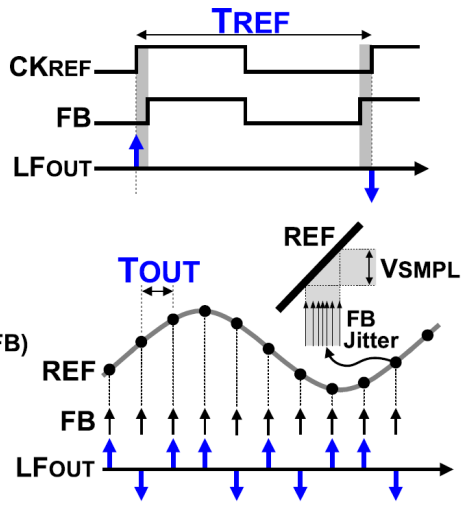
Analog bandwidth determined by sensor/initiator circuit?

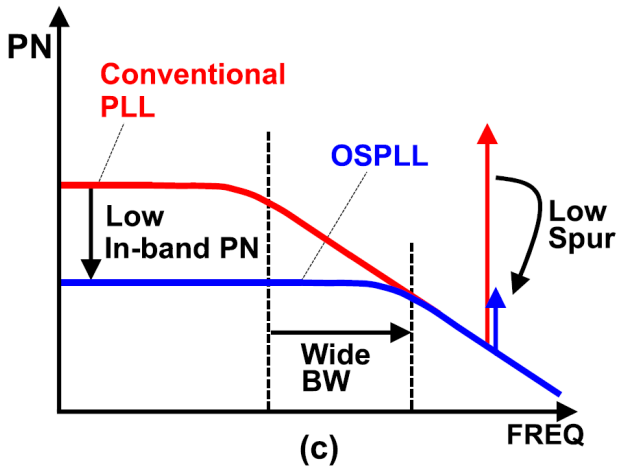
Higher density, direct clocking of sampling?

65nm technology transistor-level simulation (I)









- **Common PLL**

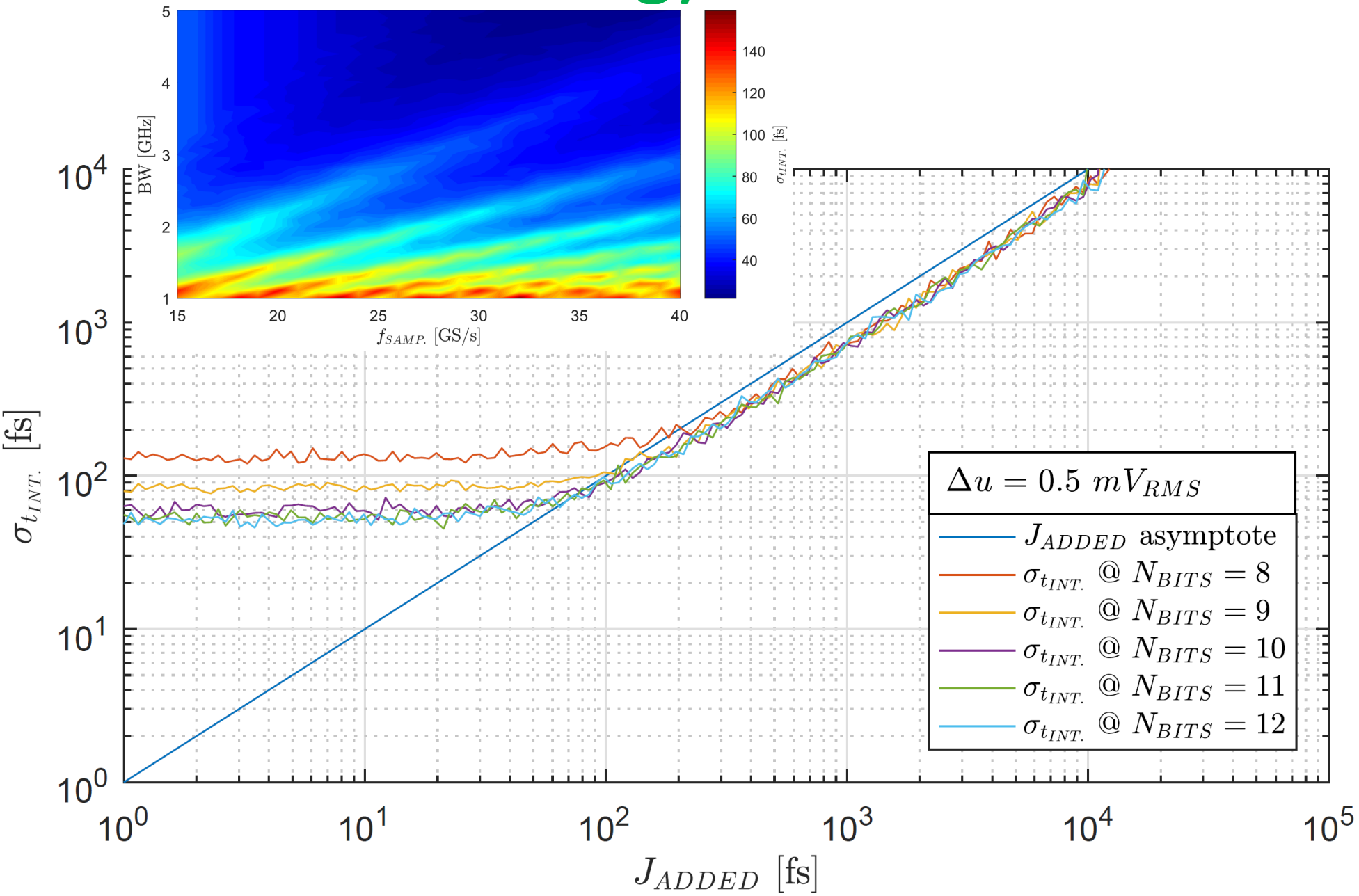
Scaling to 40GSa/s?

Dynamic range reduced ~20%

Analog bandwidth determined by sensor/initiator circuit?

Higher density, direct clocking of sampling?

65nm technology transistor-level simulation (II)



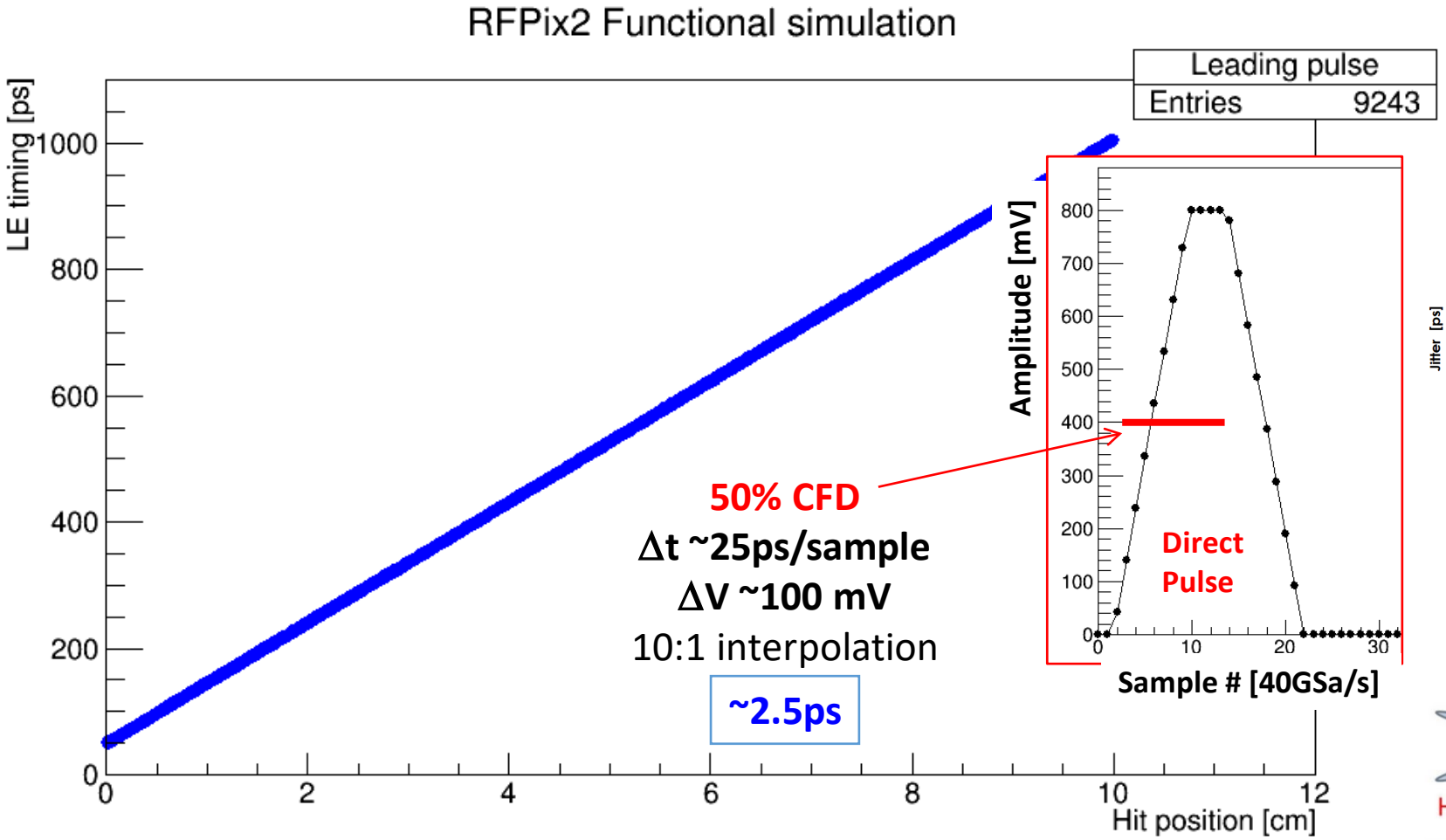
- **Added jitter contribution**

Scaling to 40GSa/s?

Dynamic range reduced ~20%

Higher density, direct clocking of sampling?

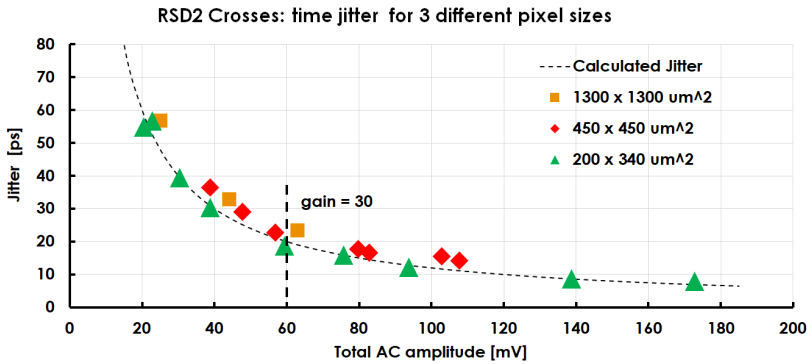
65nm technology functional MC to probe limits



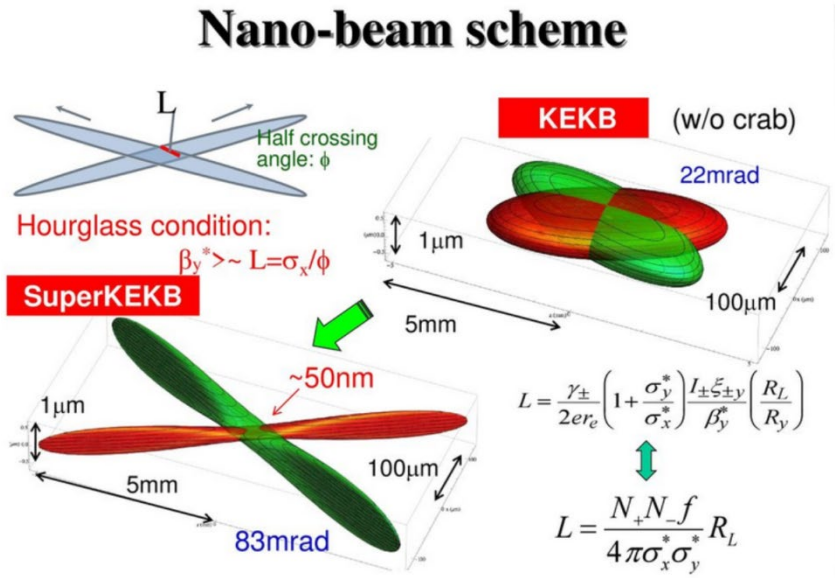
Combined event uncertainty: 10's of ps

Limits:

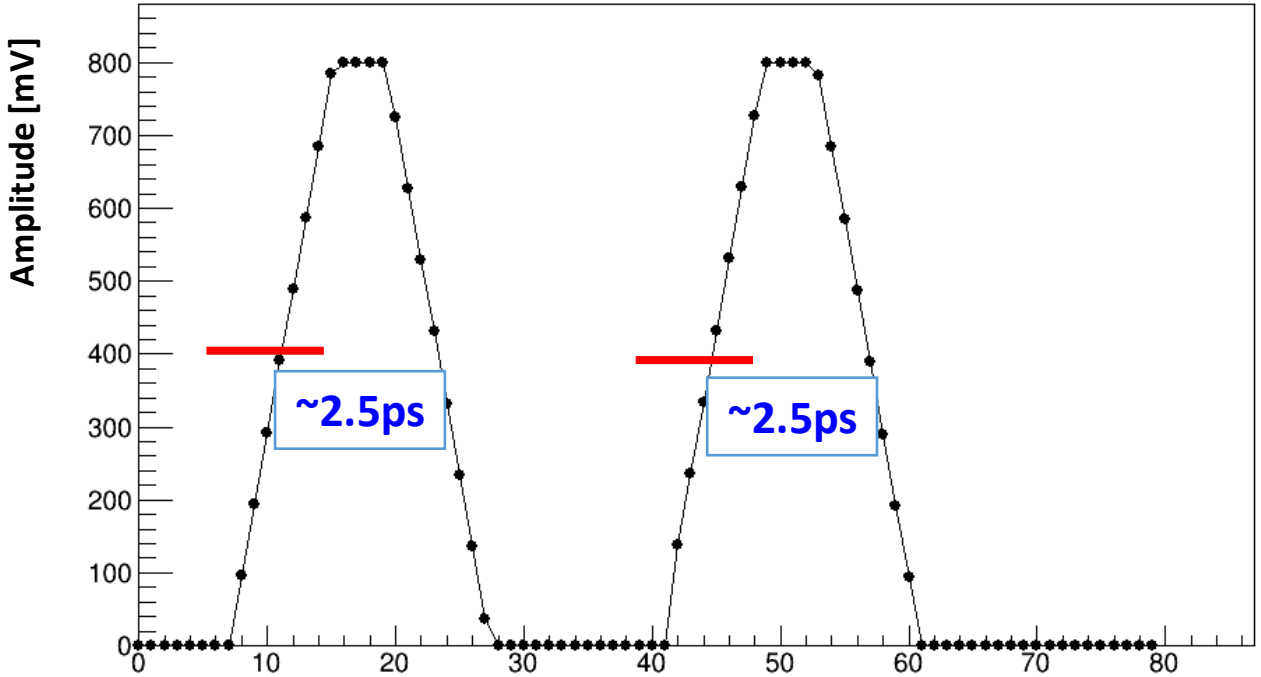
- **Initiator Circuit (SiPM or LGAD)**

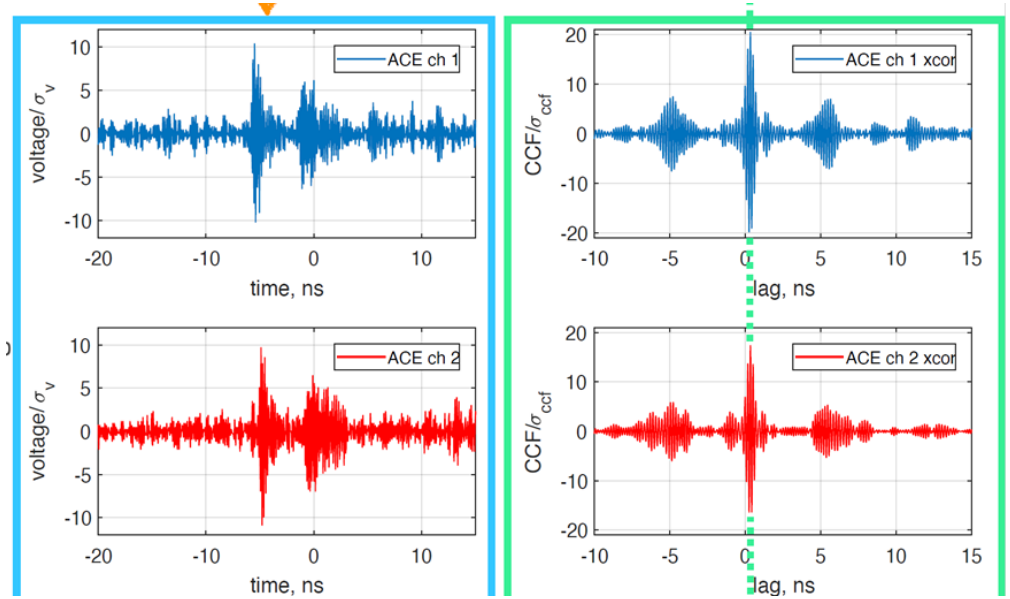


- **SuperKEKB Luminous Region**



65nm technology functional MC to probe limits





- Net contribution ~ sqrt(2) * singleLE

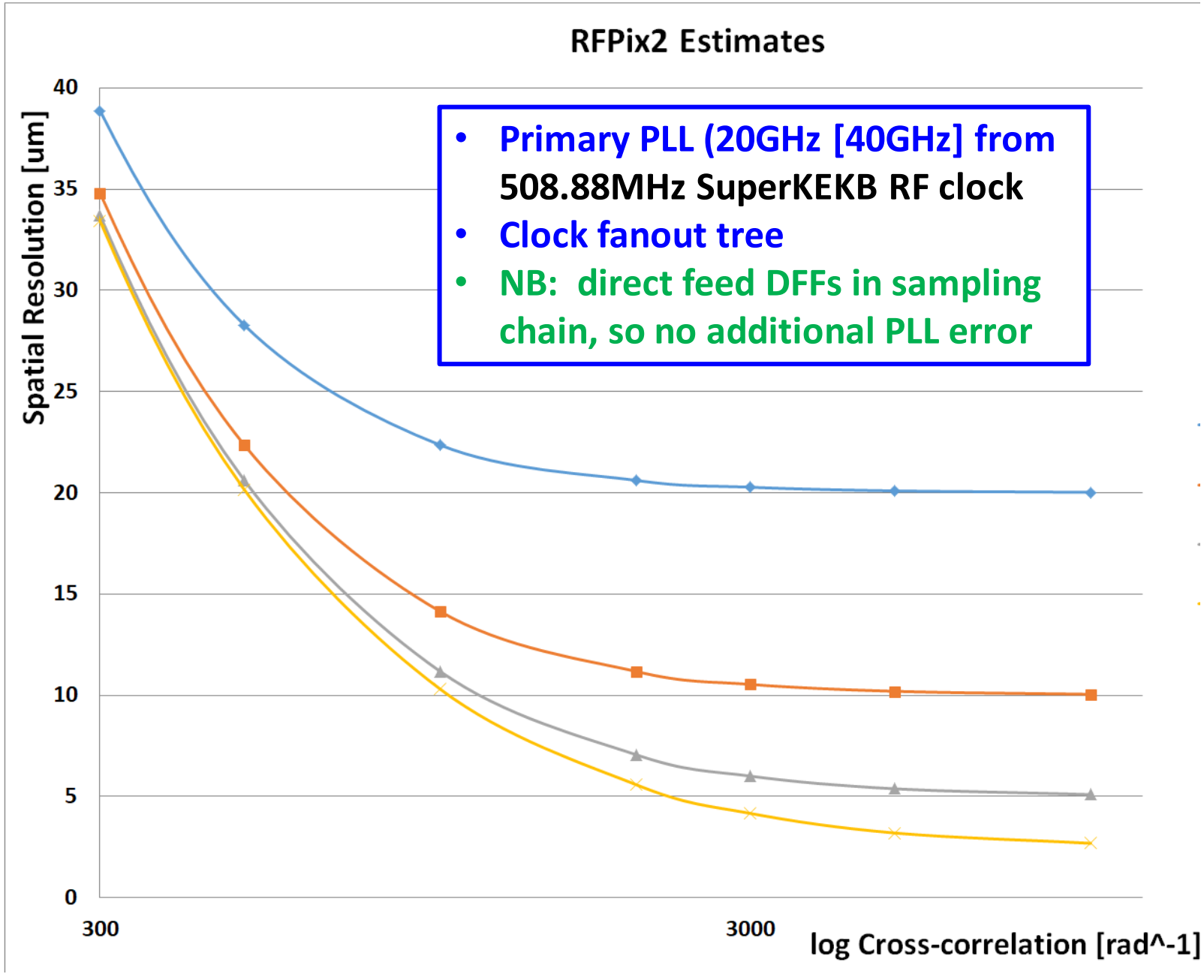
3.54ps

- However, have a lot of information on the leading edges (and pulses themselves)
- Can logically extend to more content-rich initiation signal (see Thursday talk)

- Place where 65nm shines

(lots of digital processing resources!)

RFPix2 65nm projections and ToDo



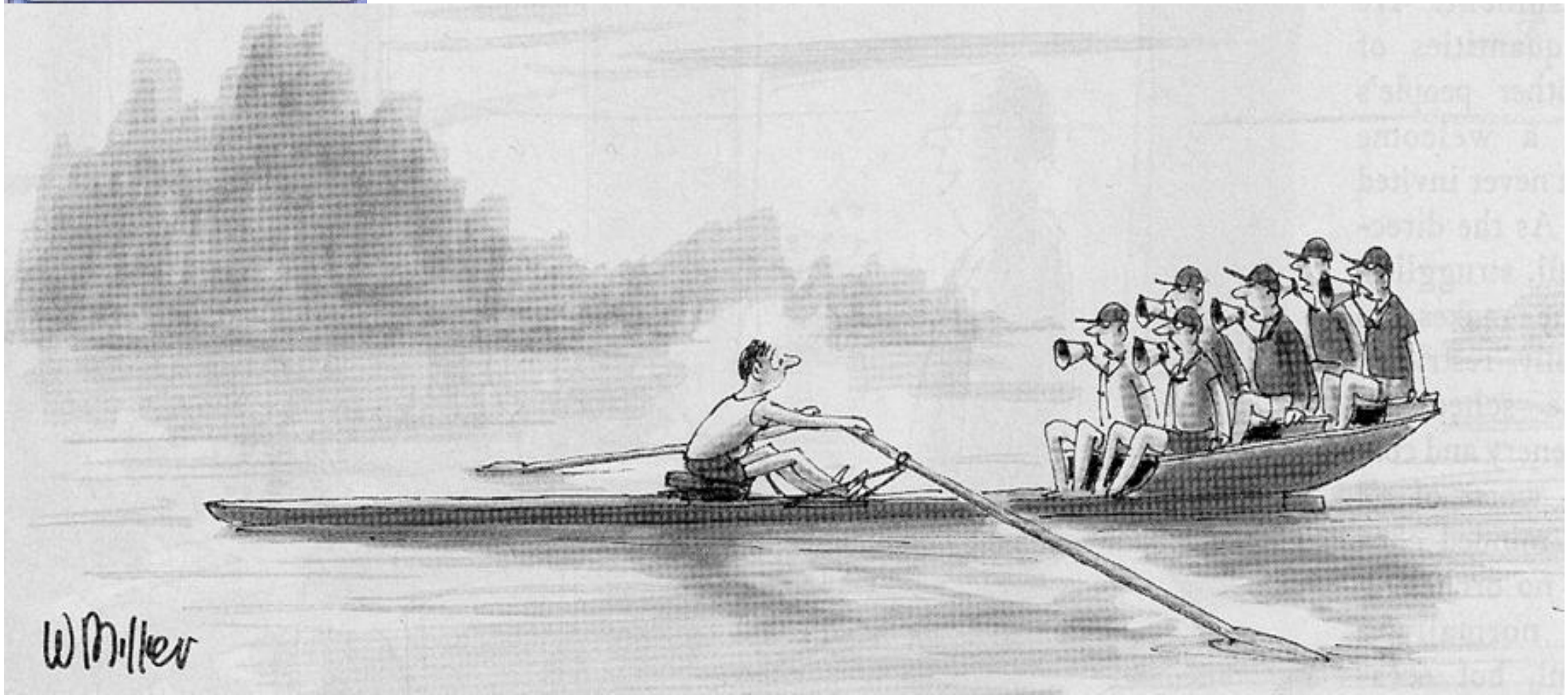
Summary

- **Sub-ps timing interesting on its own**

- **Advancing to 65nm (or lower) further extends waveform sampling options to achieve this**

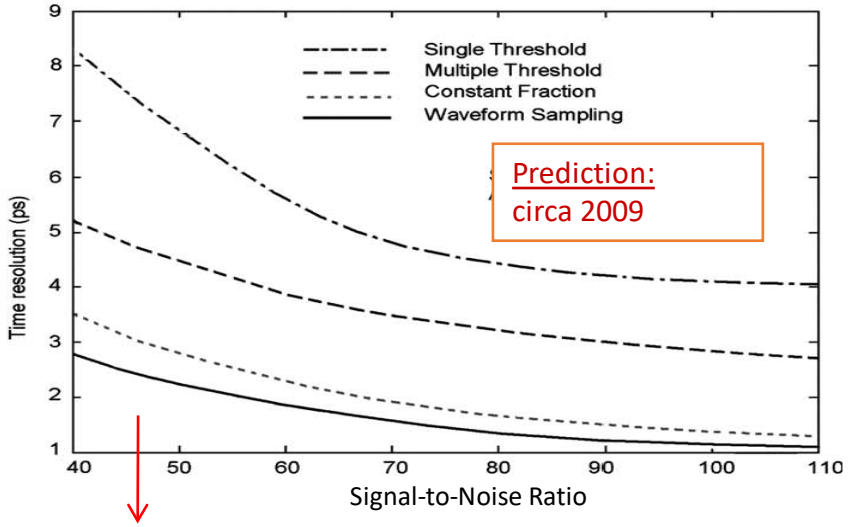
- **RFPix is largely of a concept study**
  - **However exchanging a spatial dimension (or many) for time, can have significant benefits in Giga-channel count systems**
  - **Roadmap to readout for next-generation detectors capable of producing timing of sub-ps resolution (or use differential measurements to mitigate jitter limits)**

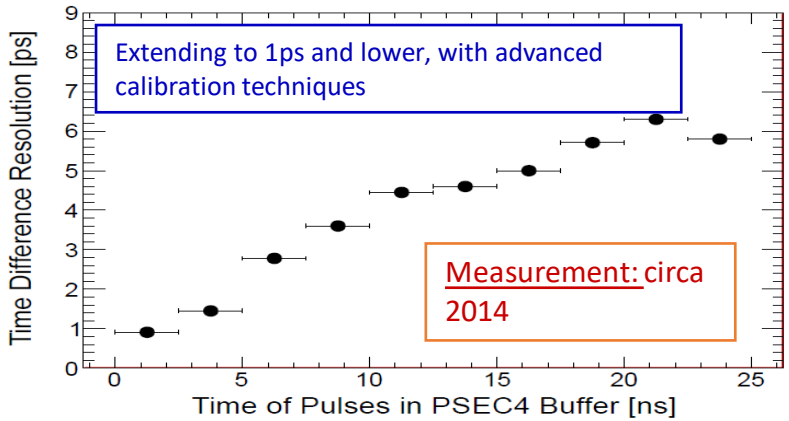
Backup Slides



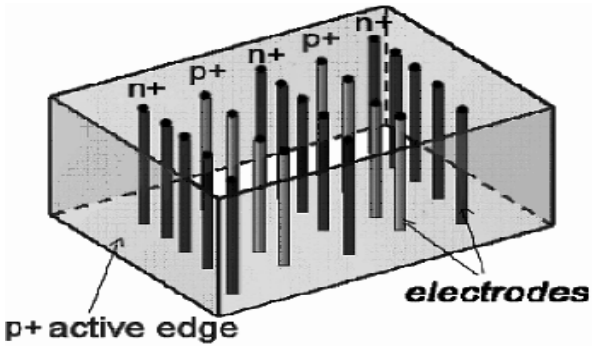
Interest in exquisite space-time Resolution

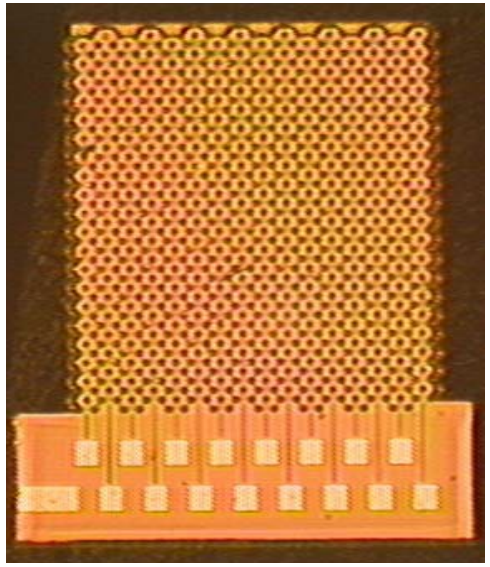
In a number of communities (future particle/astroparticle detectors, PET medical imaging, etc.) a growing interest in detectors capable of operating at the pico-second resolution and µm spatial resolution limit (for light 1 ps = 300 µm)

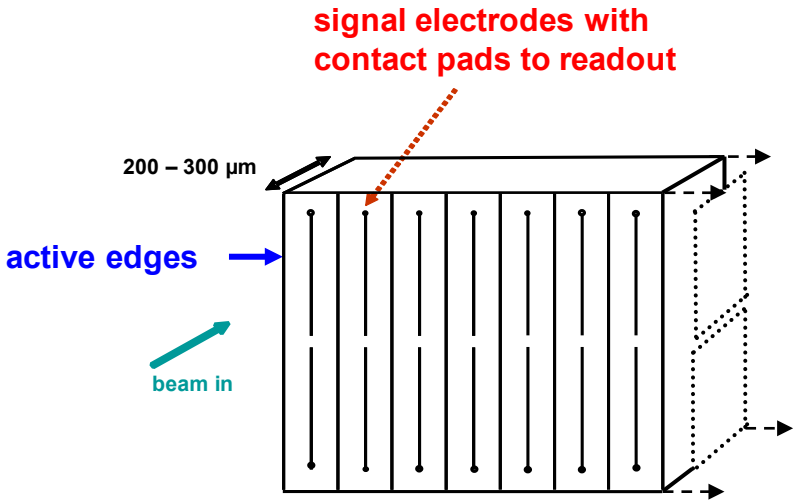


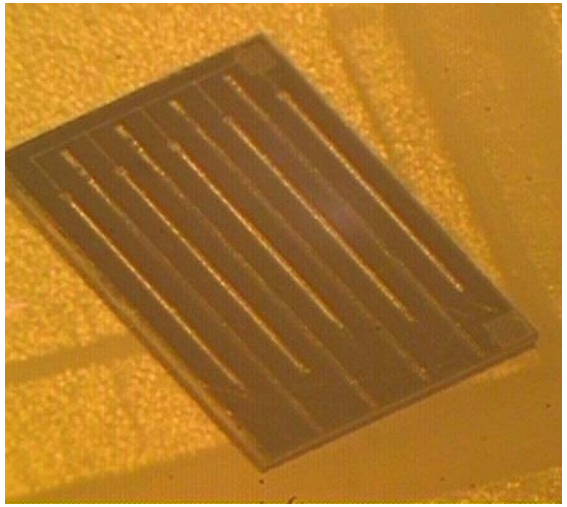


Front-End Electronics





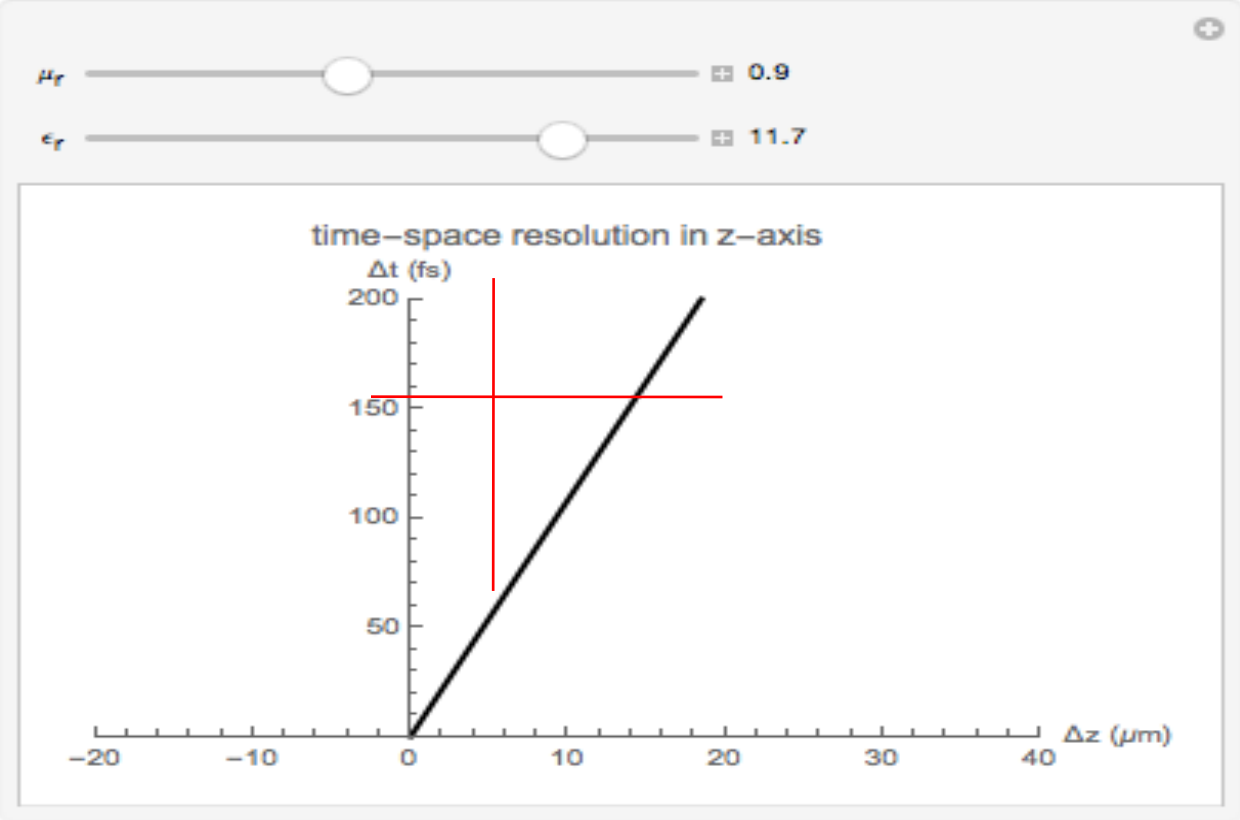




Fast signal collection x-ray detectors

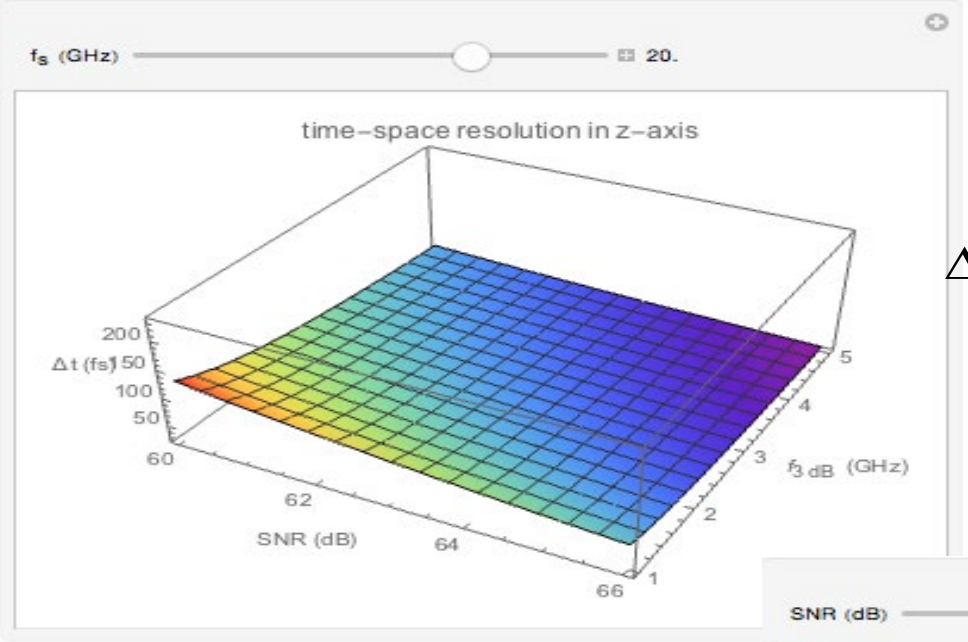
Exploration of the space-time limit

-Sampling at high sampling rate and high bandwidth
-Resolve small distances
Current Goals: Spatial resolution of 10μm in z and 20μm in rφ
In Silicon 10μm in z corresponds to timing resolution of about 100fs
20μm in rφ will depend on the SNR

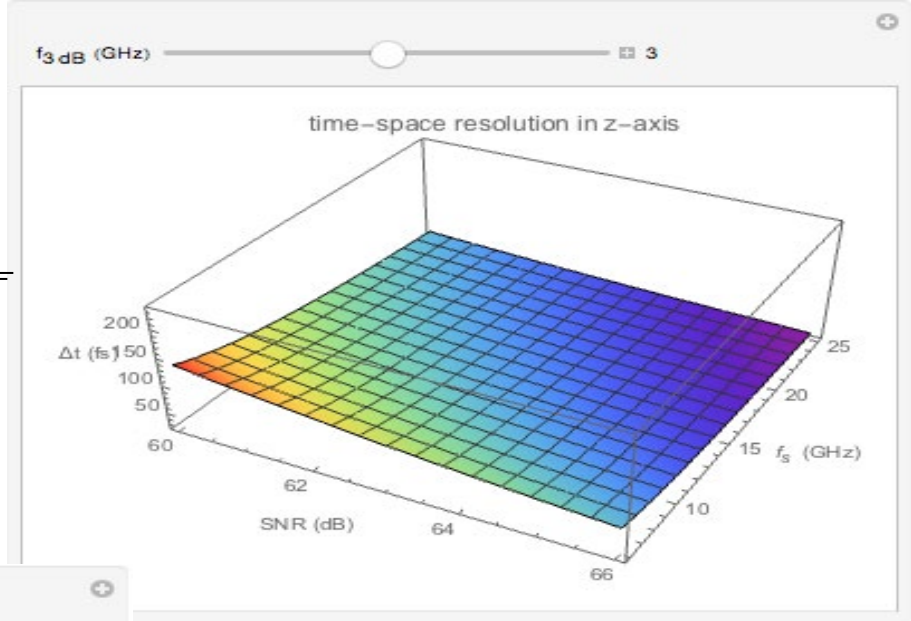


Pixel detector (PDX) at SuperKEKB

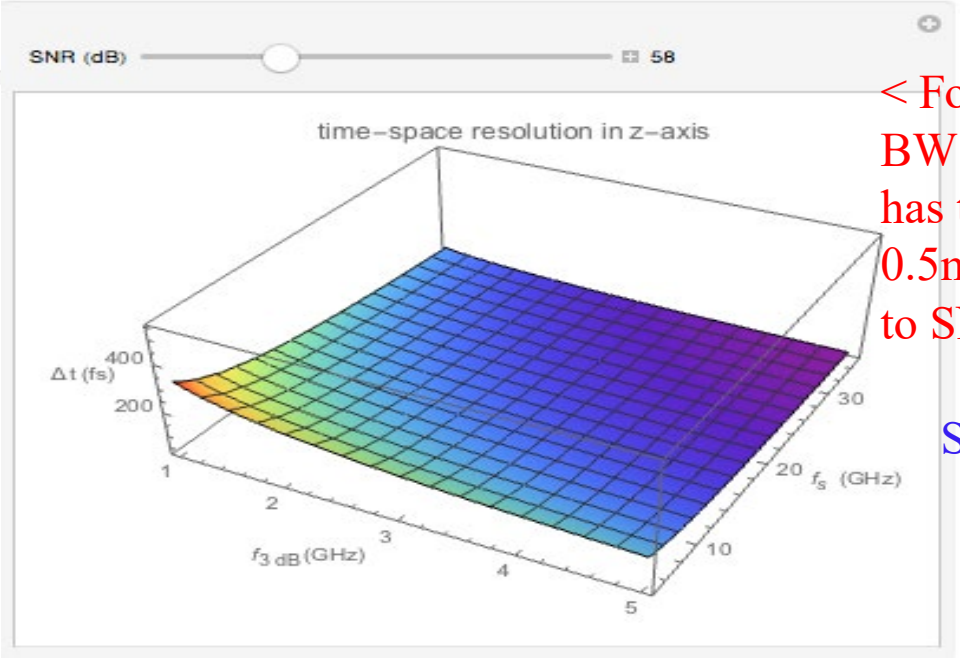
Visualizing parameters for time resolution in z



$$\Delta t = \frac{\Delta U}{U} \frac{1}{\sqrt{0.34 * BW * f_s}}$$



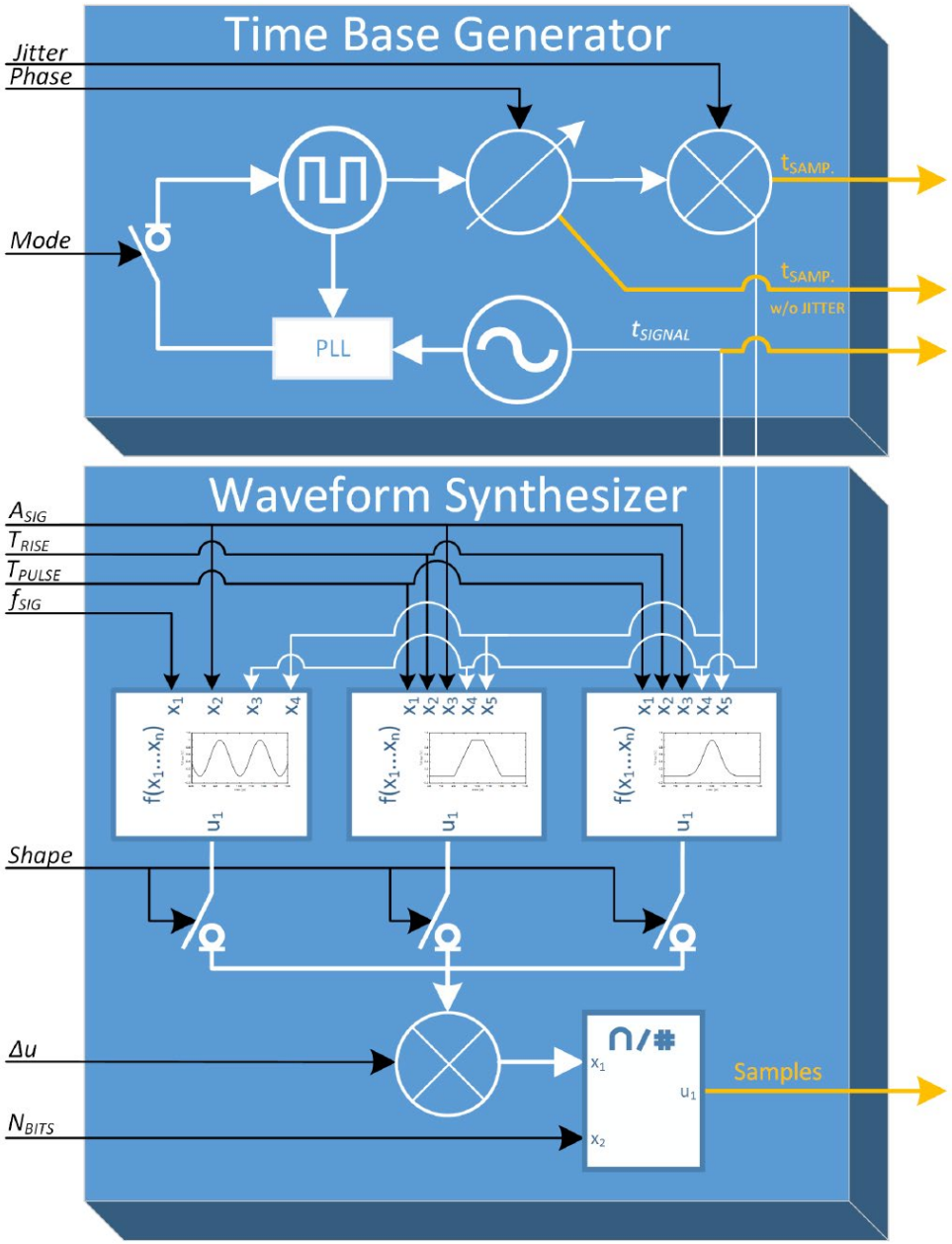
^ Need to hold sampling frequency to least at 20 GHz to have timing resolution in 100fs range



< For the above sampling freq and BW integrated noise amplitude has to be in the range or less than 0.5mV to 0.6mV corresponding to SNR~58dB (V_{pp}=1volts)

SNR~58dB corresponds to 9.4 bits for 20μm resolution in rφ (Ideal ADC)

Higher fidelity simulation

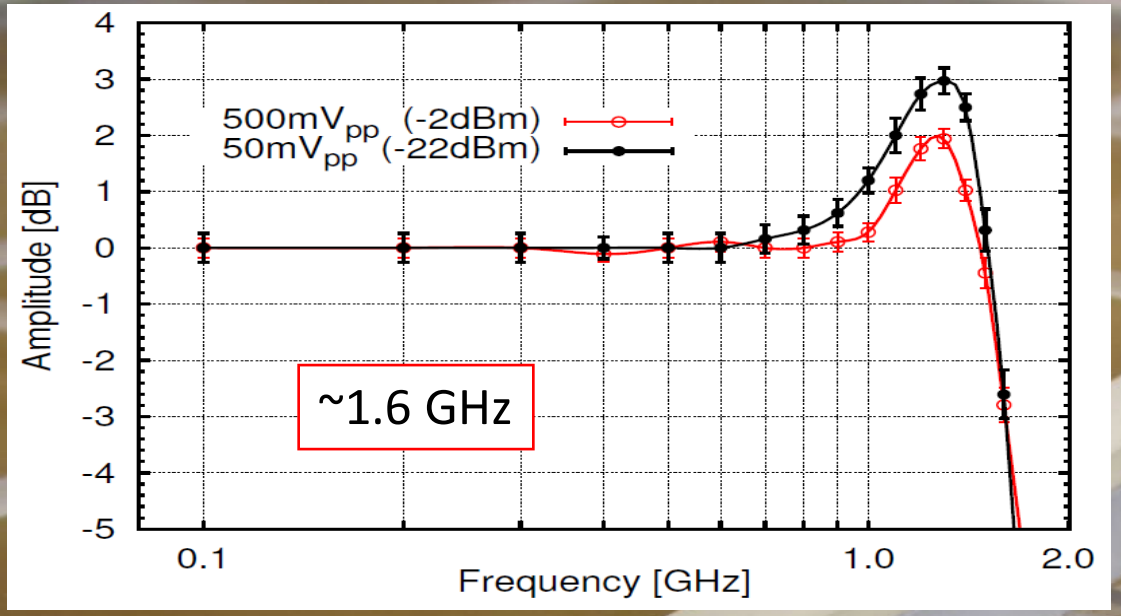


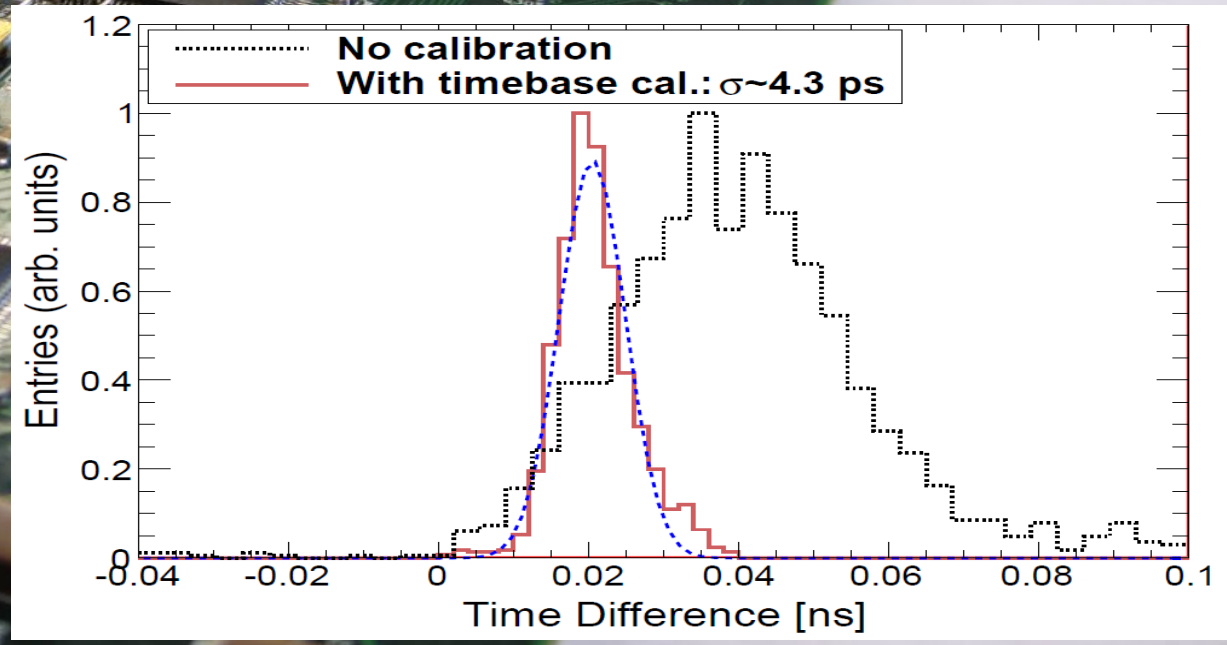
- Amplitude noise injection;
- Quantization with adjustable number of bits (N_{BITS});
- Jitter injection;
- Adjustable sampling frequency;
- Adjustable signal frequency and bandwidth;
- Adjustable time window;
- Adjustable full scale dynamic range.

The generator output provides four vectors:

- Sampled amplitude vector ($Samples$);
- Sampler time base vector with jitter ($t_{SAMP.}$);
- Sampler time base vector without jitter ($t_{SAMP.}\ w/o\ jitter$);
- Signal time base vector (t_{SIGNAL}).

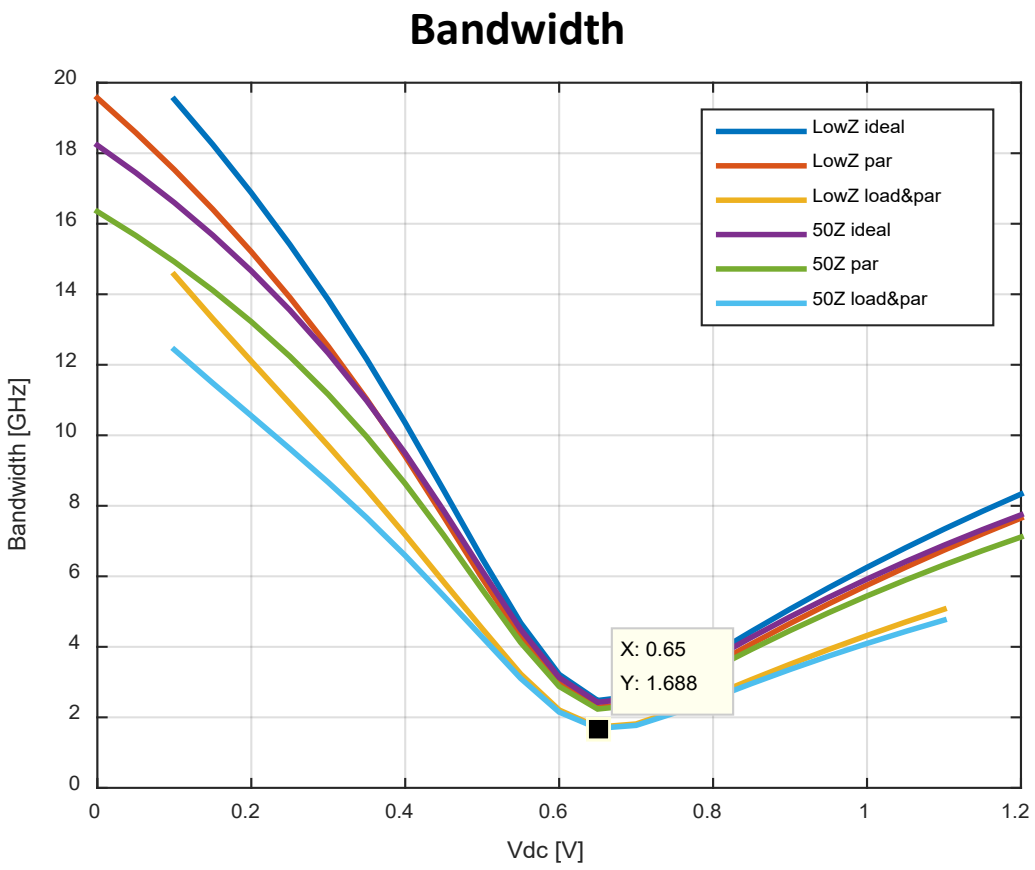
PSEC4



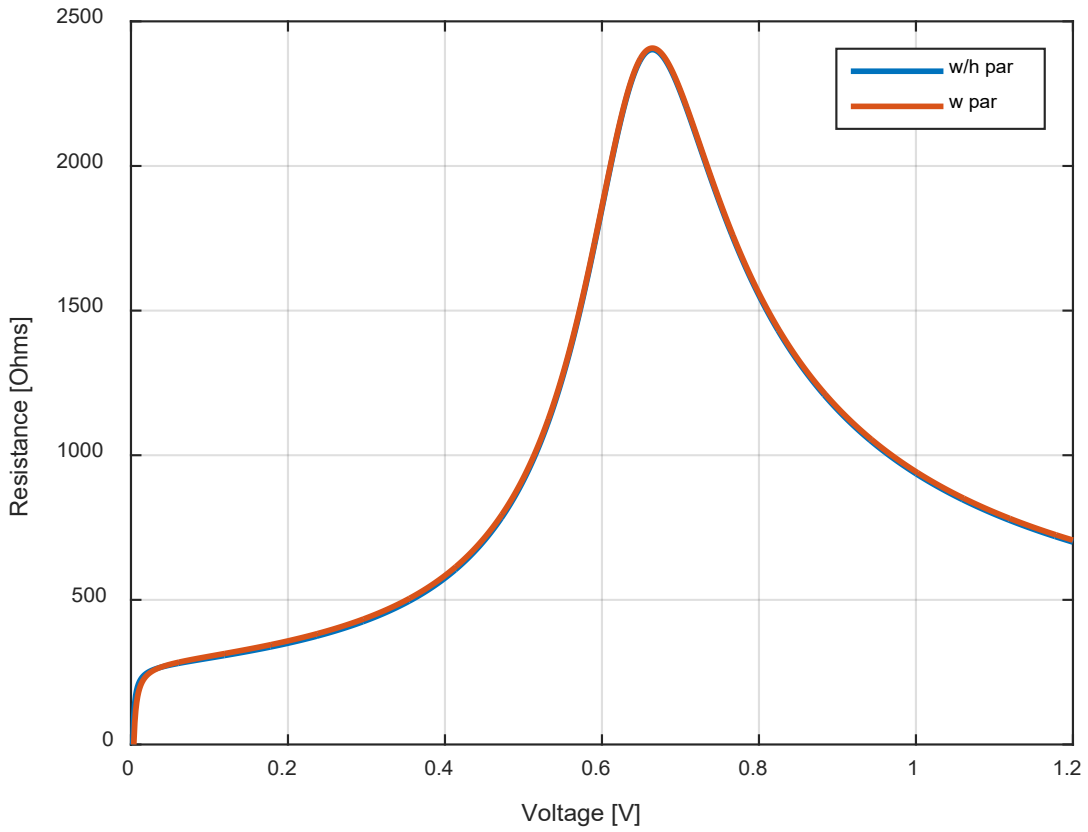


AARDVARC → μs sampling latency

Analog BW limitation – identify and improve

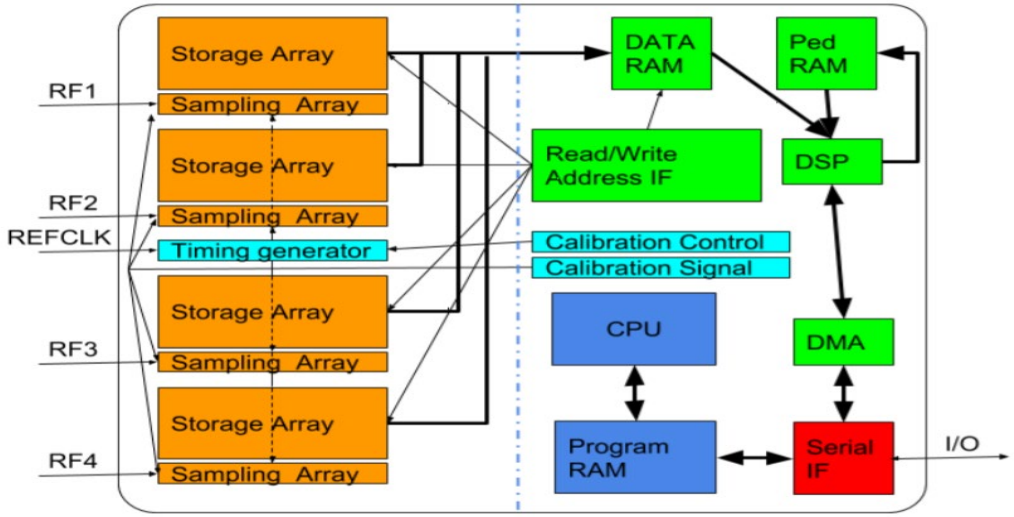


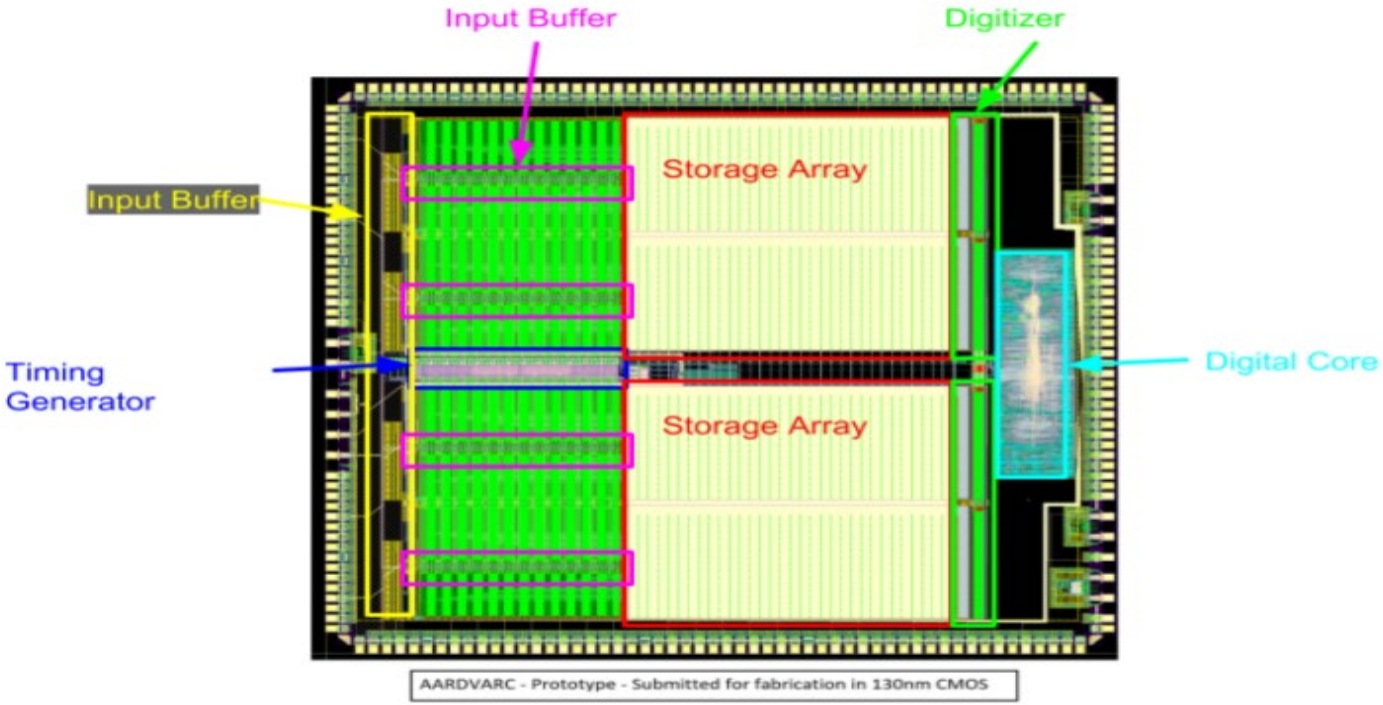
- **BWworst≈1.7GHz @665mVdc @50Ω drive**



- **Ron=2.4k @665mVdc**

AARDVARC (SoC Digital)



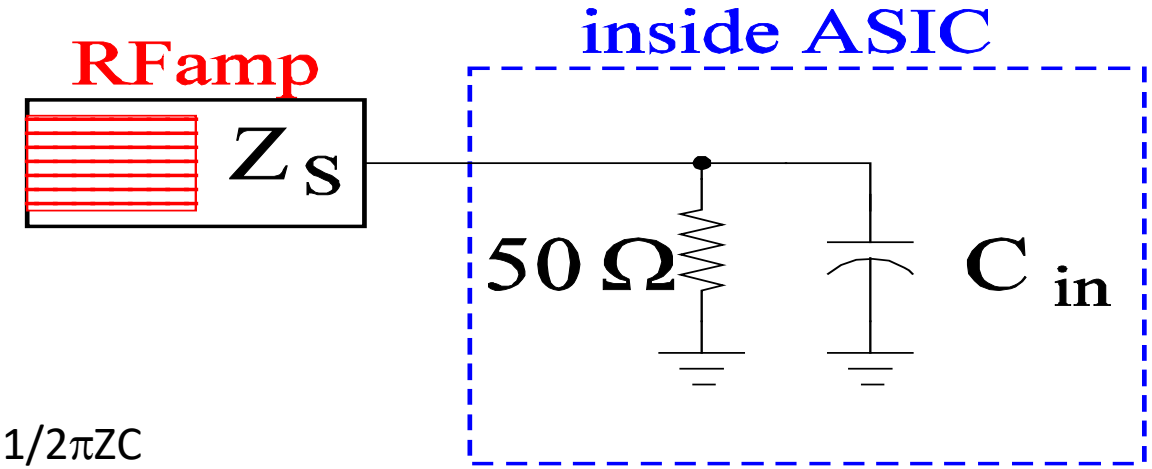


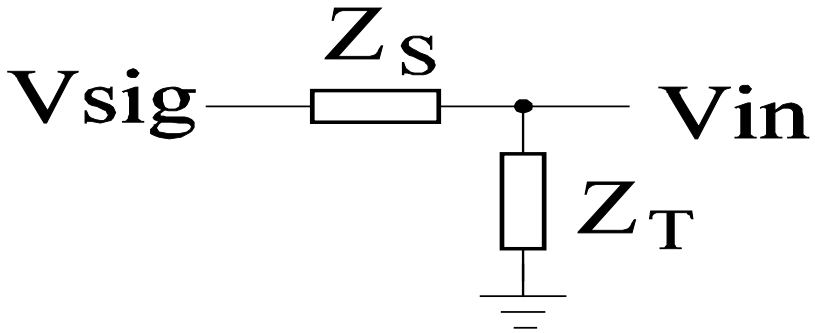
AARDVARC Parameter	Specification
Process node	130/65 nm
Channels	4/8
Sampling Rate	10-15GSa/s
Storage Samples/ch	32768
Analog BW	>2GHz
Dynamic Range	1.0 V
Time accuracy	<5 ps
Readout	Parallel/Fast Serial
ADC bits	12
Power/ch	100 mW

130nm ~5 x 5 mm

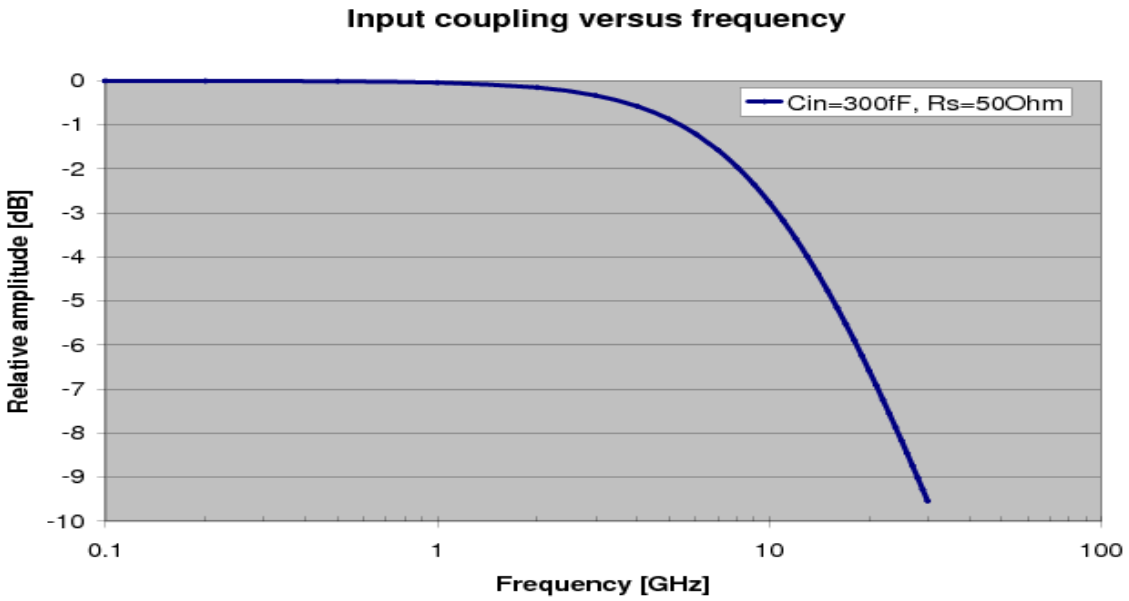
Constraint 1: Analog Bandwidth

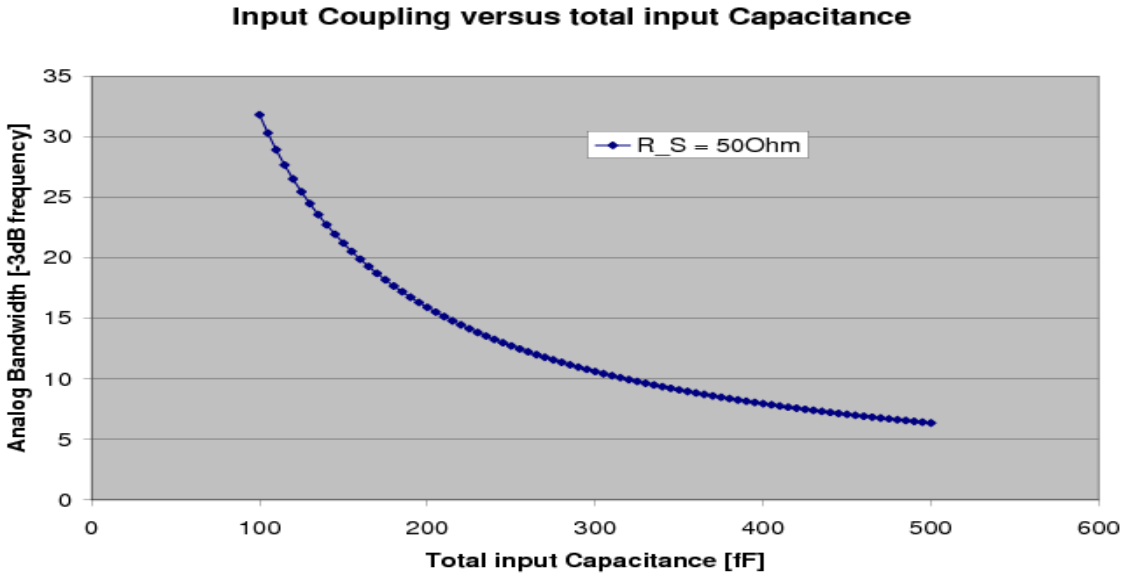
Difficult to couple in Large BW (C is deadly)





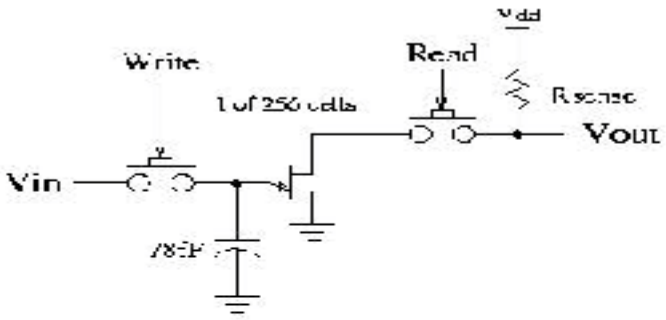
$f_{3dB} = 1/2\pi ZC$





Constraint 2: kTC Noise

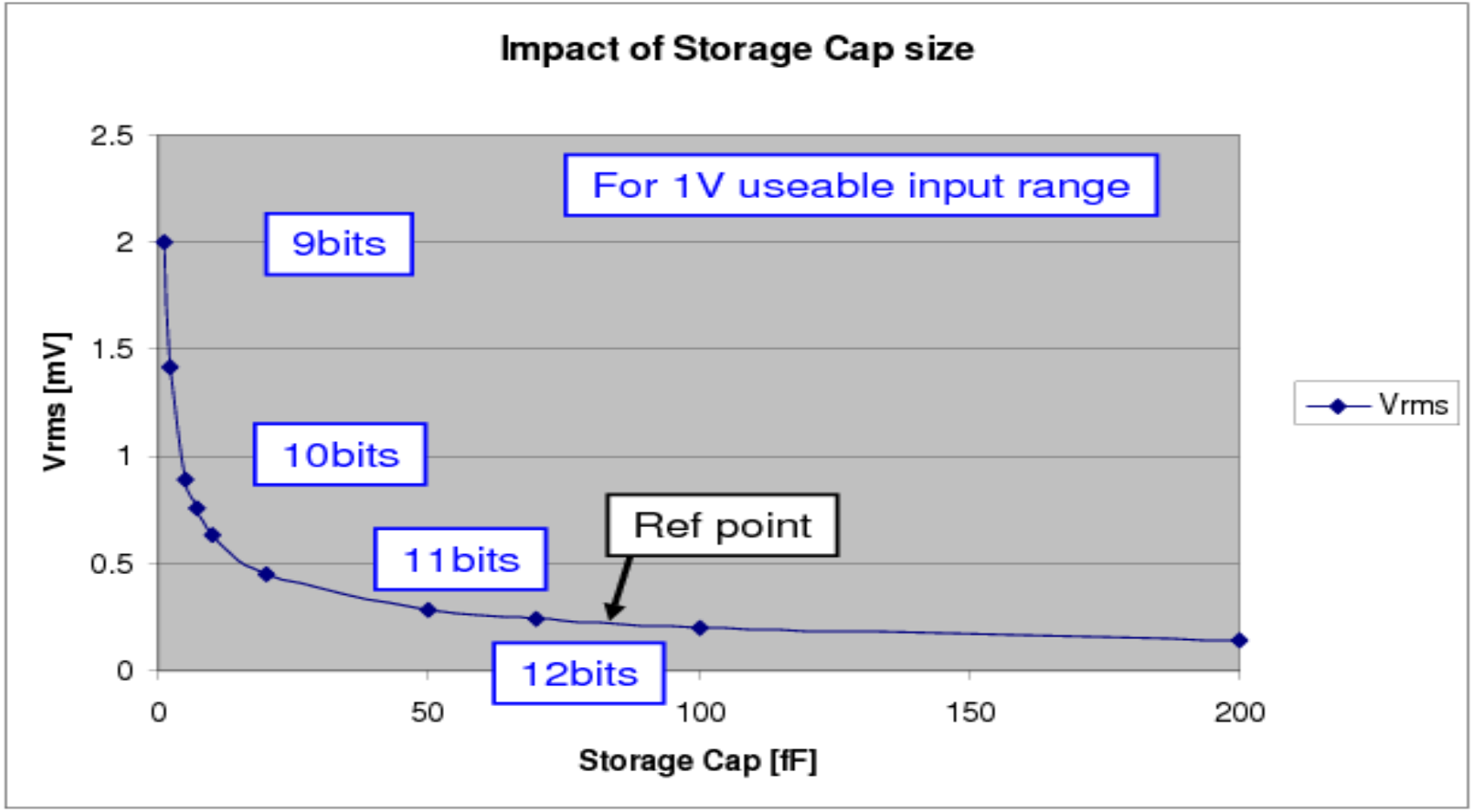
Want small storage C, but…



$$v_{rms} = \sqrt{\frac{kT}{C_{store}}} = 0.23mV$$

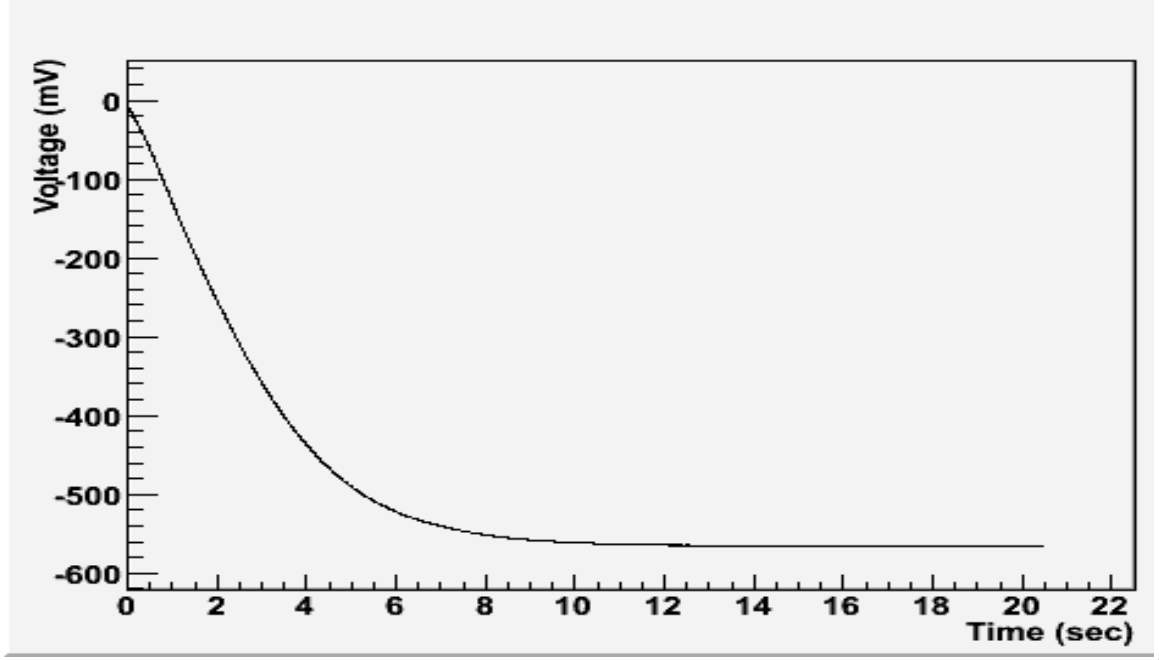
$$C_{store} = 78fF$$

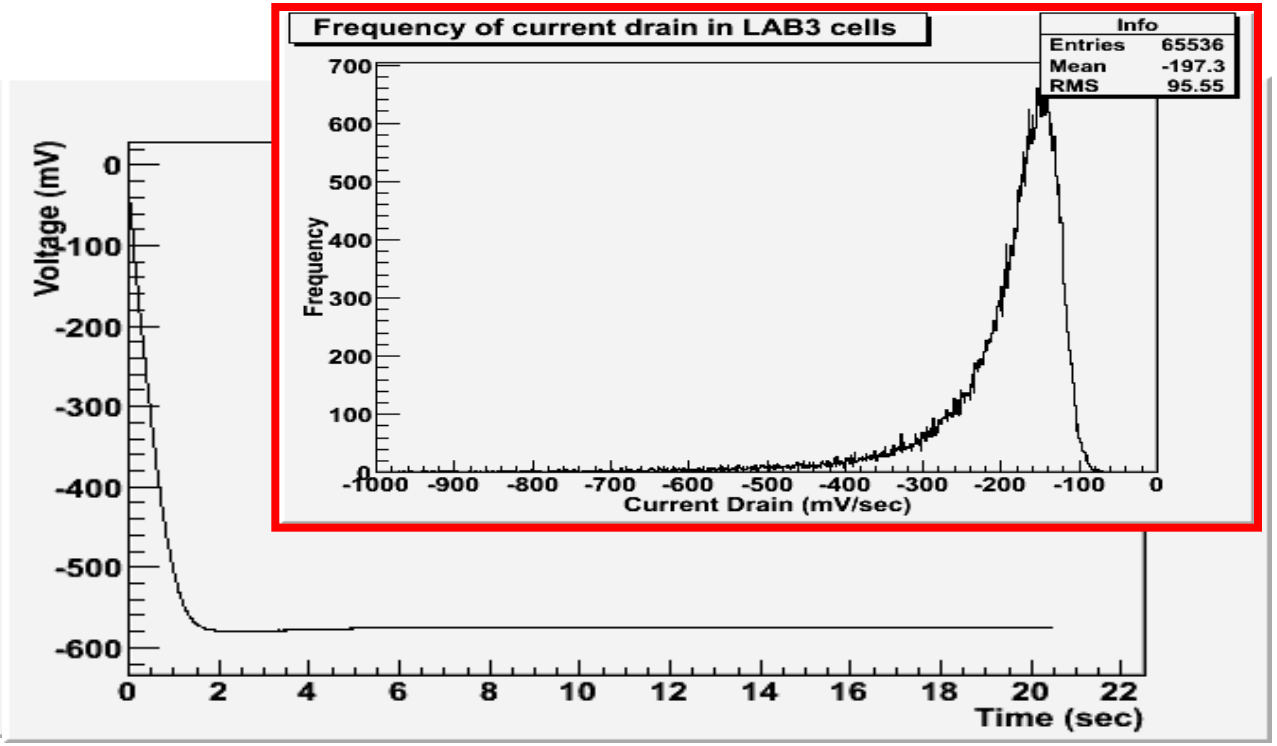
1mV on 16fF is only 100e- !



Constraint 3: Leakage Current

Increase C or reduce conversion time << 1mV



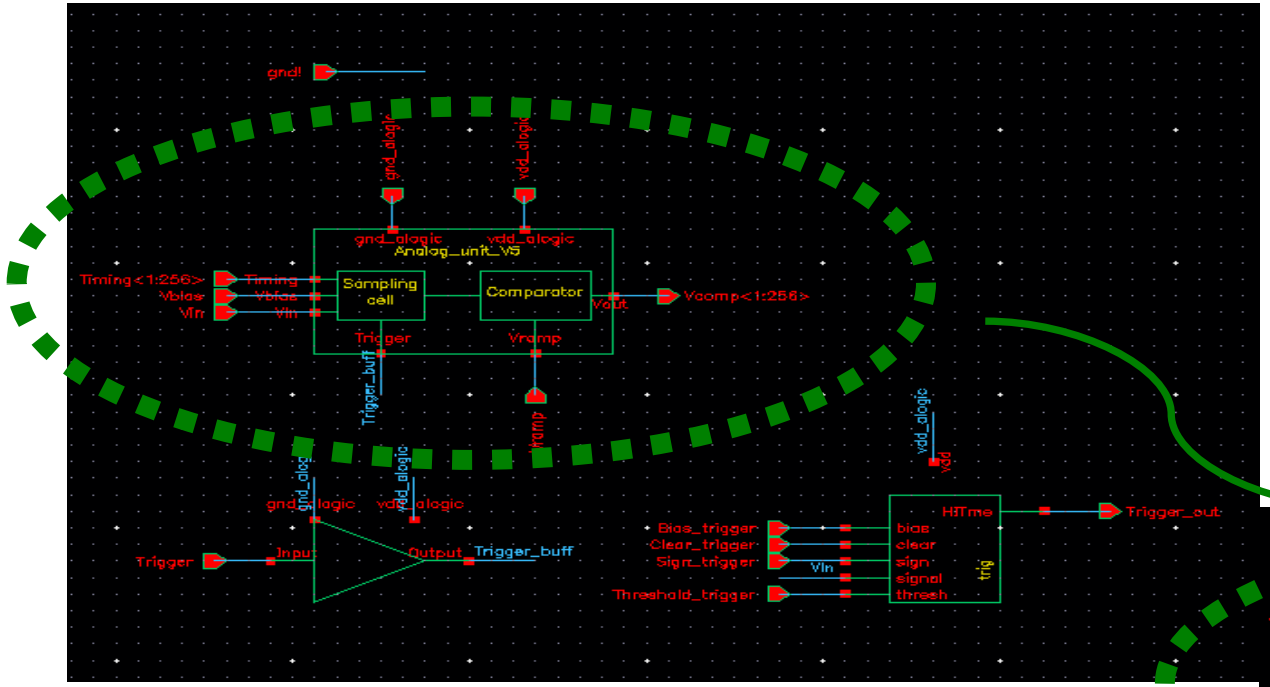


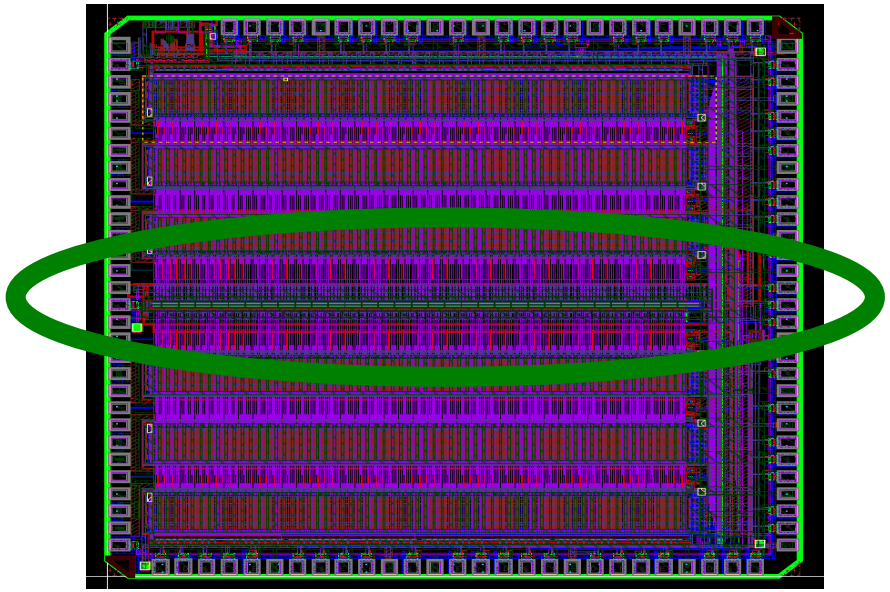
Sample channel-channel variation ~ fA → nA

leakage (250nm → 130nm)

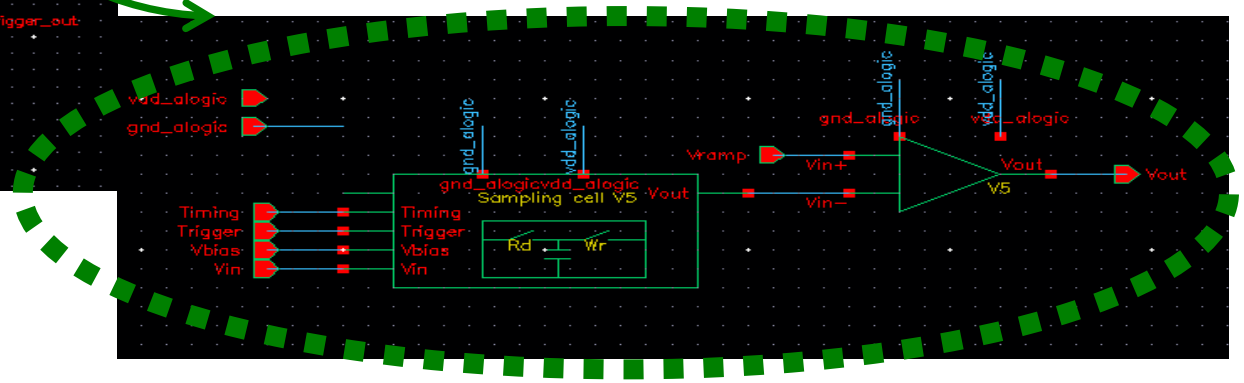
PSEC4: Sampling Analysis

Utilizing PSEC4's SCA as starting place
-Adjustable Sampling rate between 4-15 GSPS
-1.6 GHz bandwidth





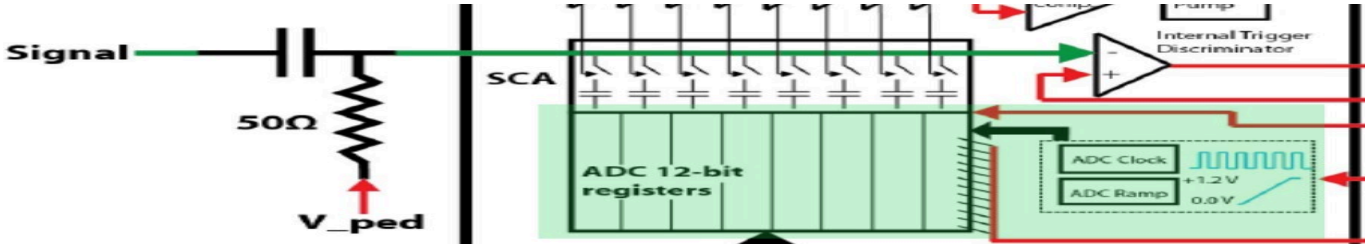
x256

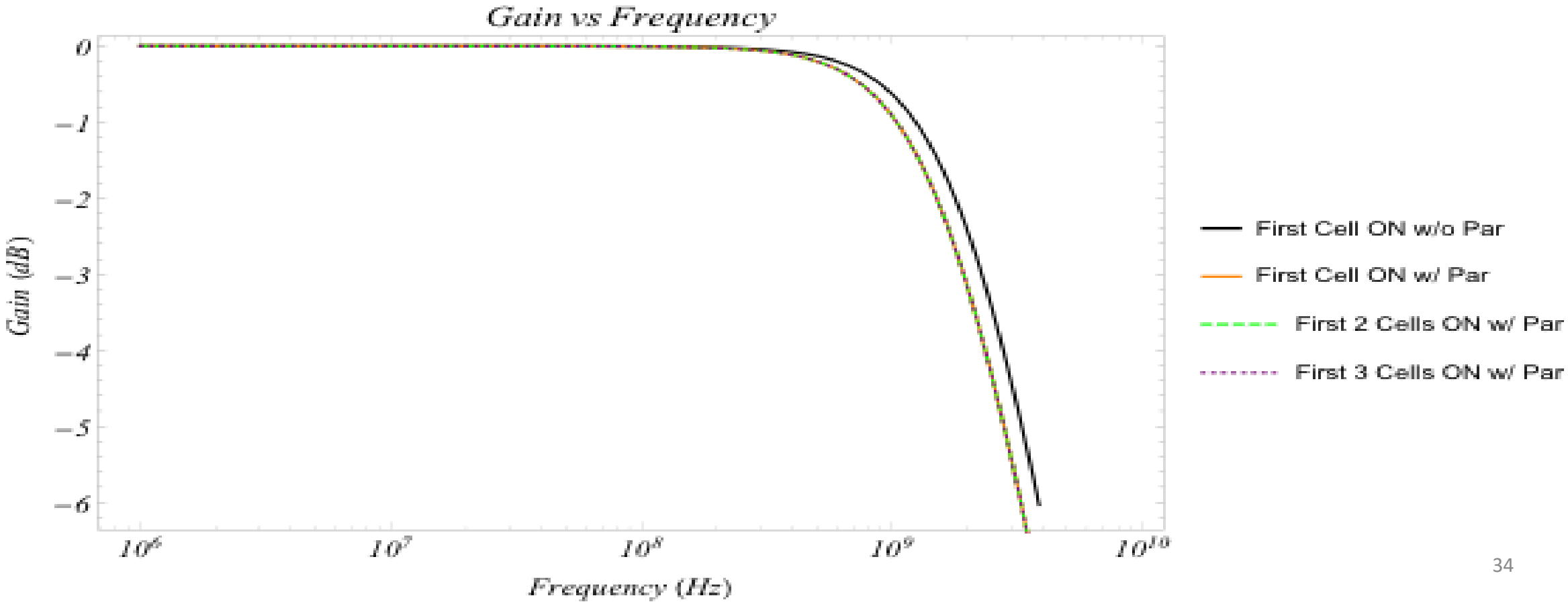


also
-0.13µm CMOS (IBM-8RF)
-10.5 bit DC dynamics

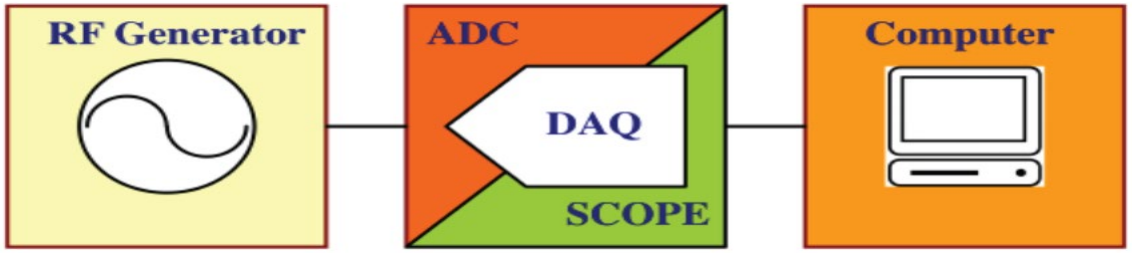
Equivalent Circuit

Multichannel sampling array



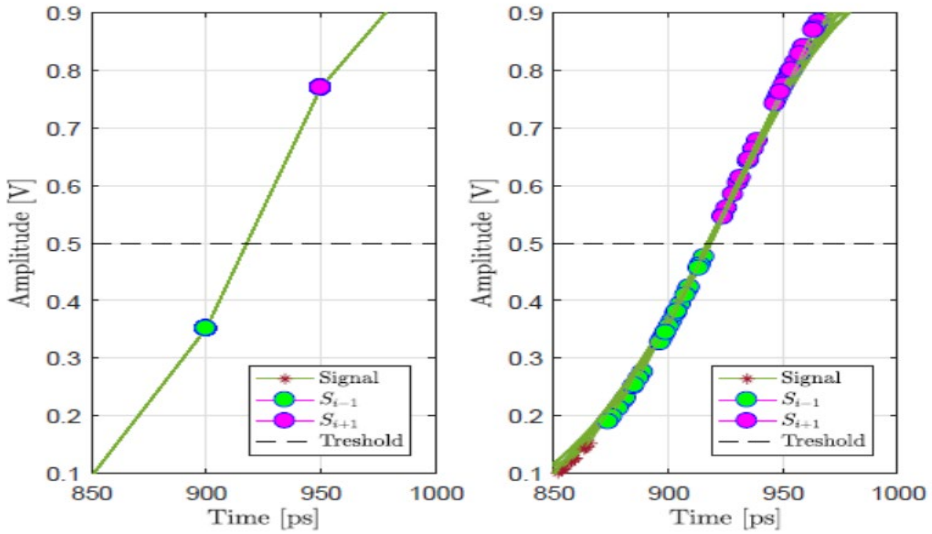


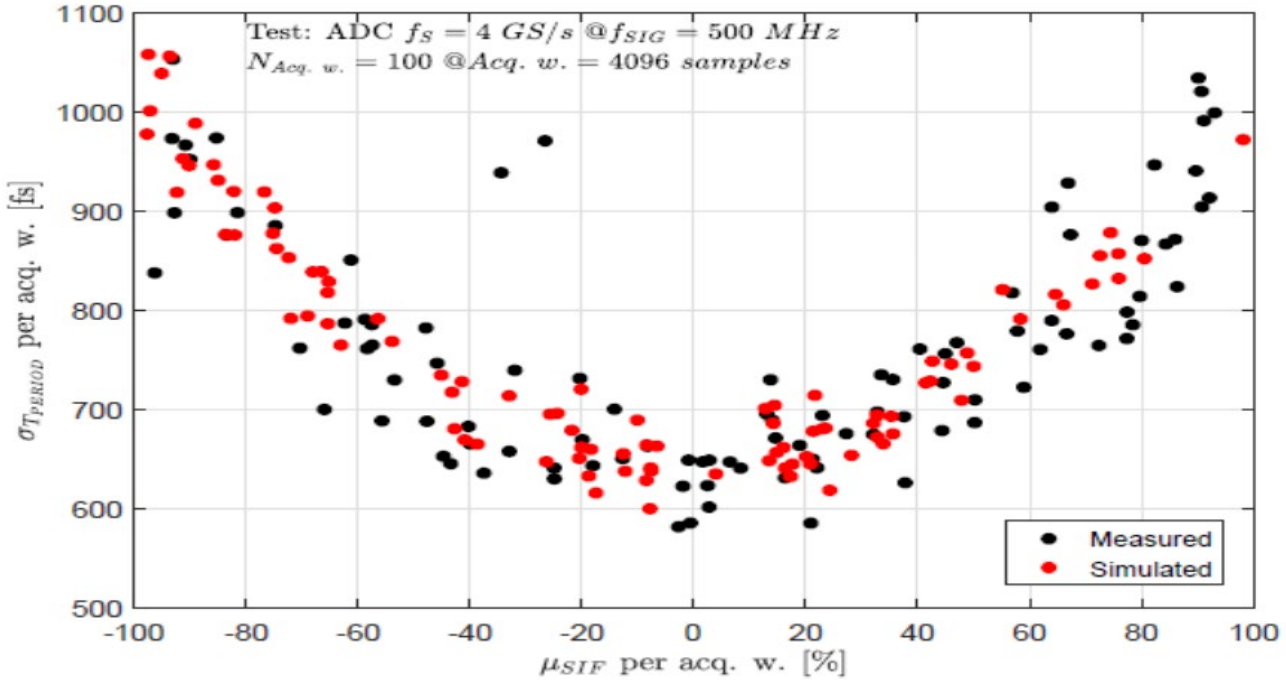
Understanding waveform sampling limits



DAQ	f_{SIG}	Measured $\sigma_{T_{PER}}$	Simulated $\sigma_{T_{PER}}$
SCO1	$3\ GHz$	$1.78\ ps$	$2.96\ ps$
SCO1	$6\ GHz$	$2.28\ ps$	$3.03\ ps$
SCO2	$3\ GHz$	$1.38\ ps$	$1.42\ ps$
SCO2	$4\ GHz$	$1.68\ ps$	$1.58\ ps$
SCO3*	$400\ MHz$	$5.68\ ps$	$5.86\ ps$
SCO3*	$500\ MHz$	$4.27\ ps$	$5.75\ ps$

* Signal amplitude equal to $0.475\ Vpp$.



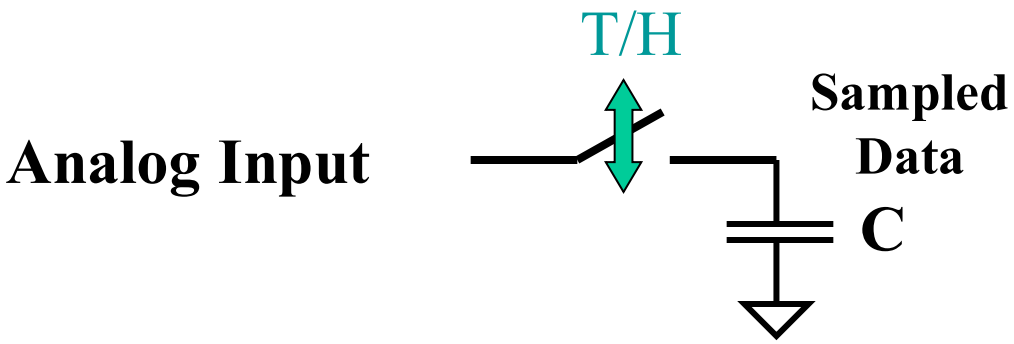


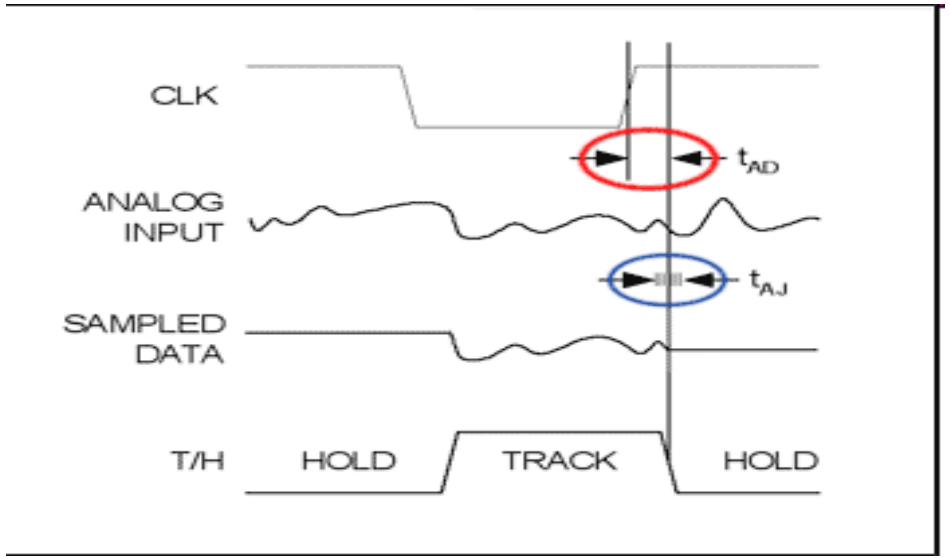
IEEE Trans. Nucl. Sci. **64 (2017) 1950-1962**.

Detailed simulation model developed to allow exploration of phase space – first need to verify results

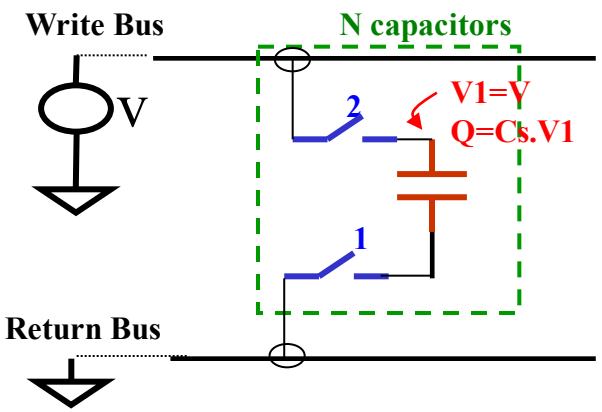
Underlying Technology

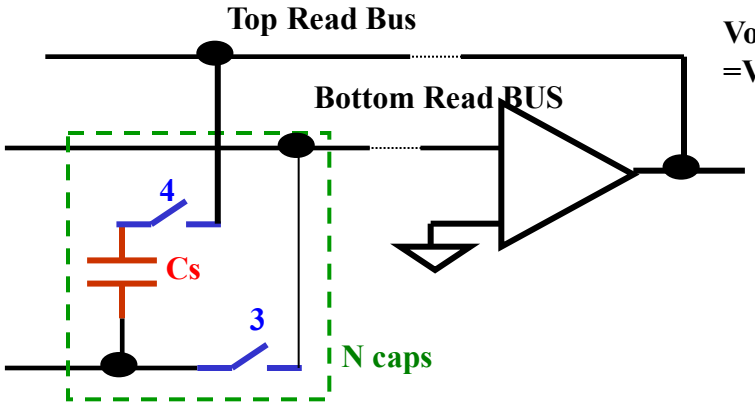
- Track and Hold (T/H)





- Pipelined storage = array of T/H elements, with output buffering

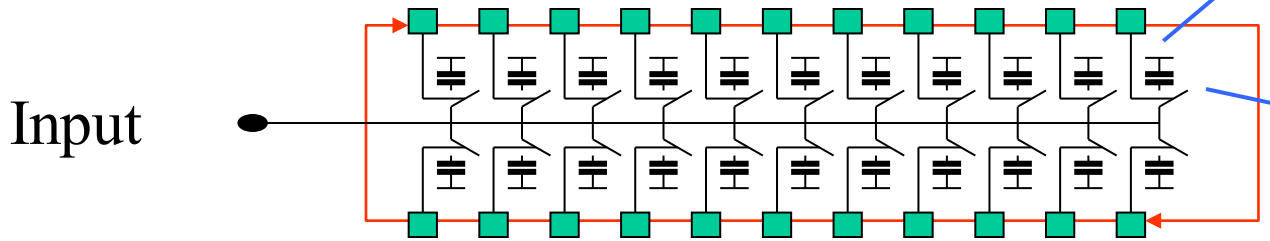


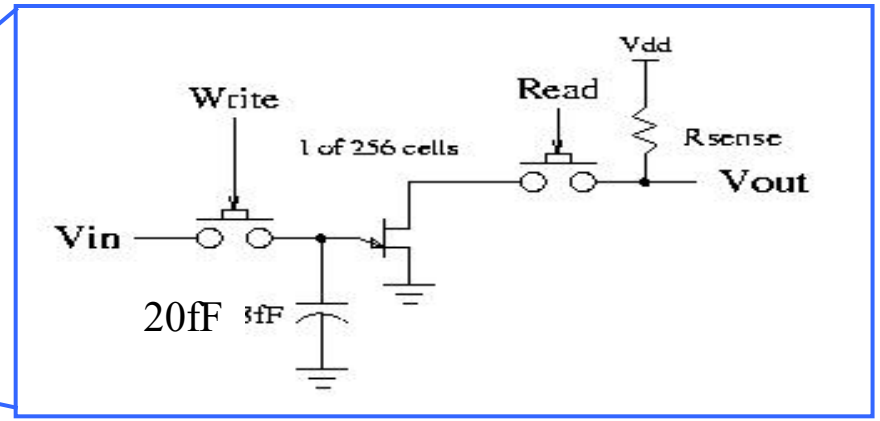


Vout=A / (1+A) * Q/Cs
=V1 * A/(1+A)

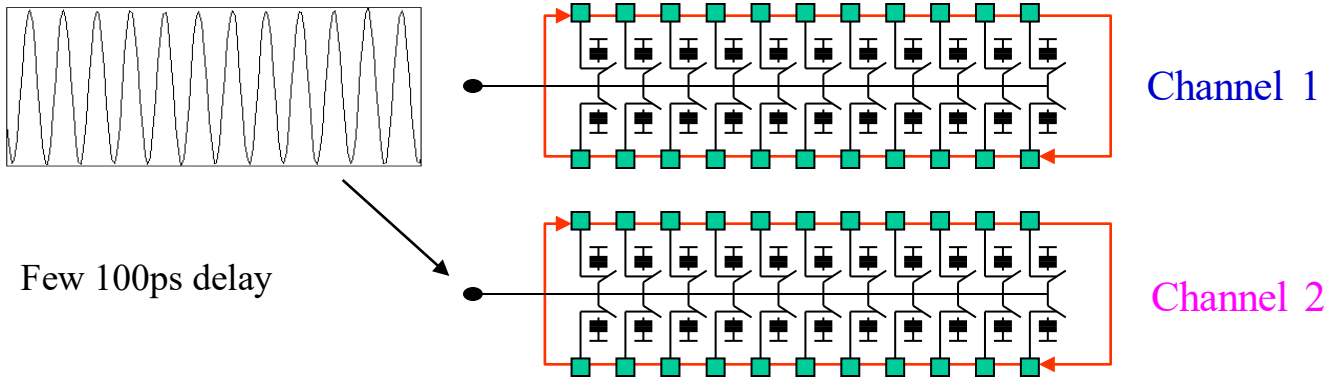
Switched Capacitor Array Sampling

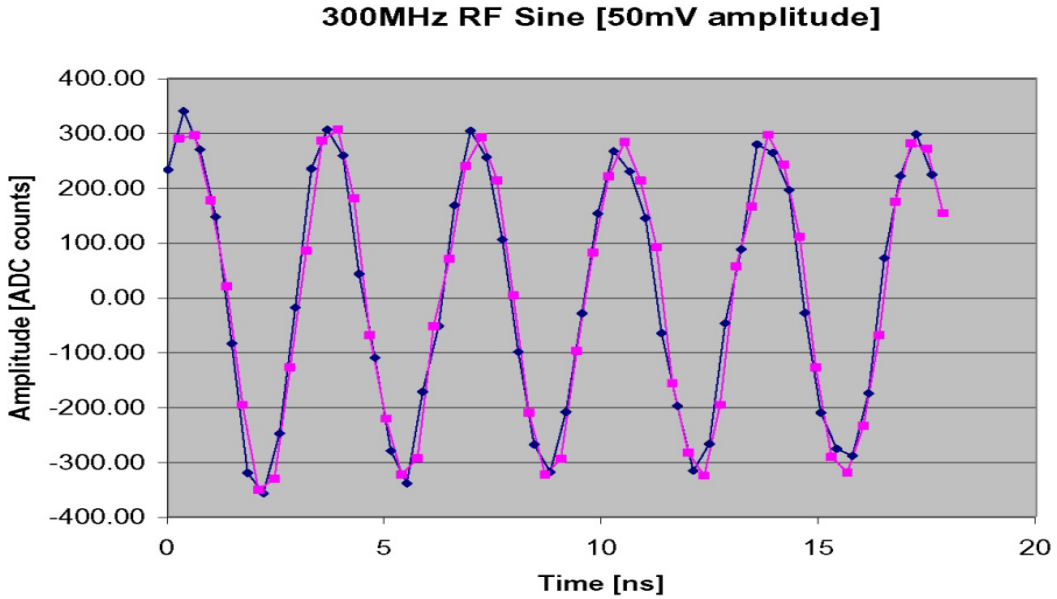
- Write pointer is ~few switches closed @ once





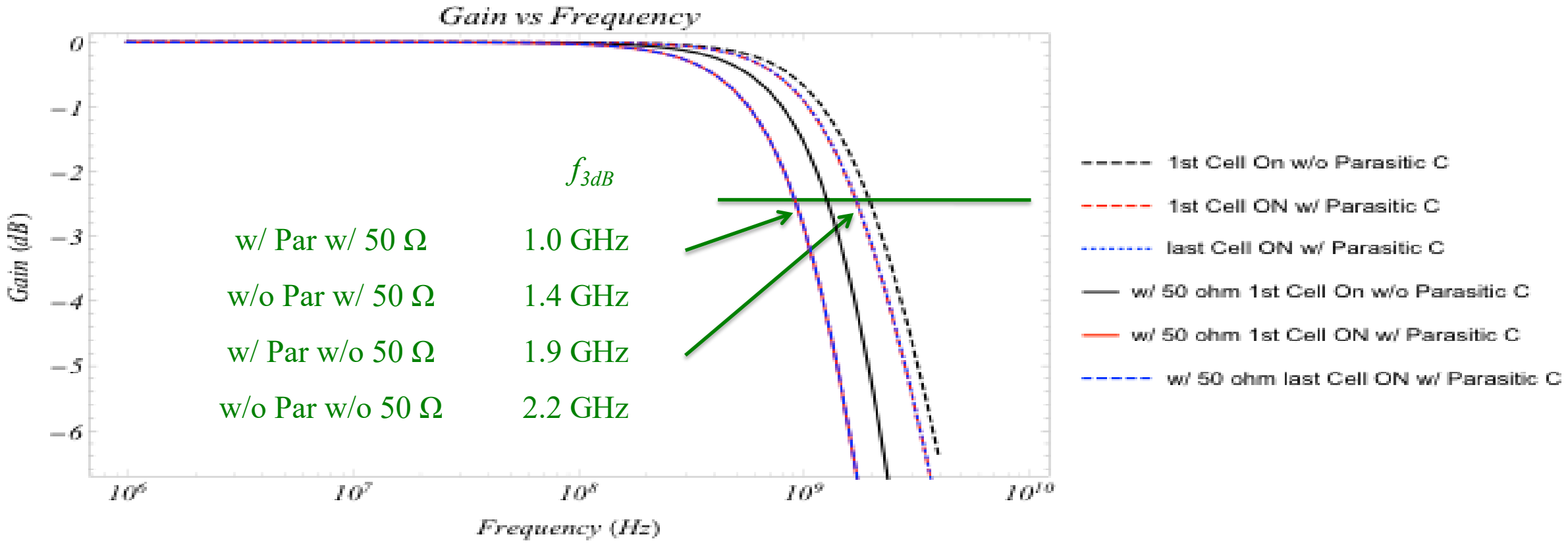
Tiny charge: 1mV ~ 100e$^-$





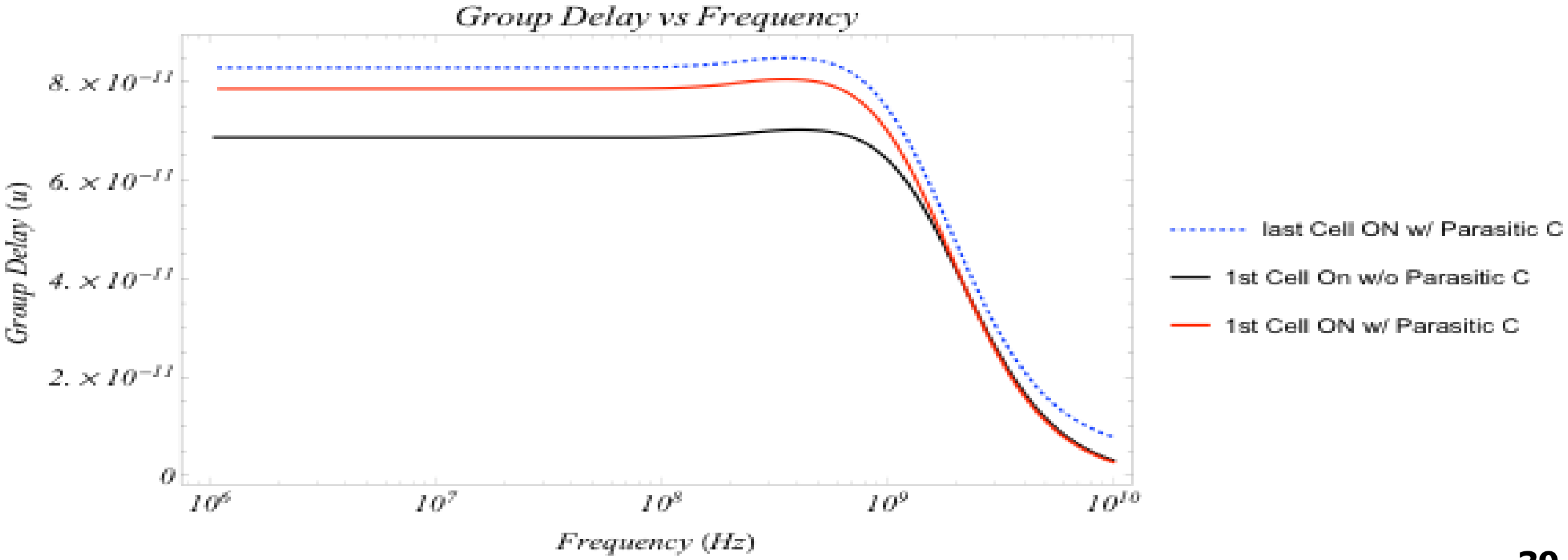
Simulation Results: Bandwidth for worst case operating bias point

Whether the 1st switch is on or the last, Gain is the same



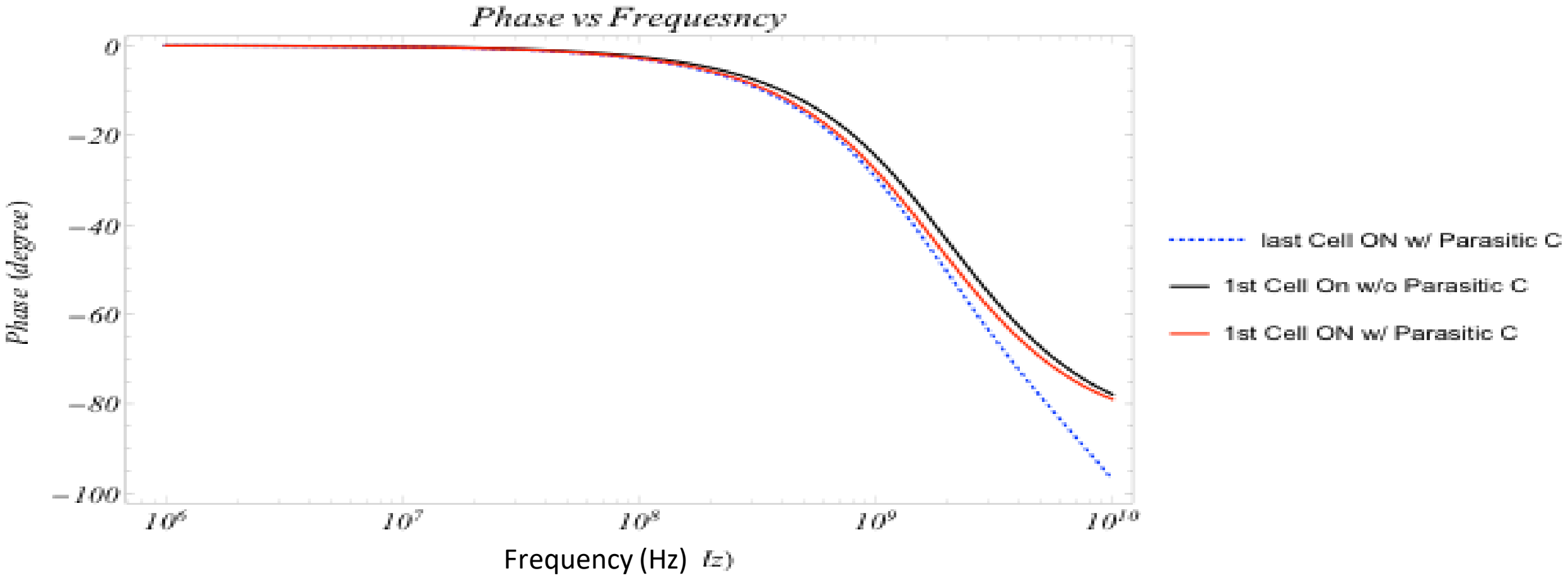
Simulation Results: Group Delay

Group Delay does vary depending which switch is on by ~25ps which puts a constraint on sampling time window



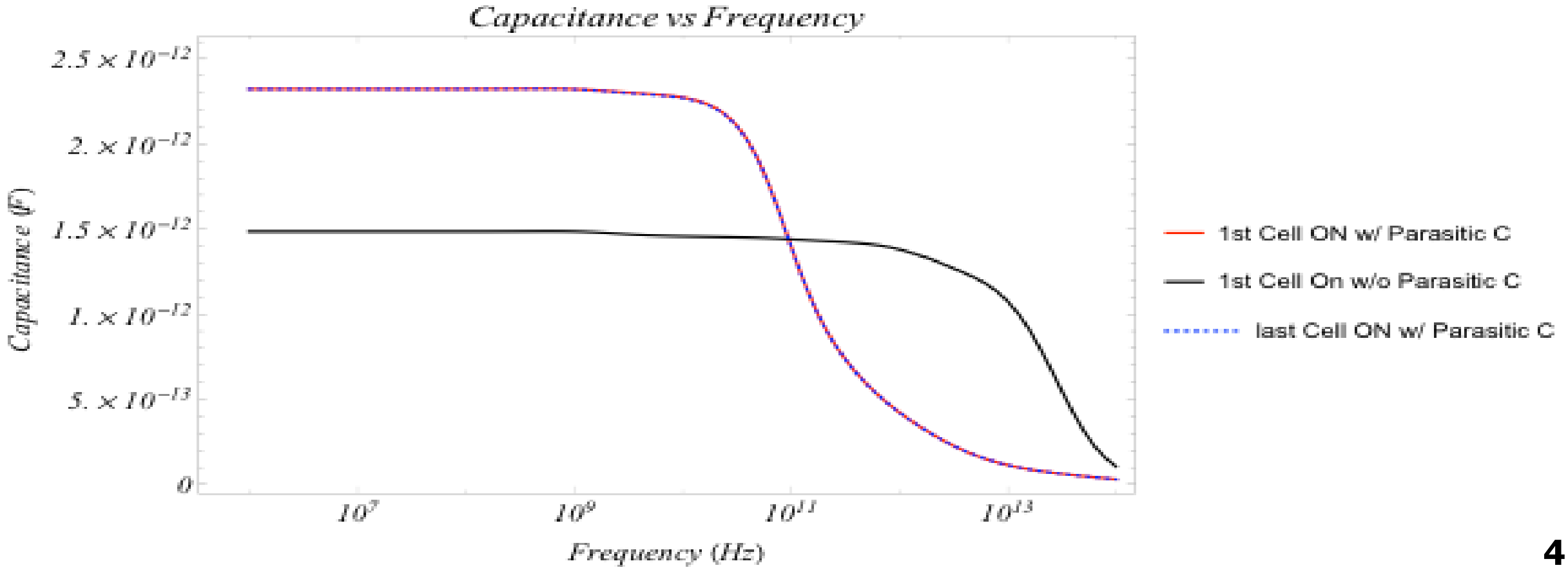
Simulation Results: Phase

- At higher frequencies Phase vs freq behavior is also different and depends on which switch is on

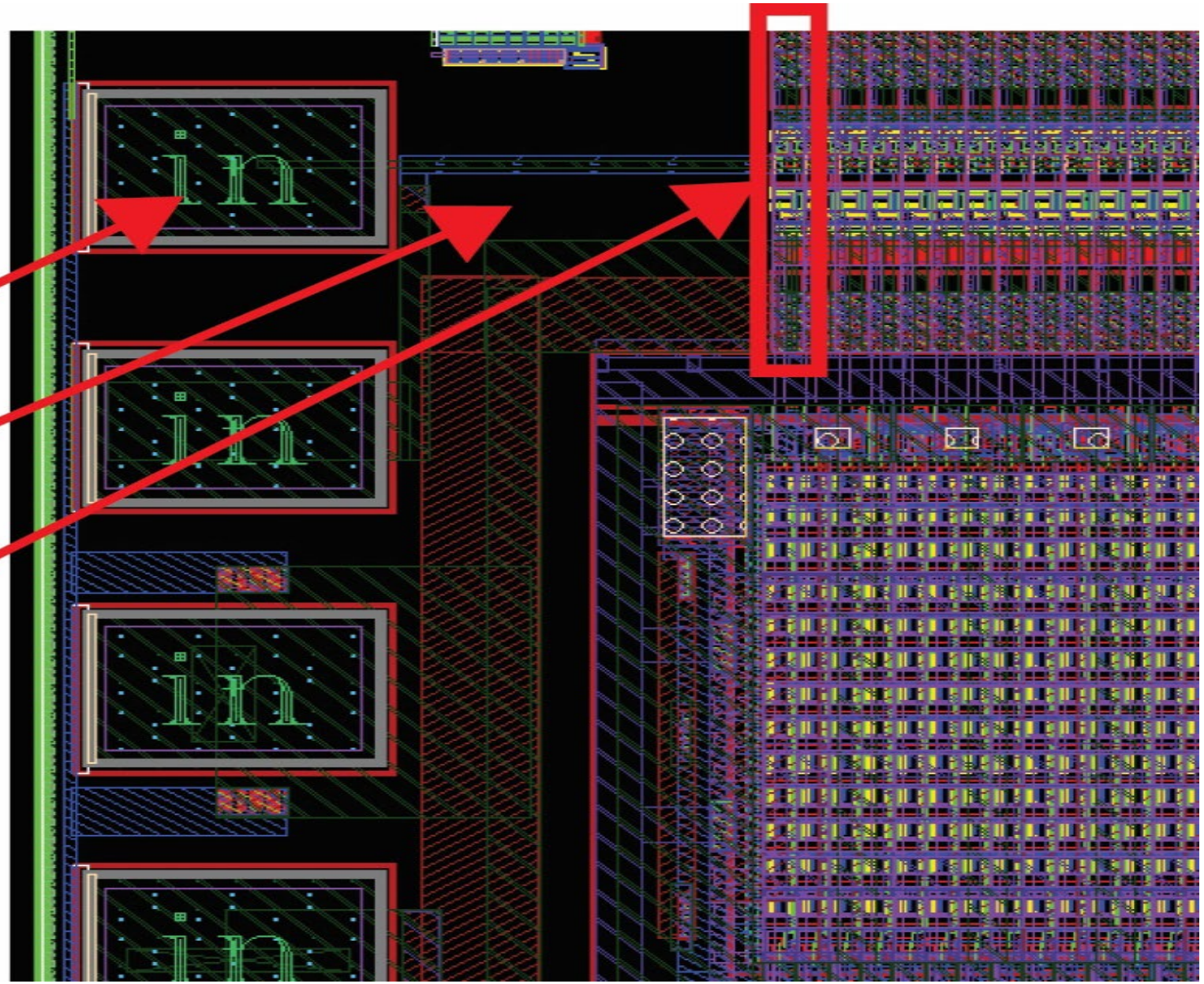


Simulation Results: Capacitance

Capacitance is 2.2 pF and does not dependent on which switch is on



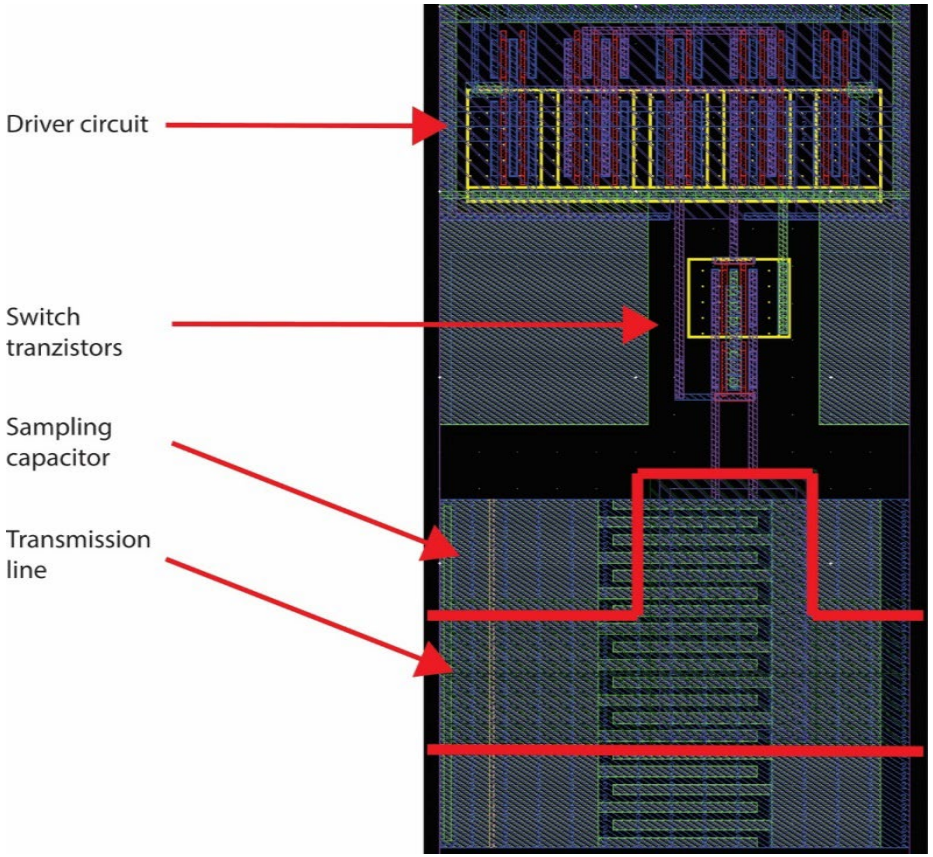
PSEC4 Analysis: Single Sampling Cell



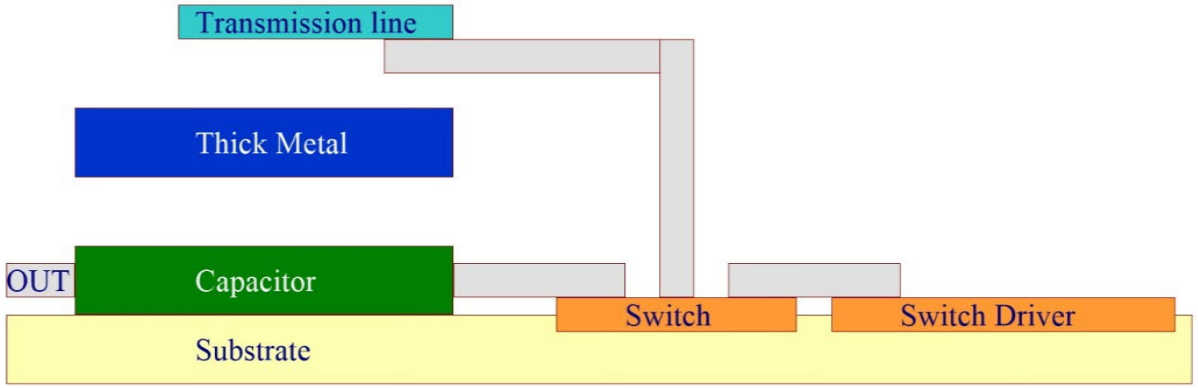
PSEC4 Analysis: Single Sampling Cell

Structure & Layout

Top view

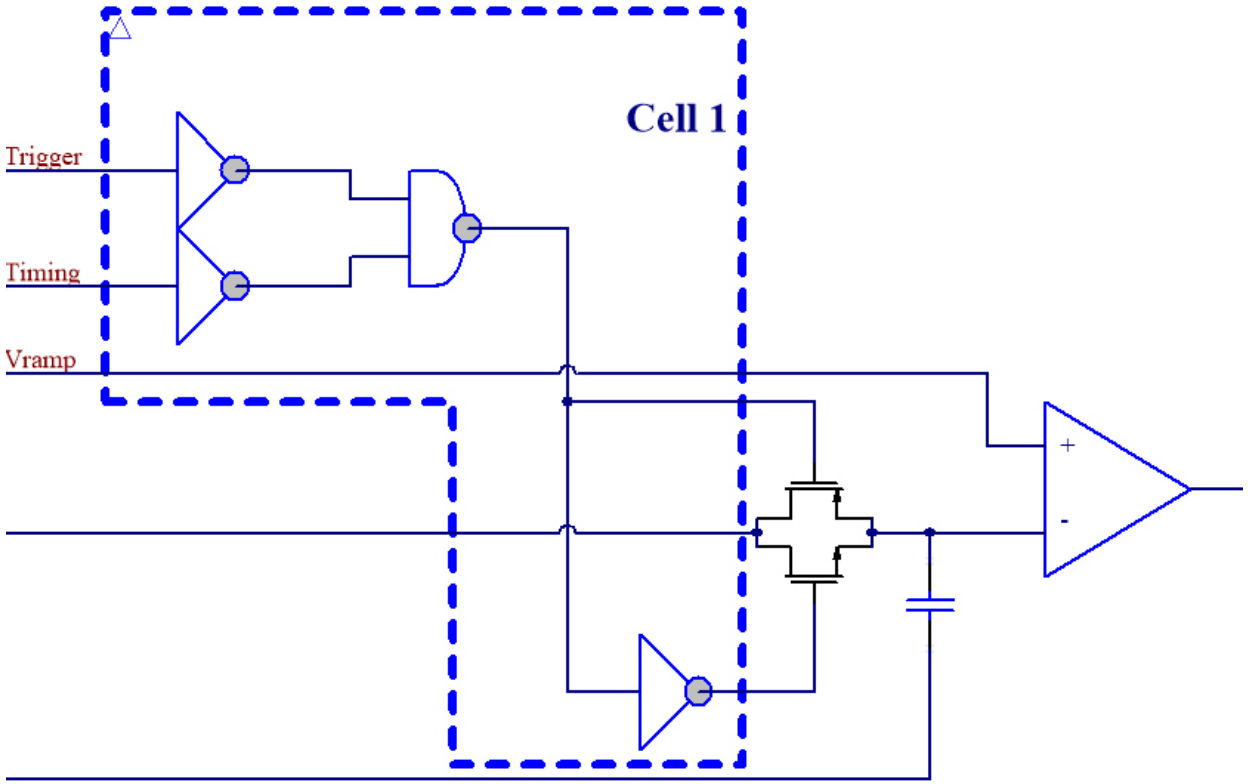


Side view



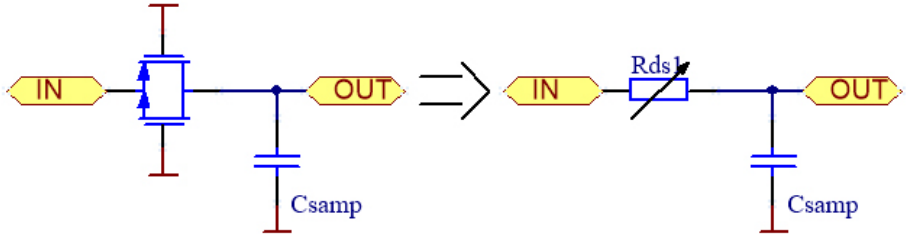
Single Sampling Cell Coupling

Simplified Schematic



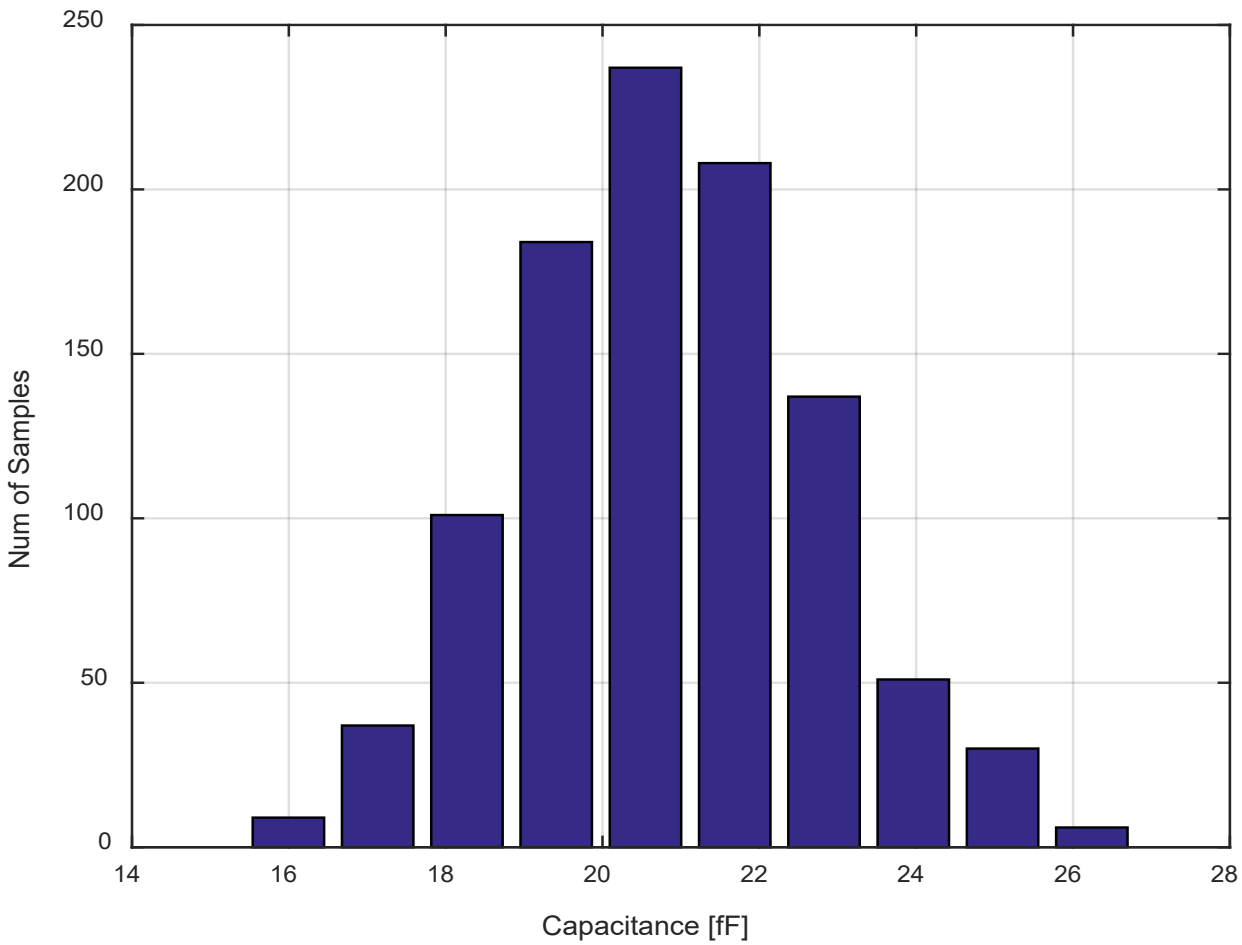
- Driver circuit
- Switch with n-p FET pair
- Sampling capacitor
- Comparator as load

Switch & Sampling Capacitor Equivalent Circuit



- Check Csampling capacitance
- Identify Ron and Roff

Sampling Capacitor Spread

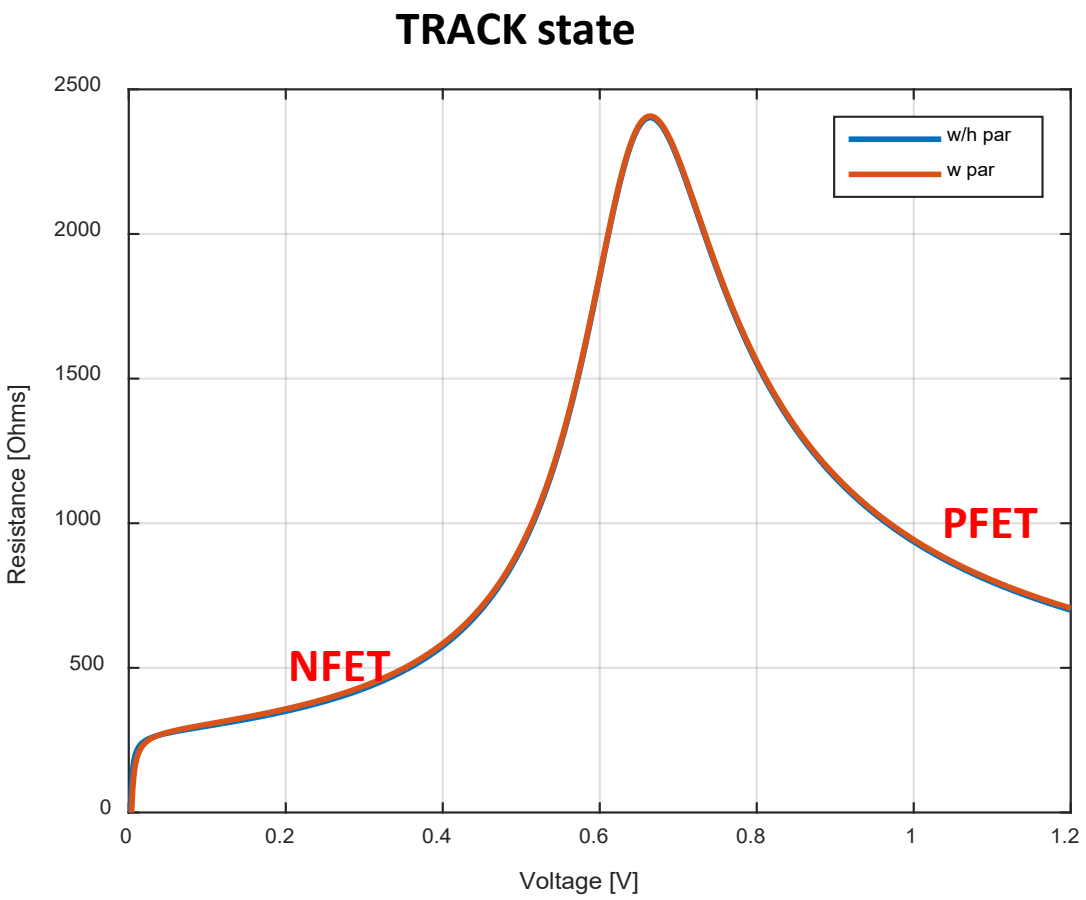


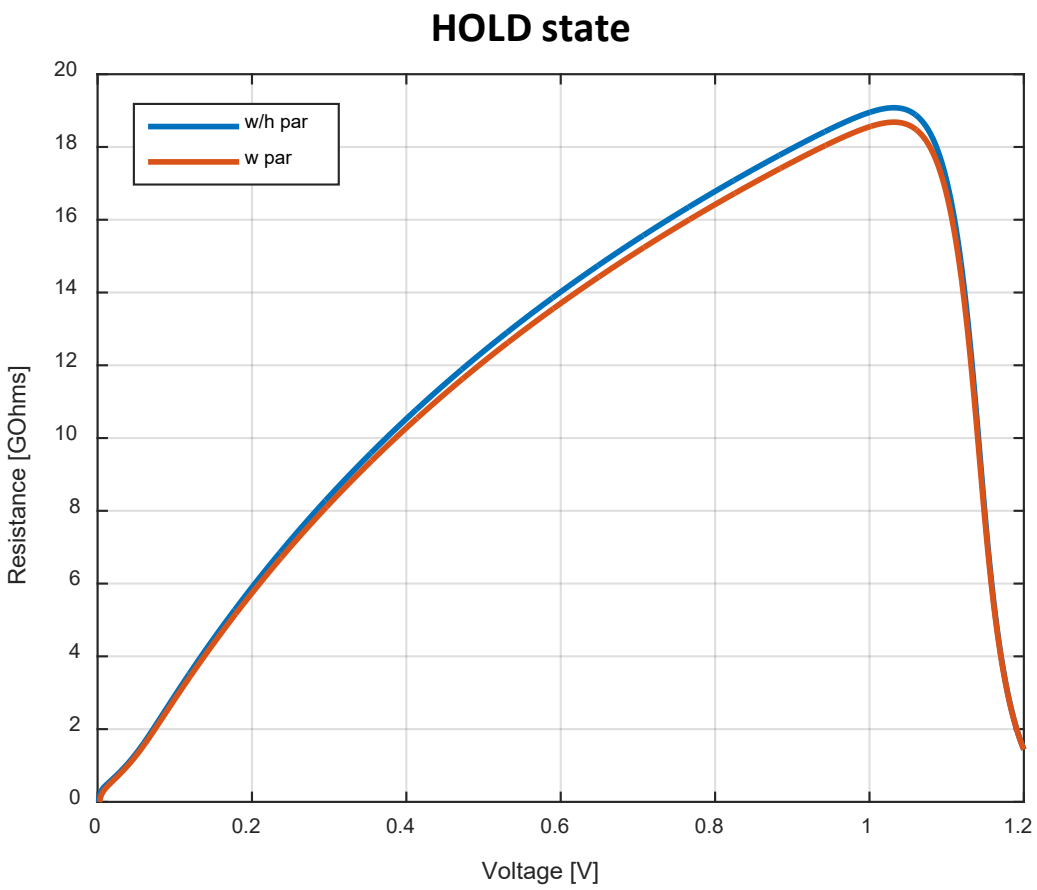
Monte Carlo with process variation and mismatches shows a discrepancy between Csampling Schematic (13.5 fF) and Measured mean (20.27 fF).

The Spread is about 1.9fF which makes the Capacitor tolerance at about 9.3%

Num. of Samp.	MEAN	STD	MIN	MAX
1000	20.27 fF	1.89 fF	14.86 fF	26.24 fF

Pass Transistor (Switch) Resistance



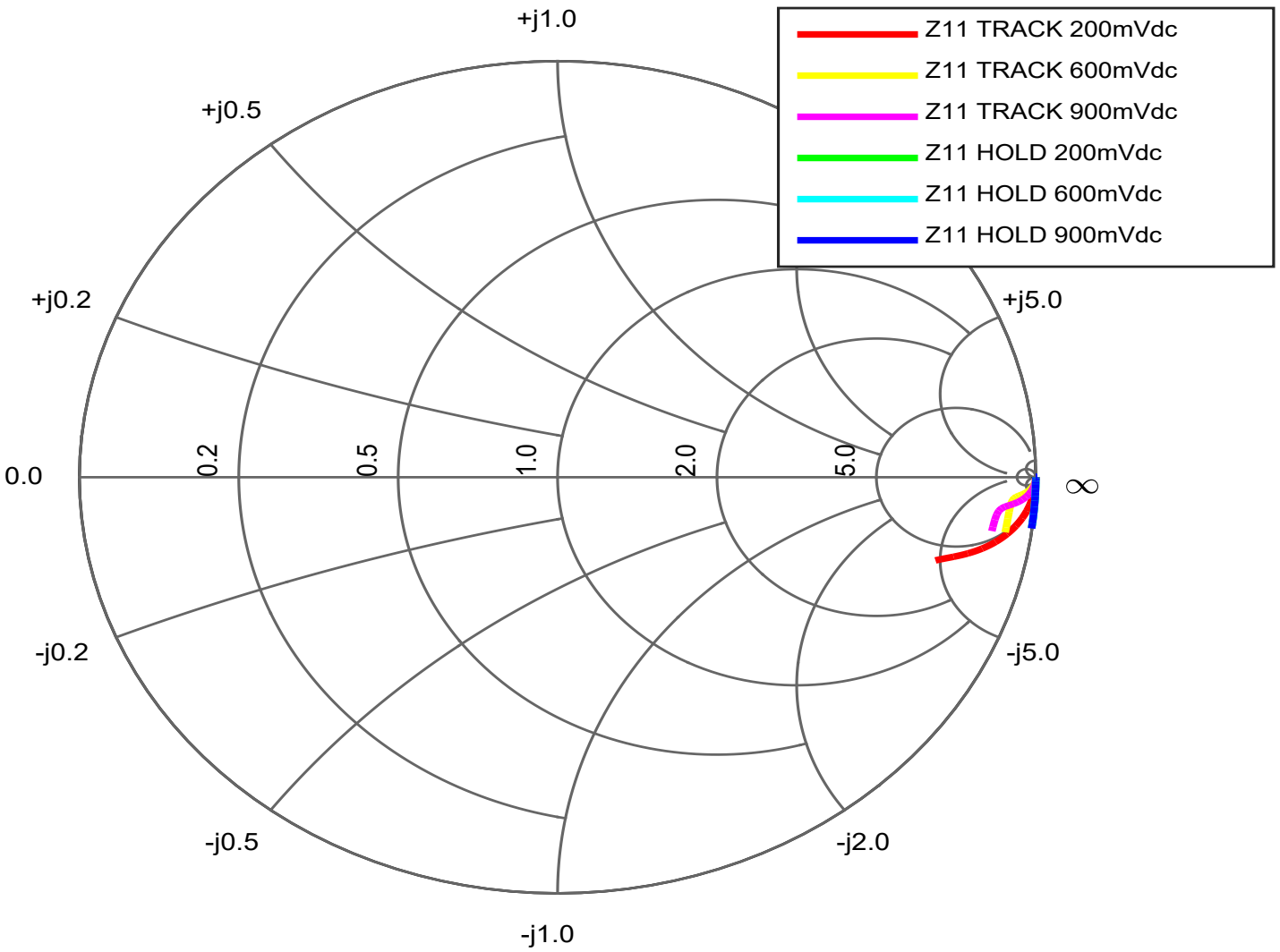


- **Ron=2.4k @665mVdc**
- **Roff is in GΩ**

- **The PFET and NFET are not matched and Ron varies considerably**

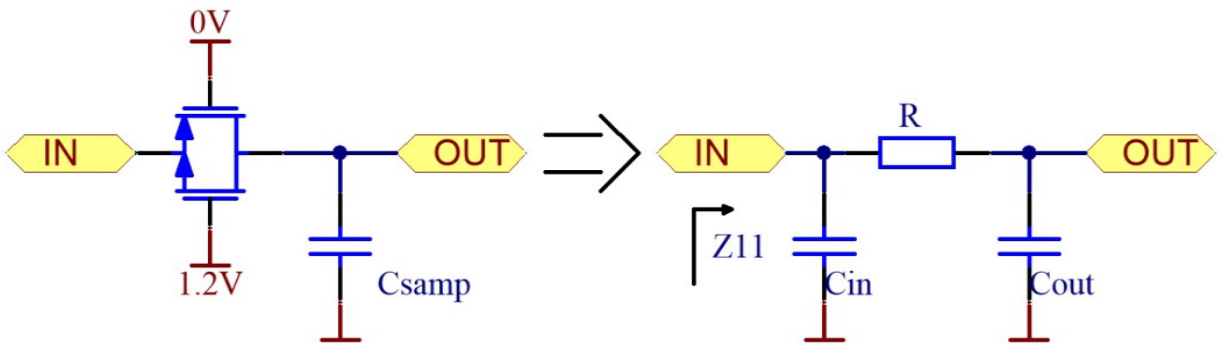
Frequency Analysis

Performance: S(Z)-parameter



The input impedance is high and it is capacitive.

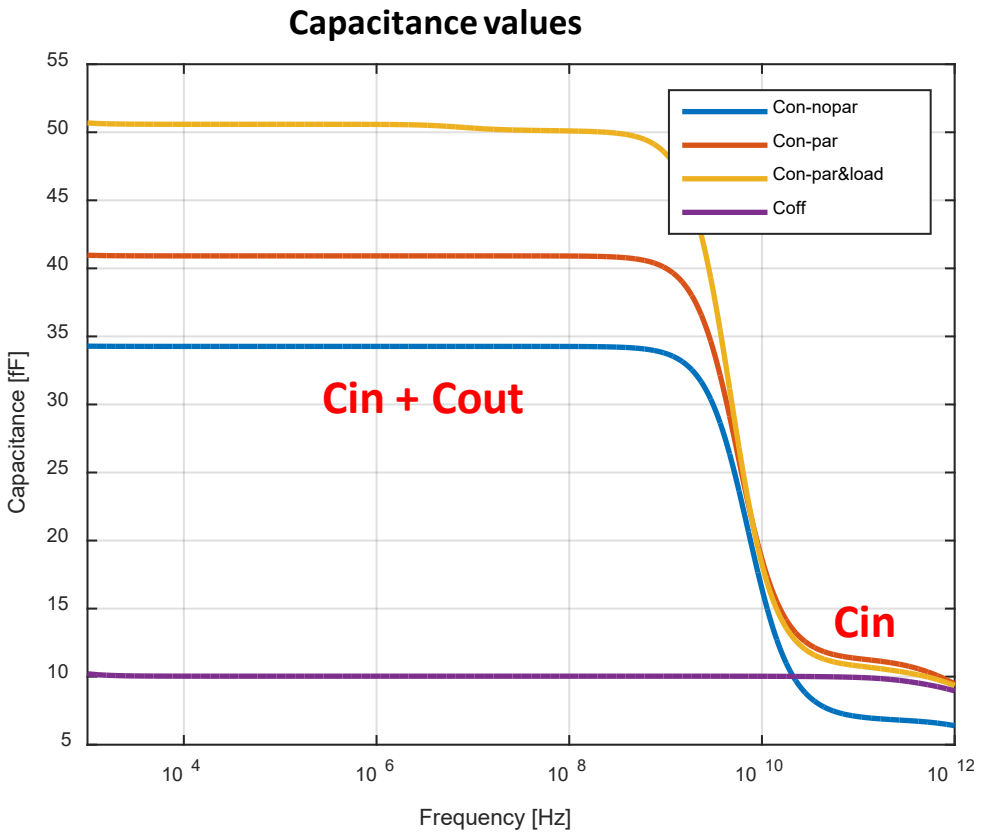
Input coupling analysis



$$Z_{11} = \frac{1 + sC_{OUT}R}{s^2 C_{IN} C_{OUT} R + s(C_{IN} + C_{OUT})}$$

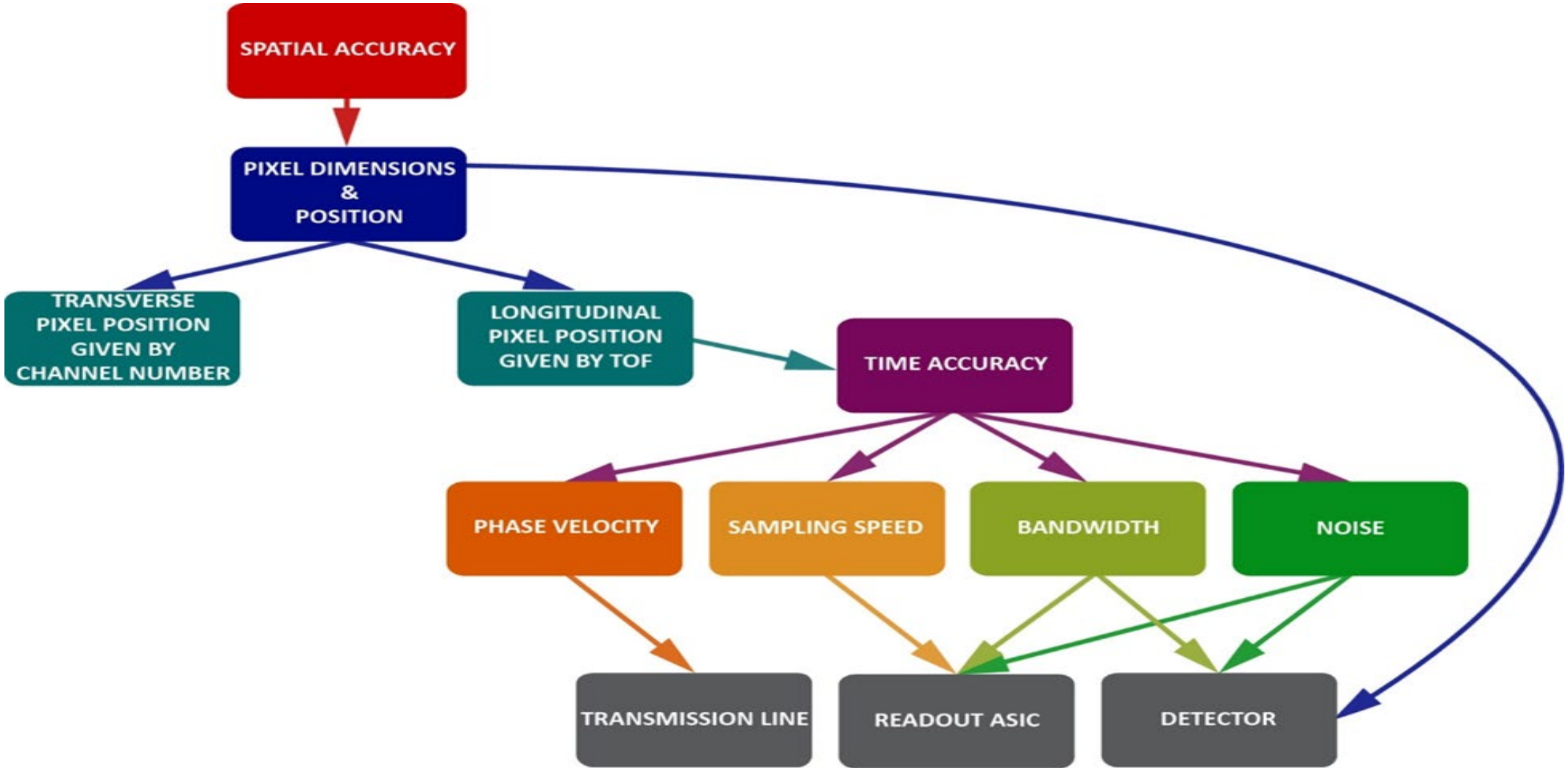
The transfer function parts:

- input parasitic capacitance of the transistor plus capacitance of the transmission line section.
- Series resistance of the transistor channel (Rds)
- Output capacitance which is formed of the parasitic capacitance of the transistor, sampling capacitor and load capacitance



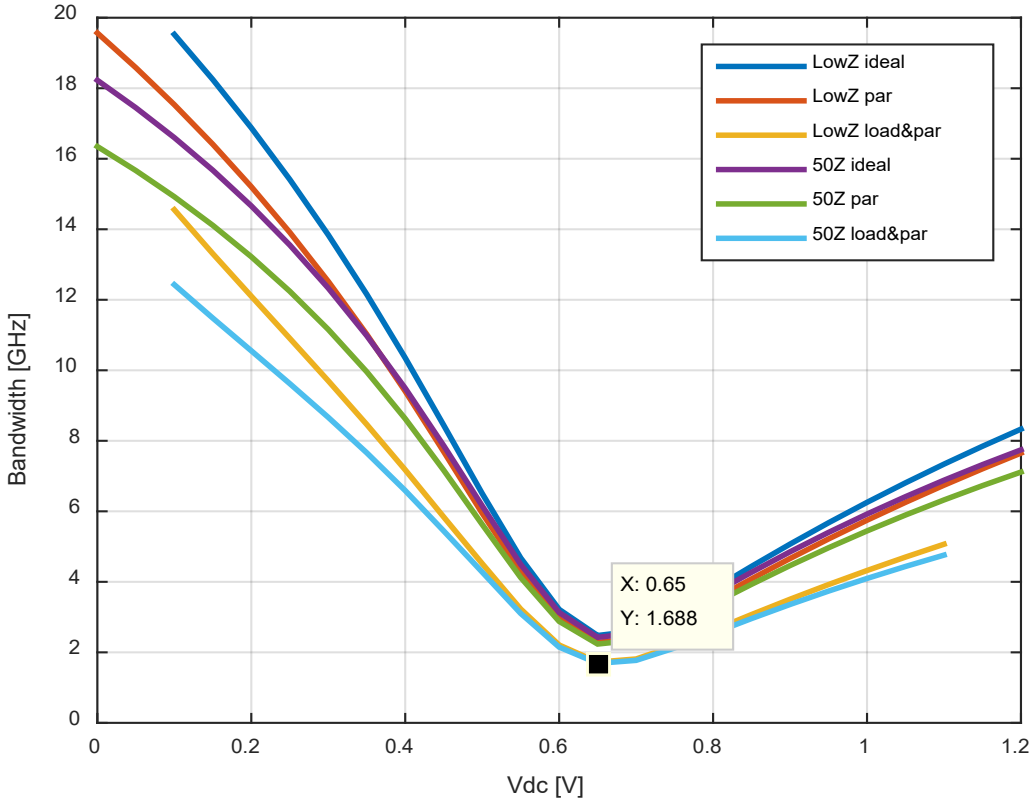
Capacitance	Value [fF]
Cin_open	8fF
Csw_out	10fF
Csamp	20.3fF
Cload	13fF

Overall optimization/interplay

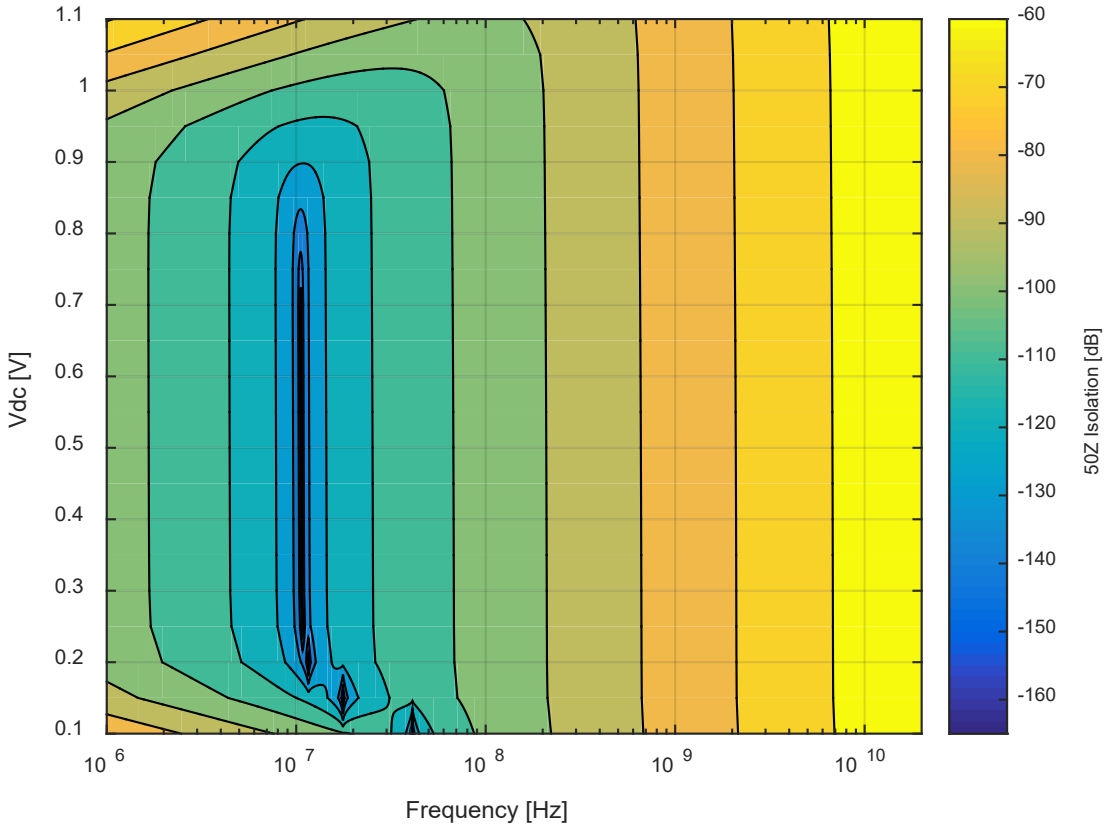


Small signal frequency response

Bandwidth



Isolation

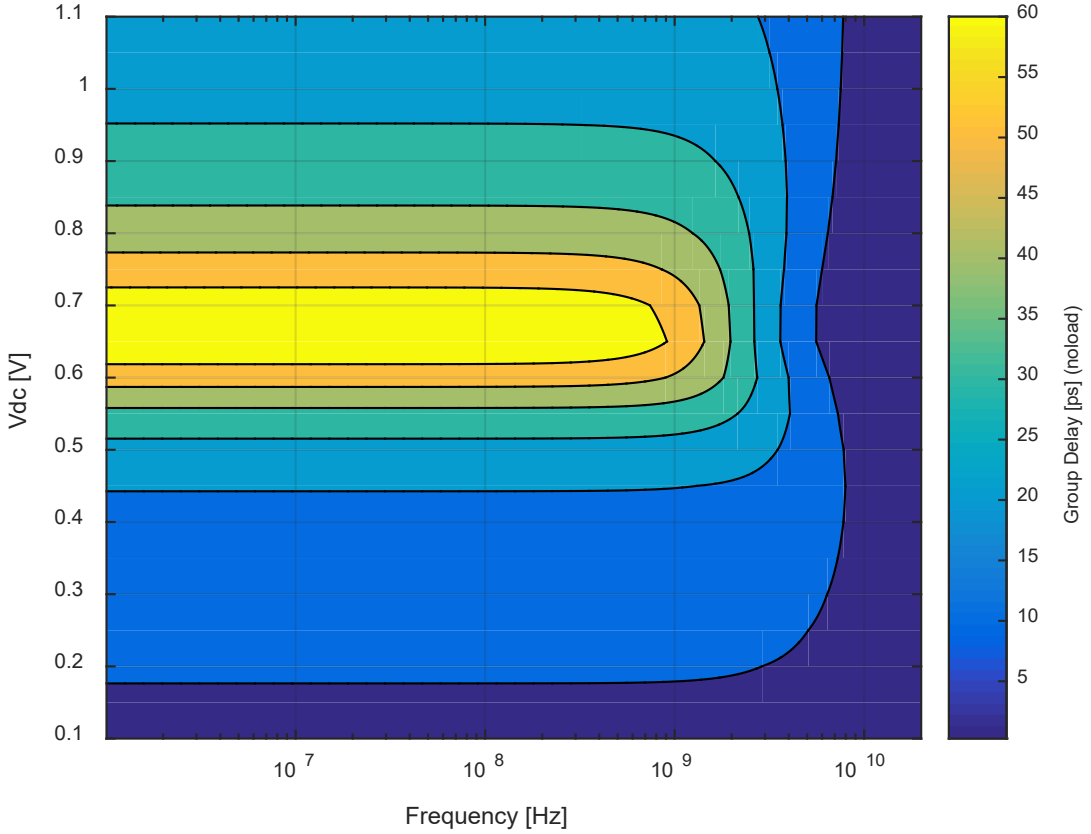


- **BWworst≈2.3GHz @665mVdc @LowZ drive**
- **BWworst≈1.7GHz @665mVdc @50Ω drive**

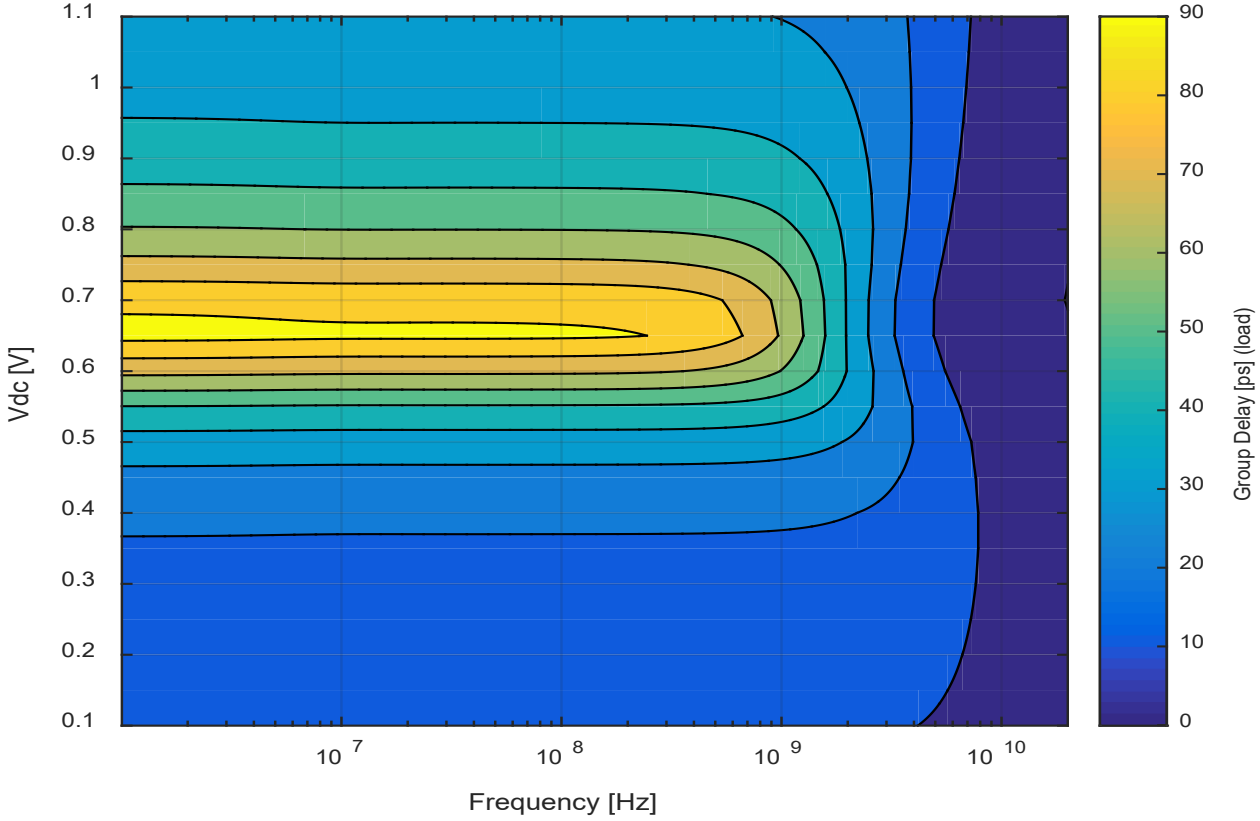
- **Isolation is over 60dB over all parameter space**

Small signal phase analysis

Group Delay without the load

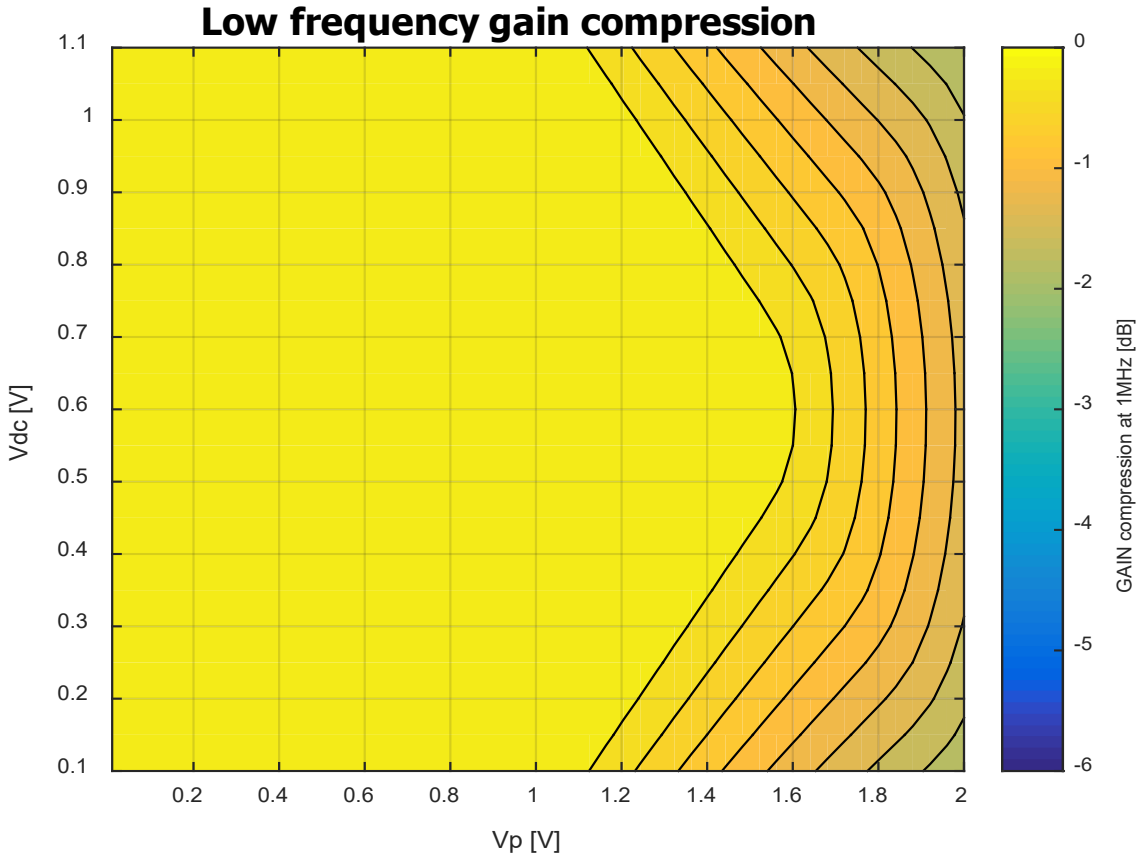


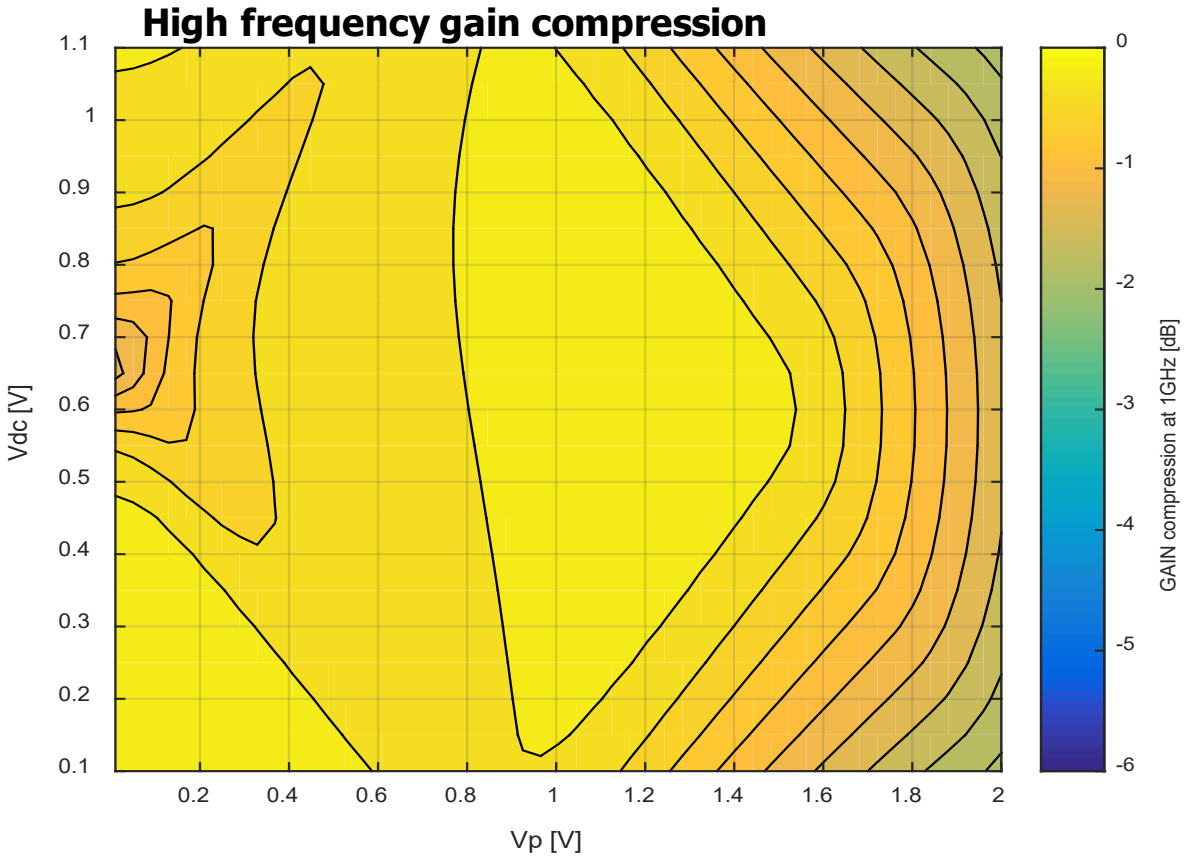
Group Delay with the load



➔ **Large group delay variation points to large distortion**

Large signal response (I)

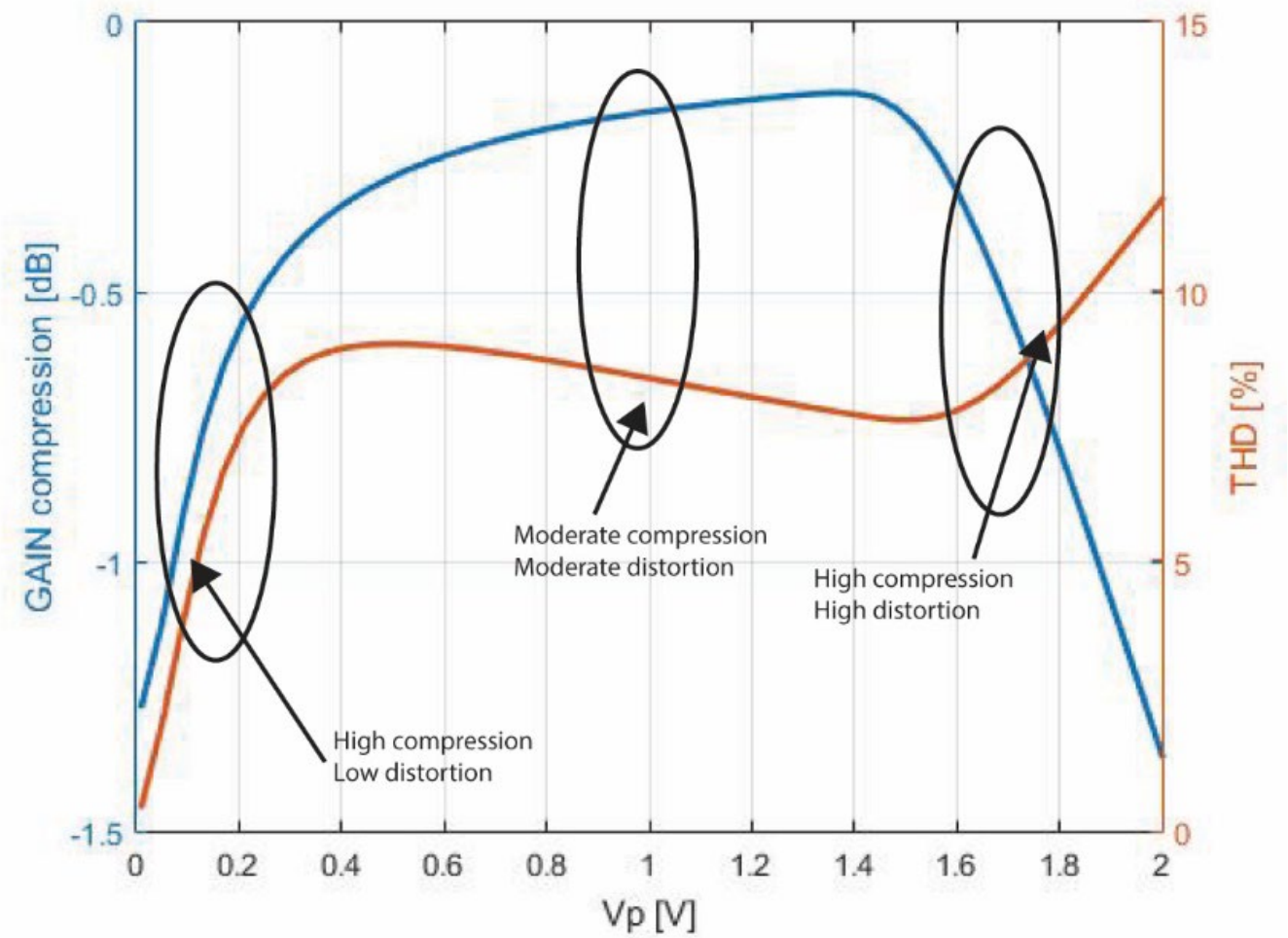




- **Full dynamic range at low frequency, compression appears when reaching the voltage threshold of the PN junctions at the drain/substrate barrier.**
- **Gain compression at lower and higher amplitudes**

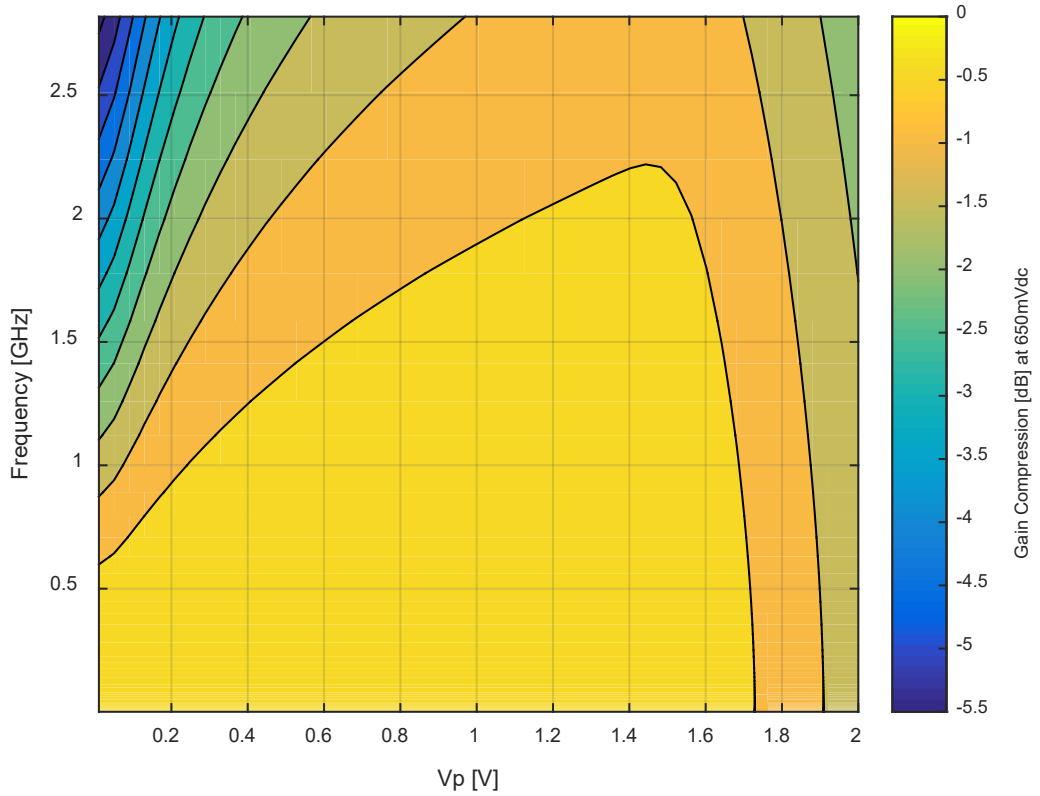
Large signal analysis (II)

High frequency gain compression & distortion



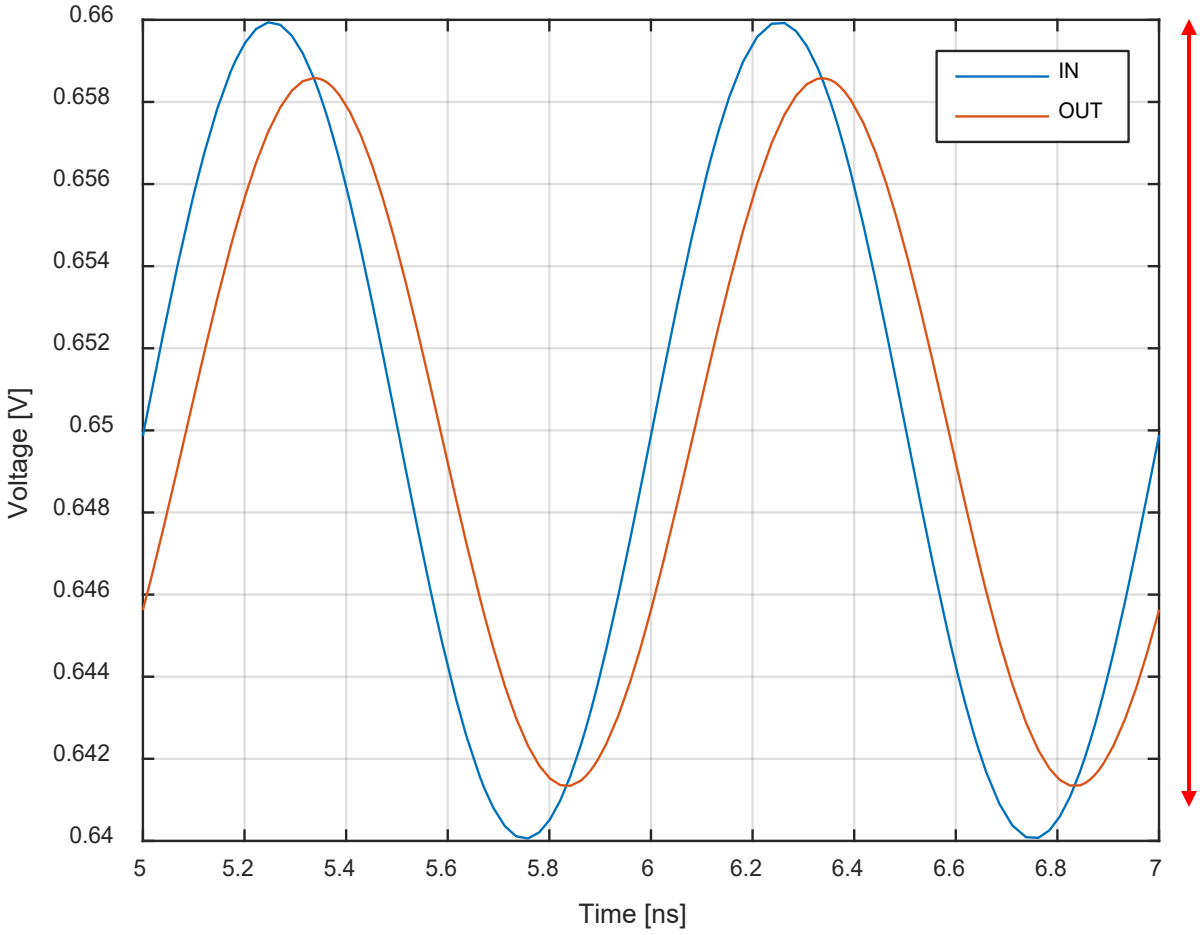
Three region of operation:

- **Low distortion & High compression**
- **Moderate distortion & Moderate compression**
- **High distortion & High compression**



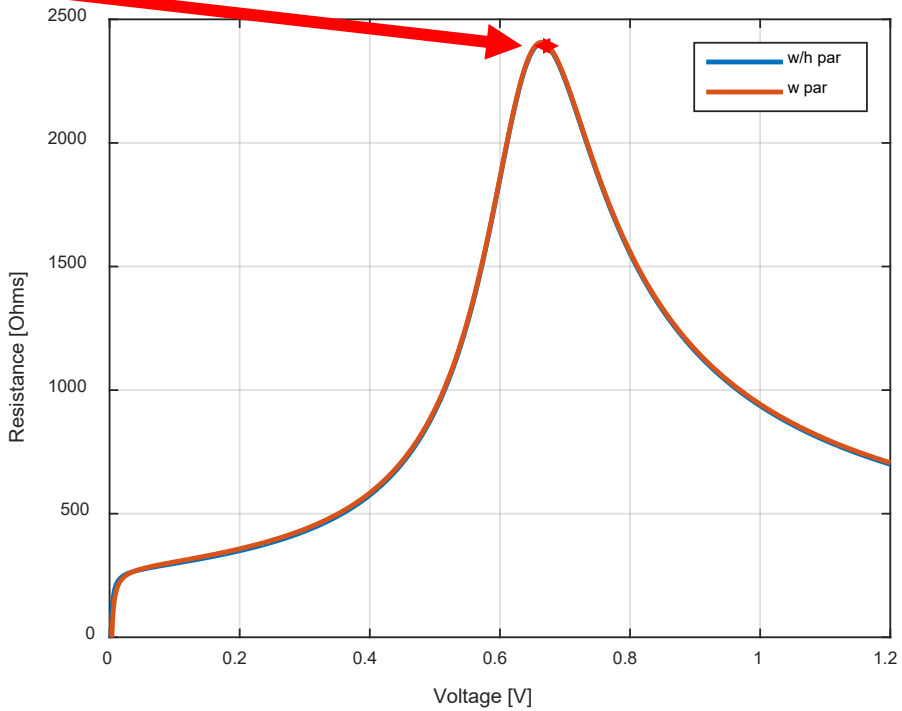
Understanding signal response

Low distortion & High compression



- **Resistance of the channel does not vary much -> Low distortion**
- **At high resistance the bandwidth is limited -> lowering of the gain (compression)**

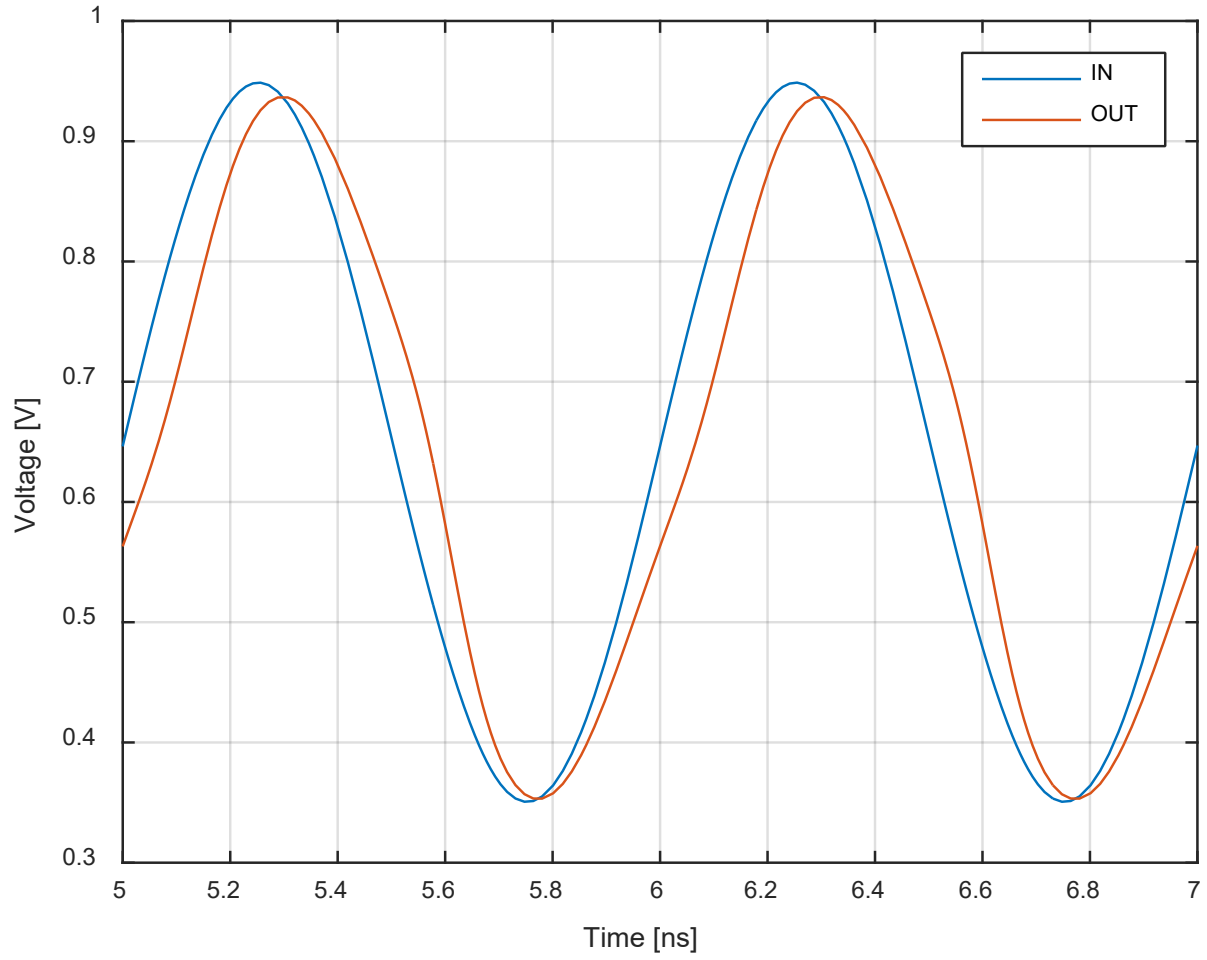
TRACK state



Understanding signal response

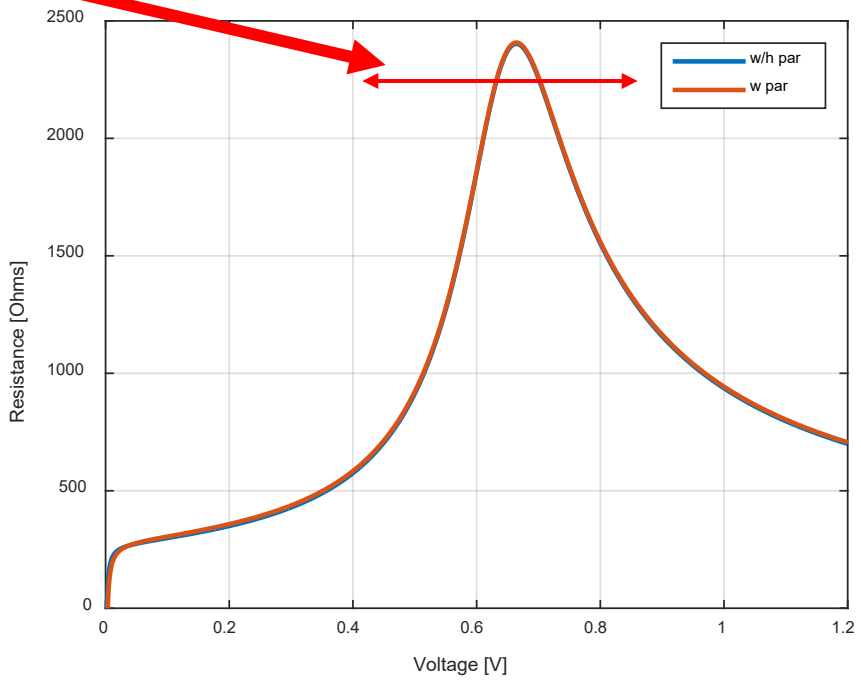
- **Resistance of the channel is varying**
  -> The bandwidth at instantaneous values of the incident voltage waveform is different

Moderate distortion & Moderate compression



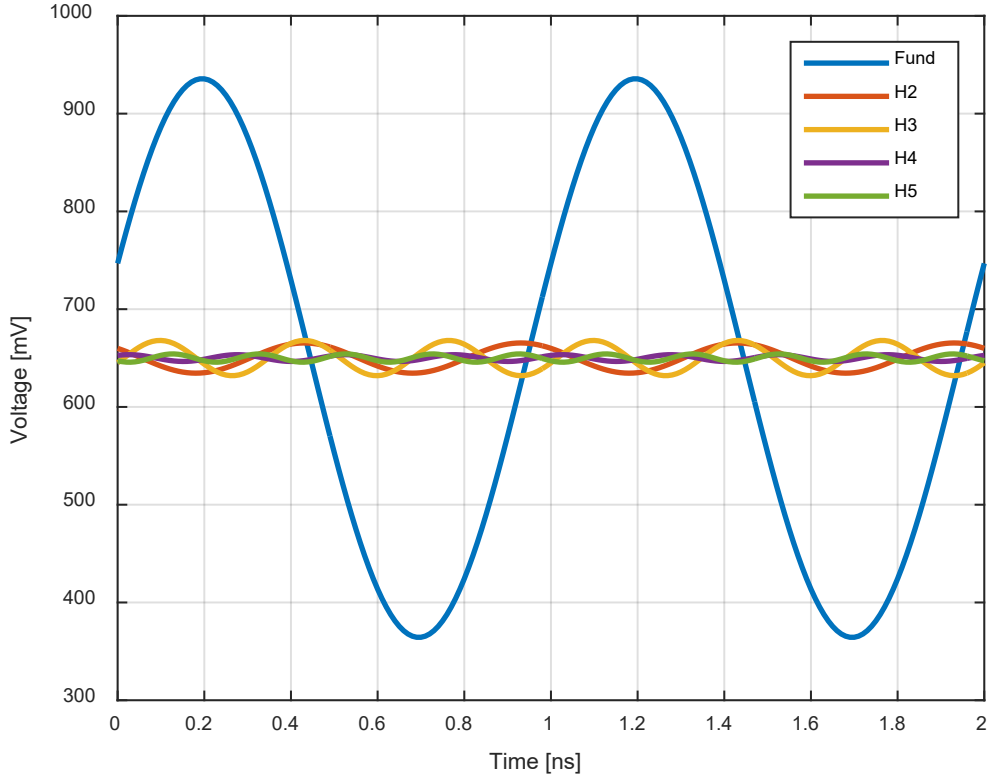
-> In frequency domain this gives rise to higher harmonics, which interfere constructively hence increasing the overall signal amplitude but also increases distortion

TRACK state

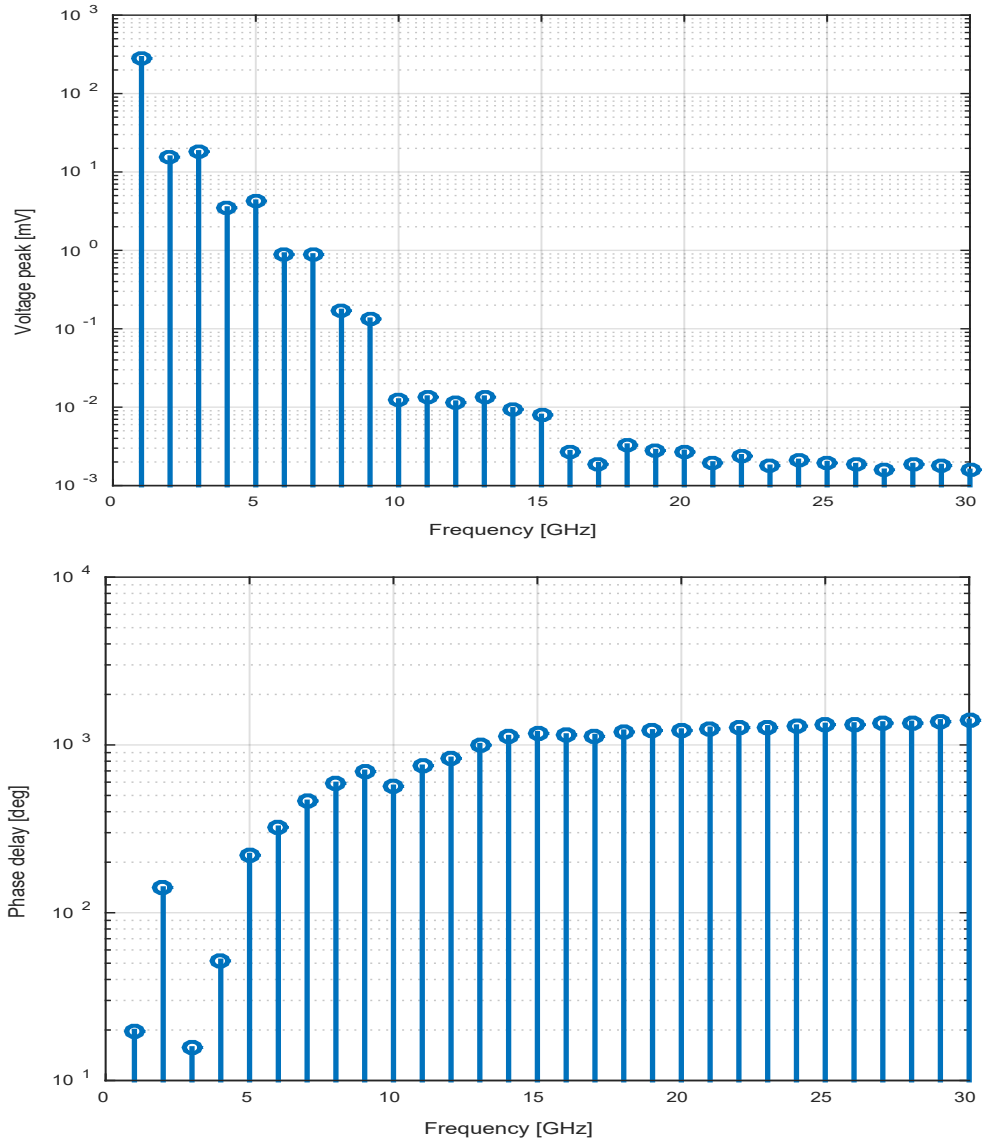


Harmonic decomposition

Time domain decomposition



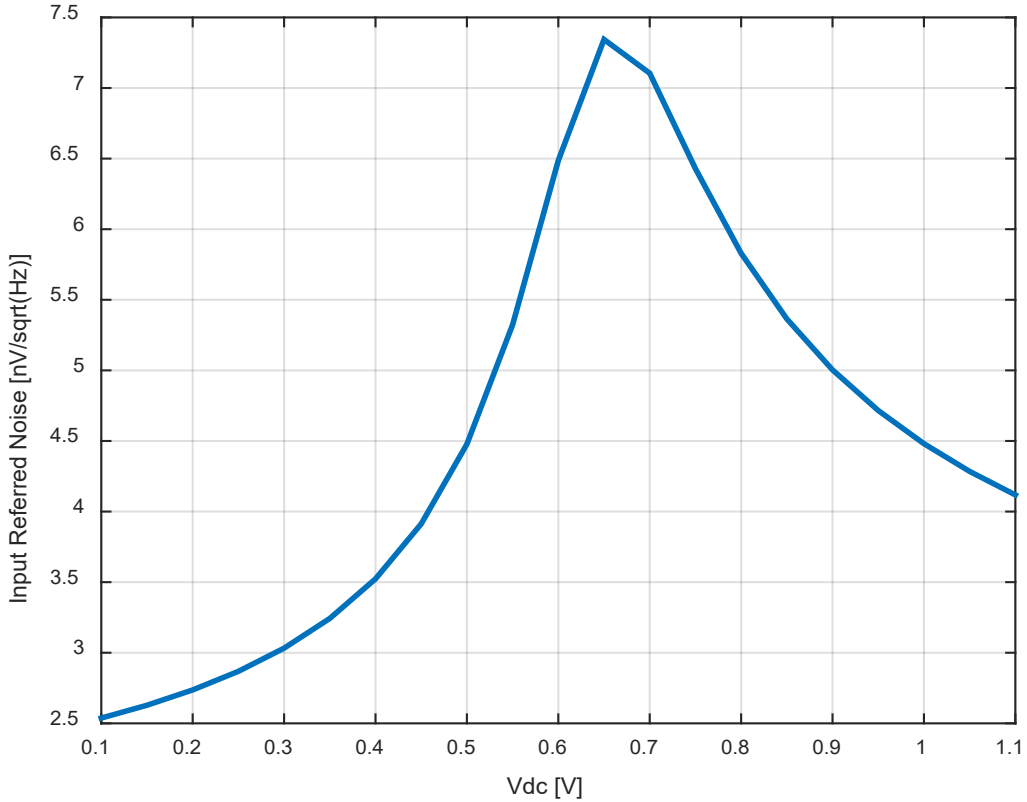
Frequency domain decomposition



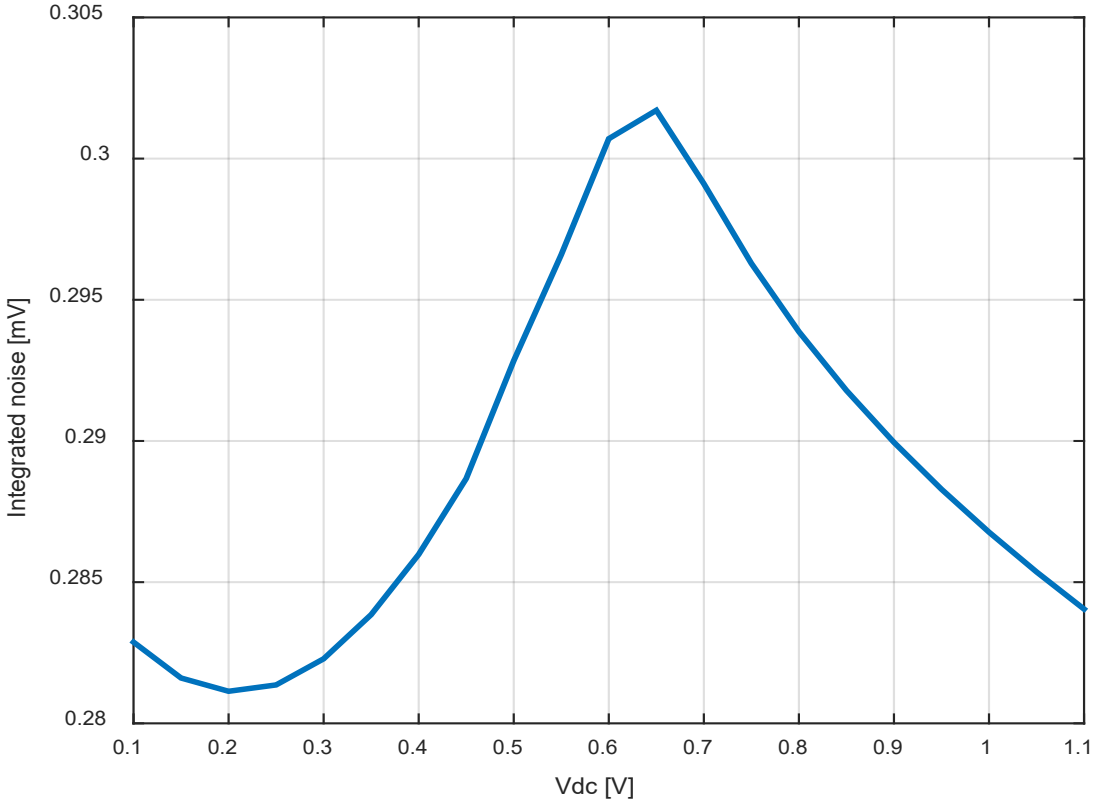
- **Constructive interference of odd harmonics and destructive interference of even harmonics at the peaks**
- **Constructive interference of second and third harmonics at zero crossing**

Noise and Distortion

Input referred noise



Integrated referred noise

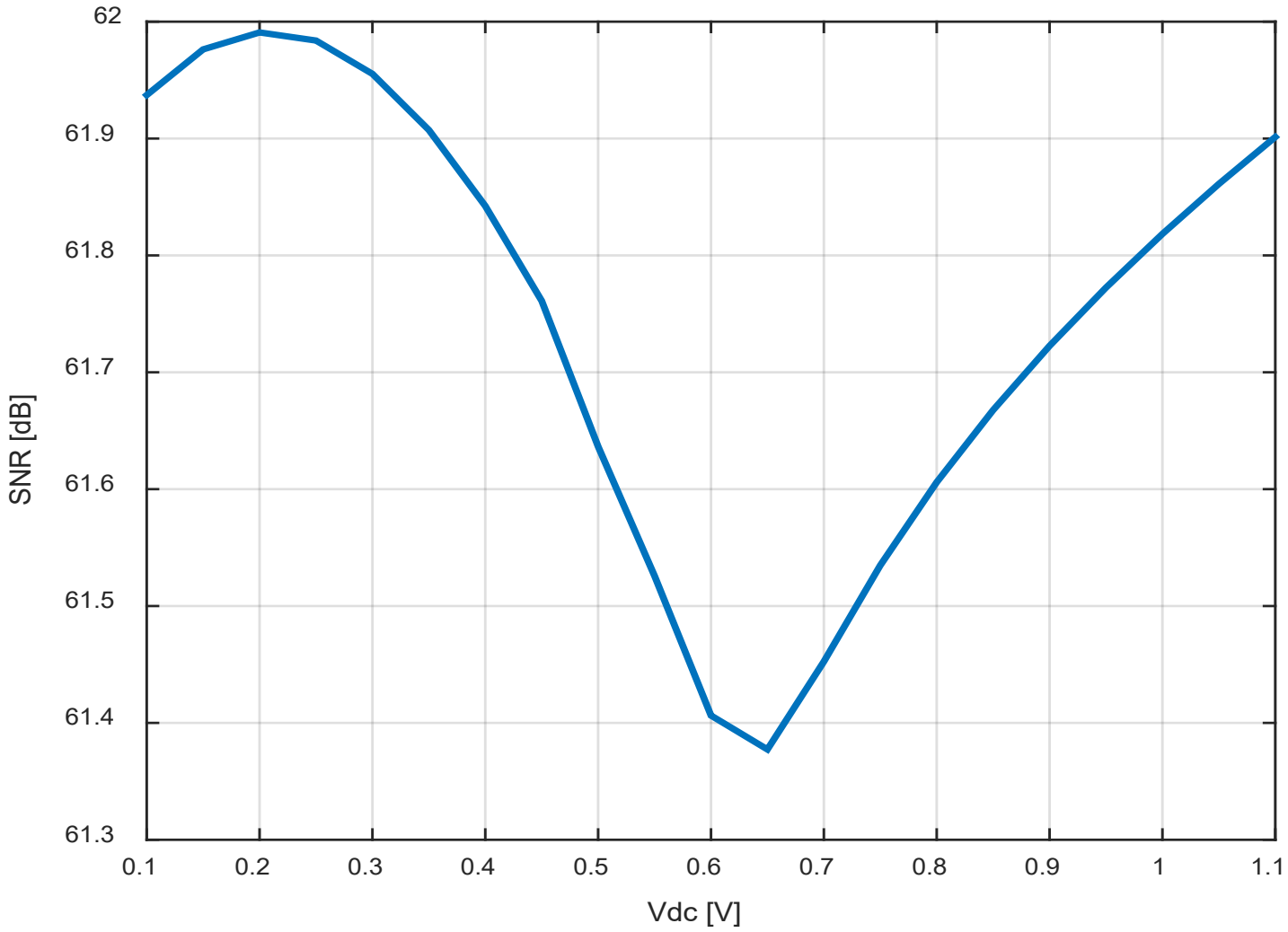


- **Noise dominated by the ON resistance of the channel**

- **Total noise is around 0.29mV ± 0.01 mV**

Noise, distortion and dynamic range

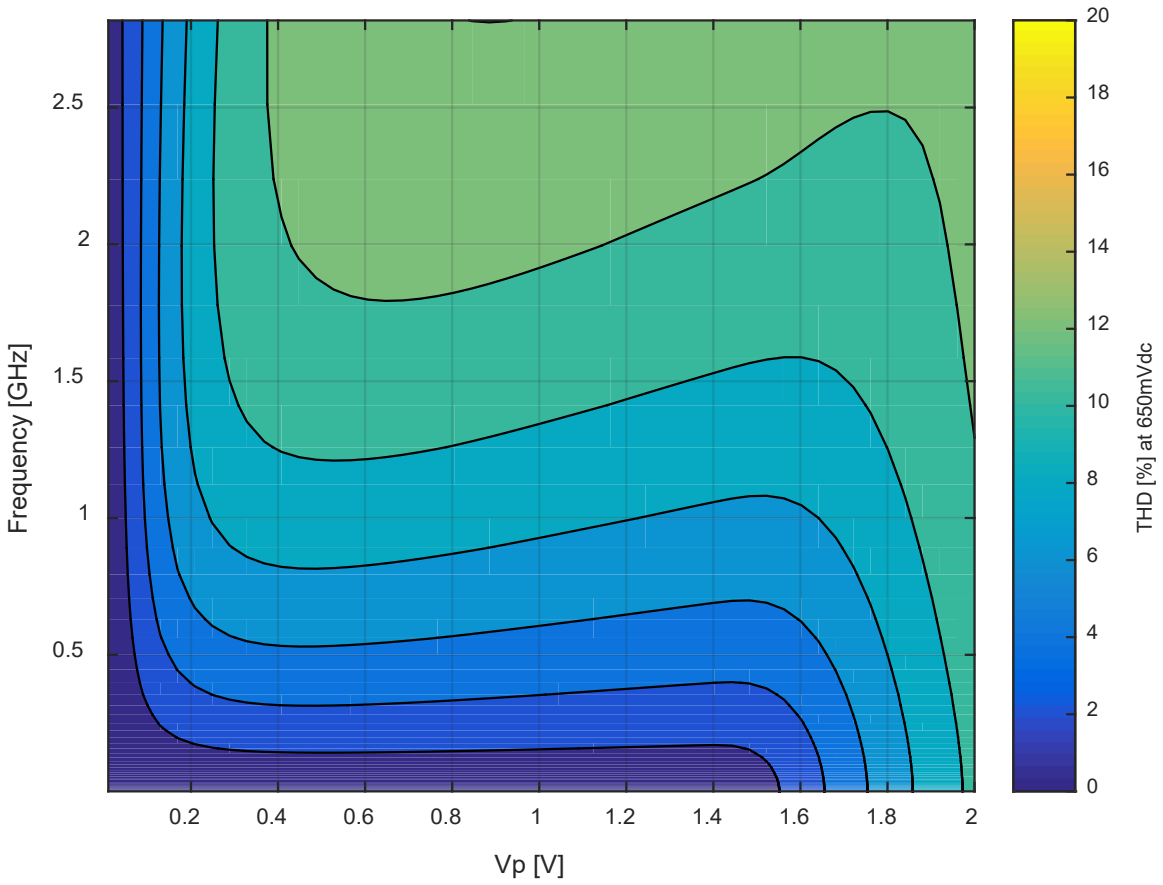
Signal to Noise Ratio at full scale input (1Vin)



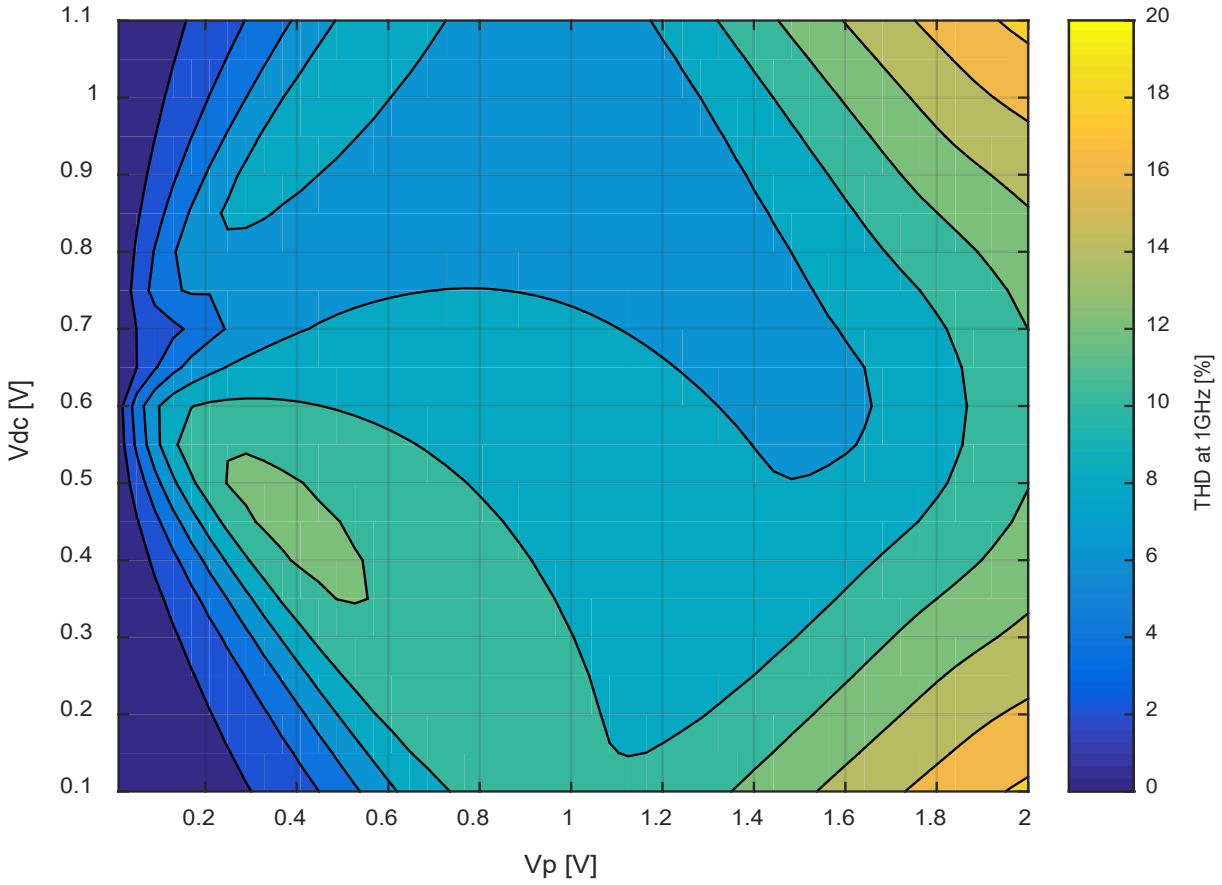
- **SNR is around 61.7dB ± 0.3 dB**

Distortion analysis

Distortion at fixed Vdc



Distortion at fixed Frequency



- **Most of the distortion comes from the Ron variation over the input voltage range**

Summary – Requirements comparison

Parameter	Measured (worst case)	Requirement
Bandwidth	1.7GHz @665Vdc @50Ω	3GHz
SNR	61.7 dB	58dB
ENOB	9.8 bits (small region)	9.4 bits

Things to improve:

- **Reduce Ron variance over the dynamic range to reduce distortion and increase the ENOB**
- **Timebase generator stability**
- **Bandwidth improvement:**
  - **Reduce Cin or reshape the channel to increase the bandwidth (first pole)**
  - **Reduce Ron overall value to increase the bandwidth (second pole)**
- **In summary:**
  - **Increase bandwidth**
  - **Need fast detector**
- **Use differential configuration to reduce pedestal error and increase noise coupling and crosstalk immunity**

Design Choices

- Input coupling
  - Differential versus single-ended input
  - Needed analog bandwidth
  - Gain needed?
- Sampling Options
  - On-chip PLL/DLL
  - External DLL
  - Analog transfer vs. interrogate in situ
- ADC and readout options
  - Sequential output select vs. random access
  - On-chip vs. off-chip ADC
  - Serial, parallel, massively parallel

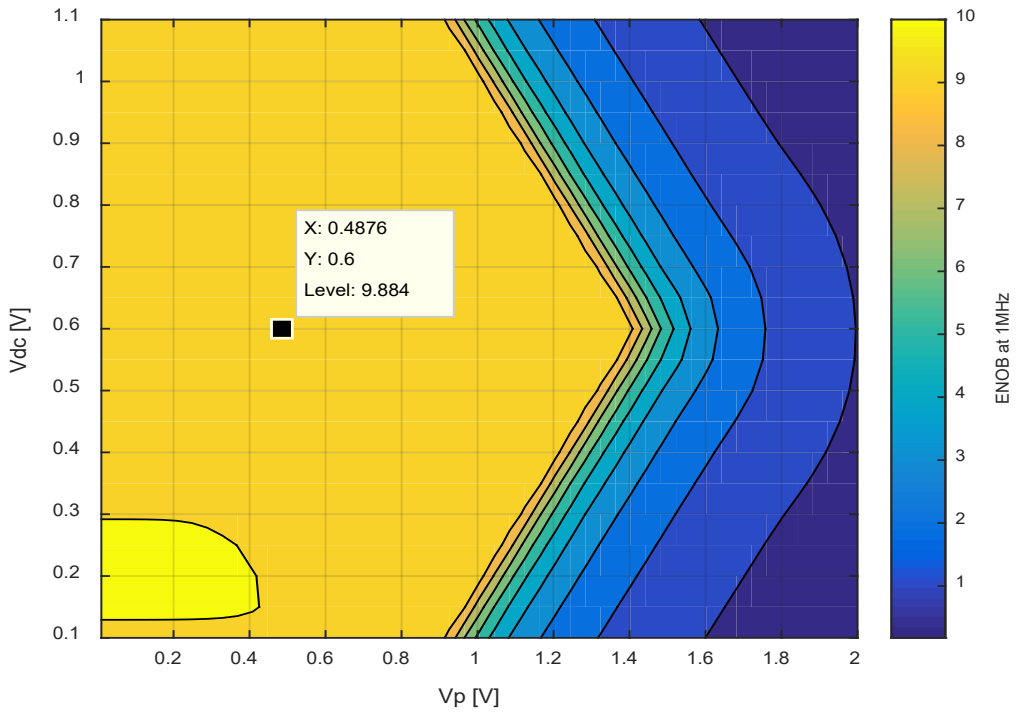
Many variants have been explored…

SINAD & ENOB assessment

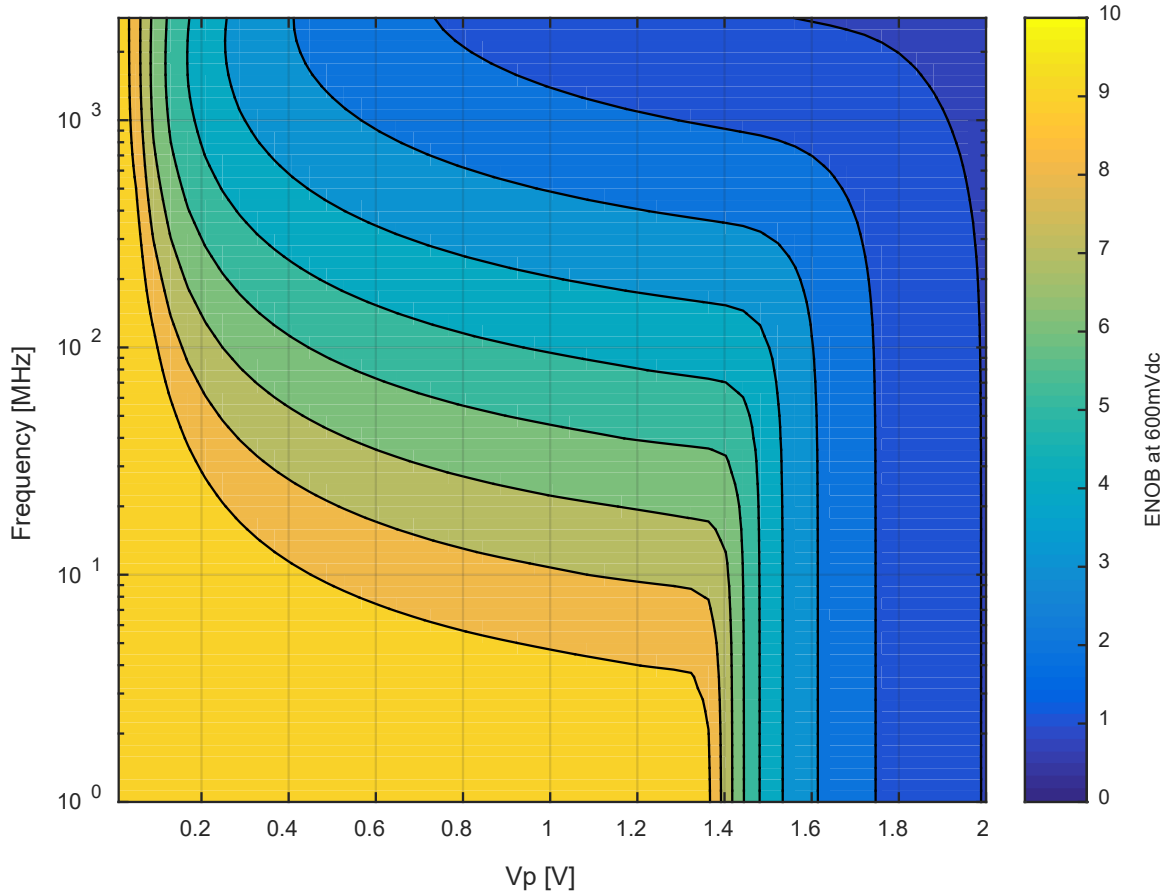
$$SINAD = -10\log_{10}\left[10^{-\frac{SNR}{10}} + 10^{-\frac{THD}{10}}\right]$$

$$ENOB = \frac{SINAD - 1.76 + 20\log_{10}\left(\frac{Fullscale}{Input}\right)}{6.02}$$

ENOB at low frequency



ENOB versus frequency



- **ENOB DOMINATED BY DISTORTION**