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# Pixel detectors with built-in signal processing and bandwidth-efficient data transmission

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A high degree of segmentation in pixel detectors is needed for recording trajectories of charged particles or impacts of X-ray photons with high spatial resolution. The desired granularity imposes severe constraints for the in-pixel processing circuits, signal readout, and power budget. Therefore, most of nowadays high-spatial resolution pixel detectors are limited to detection of deposited energy or occurrences of the event (location).. Pixel detectors under development at BNL combine high-resolution amplitude measurements with handling of charge sharing events and zero-suppressed readout at the maximum achievable speed in the event-driven form. The readout circuits are being developed to suite hybridization with pixel sensors made of various materials, i.e., Si, Ge, and CdZnTe, with a variety of finely pixelated segmentations with the largest pitch equal to 150 micrometers, operating at room or cryogenic temperatures, and suitable for operation with X-rays in a broad energy range. As the development of an Application Specific Integrated Circuits (ASICs) is a considerable effort, a universal implementation methodology suitable for reading out pixelated sensors was developed. The methodology allows building the circuital skeleton for the Configuration-Testability-Readout (CRT) management logic and is based on code written in System Verilog hardware description language, fully parametrized to reflect all crucial parameters of the ASIC to be developed. The goal is to maximize the area for the Analog Front-End (AFE) while utilizing minimal resources (routing and area) for scaling to various densities, sizes, and shapes (square or hexagonal) of the pixels. Blocks of the readout chain have also been modularized to adapt efficiently to the polarity and magnitudes of the charge signals. The AFE circuit interfaces to the recently developed event driven readout system, EDWARD, through a Readout Interface (RI) circuit.
The implementation of a high-resolution, in-pixel Analog-to-Digital Conversion (ADC) block that completes the development of the signal processing built into a pixel circuitry is discussed as well. This block adds robustness to interference and distortions due to typical circuit non-linearities, and driving strength needed for fast settling.

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