Pixel detectors with built-in signal processing and bandwidth-efficient data transmission

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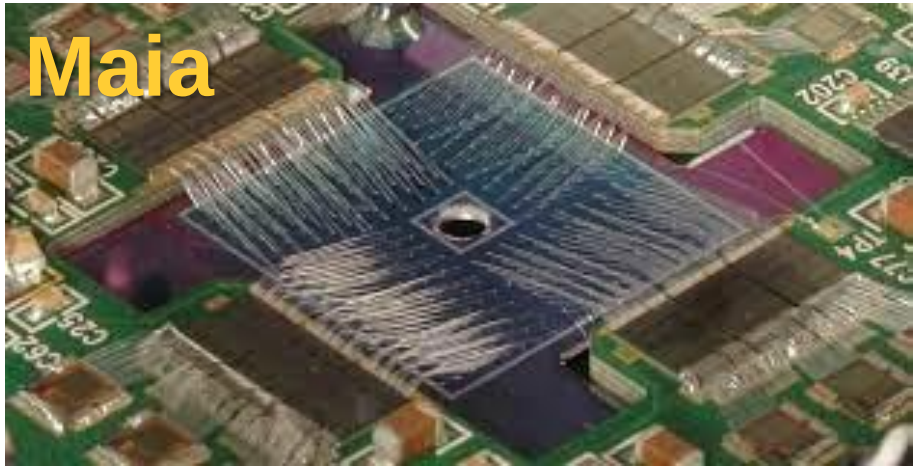
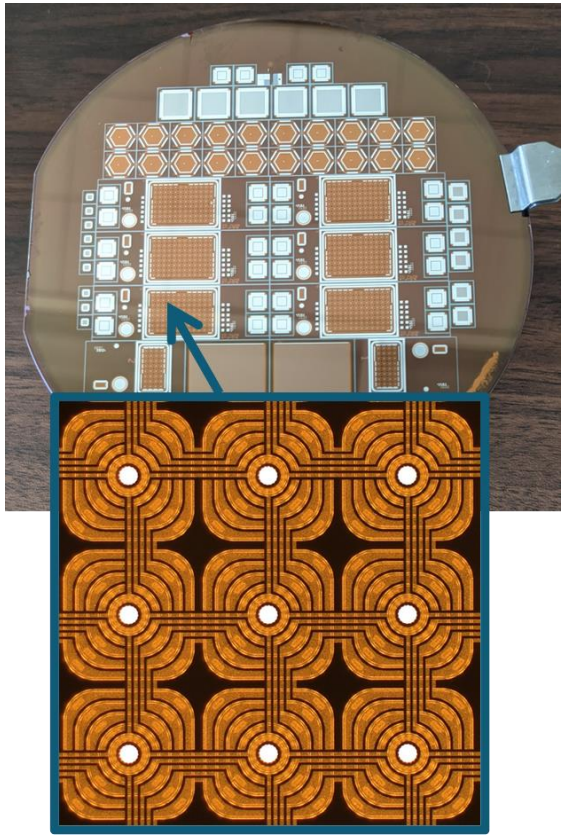
Pixel detectors: our path forward

From pixels for spectroscopy to in-pixel spectroscopy

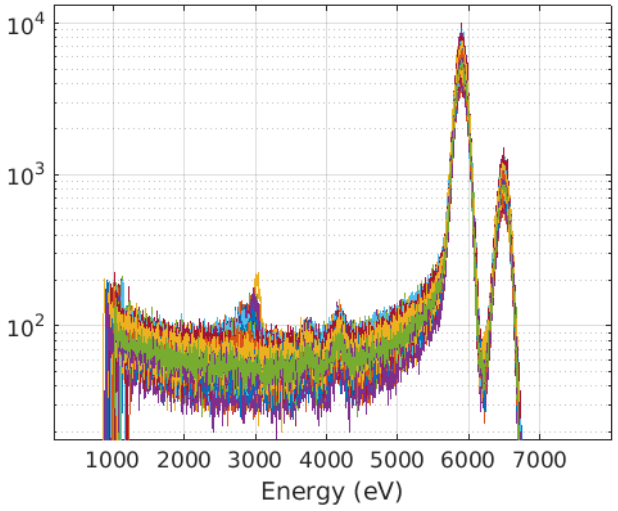


Right: Wafer with arrays of 96 (towards 384) 1mm^2 SDDs, read-out in parallel, for high-count rate fluorescence spectroscopy at synchrotrons



Hera

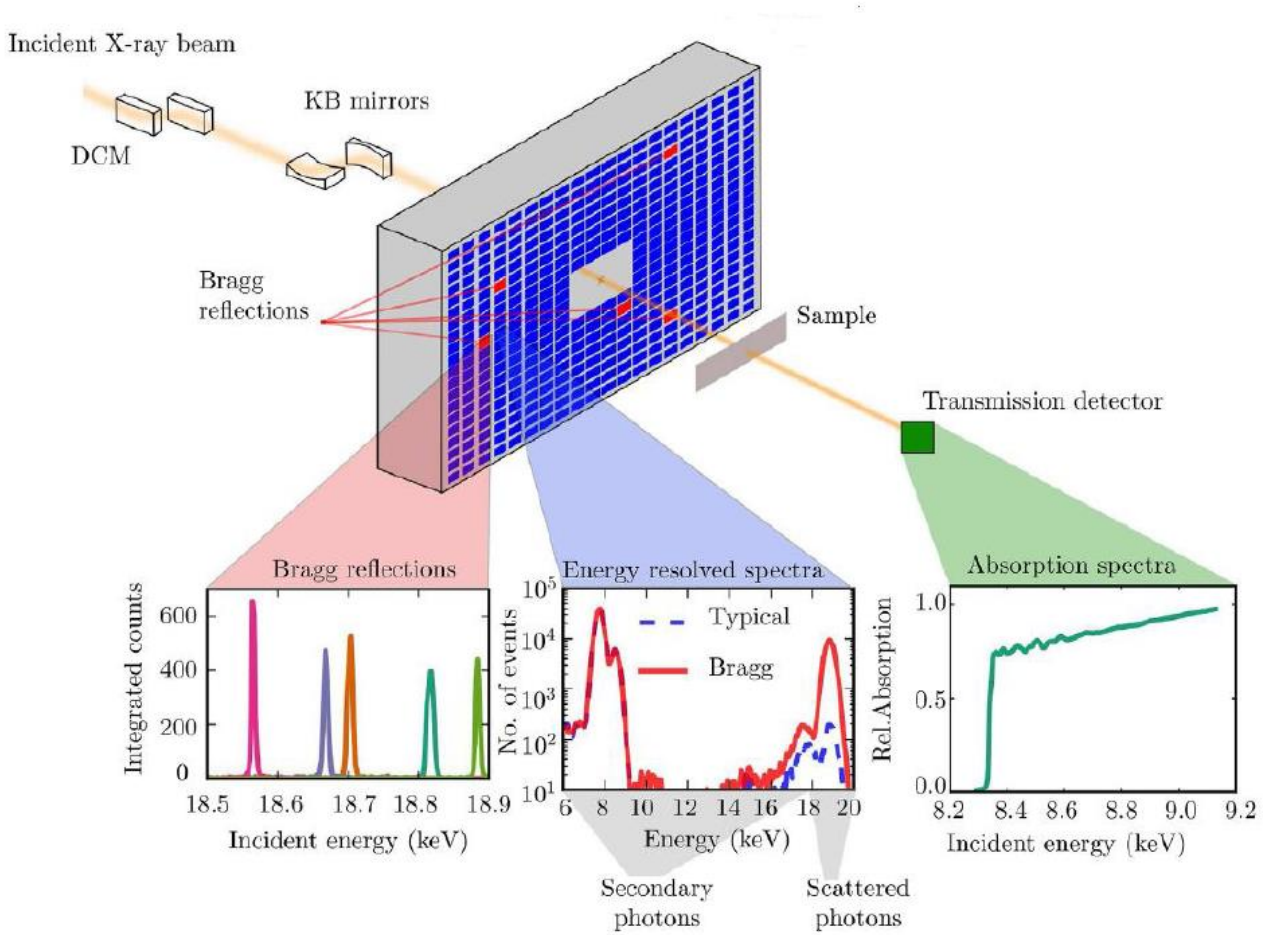
Upgrade of the Maia microprobe array with lower capacitance units, for lower noise, higher throughput and enhanced stability



Right: ^{55}Fe spectra from all 96 channels, average FWHM = 176 eV at −13◦C with 1 μs of peaking time

W. Chen at al., "Development of a Large Array of Silicon Drift Detectors for High-Rate Synchrotron Fluorescence Spectroscopy", 2023 JINST 18 P01016

Simultaneous diffraction and fluorescence mapping



H. J. Kirwood et al., *Simultaneous X-ray diffraction, crystallography and fluorescence mapping using the MAIA detector*, Acta Materialia, **144**, 1, (2018).

Experimental geometry used for the measurements at the Australian Light Source

- The incident X-ray beam passed through a double crystal monochromator (DCM) and focused on to the sample by a pair of Kirkpatrick-Baez (KB) mirrors.
- The resulting scattered and fluorescence spectra were collected on the Maia detector.

That experiment would have benefitted from a detector with better spatial resolution, and a much larger pixel count!

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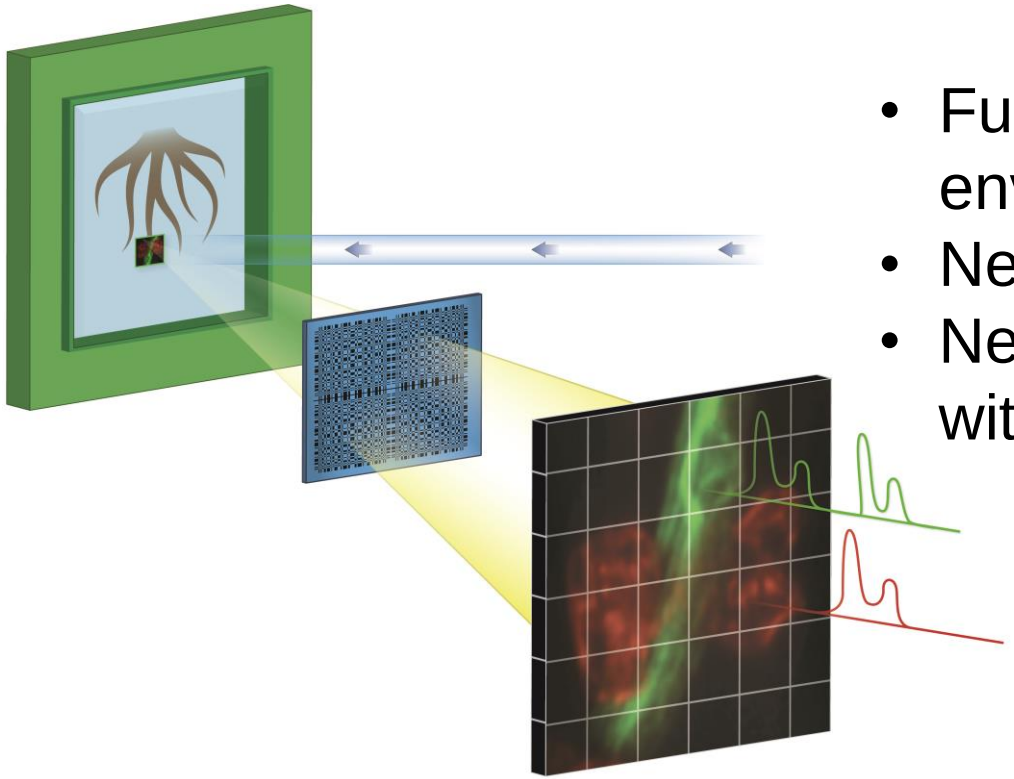
Full Field Fluorescence Imaging (FFFI) detector



- Full field fluorescence imaging for biological and environmental applications
- Needs an energy resolving pixelated detector : FFFI
- Needs optics which is achromatic: coded aperture with 10 µm pinholes

The new FFFI technique will capture images of trace element dynamics at biologically relevant timescales –typically less than one minute

research papers

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A Coded-aperture Microscope for X-ray Fluorescence Full-field Imaging

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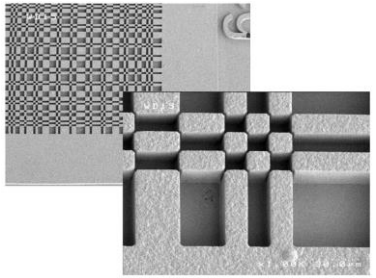
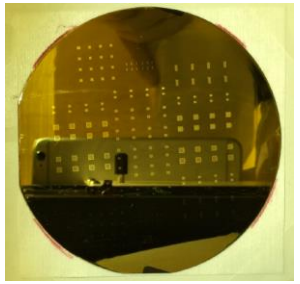
Pixelated imaging detector (10,000 pixels)

- Each pixel also has to function as a high-resolution (<200 eV) X-ray spectrometer over a broad energy range (2 – 14 keV)
- Specifications 100 µm pixel size, better than 20 e- rms, 10 bit

Development of coded aperture masks at BNL





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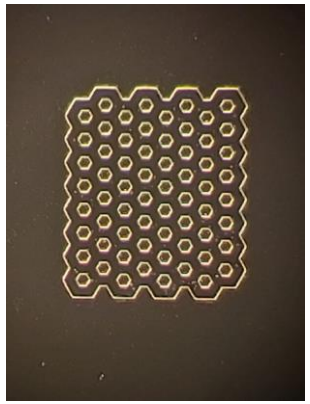
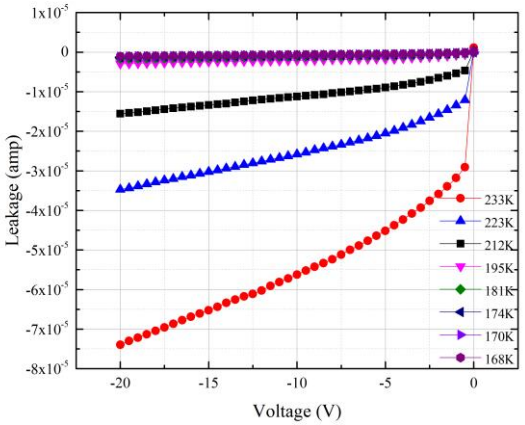
GALAHAD: Germanium Array for Low And High energy Area Detector



8X8 pixel array



Leakage Tests

- NSLS II and APS need imaging detectors for hard x-rays
- Current imaging detector architectures provide simple photon-counting or charge integration
- No existing x-ray detector offers energy-resolved images
- Adding energy resolution opens new possibilities: Laue Diffraction, high energy fluorescence imaging etc.
- BNL has expertise in all areas needed to make such an instrument:
  - low-noise ASICs; germanium sensors; cryogenic electronics

Det.	Q conv. (1 e- => eV)	Fano Factor	Energy (keV)	Fano Noise (e-)	Fano FWHM (eV)	ENC (e-)	Ele. FWHM (eV)	FWHM (eV)	Qin (ADC bin #)	FWHM (ADC bins)
Ge	2.9	0.13	30	37	250	30	204	323	194	7
	2.9	0.13	60	52	353	30	204	408	983	8
	2.9	0.13	130	76	520	70	477	706	2130	14
	2.9	0.13	250	106	721	70	477	865	4096	18

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Small-Pixel CZT Detectors for Future High-Angular-Resolution Hard X-Ray Missions

The Nuclear Spectroscopic Telescope Array (*NuSTAR*) Small Explorer Mission (SMEX) [1] was launched in June 2012 and has been a resounding success.

Recent technological breakthrough:

- low-mass, low-cost, high angular resolution, and extended energy bandwidth X-ray mirrors made with
- the mono-crystalline silicon technology [2], or
- electro-formed-nickel replicated (ENR) X-ray optics [3]

With a matched detector they enable hard X-ray observations with more than one order of magnitude better sensitivities than *NuSTAR*

Requirement	Requ. Perf.	Proj. Perf. CZT & HEXID	Science Driver
Energy Threshold	2 keV	1.5 keV	Detect <4 keV corona emission from supermassive black holes.
Energy Bandpass	2-150 keV	1.5-160 keV	Fe K-α (black holes) lines & nuclear lines (SN).
Electronic Noise (ASIC)	20 e^- RMS	13 e^- RMS	High-accuracy studies of Fe K-α lines with <200 eV FWHM energy resolution.
Energy Res. at 6.4 keV (hybrid)	400 eV FWHM	<200 eV FWHM	High-accuracy studies of Fe K-α lines.
Pixel Pitch	250 µm	150 µm	Sensitivity (AGN census) and ang. res. (source confusion).
Timing Resolution	1 ms	<1 µs	Study of quasi-periodic osc. of stellar mass black holes.

Required and projected performance of the detector-ASIC package for a hard X-ray imager

1) Harrison, F. A., Craig, W. W., Christensen, F. E., et al., ApJ, 770, 103 (2013)
2) Zhang, W., Allgood, K. D., Biskach, M. P., et al., Proc.SPIE 10699, 106990O (2018)
3) Gaskin, J., Elsner, R., Ramsey, B., et al. https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20150020499.pdf (2018)

Several sensor options: materials

Some of the materials we are working on. Other thin-film options are a-Se and perovskites

quantity	Si	Ge	GaAs	Diamond	CdTe	$Cd_{0.9}Zn_{0.1}Te$	TlBr	a-Si
E_g [eV]	**1.12**	**0.67**	1.43	5.50	1.44	**1.57**	2.68	1.90
W [eV]	**3.60**	**2.96**	4.20	13.00	4.43	**4.64**	6.50	6.00
ε	**11.7**	**16.0**	12.8	5.7	10.9	**10.0**	30.0	12
μ_e [$cm^2/(Vs)^{-1}$]	**1350**	**3900**	8000	1800	1100	**1000**	30	1-4
μ_h [$cm^2/(Vs)^{-1}$]	**450**	**1900**	400	1200	100	**120**	4	0.05
ρ [g/cm^3]	**2.33**	**5.33**	5.32	3.52	5.85	**5.78**	7.56	2.30

Characteristic parameters of typical materials for semiconductor sensors

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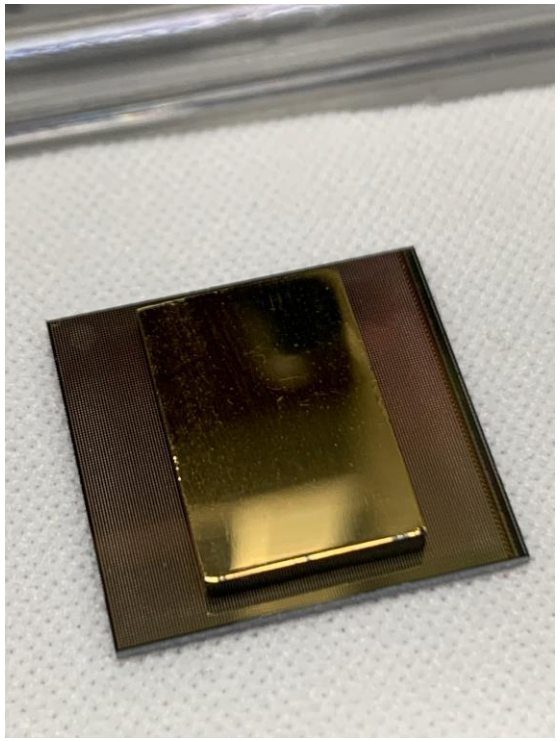
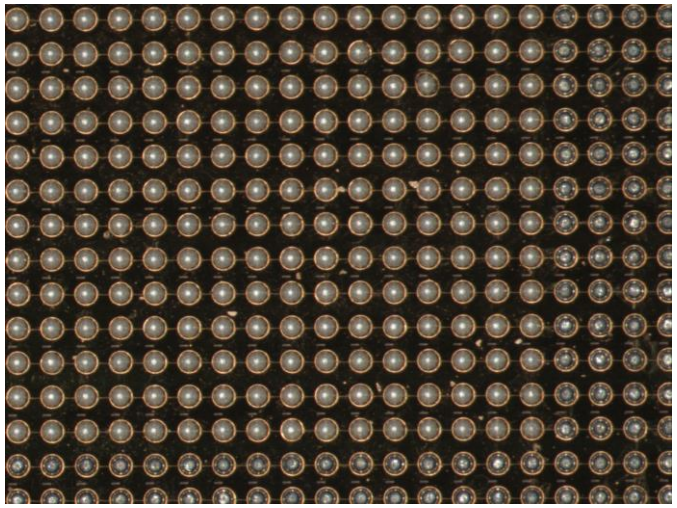
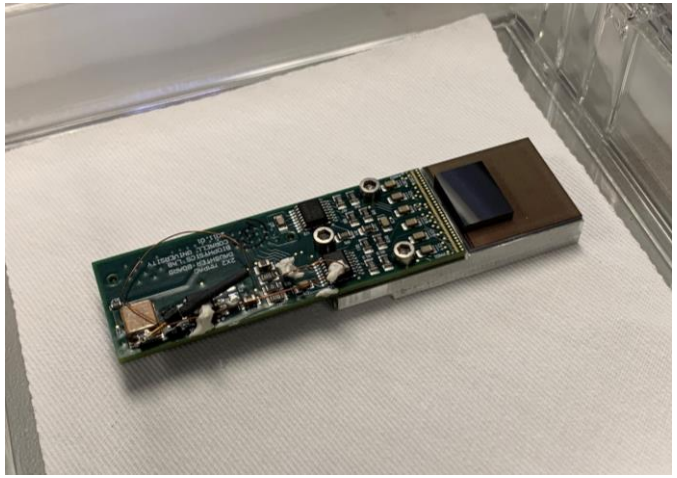
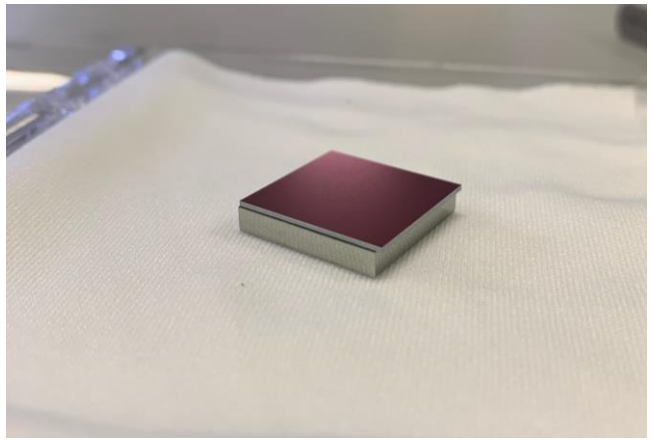
Different materials require customized interconnect solutions

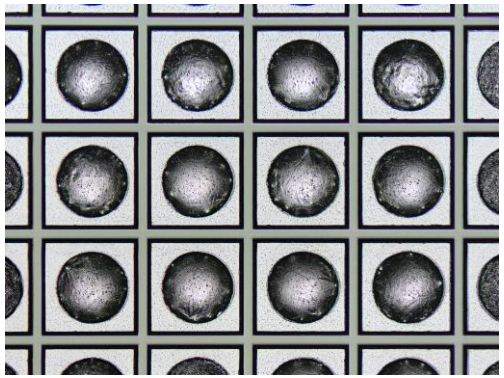




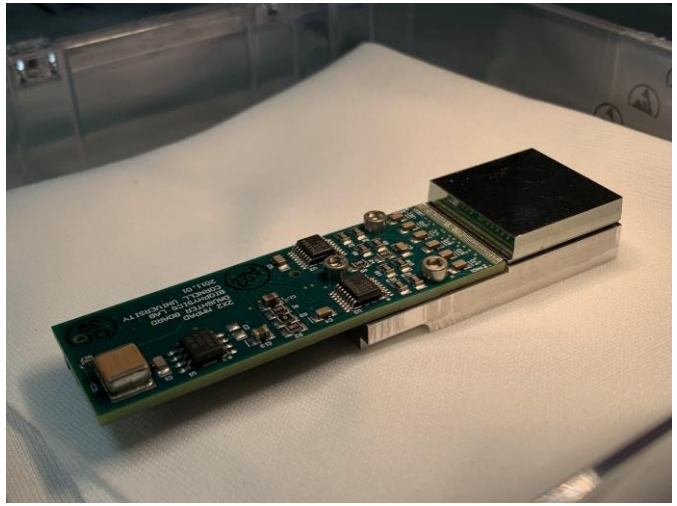


CZT sensor





Germanium sensor



Cornell's MMPAD ASIC

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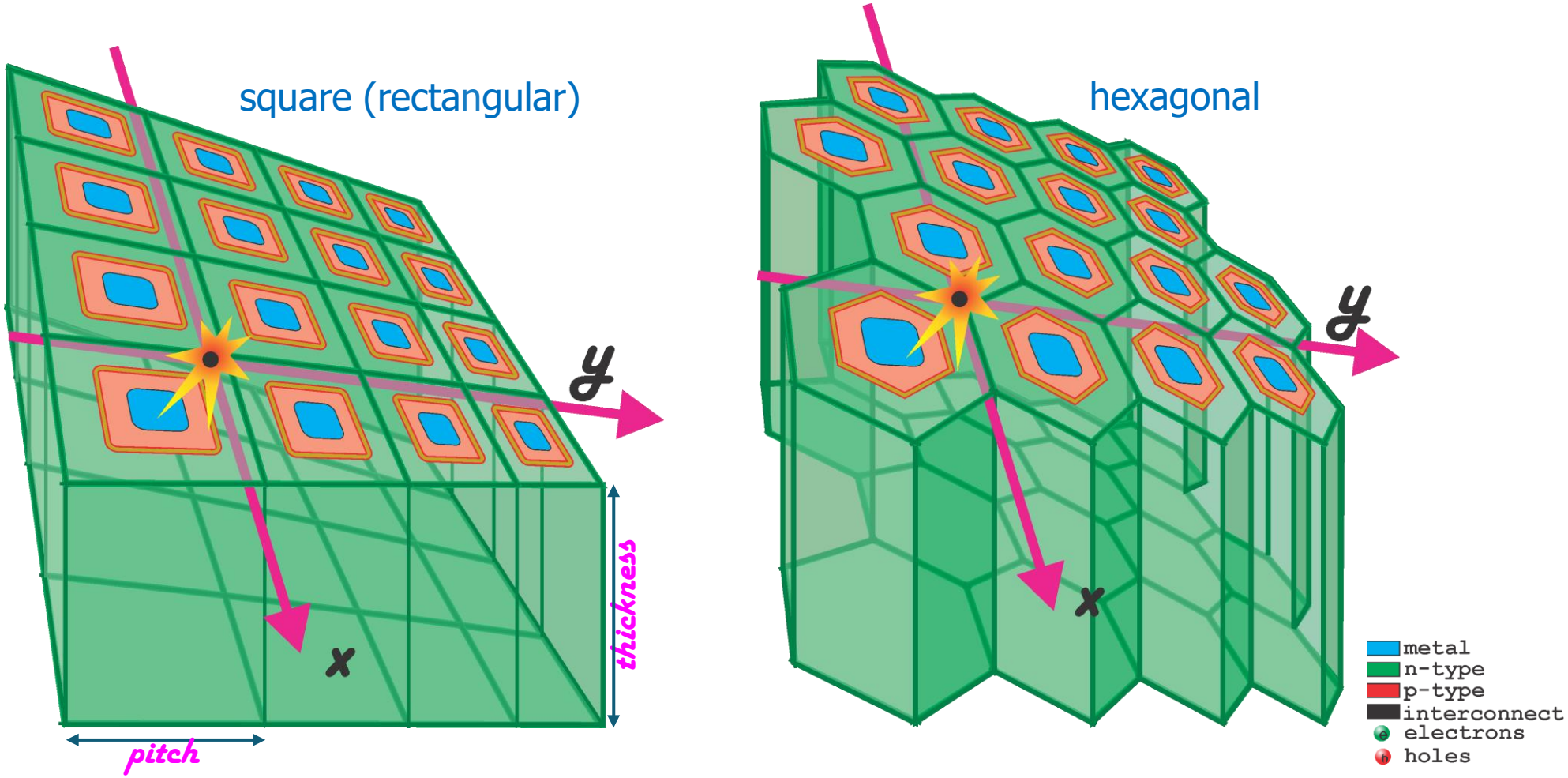
Examples of sensor/ASIC assembly bonded at BNL

Segmentation of pixel sensors

Two arrangements of segmentation of pixel detectors



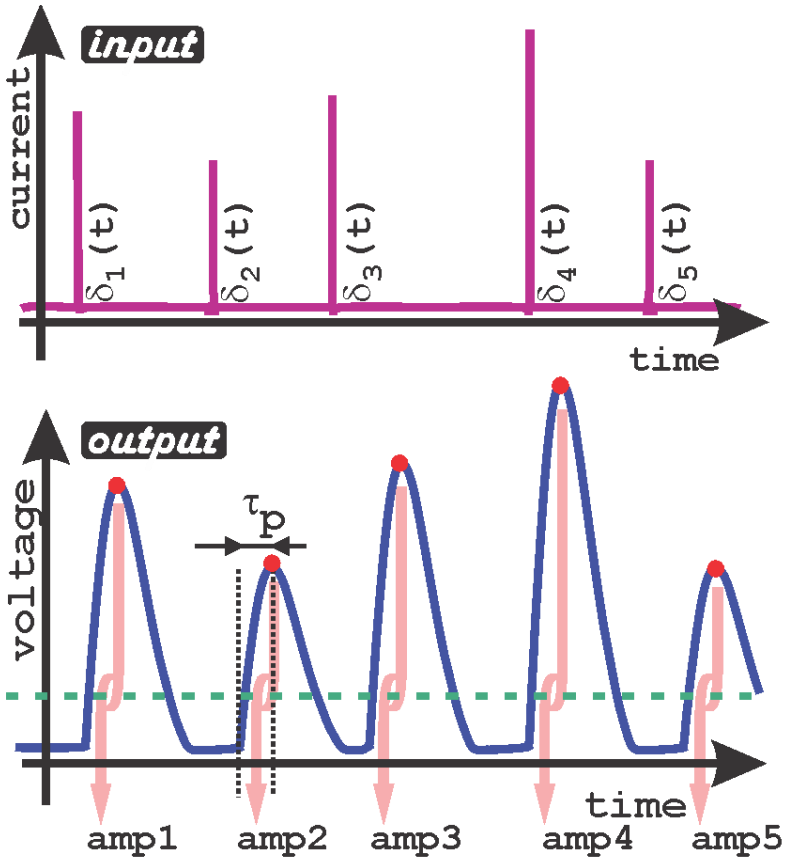
Thick sensors with long collection times

We need to measure the amplitude (∝ energy of photons) per event, arriving <u>randomly</u>, distinguishing individual pulses at high rates

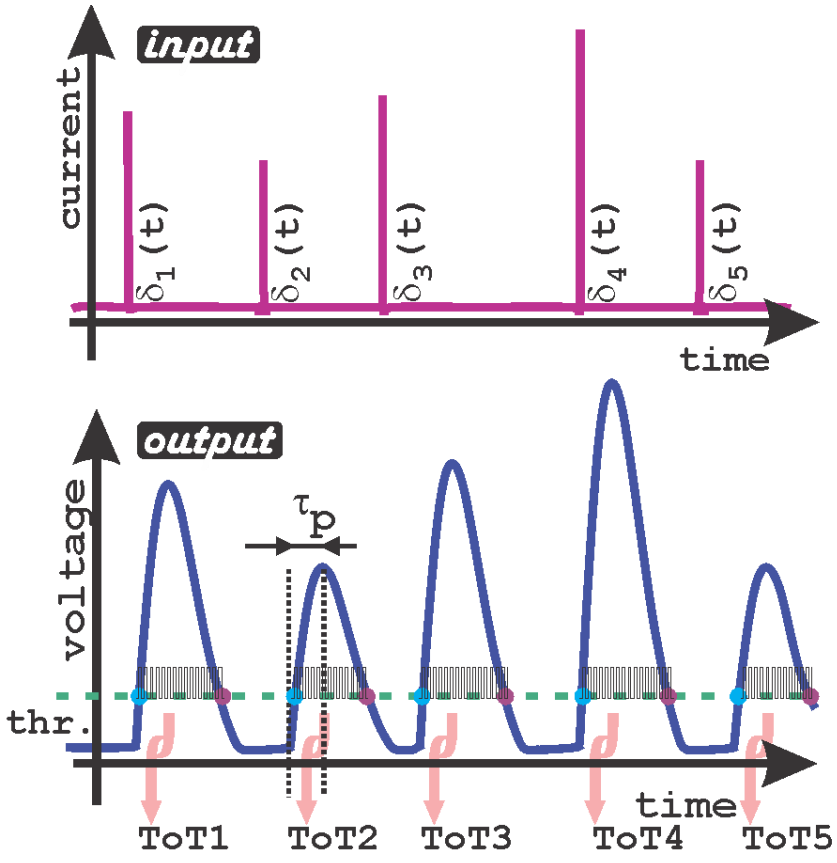
Amplitude Measurement vs. Counting (1)

Peak/extremum:

- $\tau_p >> \tau_{col}$ (worse SNR in presence of ballistic deficit)
- requires complex analog processing ⇒ extremum detector



peak - detection



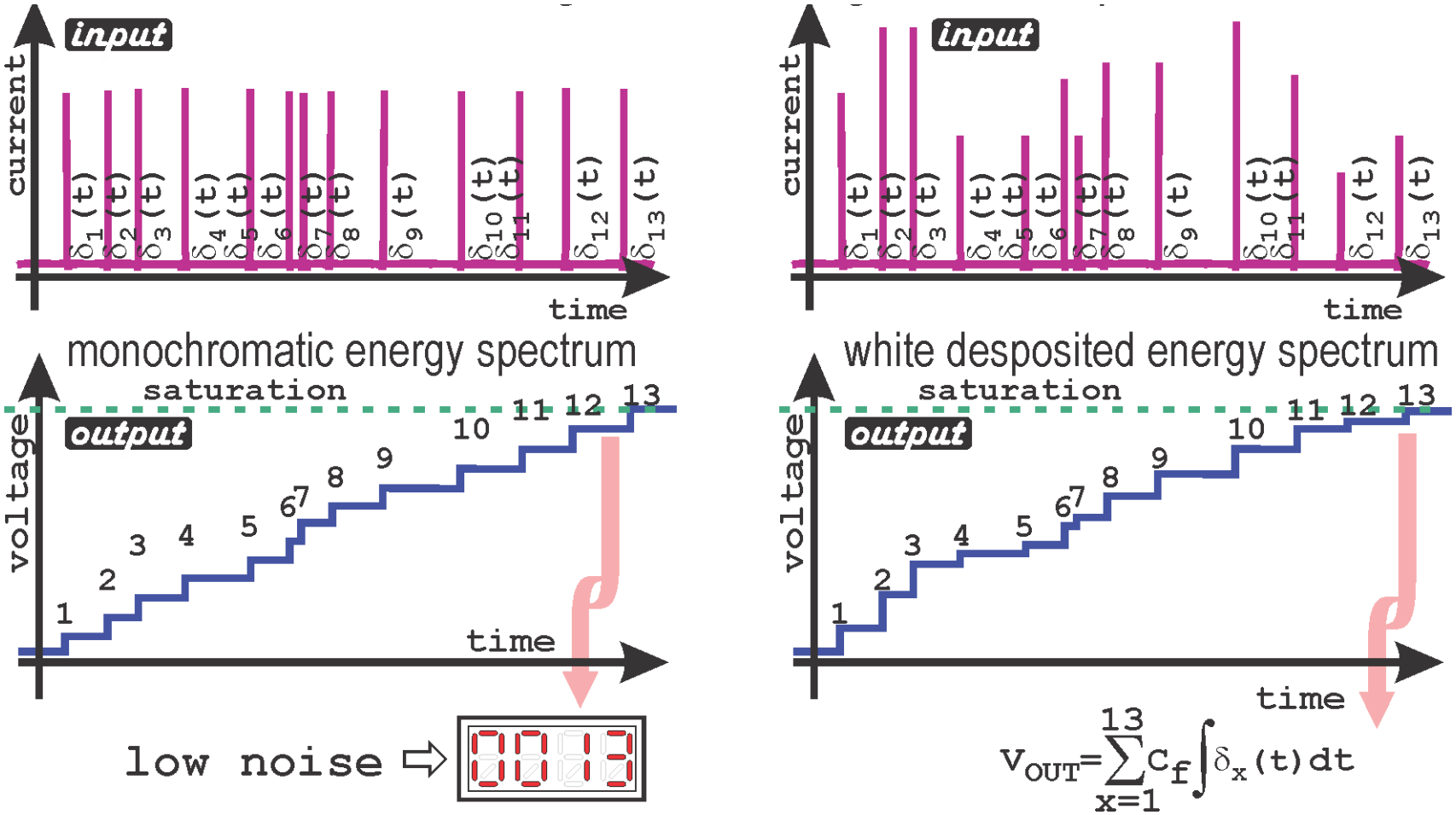
ToT measurement

ToT:

- $\tau_p > \tau_{col}$ (SNR less sensitive to ballistic deficit)
- can be operated:
  - **digital**, but requires high-speed oscillator per channel to measure time
  - **analog**, using constant current discharge and TAC but typically is less precise than digital

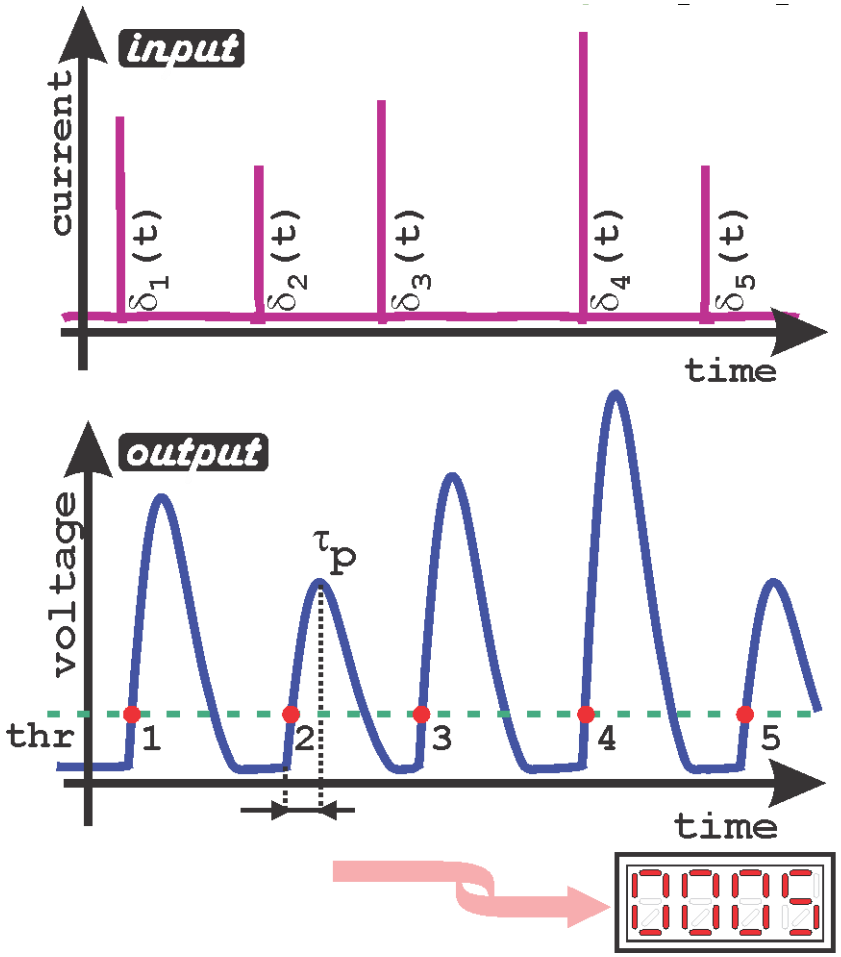
Two methods to measure amplitude in a pixel (small footprint)

Amplitude Measurement vs. Counting (2)



for higher rates, integration needs to be used for measuring amplitude (monoenergetic photons ⇒ # of photons)

Amplitude Measurement vs. Counting (3)



for higher rates, both amplitude and counting suffers from pile-up

Counting is less sensitive than **Amplitude** to:

- *all nonlinearities of pulse response of FE* ⇔ possessing of enough of amplitude to cross threshold is required (large-signal operation regime)
- *worse SNR*
- *time properties of charge collection*, incl. ballistic deficit
- *ch-2-ch* gain *variation* and process variations and mismatches;
- any secondary dependencies, such as:
  - **gain**
  - **offsets**
  - **baseline**
  - **overshoot/undershot**

Amplitude Measurement vs. Counting (4)

Amplitude measurements typically require circuitry built with:

- **very high** (80 dB and more) **open-loop gain** (CSA, shaping filter, peak/extremum detectors, S/H stages, buffers and drivers)
- **passive** R and C **components** or (wherever possible) precisely **matched** translinear **circuits** for **signal filtering needs**
- more processing stages per channel to achieve enough signal gain and filtering
- readout suitable for digitization as soon as possible
- multi-bit corrections and trimming

Circuits for **Amplitude** measurements must:

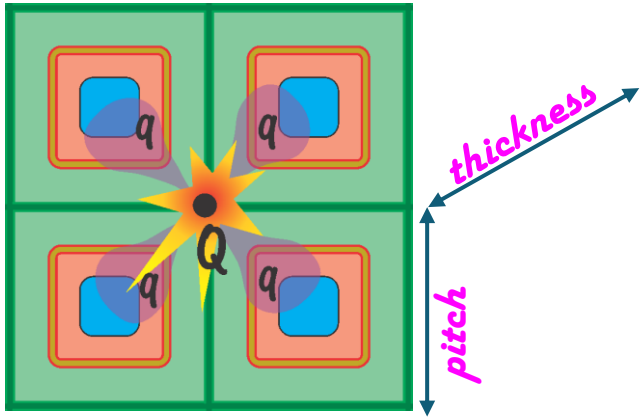
- be very **carefully designed for stability** or using topologies less prone to instabilities (one channel may be stable, but 10k channels together?)
- include **significant** degree of **digital assistance**
- possess **power distribution** reducing IR drops and leading to high PSRR

Precision amplitude measurements consume noticeably more power and occupy more silicon area

Input Signal vs. Segmentation

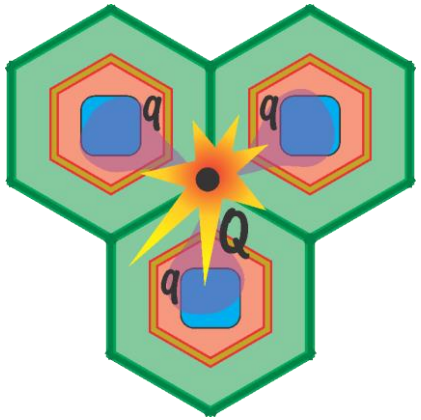
For **amplitude** measurements we cannot neglect charge sharing

square (rectangular)



Q ⇒ 4 × q

hexagonal



Q ⇒ 3 × q

fractional signals are present in most case when charge cloud is comparable to pixel pitch

sqrt(2×D×thickness/ν_{sat}) ≈ pitch (collection at carrier velocity saturation)

… and charge sharing can be handled by:

- adding fractional signals in a front-end, but charge and pedestal dispersion introduce irreversible inaccuracies
- convert to digital and add in digital domain after gain and pedestal corrections:
  - on a chip – requires area-intense resources
  - **off-line – requires reading out neighbors simultaneously with central channel**

A design to enable time-continuous amplitude spectroscopy

Operation of readouts has to cover a broad - 2 keV to 160 keV - energy range

Achieved by splitting the signal after the first amplification into a High Sensitivity Path (HSP) and Low Sensitivity Path (LSP)

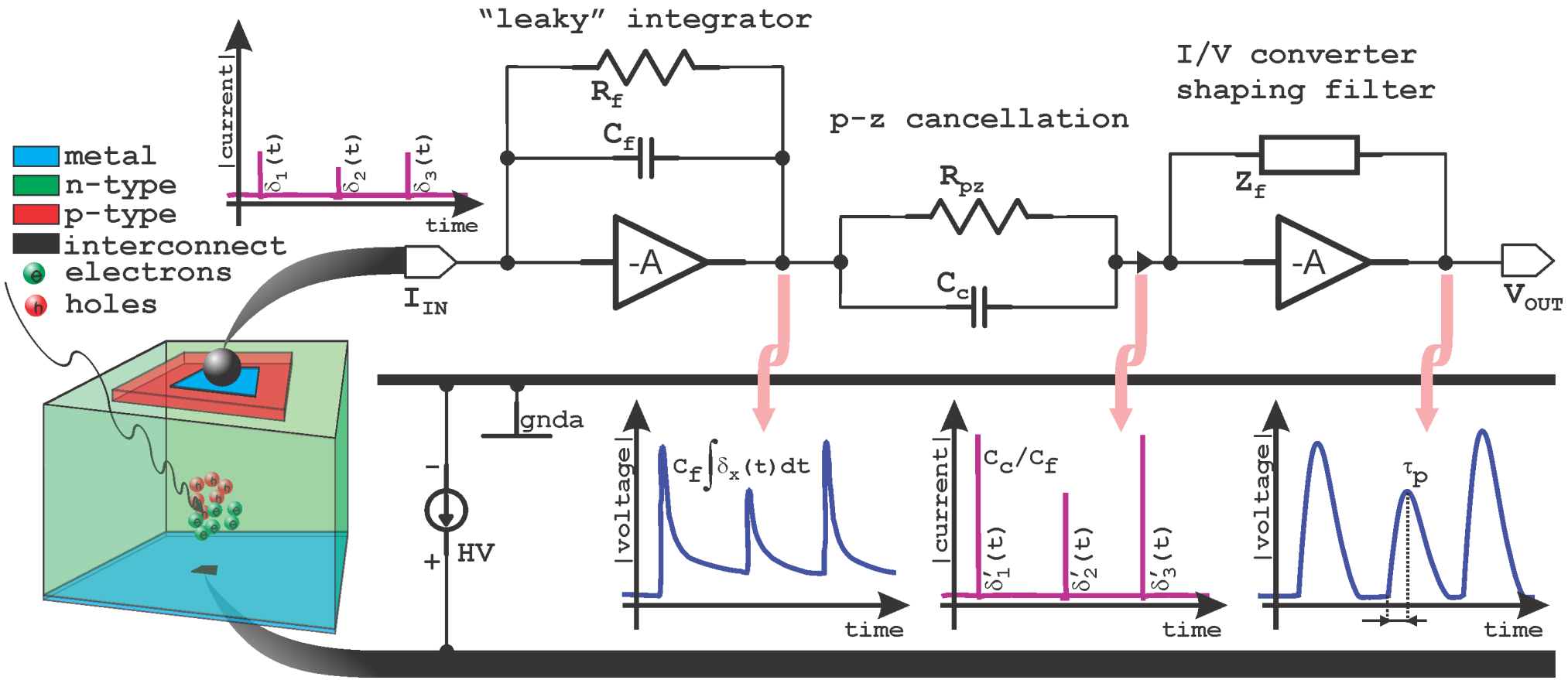
Our approach for the Charge Sensitive Amplifier (CSA) using non-linear pole-zero cancellation is commonly referred as a translinear circuit

For small signals, capacitors realize charge multiplication, whereas for large signals, Self-Cascoded-Field Effect Transistors (SCFETs) switch on to prevent saturation

The time-to-peak time of the shaping filter is 300 ns and the whole circuit consumes < 250 µW per channel (two paths), with >80% of the power being used by the CSA and shaping filter for best performance

Readout Chain and Q-sharing

Charge Processing Chain in the Pixel



In amplitude measurement **p-z cancellation allows:**

- multiplying input charge 100×-1000× before I2V conversion
- implementing sensor leakage current compensation

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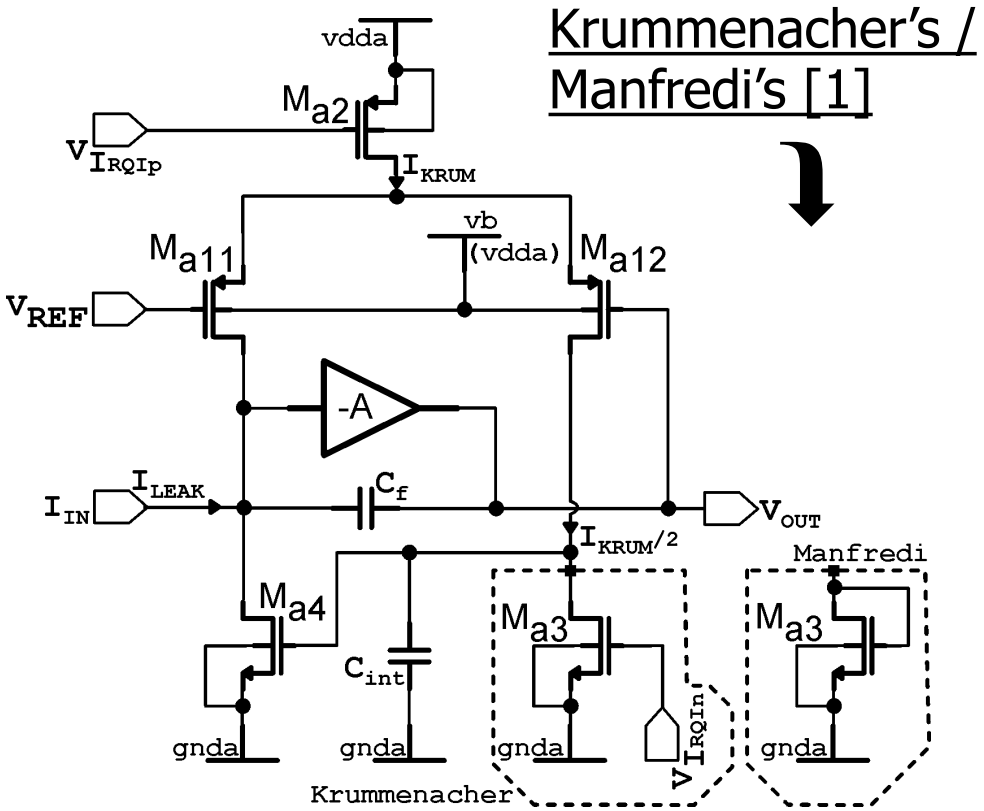
Amplitude Measuring Blocks for Grainy Pixel Detector

Common CSA concepts

all shown for holes



Most widespread solution is the Krummenacher's CSA concept

Not a good solution for our needs: ☹

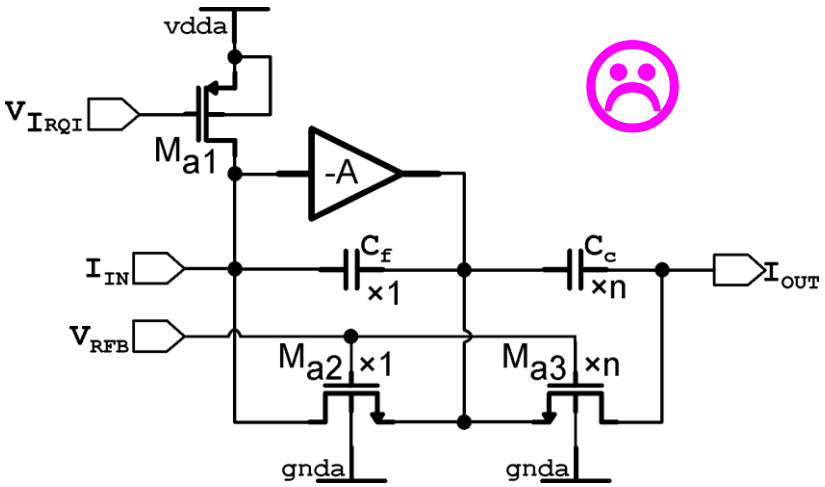
- Limited noise performance (not at the few electrons level)
- Does not allow charge gain (not connectable in p-z cancellation)

[1] F. Krummenacher, "Pixel detectors with local intelligence: An IC designer point of view", Nucl. Instrum. Methods Phys. Res., vol. A305, pp. 527-532, 1991, P.F. Manfredi, et al, "The analog front-end section of the BaBar silicon vertex tracker readout IC", Nuclear Physics B - Proceedings Supplements, Vol. 61, Is. 3, February 1998, 532-538
[2] Y. Hu, et al, "A low-noise, low-power CMOS SOI readout front-end for silicon detector leakage current compensation with capability," in IEEE TCAS I, vol. 48, no. 8, pp. 1022-1030, Aug. 2001

Common CSA concepts

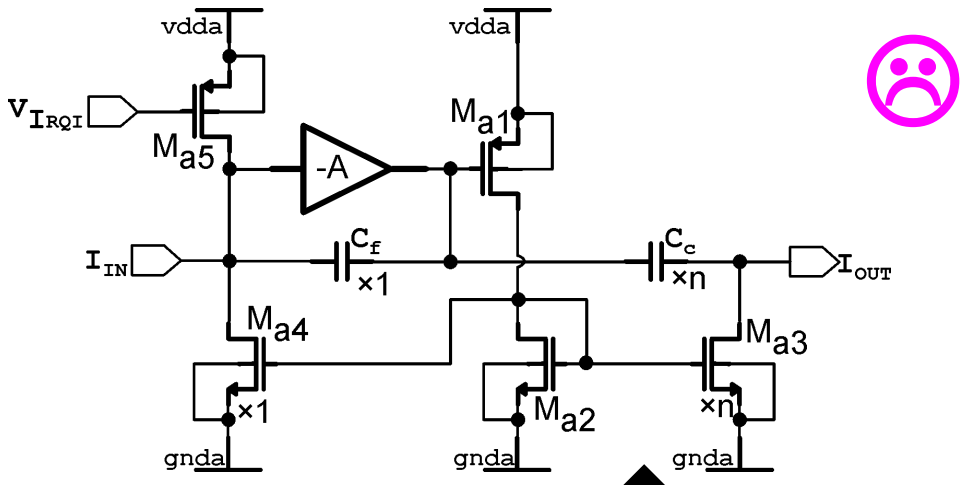
all shown for holes

Frontend solutions implementing input charge signal multiplication $I_{OUT} = n \times I_{IN}$



Common Gate Feedback (CGF) [1]

- Global bias conducive of crosstalk
- Cannot control transistor operation region at the single channel/pixel level



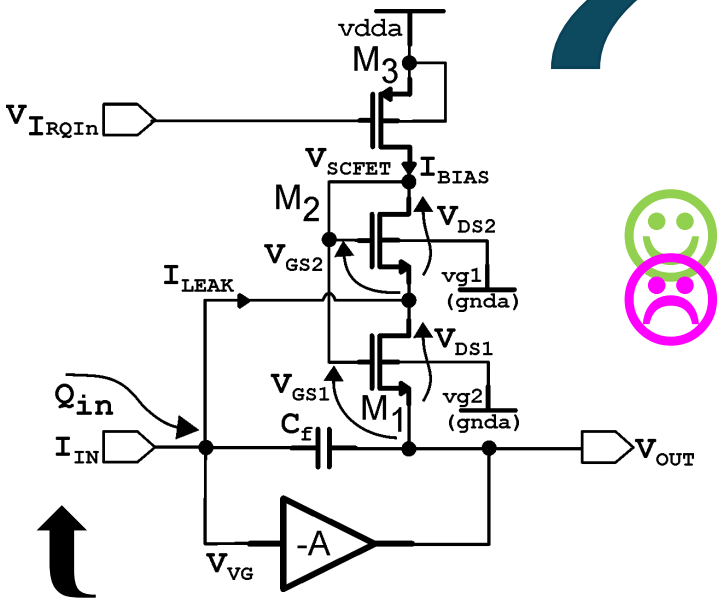
Common Source Feedback (CSF) [2]

- Potential lost of stability
- Multiplied bias current shifts the baseline

[1] G. De Geronimo et al., “A CMOS detector leakage current self-adaptable continuous reset system: theoretical analysis”, Nucl. Instr. Meth. A 421 (1999) 322-333
[2] G. De Geronimo et al., “Front-End ASIC for a GEM Based Time Projection Chamber”, IEEE Trans. Nucl. Sci Vol. 51, No. 4, August 2004 1313-1317

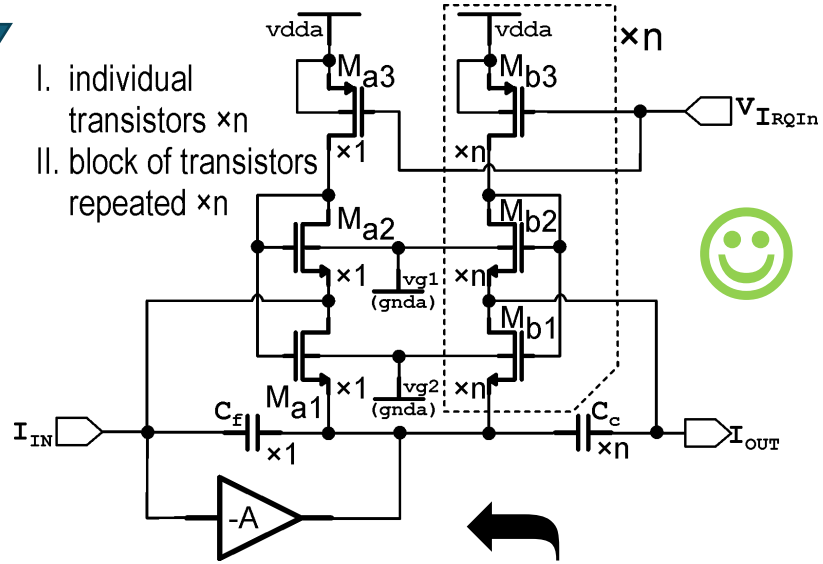
Developed SCFET CSA with P-Z

all shown for holes



CSA with **Self-Cascoded Field-Effect Transistor** (SCFET) feedback network in configuration for integration of input charge signals*

- Better noise performance
- Biasing conditions is largely independent of leakage current and photon rate
- Resulting in stable and predictable transient performance



CSA with (SCFET) configured in pole-zero cancellation scheme*, realizing multiplication (gain) of input charge signal × n

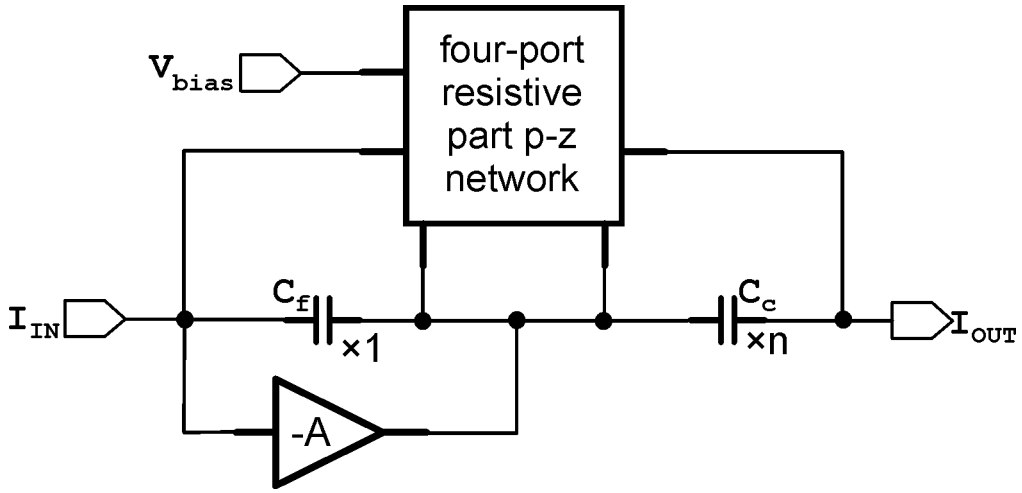
Needed for pixel to manage large number of readout channels

* G. W. Deptuch, P. Otfinowski, “Charge Sensitive Amplifier with Pole-Zero Cancellation”, provisional patent application USPTO Serial No. 63/379,887

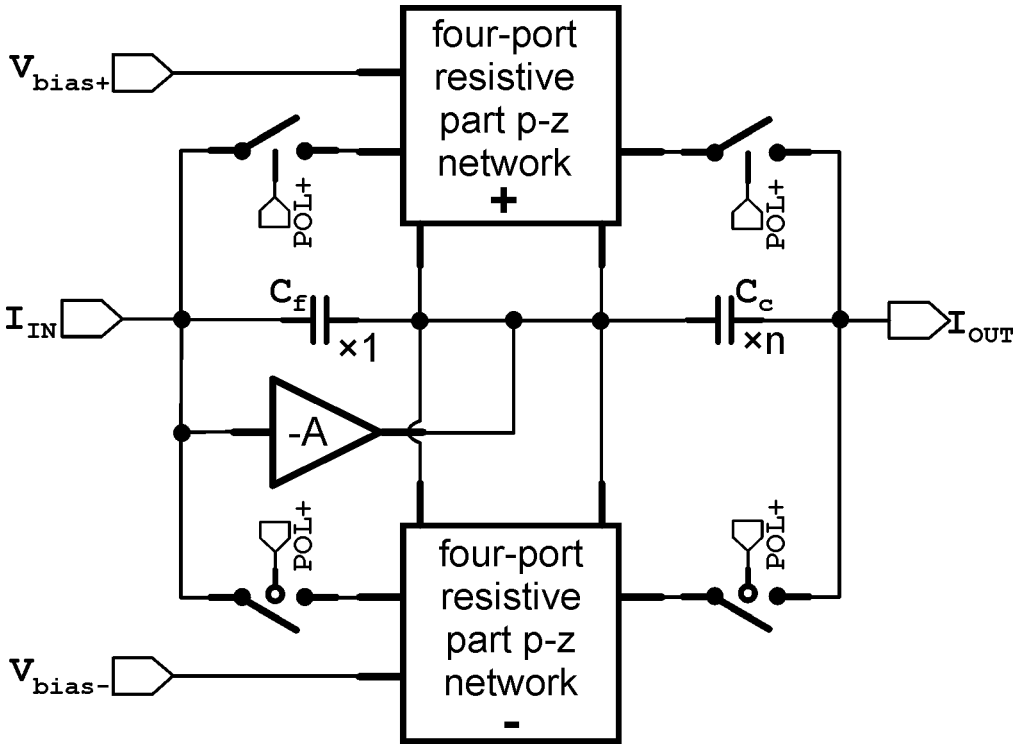
Configuration for Both Polarities

either electrons or holes programmed or switched

- Circuits can be constructed to readout both polarities
- Can be cascaded to obtain multiplied gain



configuration for processing of a single polarity of charge signals

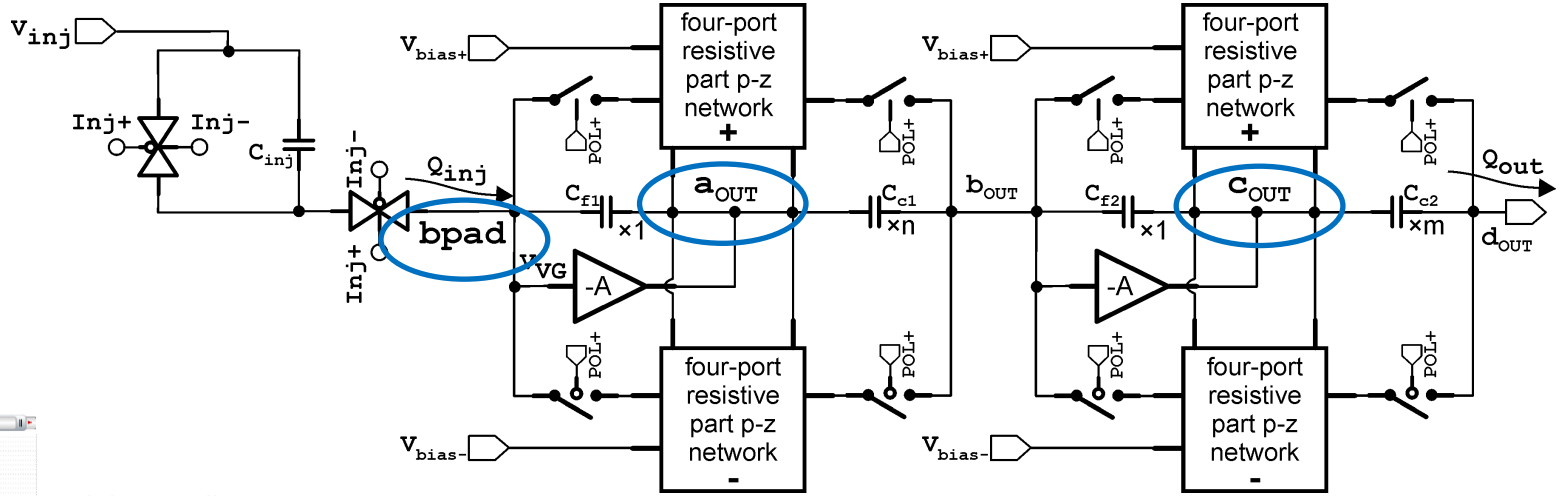


configuration for processing of both polarities of charge signals (programmed or dynamically switched using the switches)

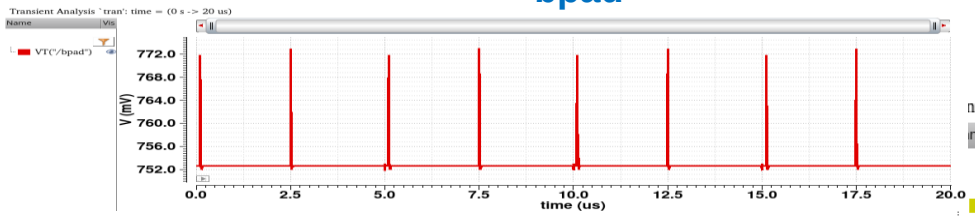
CSA in Simulation

$$I_{OUT} = n \times m \times I_{IN}$$

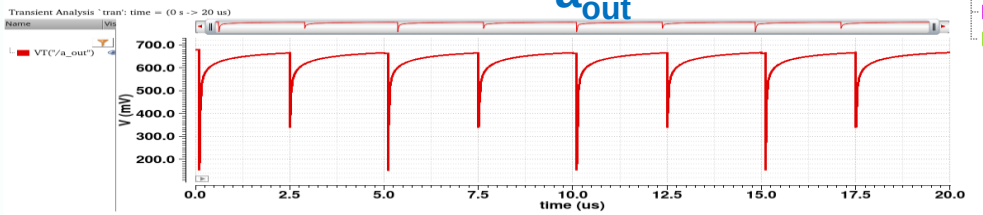
- Leaky integration works: brings back to baseline quickly
- Amplification works: translinear p-z cancellation multiplies charge



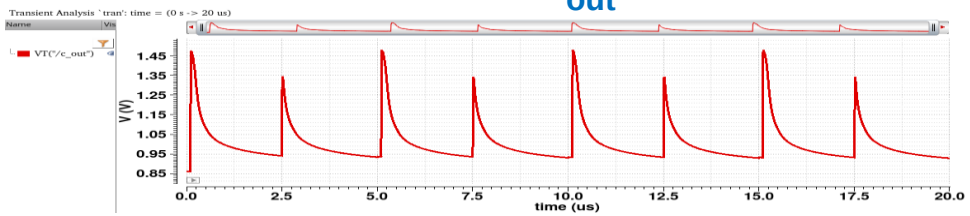
bpad

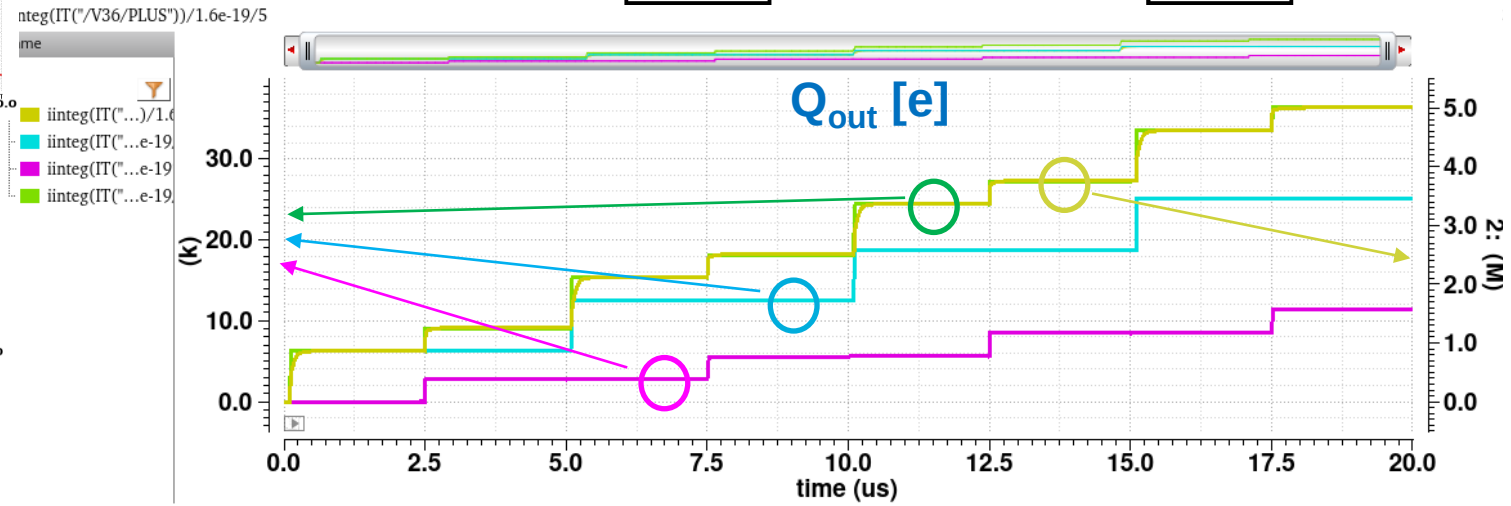


a_{out}



c_{out}





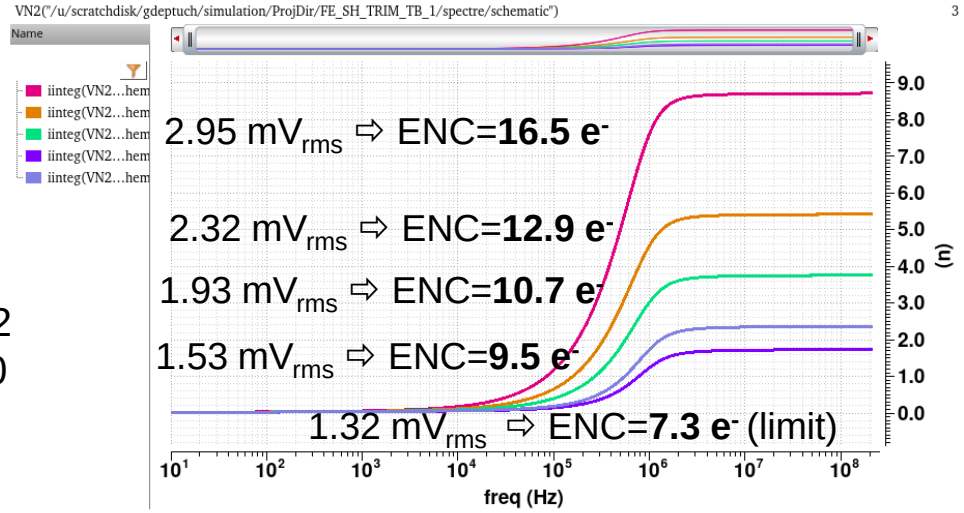
- Input- left axis: magenta ½ fC injects, cyan 1 fC injects, green summed injections.
- **output right axis: yellow Q_{out}**

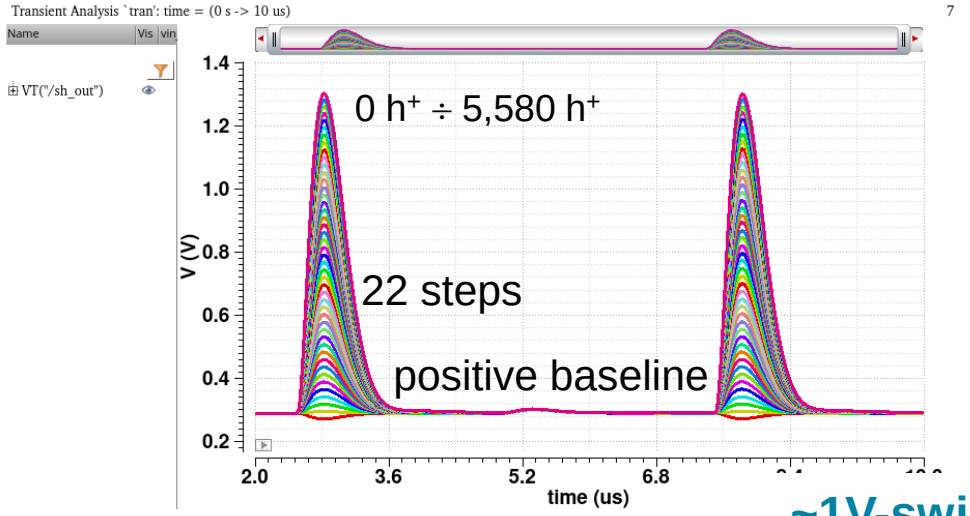
CSA + Shaping Filter in Simulations

Passive components used for the shaping filter

1real, 2complex conjugated poles, 300 ns peaking time

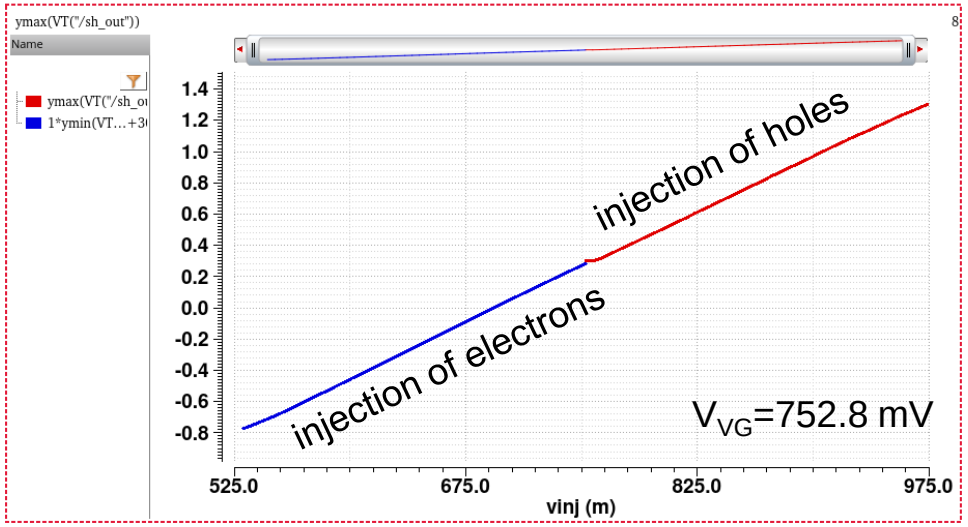
AC noise simulation for positive polarity for 0 pA, 2 pA, 12.5 pA, 25 pA and 50 pA **current biasing SCFET feedback** in CSA

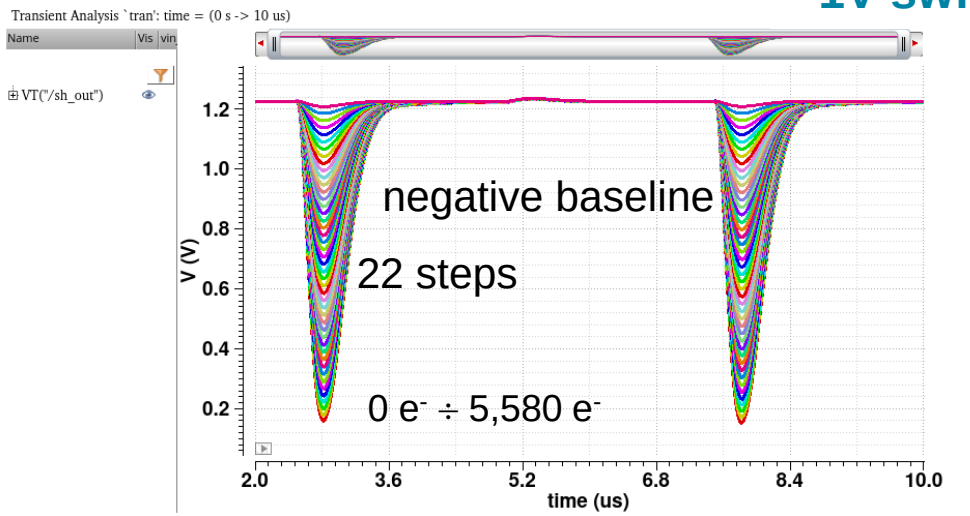




~1V-swing

linearity for positive and negative signals obtained separately





Transient noise simulations confirm we maintain better than 1% energy resolutions for all energy ranges of interest

A design to enable time-continuous amplitude spectroscopy

Sample and Hold (S/H) circuits are used for generating snapshots of the amplitudes of the central pixel and its neighbors

The circuitry includes an interface to the recently developed Event-Driven with Access and Reset Decoder (EDWARD) readout protocol, which removes the need to impose a prioritization scheme during arbitration

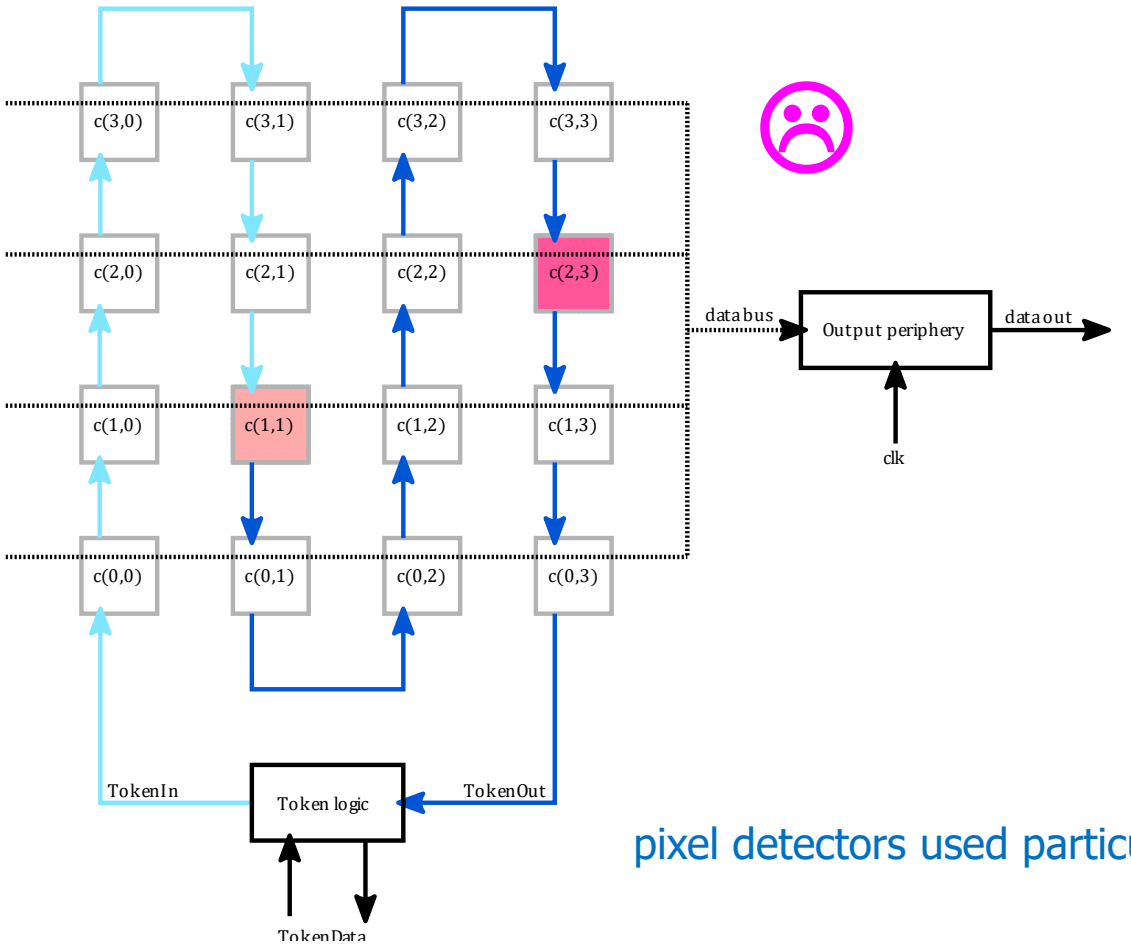
We fully integrated the EDWARD protocol into SystemVerilog hardware description code and included specifications to use it with the Configuration-Readout-Testability (CRT) development tools

This approach path was chosen to be able to efficiently design the ASICs together with similar other ASICs, in a scalable, semi-automatic way

Common Readout Schemes

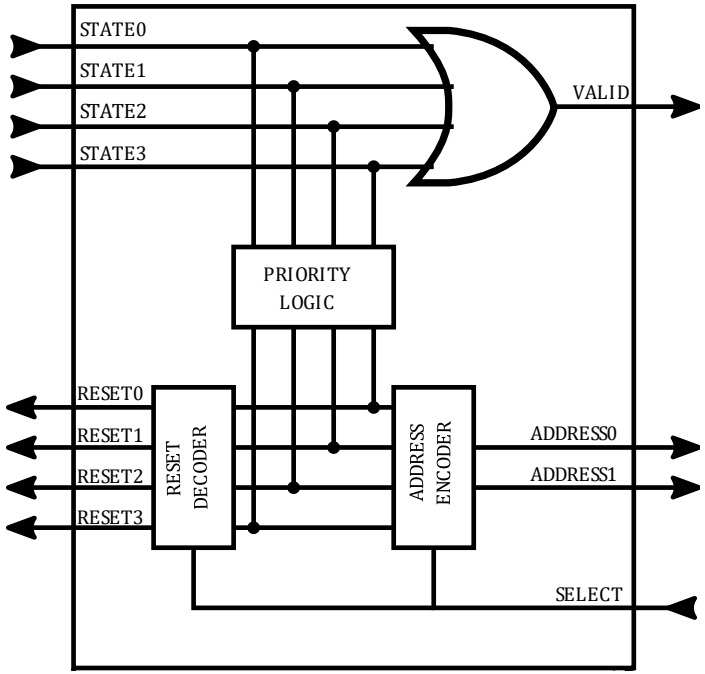
Token passing:

- varying latency (hit first or last pixel in the scan chain)



Priority encoder:

- suited only to framed (snapshoted) readouts



pixel detectors used particularly in fluorescence imaging needs to be event-driven read out

Continuous readout: we are interested in reading signal while they arrive

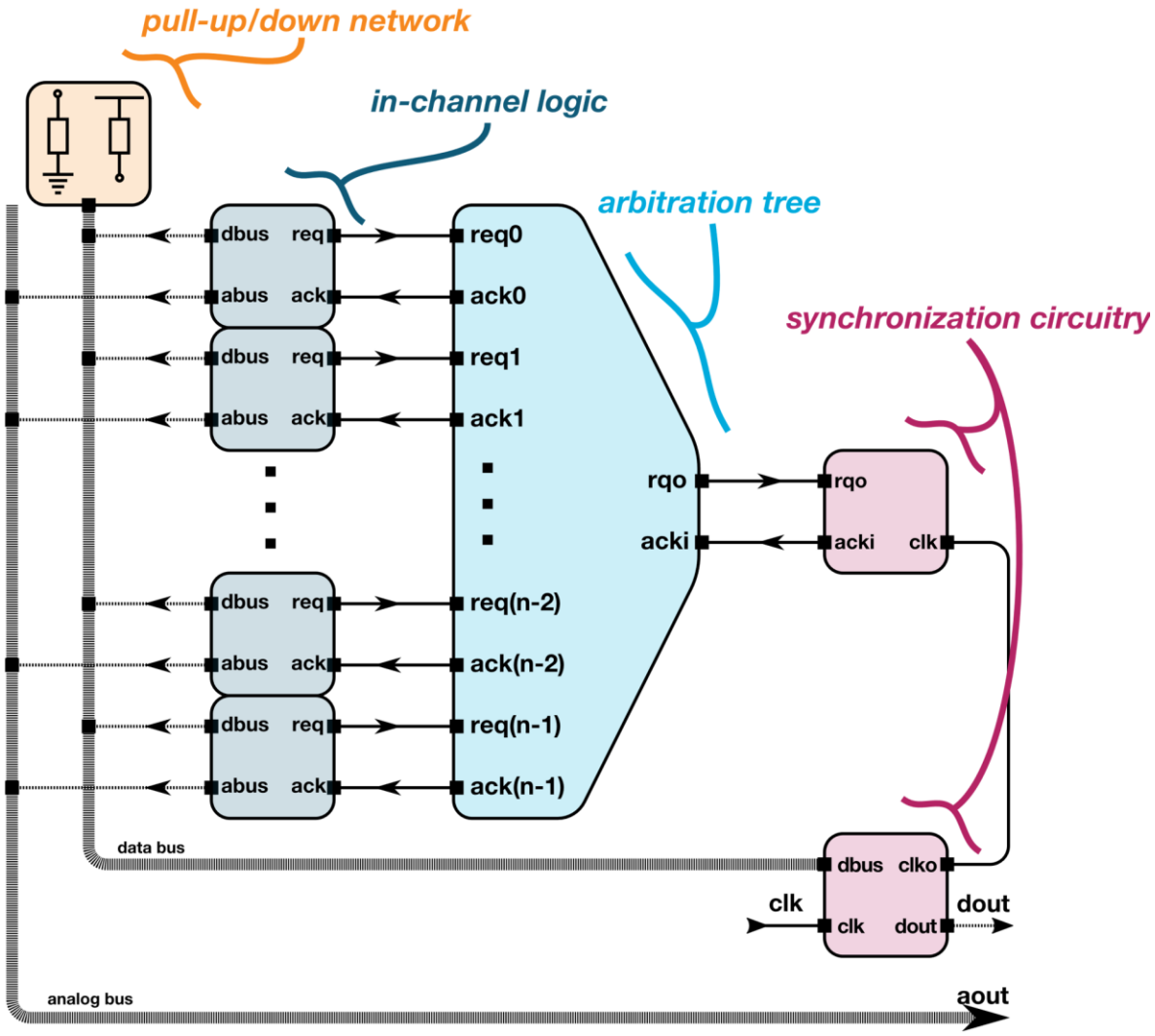
EDWARD – Event Driven With Access and Reset Decoder

Reset decoder provides guaranteed readout time for each transaction, and no dead time between them

No need to provide a clock to each pixel - requests can be sent asynchronously

Uninterrupted access to data within a pixel

No priority encoder



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Gorni, D. S., et al. "Event driven readout architecture with non-priority arbitration for radiation detectors." *Journal of Instrumentation* 17.04 (2022): C04027.

Event Driven Readout (EDWARD)

D.S. Gorni, et al., " Event driven readout architecture with non-priority arbitration for radiation detectors", 2022 JINST 17 C04027

TWEPP 2021

Introduction

The poster introduces an efficient system for collecting sparse data originating in multiple sources that operate asynchronously, ultimately sending data to the central data acquisition system in such a way that there is no direct relationship between spatial position of the channel and the order of the channels to be transmitted. The protocol and hardware architecture were developed for ASICs destined for reading out 1D or 2D multichannel radiation sensors that can be micro-strip or pixelated radiation sensors. The presented system can be used to read out both digital and analog data from the channels. It is done via shared digital data buses and analog wires.

Default bus state

The 'rqo' output from the arbitration tree is effectively the logical sum of requests from all channels. This signal, however, is not synchronized in any way with the acknowledgement tokens - the request may come after token expiration or come too late, and the token will not be able to start the transaction due to too short duration of the active state in the channel. For this reason, a mechanism should be provided to distinguish between data derived from readout of a channel and an empty state. This has been implemented as a **network of up and down pulls that delineate empty data**. The pattern thus determined can then be discarded on-chip by a peripheral circuit or off-chip in the acquisition system.

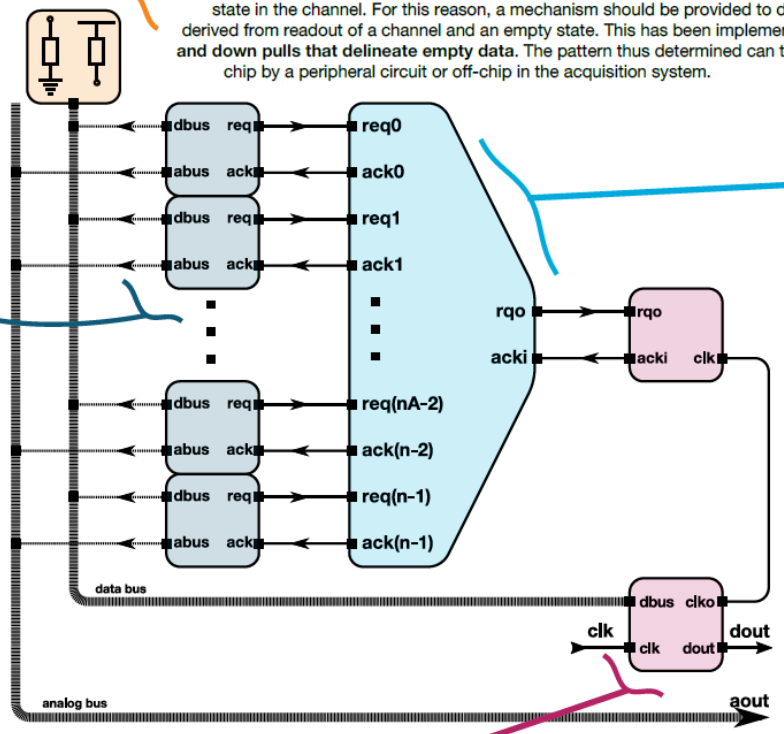


Fig.1 Block diagram of event driven readout system

In-channel logic

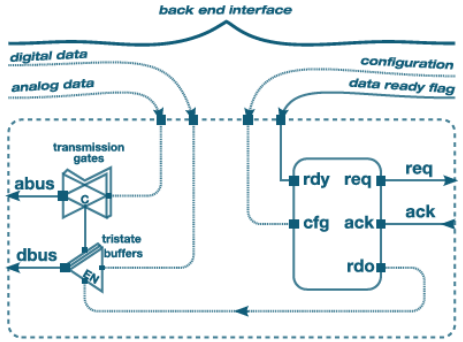


Fig.2 In-channel logic general structure

- This is a logic presented in each channel and its function is to manage readout transactions between the channel and global peripheries.
- When the data ready flag 'rdy' is set by the back end electronic (e.g. peak found, ADC conversion done) the controller block issues the read request 'req' **immediately.**
- When 'req' is active, the readout phaser block is sensitive to the transition to the active logic state on the channel acknowledge input 'ack'.
- This transition can be describes as receiving an **acknowledge token** with assigned expiration time, after which 'ack' switches back to the inactive state.

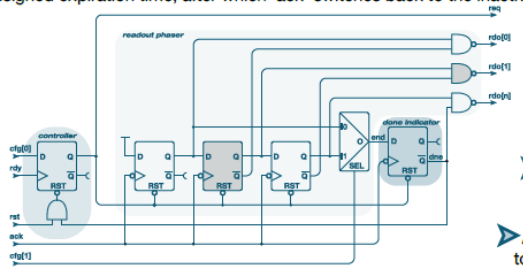


Fig.3 In-channel logic core

- The first token initiates readout transaction.
- A single transaction may consist of **multiple readout phases** in which different data (including data from adjacent channels) may be transmitted sequentially and uninterrupted by requests from other channels.
- The maximum number of phases is determined by the number of flip-flops in the phaser chain. However, the actual number of phases can be dynamically reduced by various 'cfg' configurations.
- Only one bit of the redaout control 'rdo' is active during each transaction This active bit is used to enable the corresponding bank of tristate buffers and transmission gates.
- After the last phase is processed done flag 'dne' is set and in result next token initiates reset procedure for in-channel logic during which 'req' is cleared.

Synchronization

The data are latched inside the output periphery by the clock 'clk'. Latching of the data synchronizes the readout with the data acquisition system. Data are latched before generation of each new token, yielding a new set of latched data for each token. Data can be sent serially off the chip. The **serialization clock is used therefore for generating readout tokens** through its appropriate division, whereas the duty cycle and frequency of the divided clock 'clko' can be decided with a significant level of a latitude.

Arbitration tree

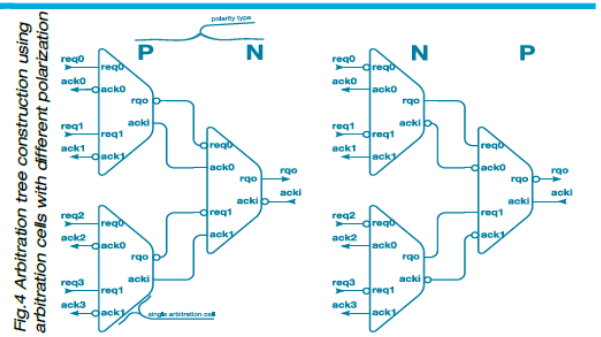


Fig.4 Arbitration tree construction using arbitration cells with different polarization

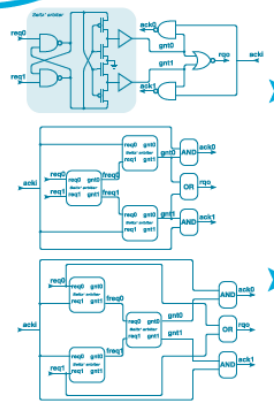


Fig.5 Different embodiments of arbitration cell

- An arbitration cell upon receiving read request signals 'reqX', selects one of the read request signals and routes an acknowledge token 'acki' that reaches this cell as routed from another arbitration cell located above in the arbitration tree to the direction from which the read request signal has been accepted. Routing is done in a form of gating of the acknowledge signal with the use of grant signals (gnt0, gnt1) generated by the arbiter. The arbiter decides which of the two read request signals is selected and there is **no priority between signals.** When two read request signals arrive simultaneously, one of them is selected, whereas the selection is random.
- Basically, almost all the arbitration cells need to be able not only to decide which of the two read request signals can be services but also whether new read request signals arrive during the active level of the acknowledge signal. The latter goal is rising a need of arbitrating between the read request signals and the acknowledge signals, leading to the general concept of the readout control system with **arbitration that is operated without distributing any system clock.**

Design and results

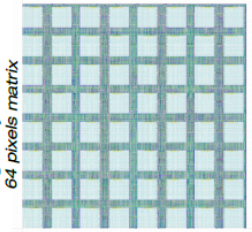


Fig.6 Layout of the 64 pixels matrix

In Fig.6 layout of the pixel matrix consisting of 64 channels is presented. Physical design was implemented with the use of the tools for automatic P&R and TSMC 65nm Standard Cell Library with added designs for Seitz' arbiters. The squares shown in the figure are placeholders for the analog frontend.

Transistor level simulation results are shown in Fig. 7. During transaction each channel sends its address (6bits) and group sends its address (8bits). Merged value is observed on digital bus. Config '00' result in one readout phase and '01' in two phases. It is worth to note how token is passed from one channel to other after transaction is done. Token is reused and **no dead time is observed.**

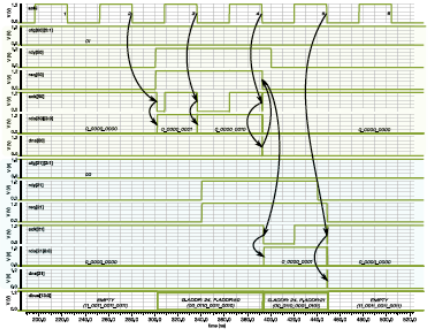
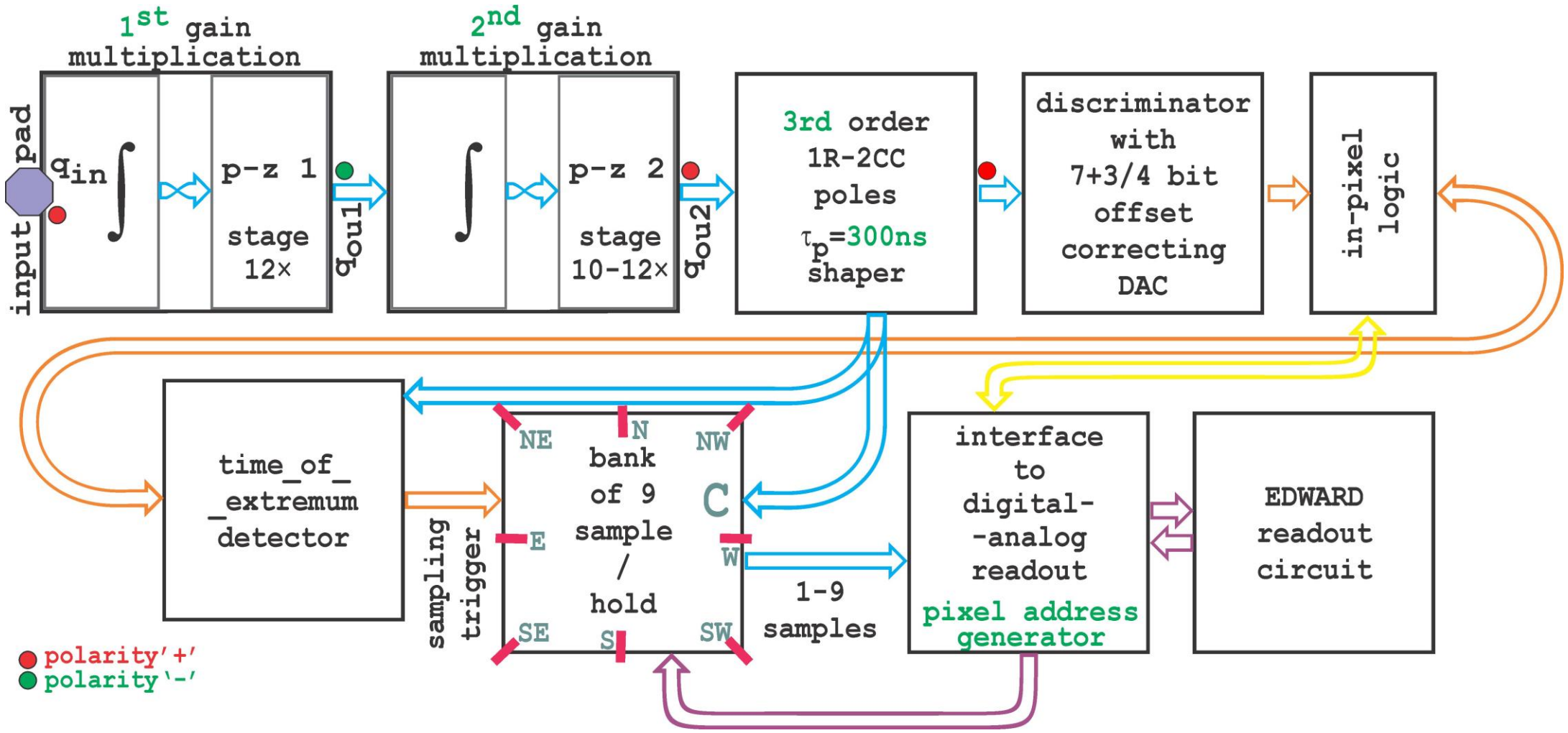


Fig.7 Design simulation results

Blocks Put Together

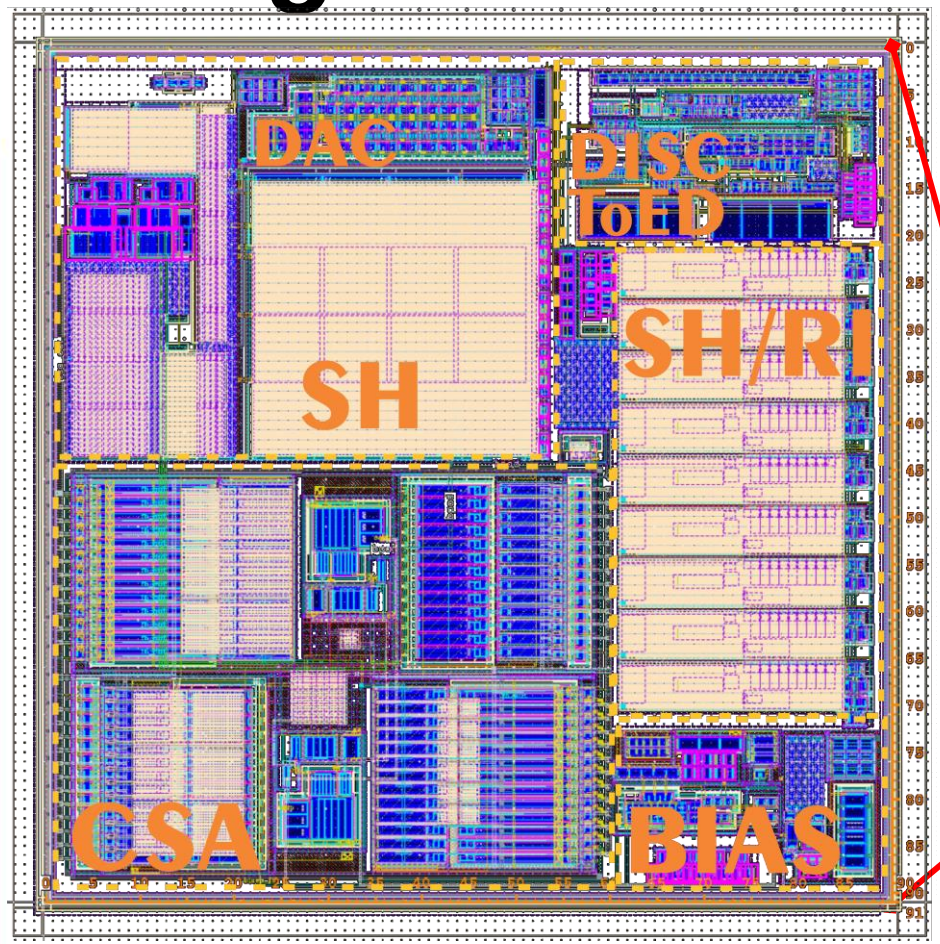
Amplitude Measuring ASIC

PAMPED: Pixels with AMPlitude and Event-Driven readout

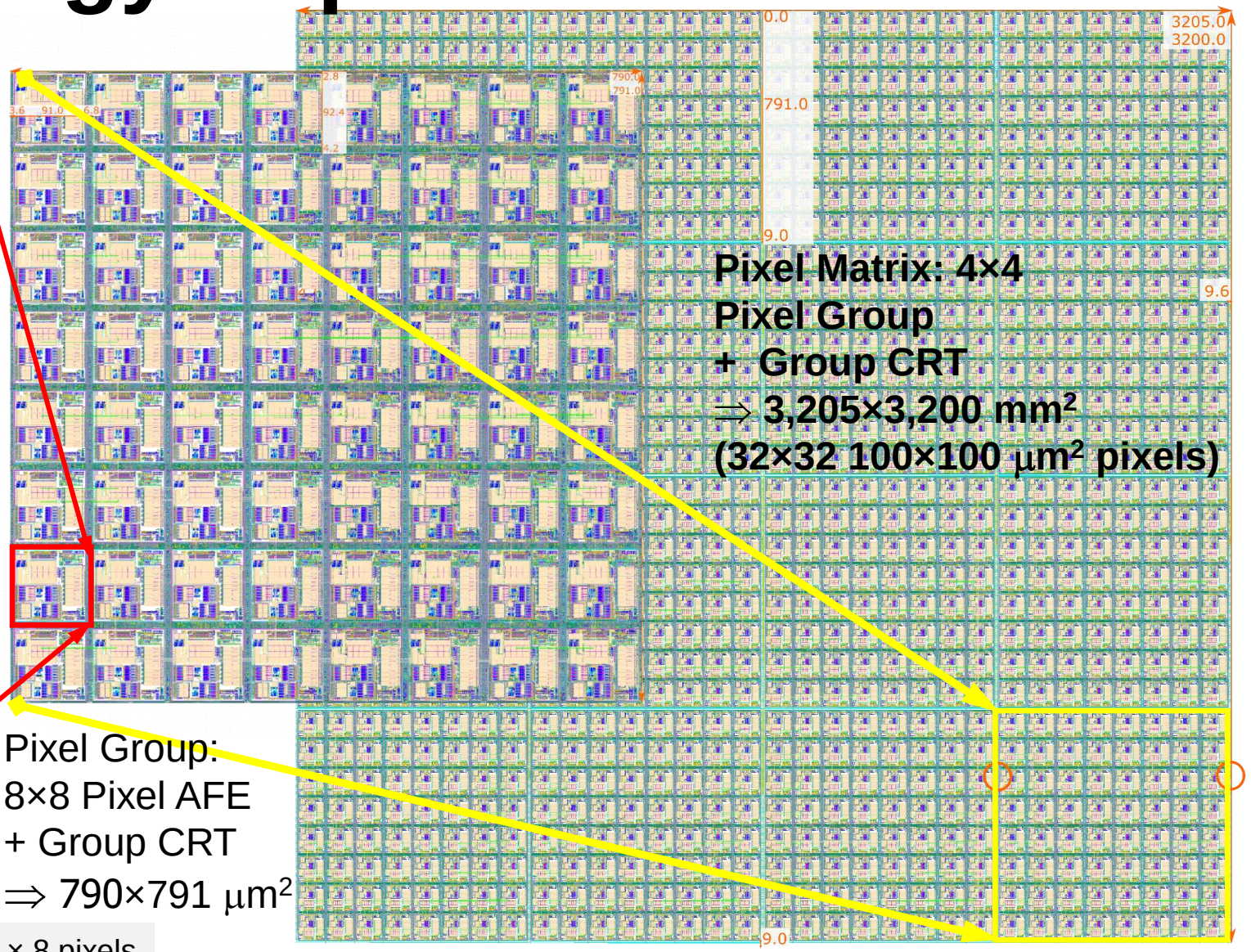


detect X-rays < 2 keV ⇒ ENC=O(10 e^-) + ~10b DR in ~100 ×100 μm^2

Design Methodology of pixel detector



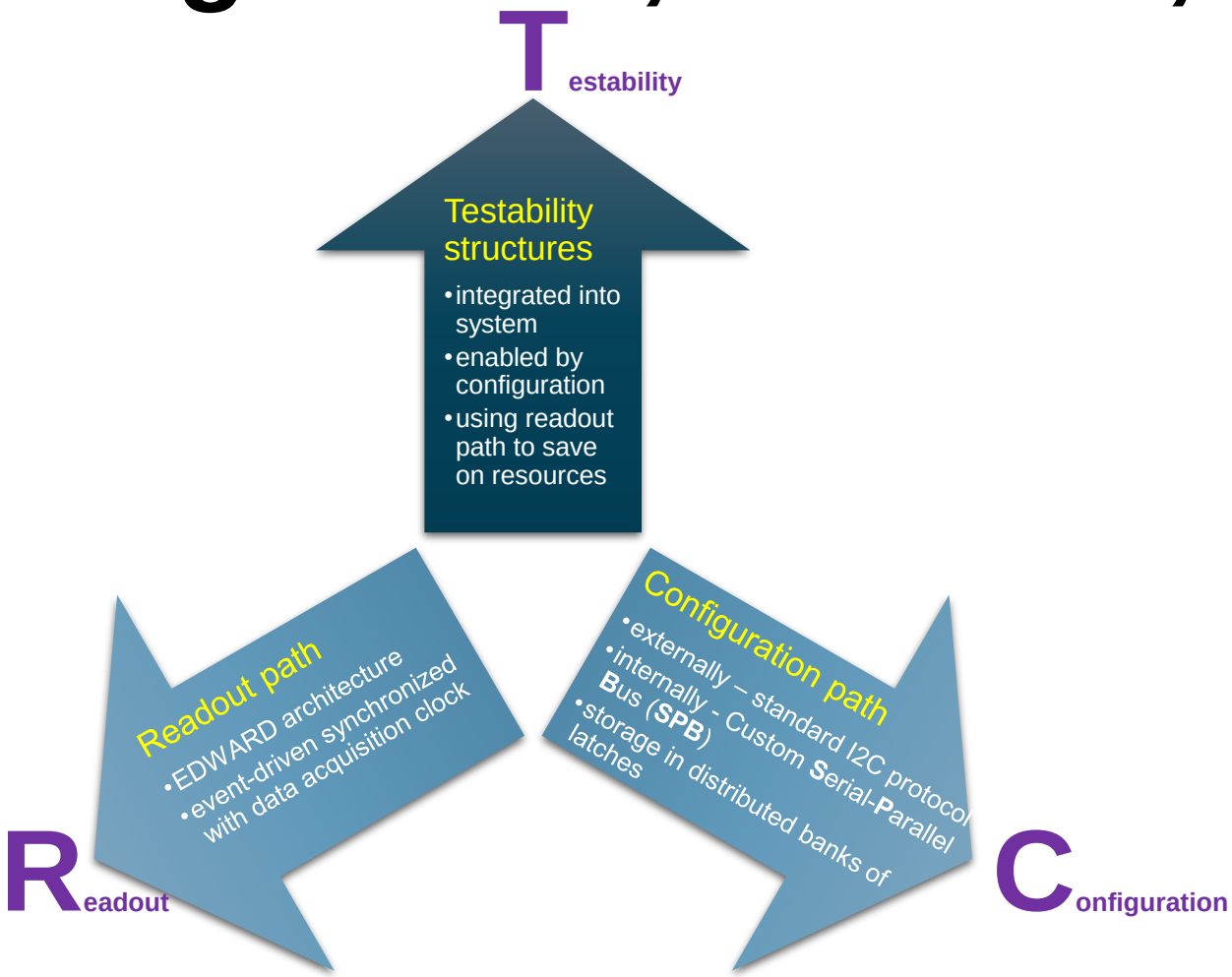
Pixel AFE: CSA, SH w DAC, DISC, TeOD, SH/RI + BIAS ⇒ 90×91 μm²

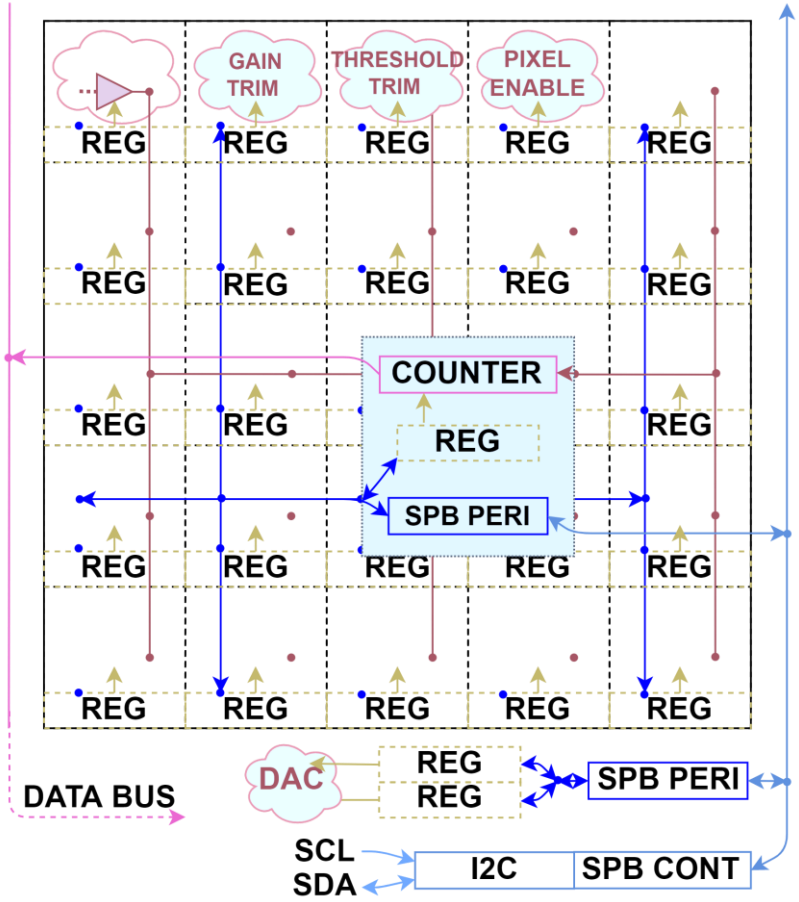


Pixel Group:
8×8 Pixel AFE
+ Group CRT
⇒ 790×791 μm²

32 × 32 pixels matrix obtained by tiling 4 × 4 basic 8 × 8 pixels groups ⇒ suitable for continued tiling.

Configuration, Readout, Testability



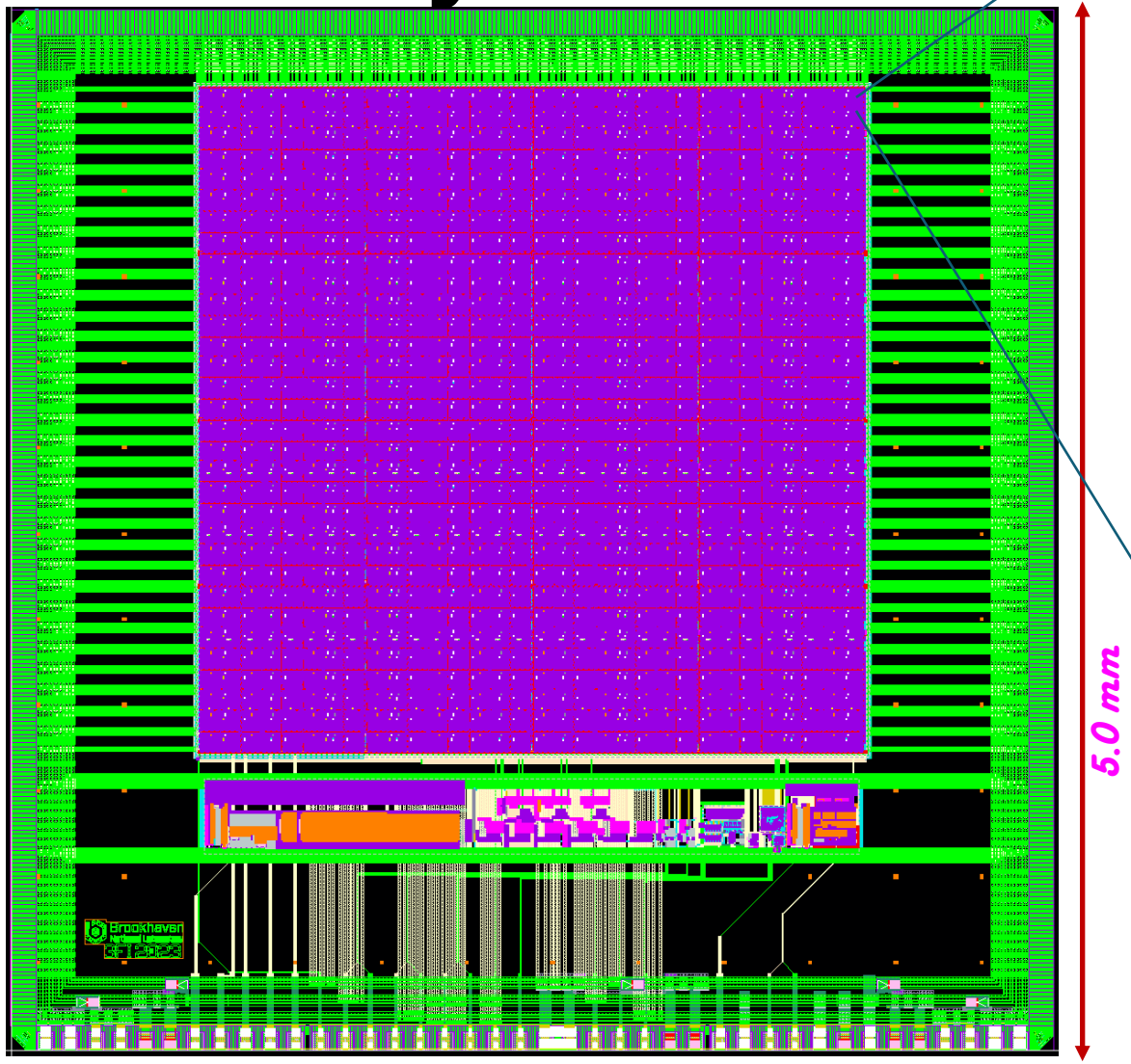


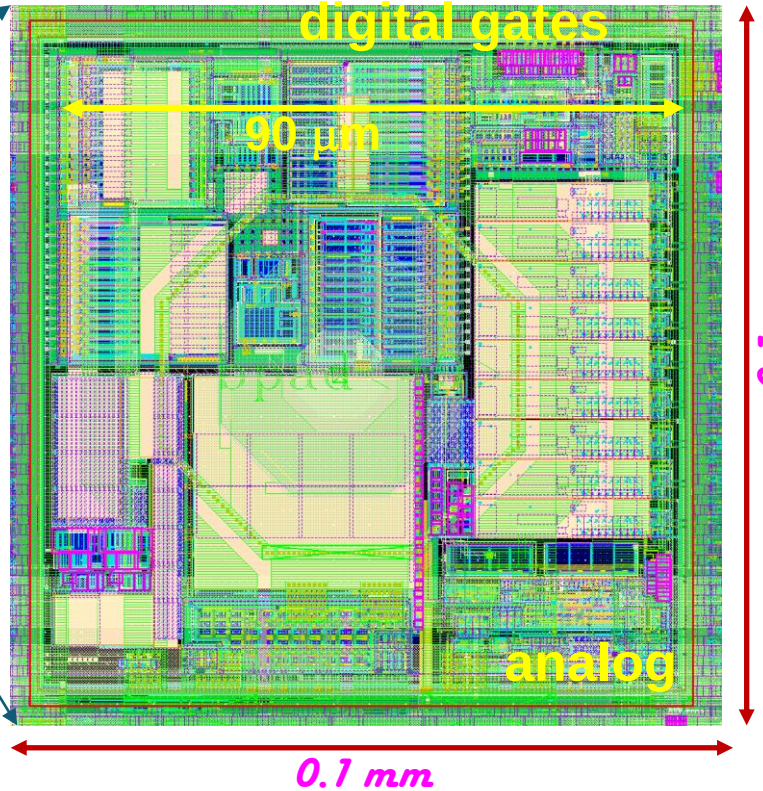
Pixel can be reached directly and addressed directly

Co-Designed **PLATFORM:**

- RTL code of complete Configuration-Testability-Readout
- parametrized and scalable for “virtual painting” of back-bones of pixel detectors
- **code with implementation constraints shareable with interested parties**

ASIC Layout





About 4,000 transistors / pixel,
Ratio of 20:80 analog:digital,
Process CMOS 65 nm,
Submitted for fabrication through CERN/IMEC/TSMC Foundry Services.

Two new IPs:

- PCT, WO/2022/221068 - Event-Driven Readout System with Non-Priority Arbitration for Multichannel Data Sources
- Provisional patent application Serial No. 63/379,887 “Charge-Sensitive Amplifier with Pole-Zero Cancellation”

Main features:

- matrix of 32×32 100×100 μm^2 pixels;
- event-driven readout @ 10 Mhit/s (limited by analog) with:
  - digital output providing addresses of central, hit pixels;
  - analog output providing analog values of central hit pixels and its neighbors (sampled values when central pixel reaches its extremum);
- ENC$\in$(10 e^-, 20 e^-);
- signal swing 1.2 V $\Rightarrow$ targeted DR eq. 10 bit;
- both signal polarities can be handled;
- power consumption ~200 μW per pixel;

Brookhaven National Laboratory

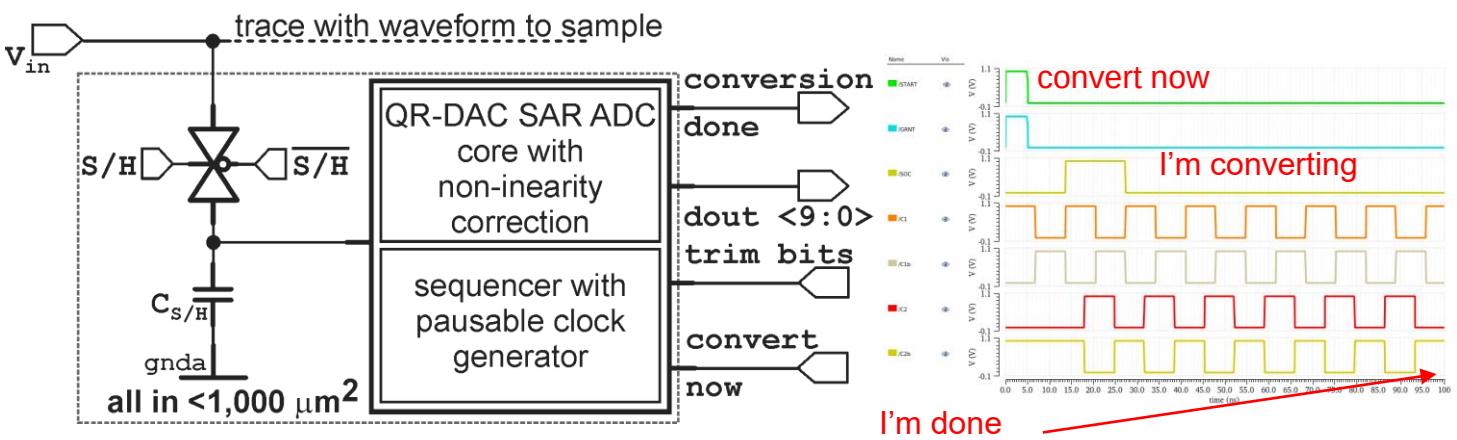
In-Pixel Conversion

1000 μm² ADC per pixel

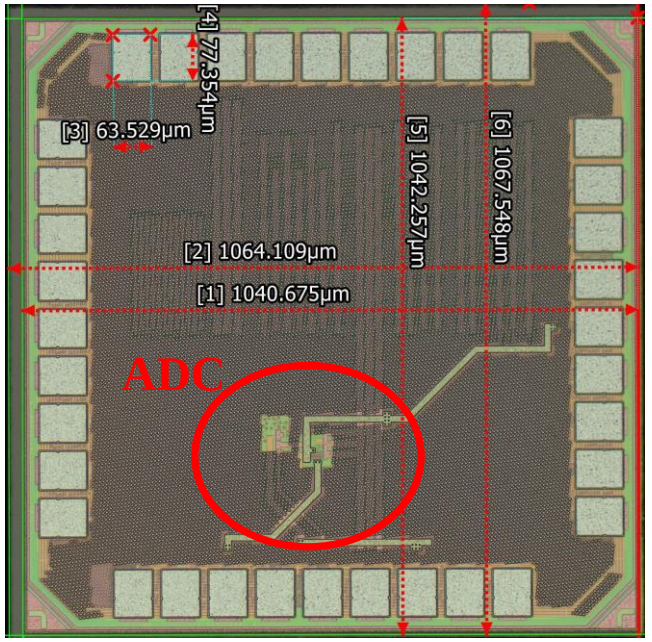
block of 9 S/H (suitable for sampling but primarily driving output lines with <1% amplitude distortions) requires about 22×45 μm2 =~1000 μm²

let's develop

low-rate (~1 Mbps)**, medium-resolution** (10 bit) and **extremely small Si footprint** (1000 μm²), **low power** (<100 μW when ON) converter for distributed (parallel) in-situ operation: aka S/H-ADC cell



major features: autonomous operation



InPixADC_P1 under testing

charge redistribution with internal sequencer

Self clocked ADC – becomes alive when is converting

Summary

Presented design flow for pixel Readout ASIC:
- suitable for amplitude spectroscopy with handling of charge shared events
- providing continuous time of operation to handle asynchronous signals
- equipped with true event driven readout
- with analog output, but per/pixel ADC is the next step

Acknowledgements

This is the work of a large team: including sensors, ASIC, DAQ, interconnect, and system at the Instrumentation Division; Photon Science and other teams

Particular thanks to Grzegorz Deptuch, Abdul Rumaiz, Gabriele Giacomini, Don Pinelli and Henric Krawczynski

Thank you!