# Latest results on timing performance of monolithic silicon pixel detectors

Stefania Maria Beolé

# Pixel detectors state of the art


- ALPIDE: Tower Semiconductor 180nm CMOS Imaging Sensor (CIS) (Process development 2012-2016)
  - 512 x 1024 pixels of 28 x 28 $\mu m^2$
  - Full CMOS in the pixel (deep pwell): Amplification, Discrimination, multi event buffer
  - Ultra-low power < 40mW/$cm^2$ (< 140mW full chip):
    - 40 nW front end, sparse readout
    - Matrix 6 mW/$cm^2$, up to 40 mW/$cm^2$ including periphery
  - Detection efficiency > 99%
  - Spatial resolution ~5$\mu m$
  - Low fake-hit rate: << $10^{-6}$/pixel/event ($10^{-8}$/pixel/event measured during commissioning)
  - Radiation tolerance:
    - 270 krad total ionising dose (TID),
    - > 1.7 $10^{13}$ 1MeV/neq non-ionising energy loss (NIEL)

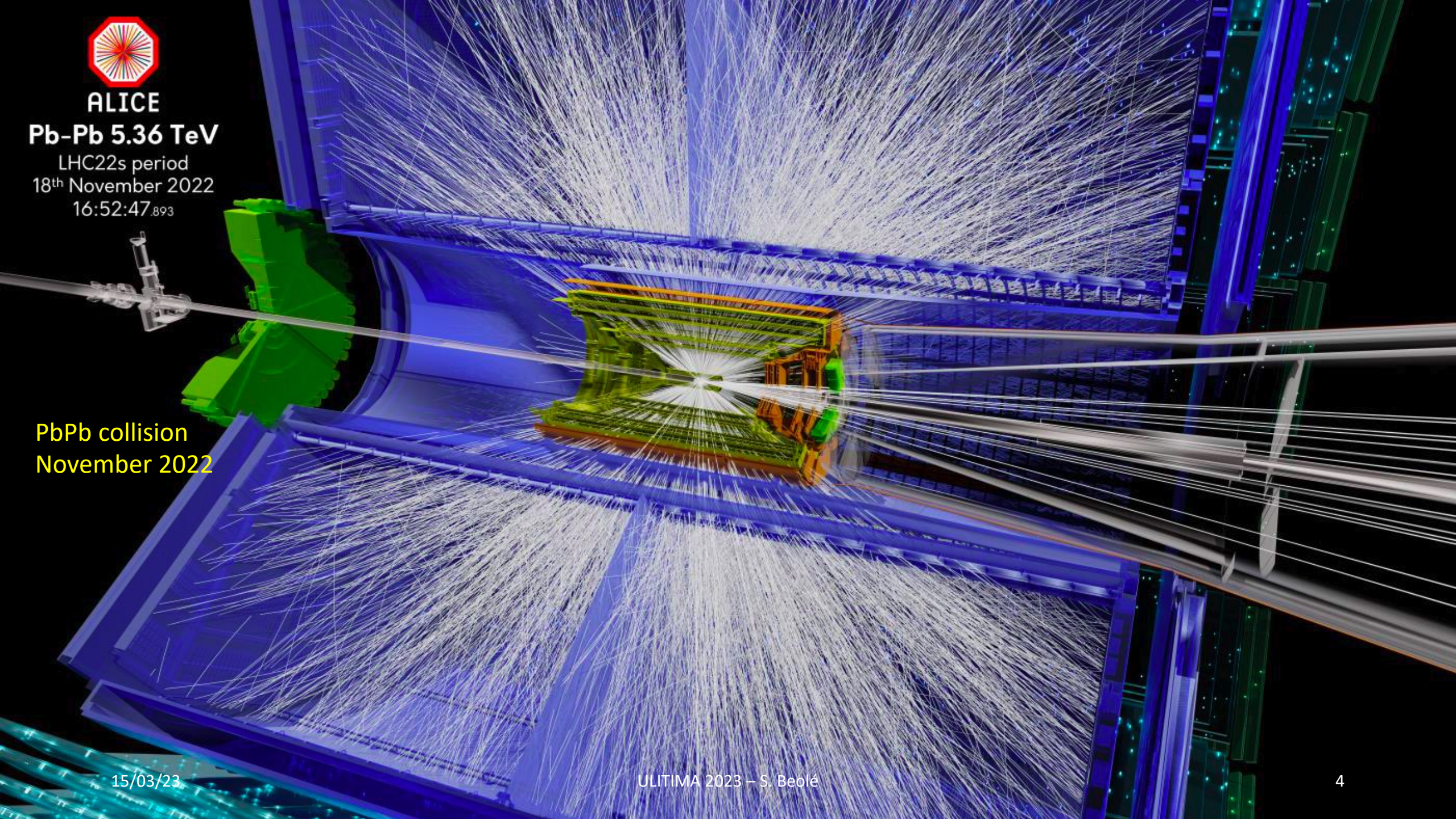
- R&D effort within the ALICE collaboration
  - excellent collaboration with foundry
  - more than 70k chips produced and tested

- ALICE ITS pioneers large area trackers built of MAPS (EIC, ALICE 3, FCC?)

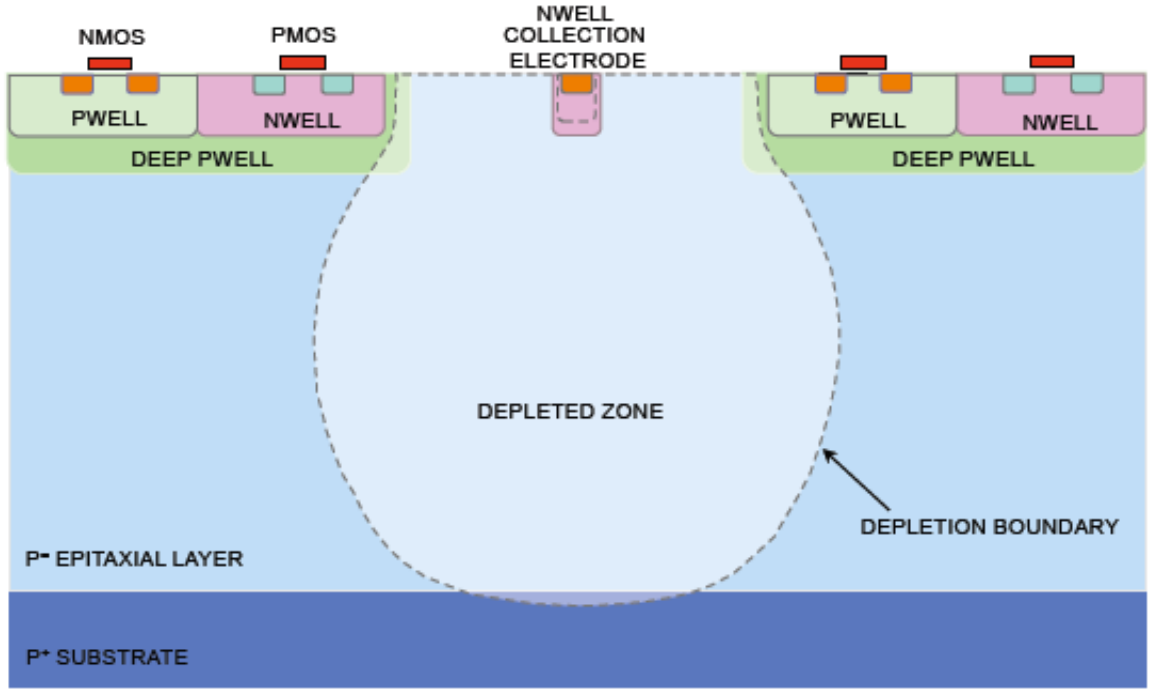
# Pixel detectors state of the art

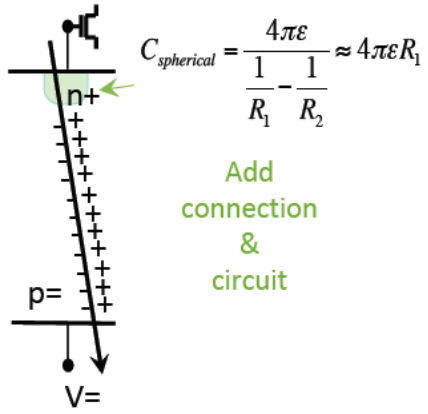

- Pro: satisfies Nicolo's requirements
  - good spatial resolution
  - low material budget
  - low power consumption
  - fully efficient
- Limits:
  - Standard process: sensitive epitaxial layer not depleted -> slow response, integration time > 2µs
  - limited radiation hardness

**works very well in PbPb at 50kHz**


ALICE
Pb-Pb 5.36 TeV
LHC22s period
18th November 2022
16:52:47.893
PbPb collision
November 2022

# ALPIDE: Standard process: sensitive epitaxial layer not depleted




$$C_{spherical} = \frac{4\pi\varepsilon}{\frac{1}{R_1} - \frac{1}{R_2}} \approx 4\pi\varepsilon R_1$$

Add connection & circuit

Planar junction
Depletion width $= \sqrt{\frac{2\mathcal{E}|V|}{qN_A}}$

Spherical junction
Outer depletion radius $= \sqrt[3]{\frac{2\mathcal{E}|V|}{qN_A}\frac{3R_1}{2}}$

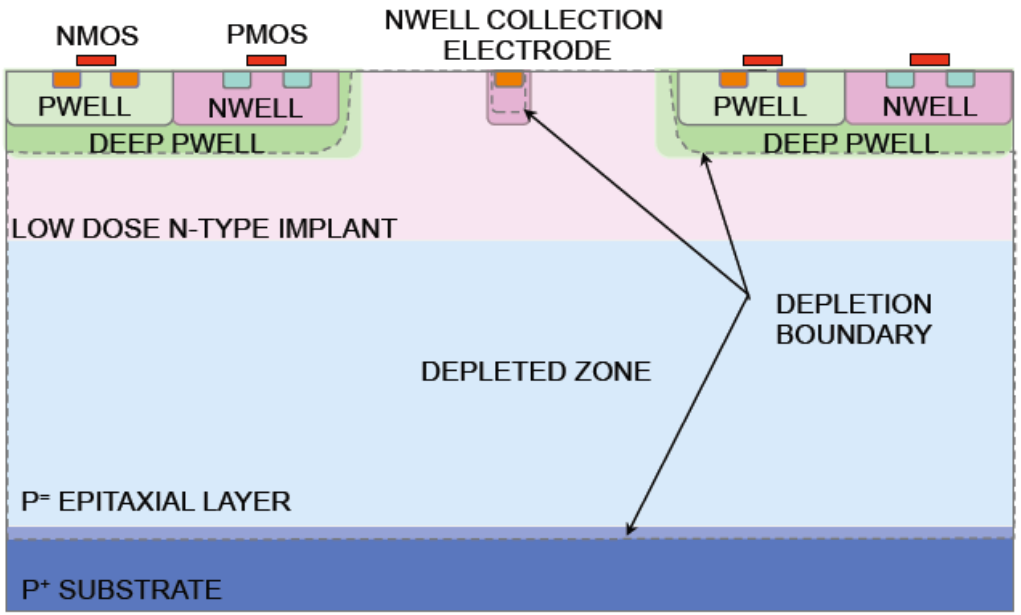
- Signal charge is collected from the non-depleted layer, diffusion dominated and prone to trapping after irradiation
- Planar vs spherical junction
  - Planar junction: depletion thickness proportional to **square root of reverse bias**.
  - Spherical junction : depletion thickness proportional only to **cubic root of reverse bias**, inner radius R1 to be kept small for low capacitance
- Deep well and substrate limit extension of the depletion: to fix this -> pixel design/process modification, see next slide.

Tower Semiconductor 180nm



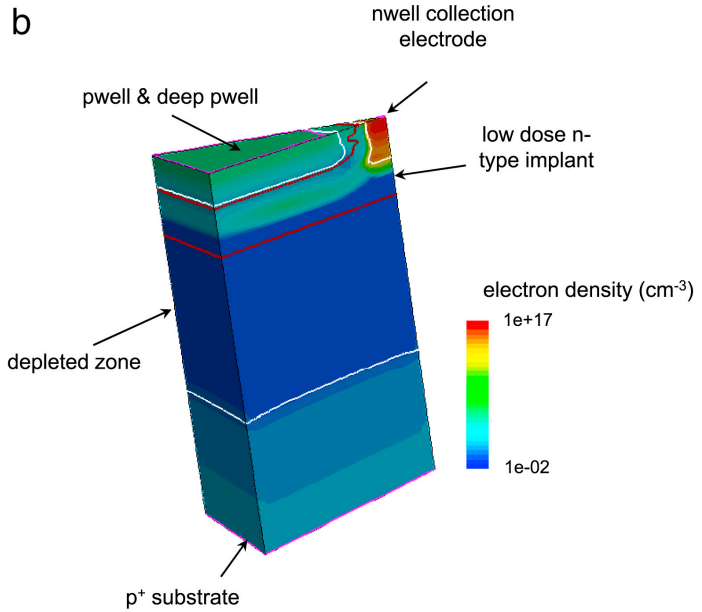
W. Snoeys

# Sensor optimization (1): DEPLETED MAPS



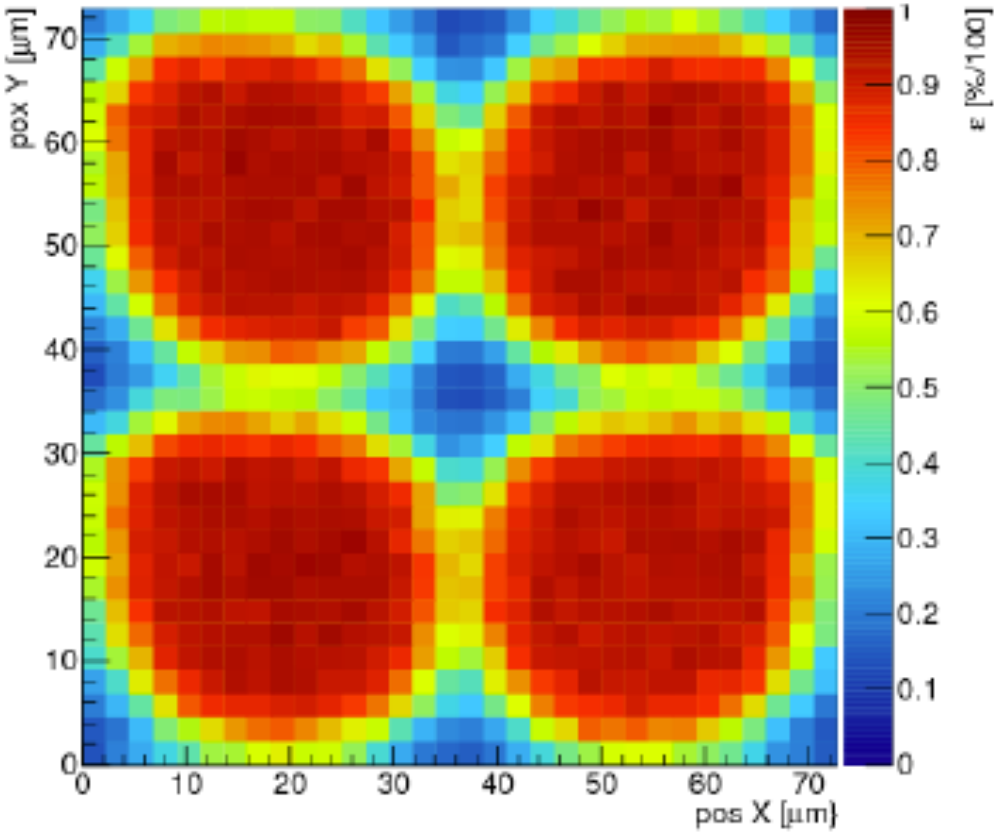

https://doi.org/10.1016/j.nima.2017.07.046 (180nm)

- GOAL: create planar junction using deep **low dose n-type implant** and deplete the epitaxial layer
- initial interest from ATLAS followed by many others: MALTA/TJ MONOPIX development (Bonn, CPPM, IRFU and CERN)




Tower Semiconductor 180nm

# Sensor optimization (1): results

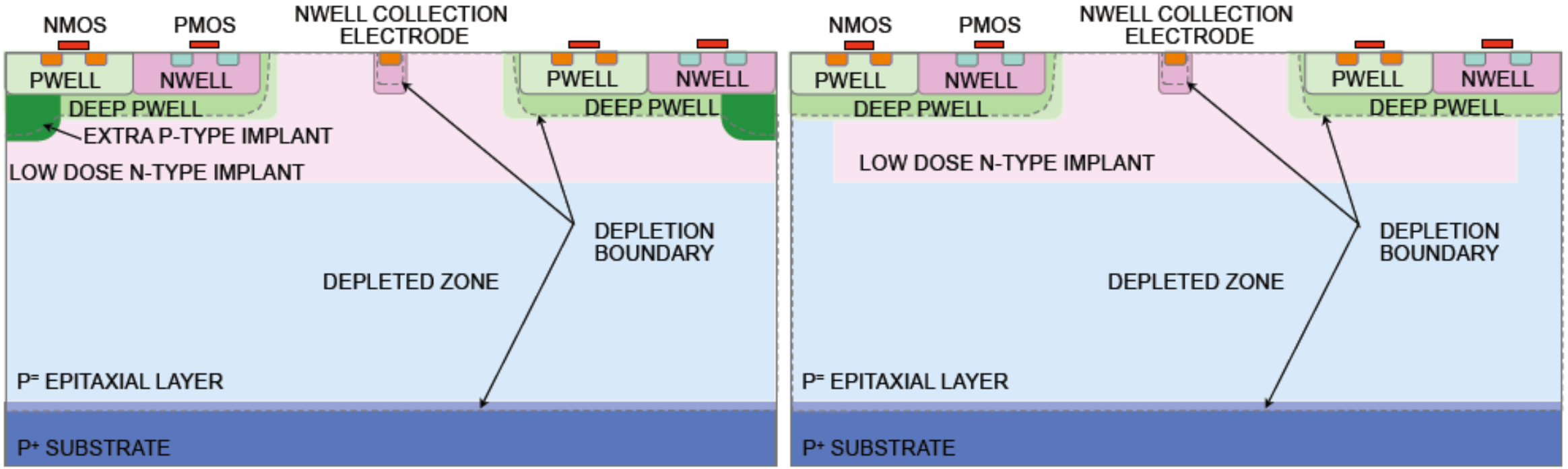



However:

- efficiency loss at ~ $10^{15}$ 1 MeV $n_{eq}/cm^2$ on the pixel edges and corners due to a too weak lateral field
- Lateral electric field not sufficient to push the deposited charge towards the small central electrode.
- Efficiency decreases in pixel corners
- Effect amplified by radiation damage

https://doi.org/10.1016/j.nima.2019.162404

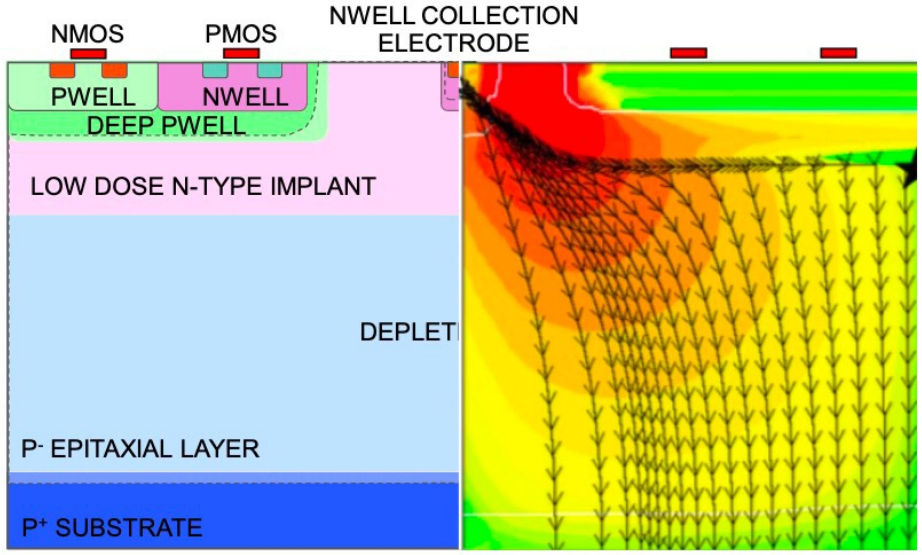
# Sensor optimization (2): improvement of the lateral field




3D TCAD simulation M. Munker et al. PIXEL2018 https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

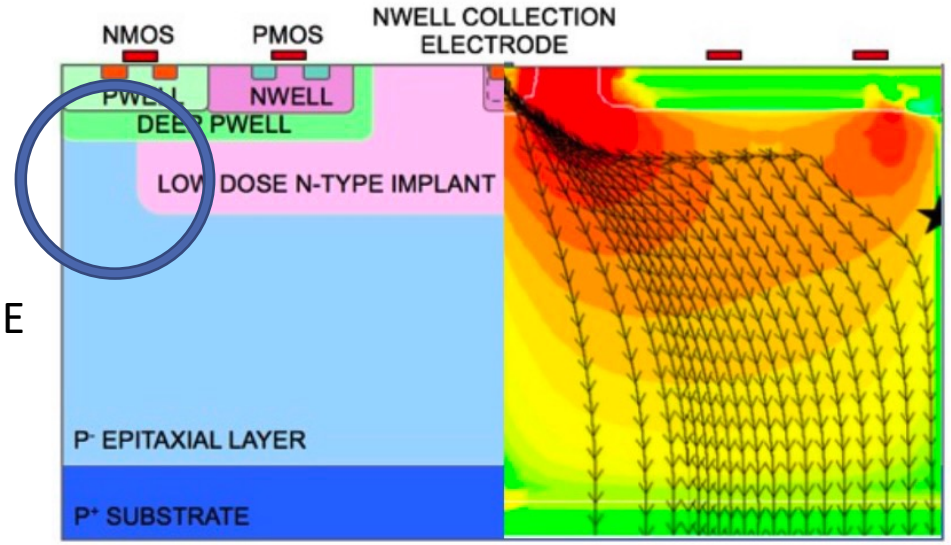
- Additional deep p-type implant or gap in the low dose n-type implant improves lateral field near the pixel boundary and accelerates the signal charge to the collection electrode.

# Sensor optimization (2): improvement of the lateral field



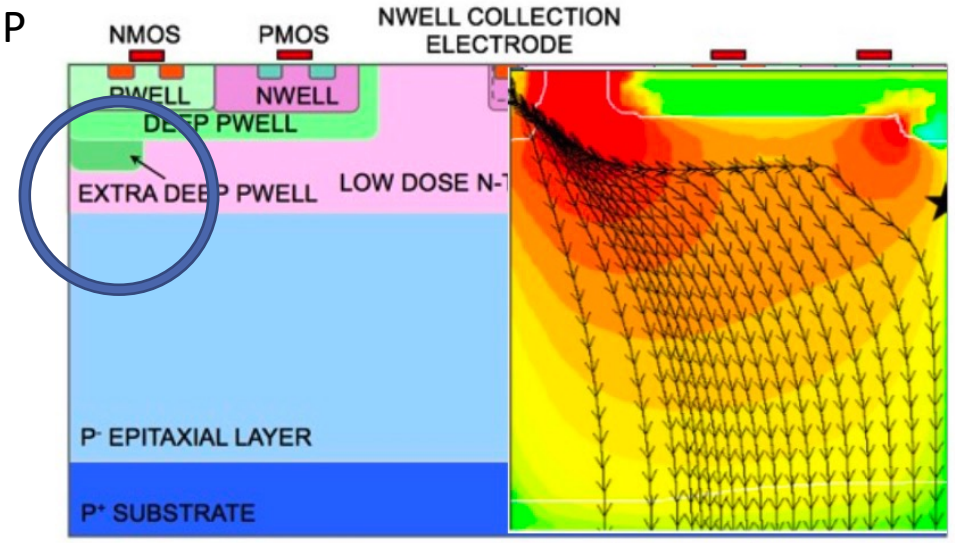

**Standard modified process**

GAP IN THE N LAYER




**Gap in the n- layer (NGAP)**

EXTRA DEEP P-WELL



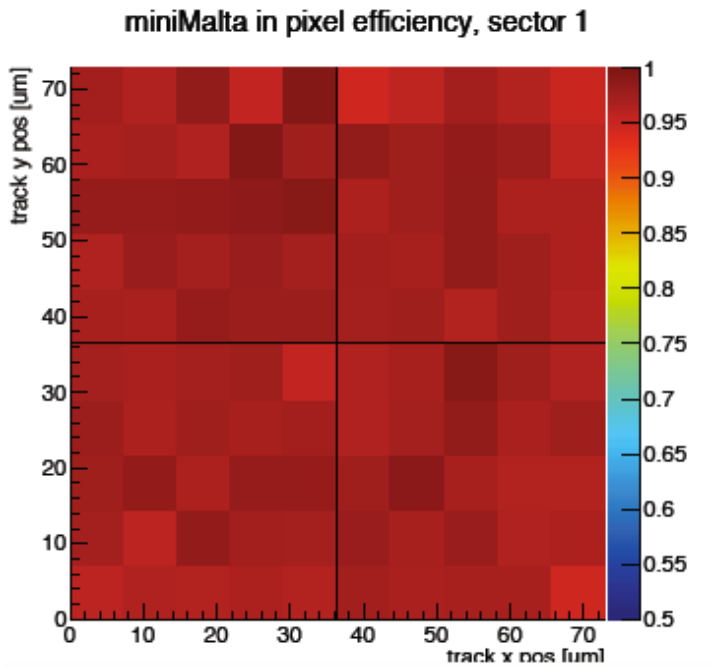

**Extra deep p-well (EDPW)**

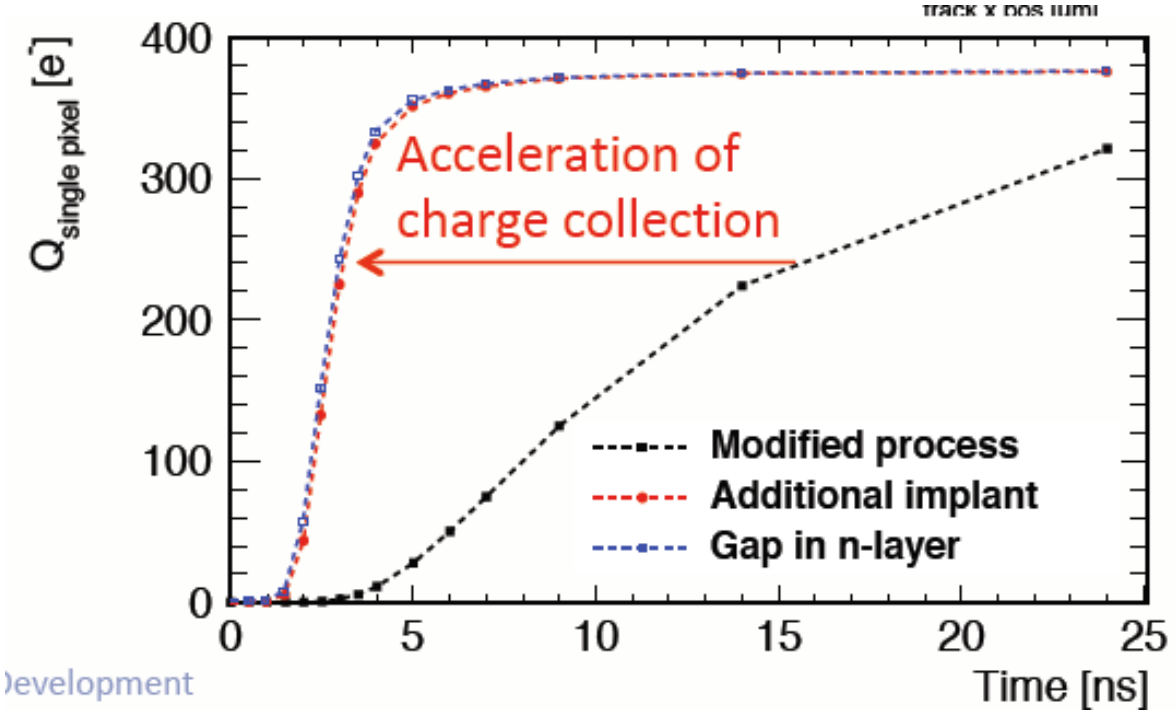
Process modifications to improve charge collection in the pixel edges

3D TCAD simulation M. Munker et al. PIXEL2018 https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

Tower Semiconductor 180nm

# Sensor optimization (2): results




- Full detection efficiency at $10^{15}$ $n_{eq}/cm^2$
- better sensor timing

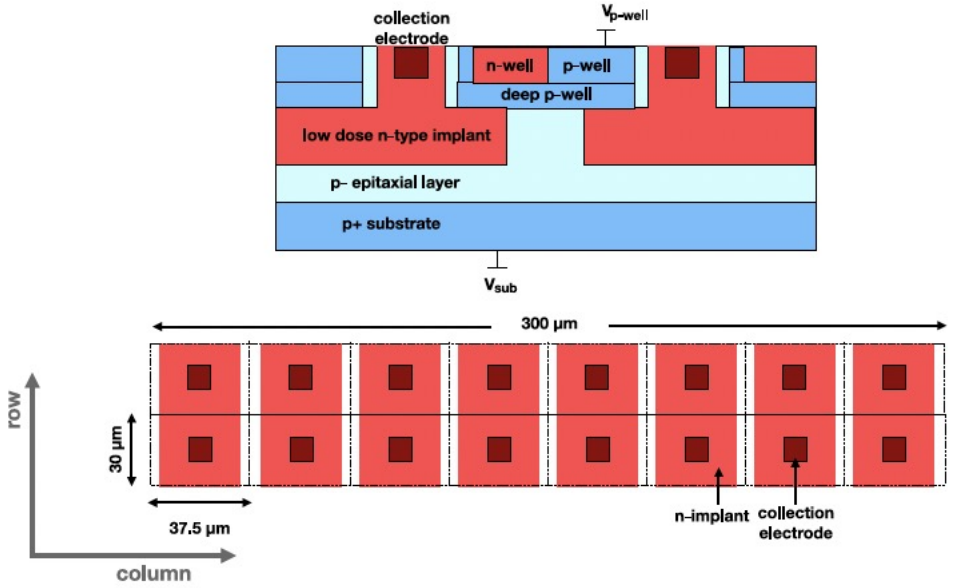
H. Pernegger et al., Hiroshima 2019,
M. Dyndal et al 2020 JINST 15 P0200

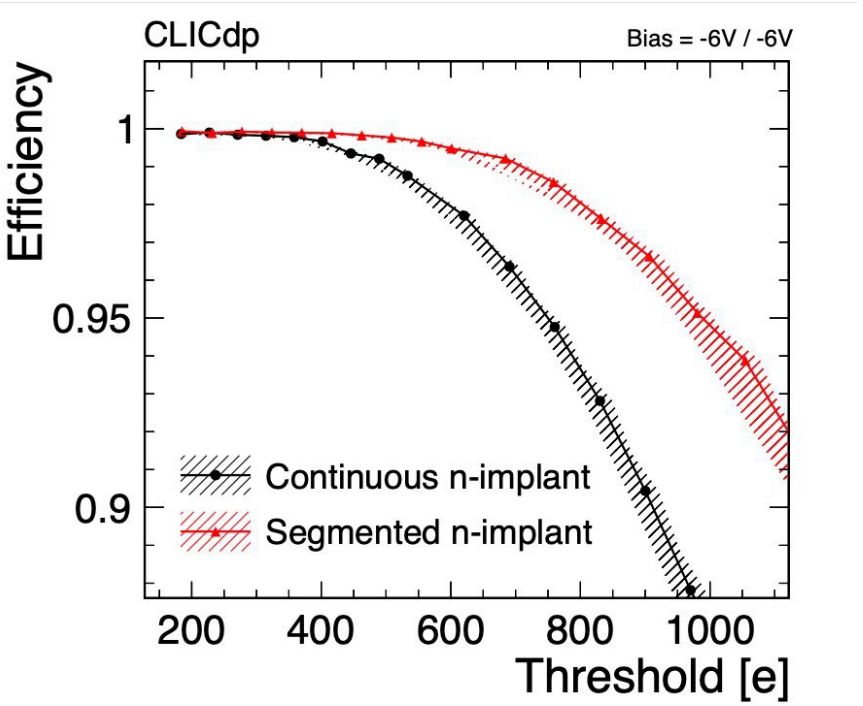
3D TCAD simulation M. Munker et al. PIXEL2018
https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

Tower Semiconductor 180nm

# Optimization example: CLICTD

- CLICTD 180 nm monolithic sensor: modified 180nm CMOS imaging process with small-collection electrode
- Target: CLIC tracker
  - **a matrix of 16 x 128 detection channels**
  - **size of 300 µm x 30 µm. In column channels are segmented into eight sub-pixels**
  - Simultaneous time and energy measurement per channel
- Exploring
  - large parameter space of sensor-design modifications: **segmentation in the low dose n-type implant** along the column
    - Reduced charge sharing leads to higher concentration of charge in one pixel cell -> Improved efficiency at high thresholds
  - substrate materials (epitaxial, high resistivity Cz)
  - thicknesses (40-300 µm)



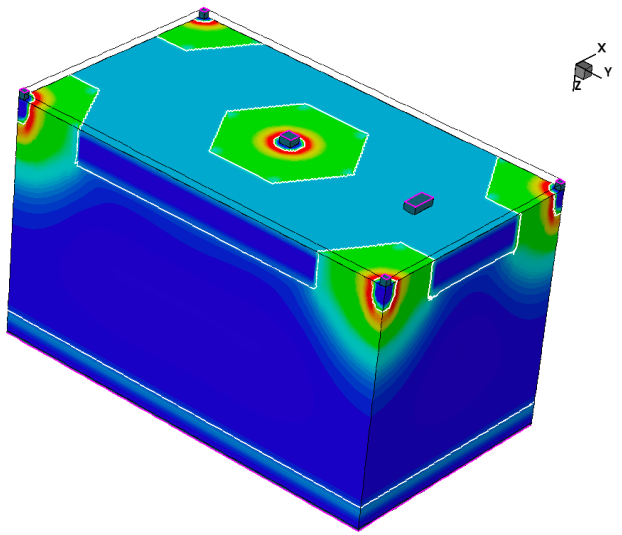

K. Dort et al: NIM, A 1006 (2021) 165396

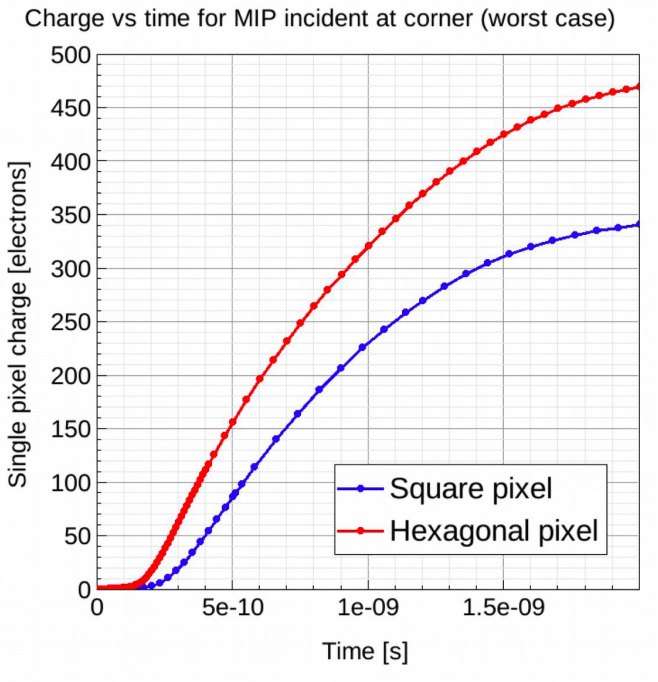
# FASTPIX

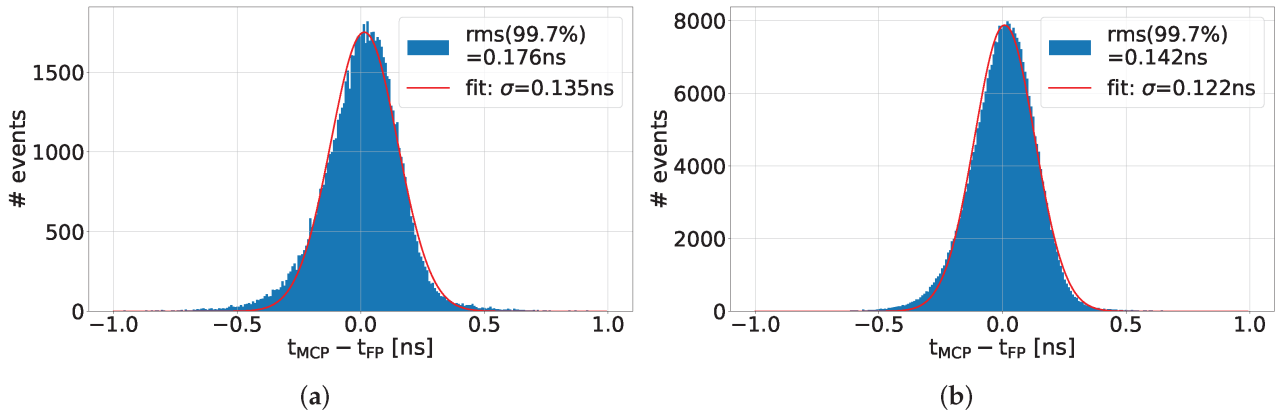
- Hexagonal design reduces the number of neighbors and charge sharing → **higher efficiency**
- Hexagonal design minimizes the edge regions while maintaining area for circuitry → **faster charge collection**
- Optimisations important not only for timing, but also for efficiency and radiation tolerance

Preliminary test-beam results showed MIP time resolution of approximately 120-130 ps

Simulated hexagonal unit cell – electrostatic potential:






Seed-pixel time residuals after timewalk correction for the inner region of the 10 μm (**a**) and 20 μm (**b**) pitch matrix.

More news on most recent results in Justus Braach's presentation later on this afternoon



J. Braach et al. Instruments 6 (2022) 13

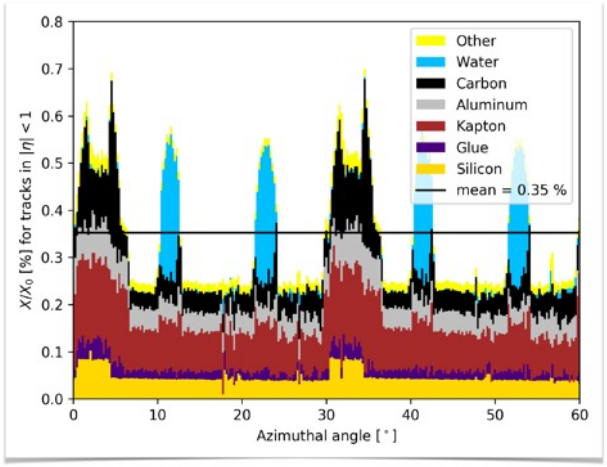


Tower Semiconductor 180nm

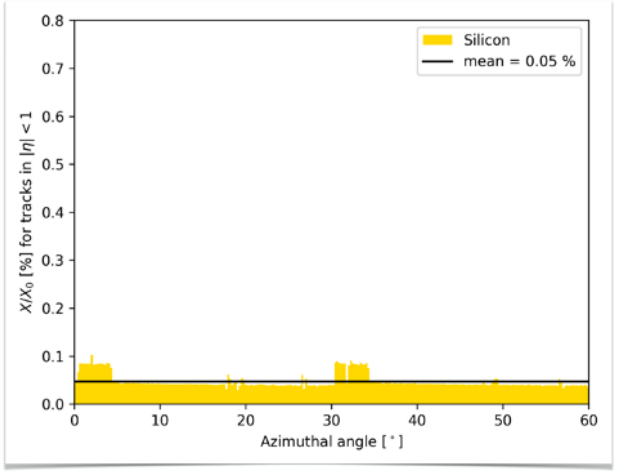
# Moving to 65 nm: ALICE ITS3 + EP R&D development

- GOAL for ALICE ITS3:
  - improve determination of primary and secondary vertices at high rate
  - go closer to interaction point
  - reduce material budget $X/X_0$ 0.35%→0.05%
- "SILICON ONLY" TRACKER?
  - exploit stitching → large area sensors
  - thin and bend → sigle sensor half layers
- TECHNOLOGY CHOICE:
  - 65 nm TPSCo (Tower & Partners Semiconductor): 300mm wafers and stitching available
  - 65 nm → lower power consumption
  - 7 metal layers

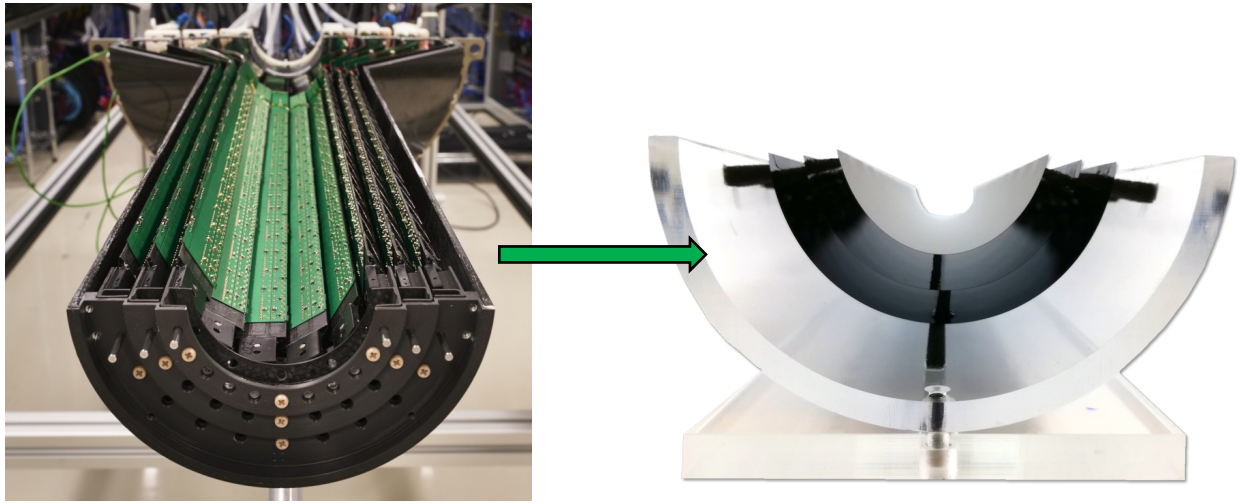
Interesting for EIC, NA60+, ...




ITS2 Inner Barrel

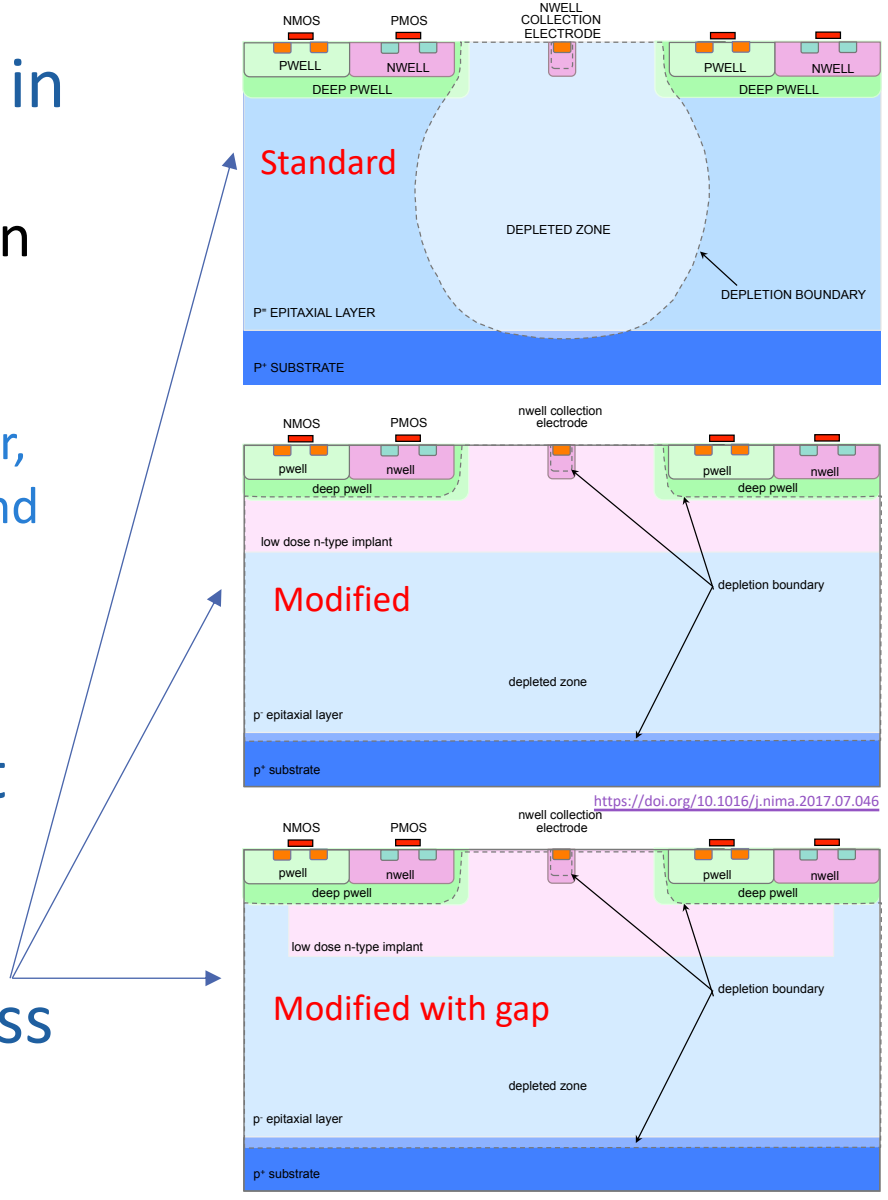



ITS3 mechanical mockup



# Optimization of the sensor: same approach as 180nm

- Process optimization: more needed/beneficial in 65 nm due to a **thinner epitaxial layer**
  - Add and adjust the low-dose deep n-well implant in the pixel to obtain easier depletion
  - Adjust the deep p-well implant
    - improve the isolation between the circuit and the sensor,
    - prevent punch through between deep n-type implant and circuitry
    - prevent local potential wells retaining the signal charge.
- 4 process splits: moving gradually from default to optimized process
- 3 main pixel designs implemented in all process splits



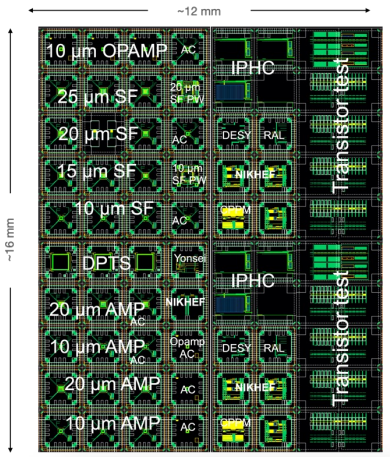

https://doi.org/10.1016/j.nima.2017.07.046

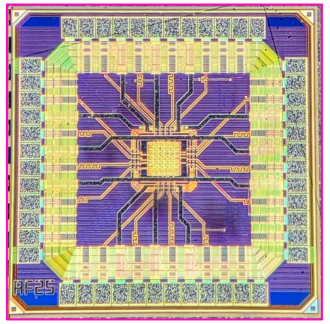
https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013


https://doi.org/10.22323/1.420.0083

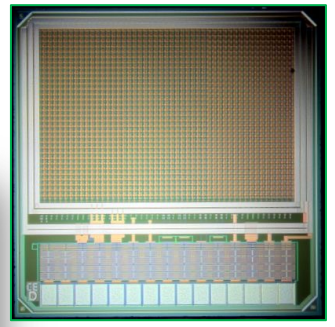
# First test submission: MLR1

- Submitted in December 2020
- Main goals:
  - Learn technology features
  - Characterize charge collection
  - Validate radiation tolerance
- Each reticle (12×16 mm$^2$):
  - 10 transistor test structures (3×1.5 mm$^2$)
  - 60 chips (1.5×1.5 mm$^2$)
    - Analogue blocks
    - Digital blocks
    - **Pixel prototype chips: APTS, CE65, DPTS**
- Testing since September 2021:
  - huge effort shared among many institutes
  - laboratory tests with $^{55}$Fe source
  - beam tests @ PS, SPS, Desy, MAMI

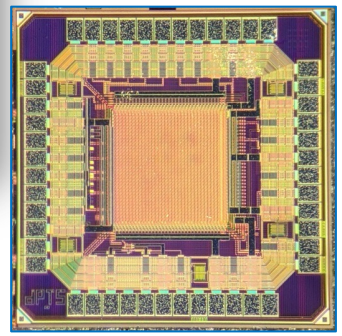


APTS:
- 6×6 pixel matrix
- Direct analogue readout of central 4×4 submatrix
- Two types of output drivers:
  1. Traditional source follower (APTS-SF)
  2. Very fast OpAmp (APTS-OA)
- 4 pitches: 10, 15, 20, 25 µm



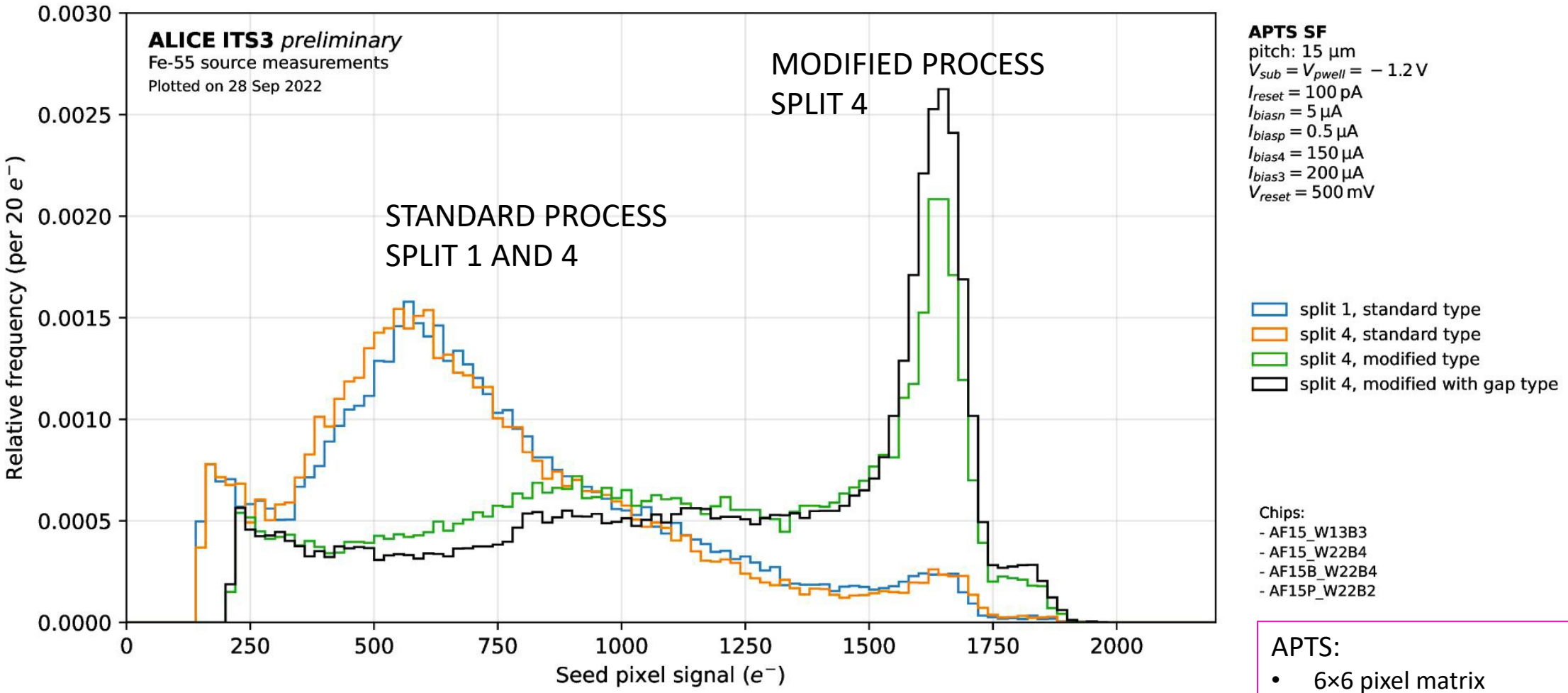
CE65:
- 2 matrix sizes, 15 or 25 µm pitch
- Rolling shutter readout (50 µs integration time)
- 3 in-pixel architectures:
  1. AC-coupled amplifier
  2. DC-coupled amplifier
  3. Source follower



DPTS:
- 32×32 pixel matrix
- Asynchronous digital readout
- Time-over-Threshold information
- Pitch: 15×15 µm$^2$

AREA: 1.5×1.5 mm$^2$

# Chosen results for APTS: charge collection



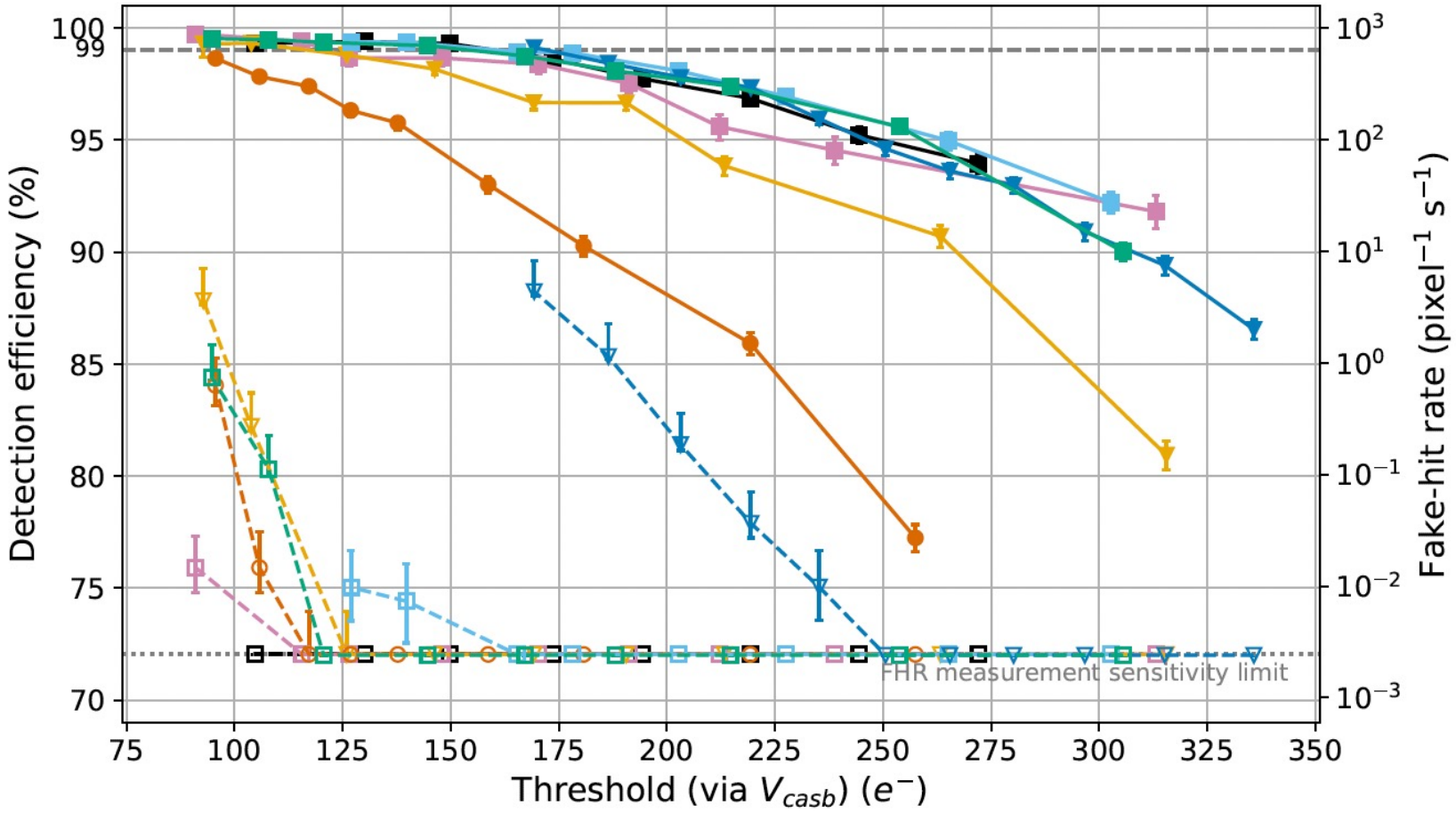

**APTS SF**
pitch: 15 µm
$V_{sub} = V_{pwell} = -1.2\,V$
$I_{reset} = 100\,pA$
$I_{biasn} = 5\,\mu A$
$I_{biasp} = 0.5\,\mu A$
$I_{bias4} = 150\,\mu A$
$I_{bias3} = 200\,\mu A$
$V_{reset} = 500\,mV$

split 1, standard type
split 4, standard type
split 4, modified type
split 4, modified with gap type

Chips:
- AF15_W13B3
- AF15_W22B4
- AF15B_W22B4
- AF15P_W22B2

APTS:
- 6×6 pixel matrix
- Direct analogue readout of central 4×4 submatrix
- Two types of output drivers:
  1. Traditional source follower (APTS-SF)

# Chosen results for DPTS: radiation hardness




**Detectors operated at 20°C**

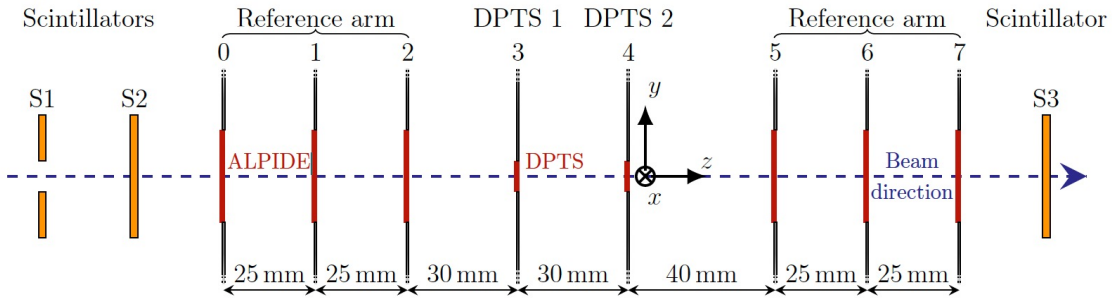
- Detection efficiency
- Fake-hit rate
- Non-irradiated
- $10^{13}$ 1MeV $n_{eq}$ cm$^{-2}$
- $10^{14}$ 1MeV $n_{eq}$ cm$^{-2}$
- $10^{15}$ 1MeV $n_{eq}$ cm$^{-2}$
- 10 kGy
- 100 kGy
- 10 kGy + $10^{13}$ 1MeV $n_{eq}$ cm$^{-2}$

DPTS:
- 32×32 pixel matrix
- Asynchronous digital readout
- Time-over-Threshold information
- Pitch: 15×15 µm$^2$

Detection efficiency and FHR for different irradiation levels

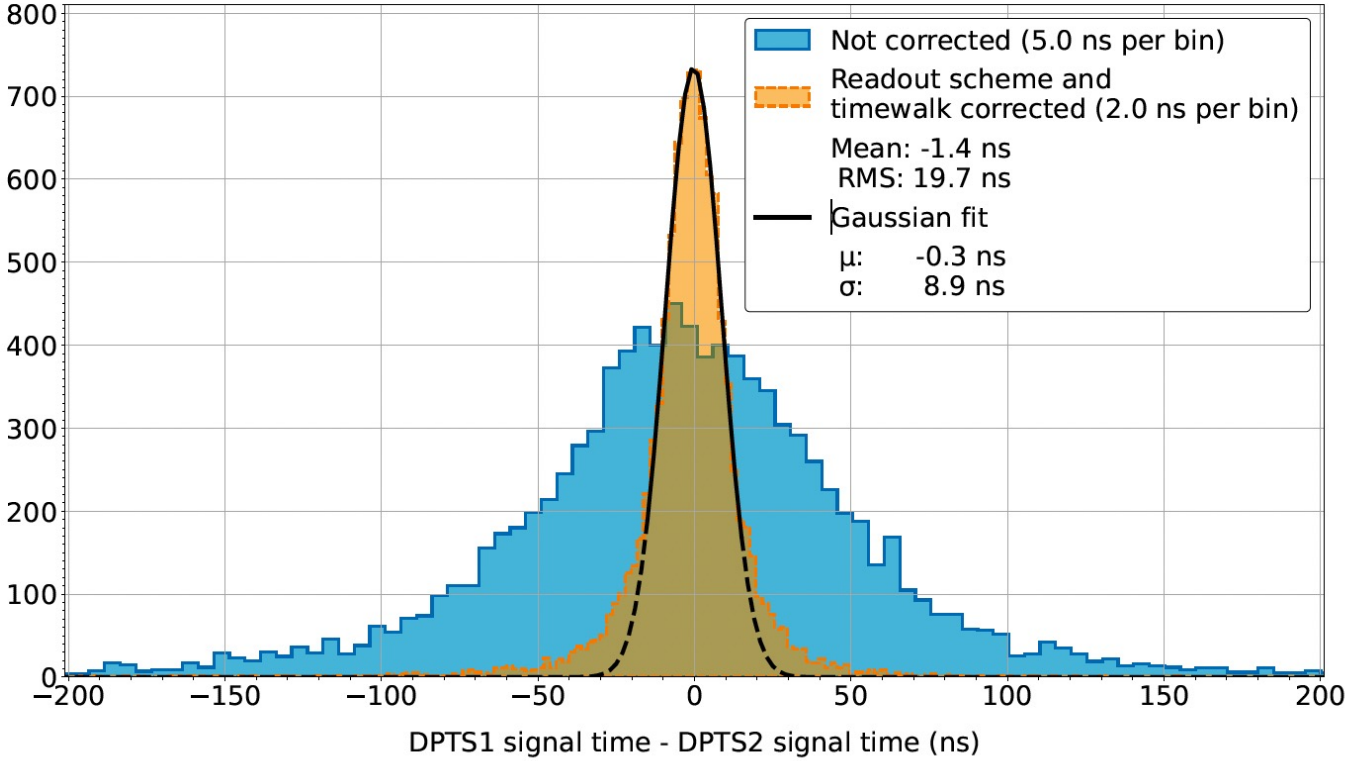

Gianluca Aglieri Rinella et al. arXiv:2212.08621v2

# DPTS Timing resolution




Sketch of the beam test telescope

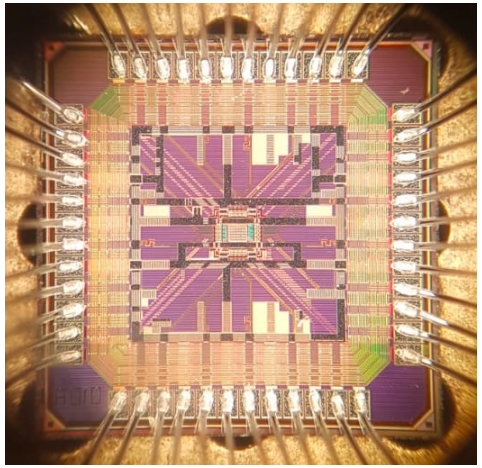
- Two DPTS are sandwiched between reference planes made of ALPIDE chips.
- Two scintillators (S2 and S3), operated in coincidence, and one featuring a 1mm hole (S1), operated in anti-coincidence, are used for triggering.
- The trigger can also be provided by one of the two DPTS
- Beam: 5.4 GeV/c electrons




- Time residuals distributions of two DPTSs with no corrections (blue) and with readout scheme and time walk corrections applied (orange)
- FE parameters not optimised for timing performance($I_{bias}$=10nA) : more results coming soon


Gianluca Aglieri Rinella et al. arXiv:2212.08621v2

# APTS OpAmp



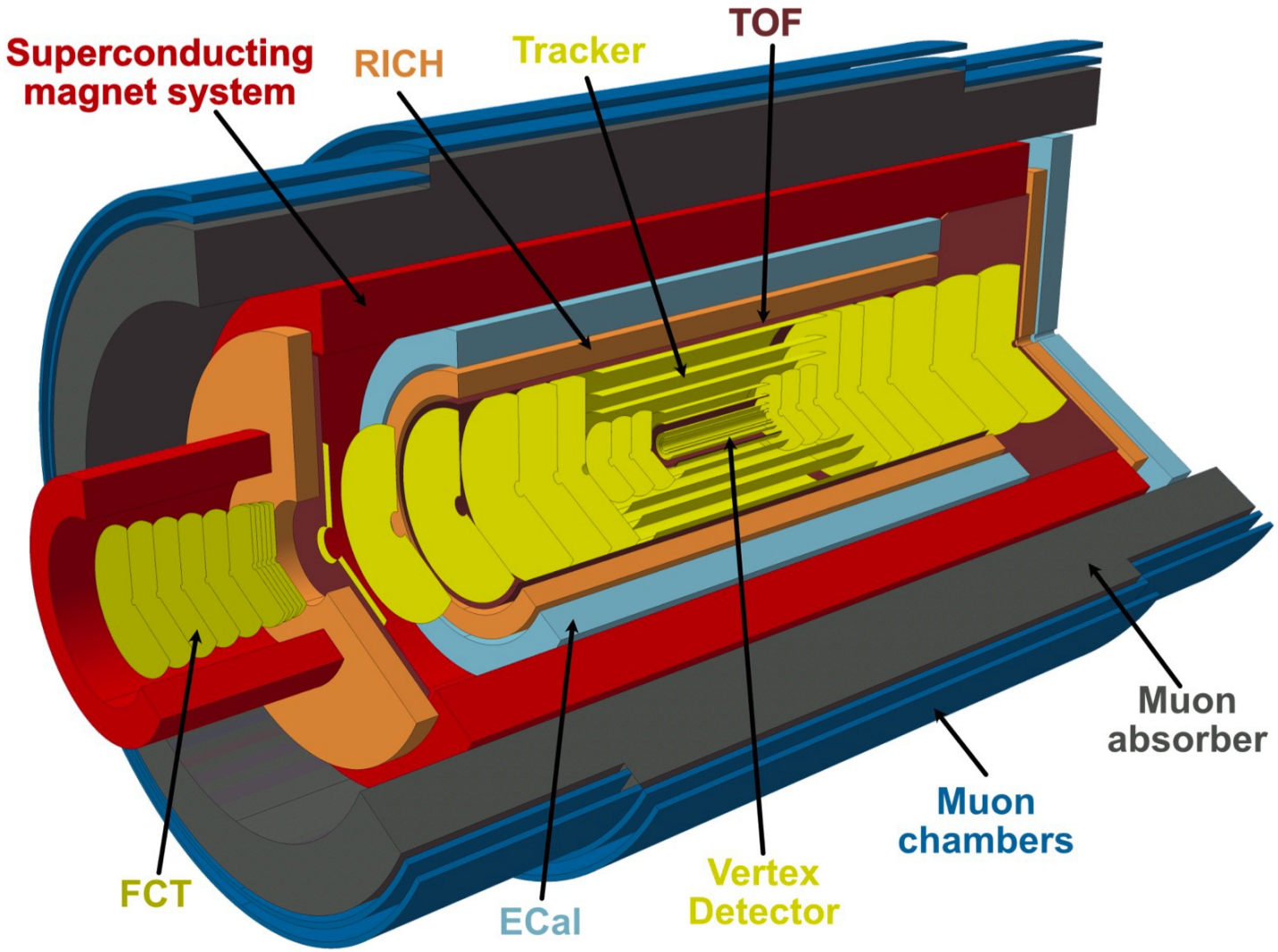
- Analog output test structure with OpAmp to start test the timing performance of the technology

- First results from June 2022 beam test available:
  - timing performance
  - efficiency

More news in Bong-Hwi Lim’s presentation, next one

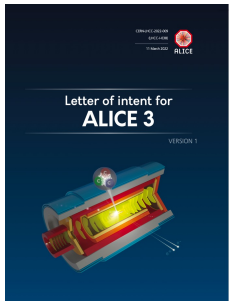
# Large future silicon based experimental set-ups

LHC timeline after RUN 4:


## ALICE3

Ambition to design a new experiment to continue with a rich heavy-ion programme at the HL-LHC" mentioned in the Update of the European strategy for particle physics



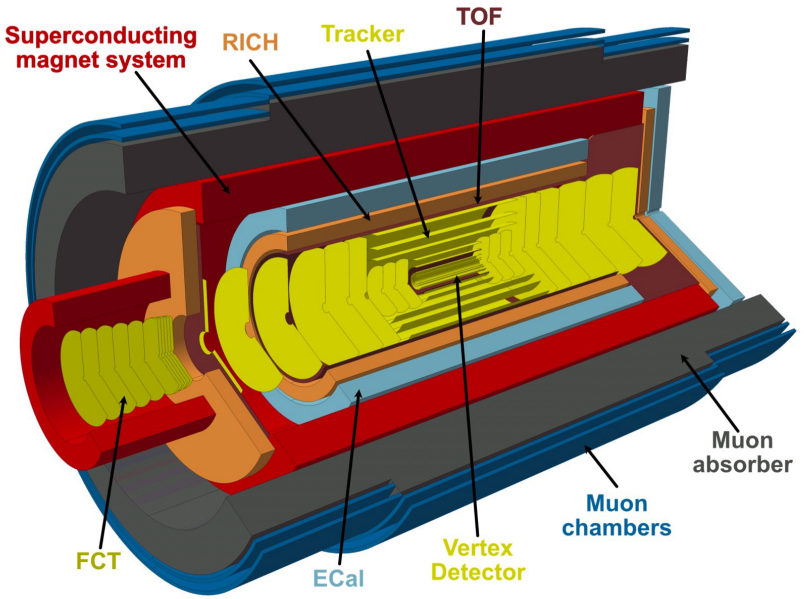

arXiv:2211.02491

LoI positively reviewed by LHCC last year

# ALICE3 Time of Flight

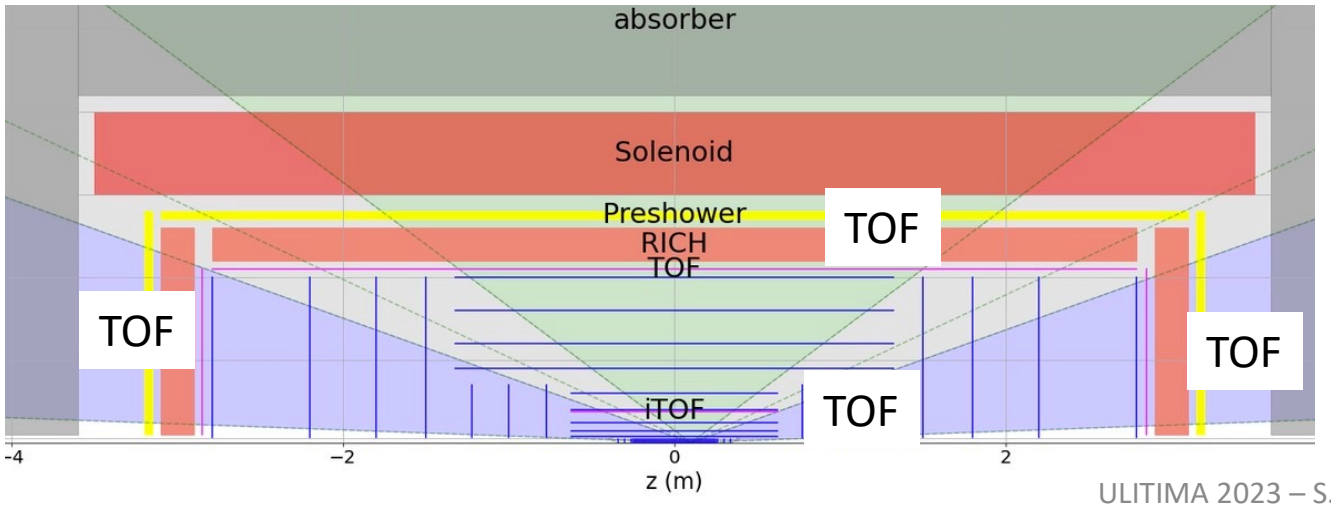
**Innovative detector concept**

- Compact and lightweight all-silicon tracker
- Retractable vertex detector
- Extensive particle identification
- Large acceptance
- Superconducting magnet system
- Continuous read-out and online processing




TOF

- outer TOF at R ≈ 85 cm
- inner TOF at R ≈ 19 cm
- forward TOF at z ≈ 405 cm




Separation power ∝ $L/\sigma_{TOF}$

- distance and time resolution crucial
- larger radius results in lower $p_T$ bound

2 barrel + 1 forward TOF layers 45 m$^2$ in total

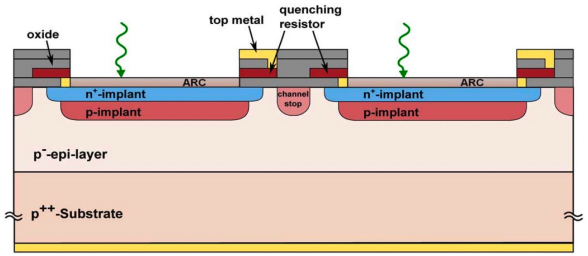
**Silicon timing sensors ($\sigma_{TOF}$ ≈ 20 ps)**

Material budget: 1-3% X/X0

Power consumption: <50mW/cm$^2$

# Choice of technology for TOF

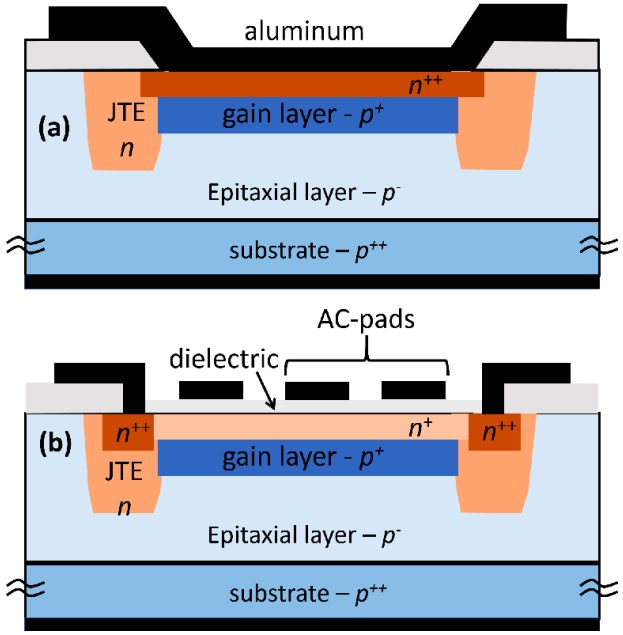
## SIPM




- Timing resolution of ~ 20 ps only for photons detection so far
- Feasibility to be demonstrated with charged particles

see Alberto Gola's talk

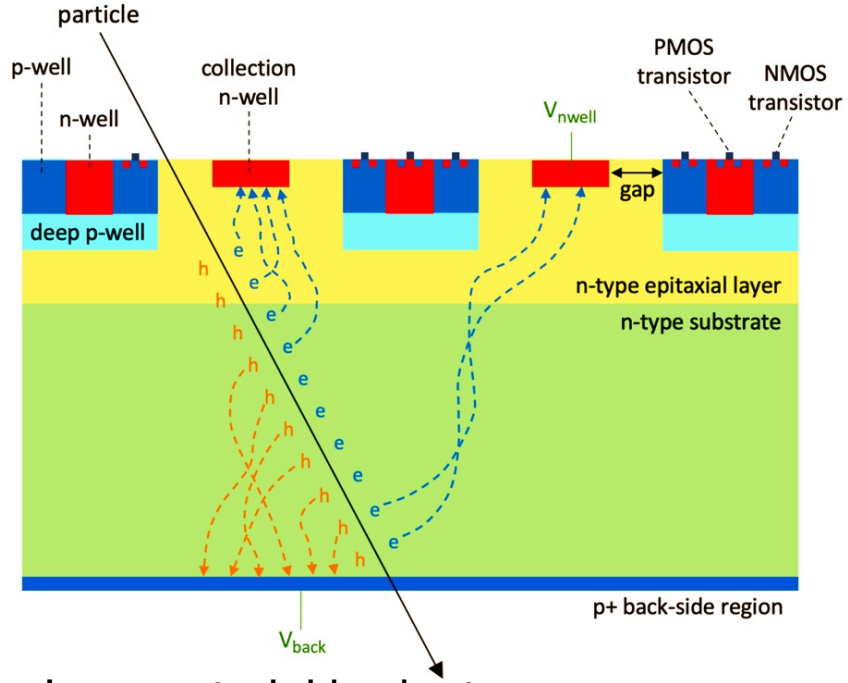
## L-GAD




- Timing resolution of ~ 30 ps demonstrated with 50 µm up to (1-2)$10^{15}$ 1-MeV-$n_{eq}$/$cm^2$
- thinner LGADs produced by different manufacturers

see Nicolò Cartiglia's talk

## HV DEPLETED MAPS

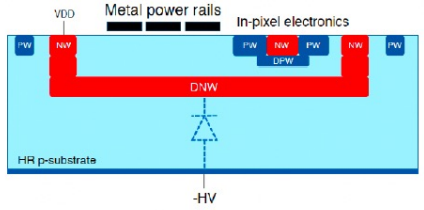



Low material budget
- High SNR
- Low power
- Investigation on innovative design to proof timing performance

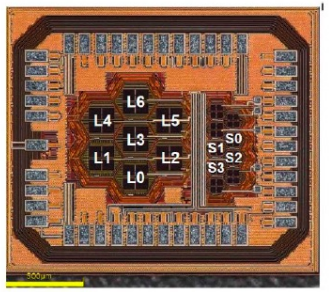
some examples in the next slides

# TIMING WITH MONOLITHIC SENSORS: OPPORTUNITIES AND CHALLENGES

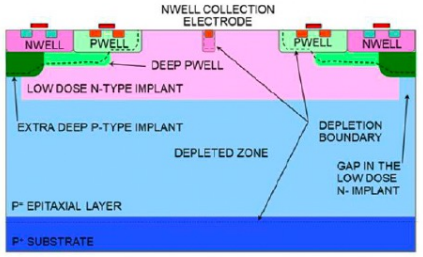
- Advantages:
  - Potentially 100% efficiency
  - Excellent radiation hardness demonstrated for several processes
  - Cost-effectiveness–on chip digitization, time-tagging and data pre-processing




Y. Degerli et al., 2020 JINST 15 P06011




G. Iacobucci et al., 2019 JINST 14 P11008




T. Kugathasan et al., Nucl. Inst. Meth. A Vol. 979, Nov. 2020

**Several monolithic projects targeting enhanced timing resolution**

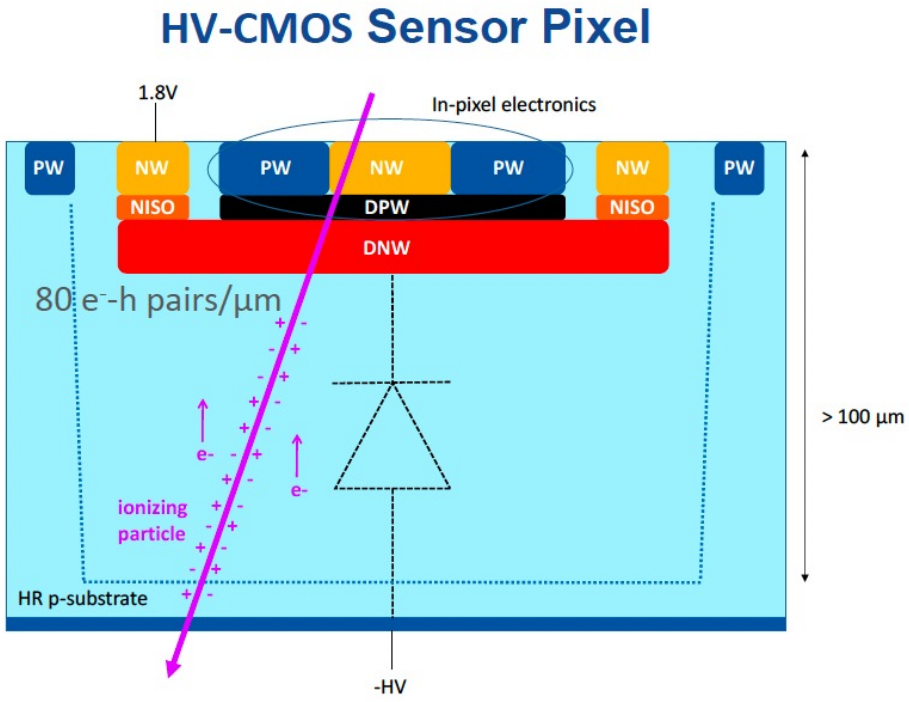
Lorenzo Paolozzi,
Tuesday afternoon

- Challenges
  - Fast collection (100s of ps) and low capacitance at the same time
  - Low power consumption
  - **20 ps resolution obtained experimentally recently by Monolith project** (https://arxiv.org/abs/2301.12244), not yet in reach for the other developments...

# TIMING WITH HV-CMOS/DMAPS

- Development of a monolithic timing sensor in a commercial HV-CMOS process (150-110 nm)

- LFoundry 150 nm HV-CMOS is one of the CMOS processes studied extensively for the CMOS option of the ATLAS Inner Tracker Upgrade
- Several large size demonstrators already designed and tested for tracking applications (LF-CPIX, LF-MONOPIX1, LF-MONOPIX2) in this process with proven radiation hardness (Bonn, IRFU and CPPM coll.)
- Wafers can be thinned and backside processed (for backside polarization and good charge collection uniformity)




DNW/HR p-substrate charge collection diode

- HV (≥ 300 V) applied on the substrate (from top or back)
- Large depletion depth (≥ 300 µm)
- **Charge collection by drift (fast)**
- **No internal amplification**
- **Electronics can be integrated inside charge collection diode**

# HVCMOS/DMAPS 150nm: CACTUS* and MiniCactus

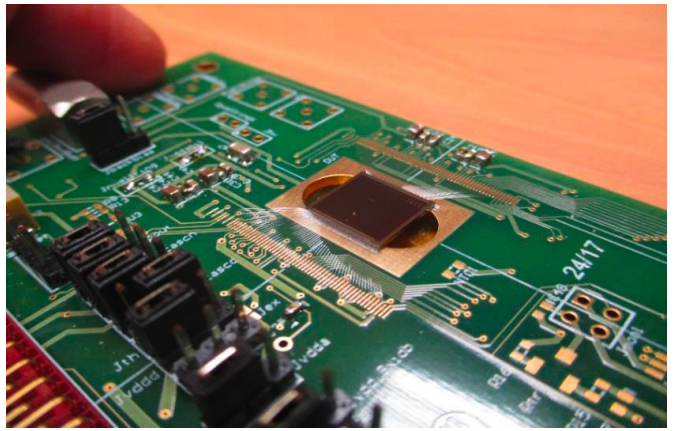
CACTUS demonstrator for timing in LFoundry 150 nm process designed in 2019

- Expected timing resolution from Cadence & TCAD simulations: **50-100 ps**

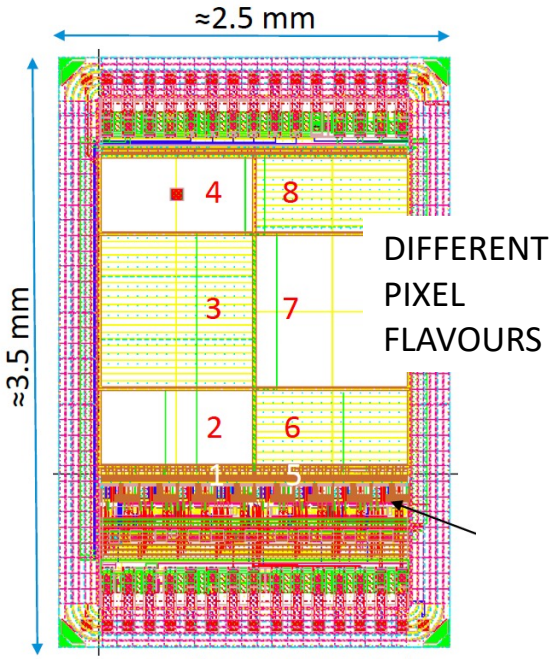
- Promising results obtained with the CACTUS detector:
  - high breakdown voltage, homogenous charge collection, deep depletion depth
  - good yield
- but:
  - very low S/N observed
  - Very long & large power rails needed to distribute power into pixels increased significantly detector capacitance in CACTUS
  - Timing possible only with high thresholds (leading to very low efficiency)

**MiniCACTUS** is a smaller detector prototype designed in order to address the *low S/N issue* of CACTUS

- Main change in MiniCACTUS: FE integrated at column level, pixels mostly passive



The CACTUS demonstrator on PCB (chip size : 1 cm x 1 cm)




Layout of MiniCACTUS chip



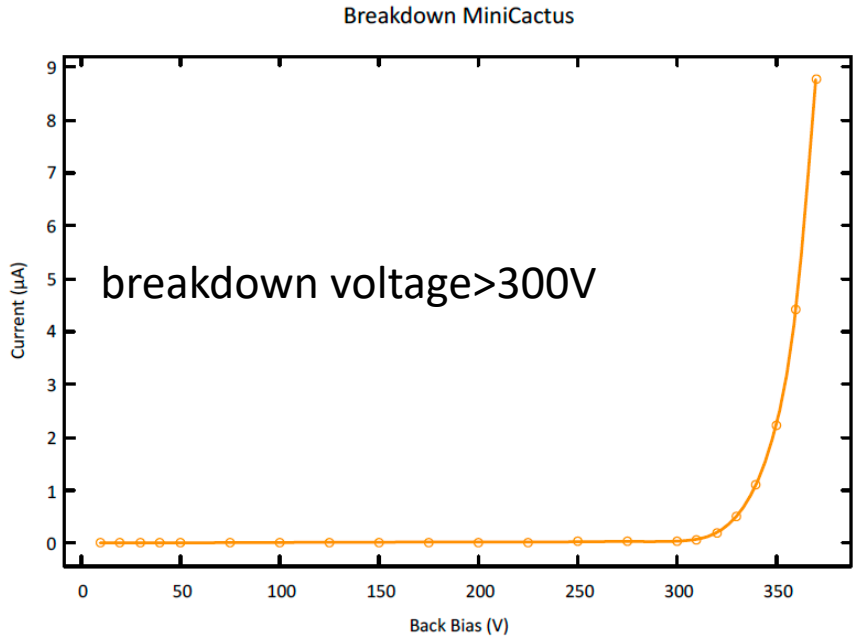
Y. Degerli et al. JINST 15, 2020



*CMOS ACtiveTiming µSensor

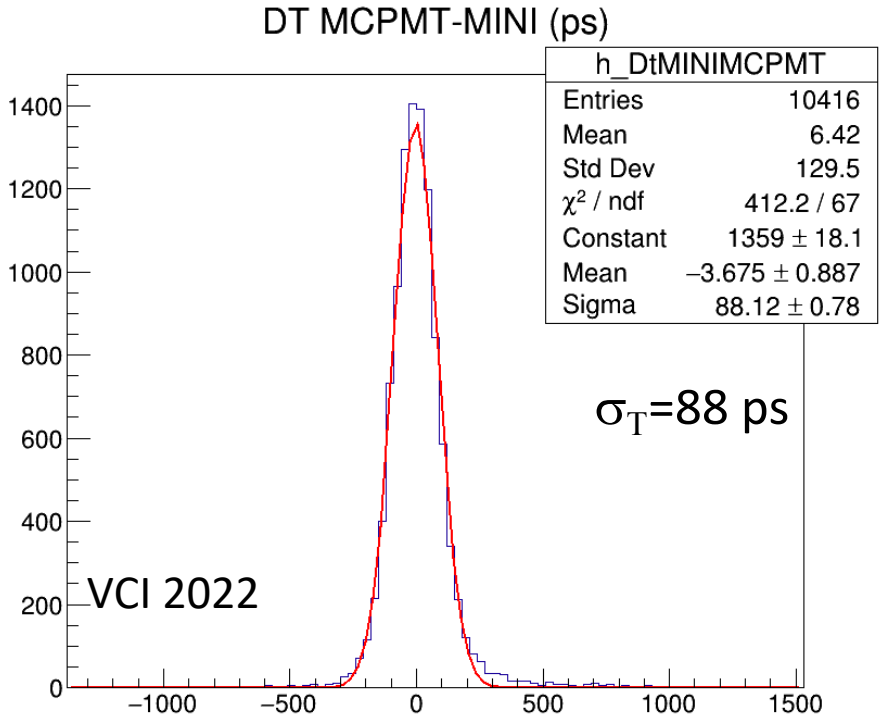
# Mini-CACTUS performance

- Laboratory characterization:
  - Sensors can be biased safely @ -300V (checked on several chips with different thicknesses: 100 µm, 200µm, unthinned)
  - Best S/N observed on 0.5mm$^2$ pixels
  - Noise$_{DigOut}$:
    - 179.4e$^-$(thickness: 200µm)
    - 155.9e$^-$(thickness: 100µm)




Y. Degerli et al. NIM A 1039 (2022) 167022

- Test beam on H4 line at SPS-CERN
- results: $\sigma_T$=88 ps
  - **pixel area 0.5 x 1 mm$^2$,**
  - **thickness 200 µm**
  - **reverse bias=-280V**
  - Worse timing resolution measured with 100 µm sensor (lower S/N and ringing from digital)
  - Small pixels have worse performance, probably due to charge sharing effects

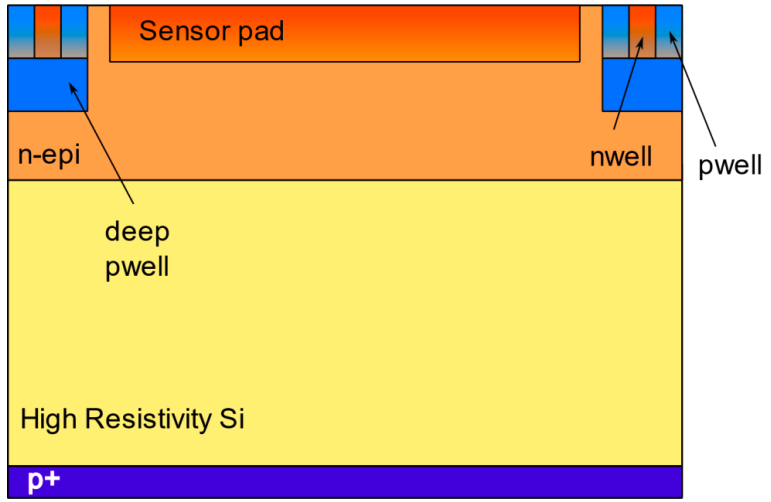


# DEPLETED MAPS 110nm: ARCADIA

110 nm Technology, 6 metal layers developed between INFN and LFoundry

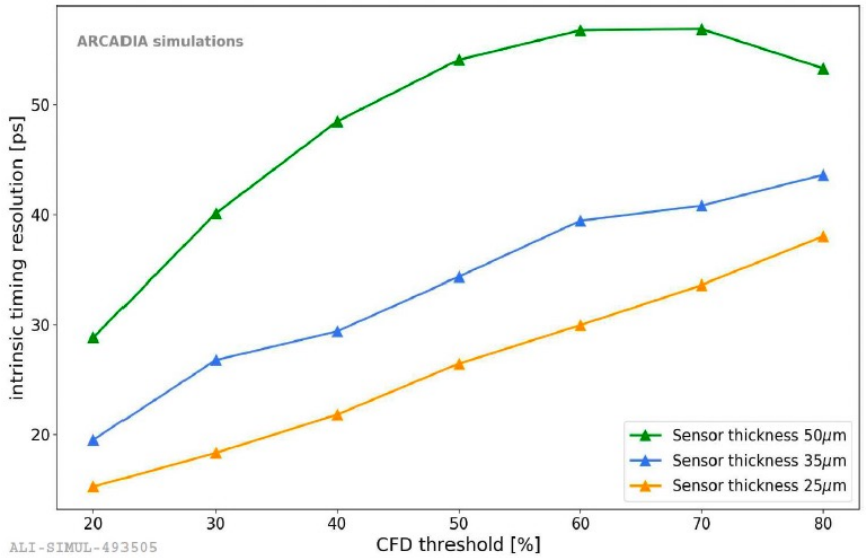
- 3D simulations necessary to quantify accurately the effect of weighting field non-uniformity at the borders
- Electric Field and Weighting Potential evaluated with TCAD simulations
- Intrinsic timing resolution with MIPs evaluated with AllPix2 on a 3x3 pixel domain

ARCADIA pad sensor




L. Pancheri 2022

**50 µm pitch,** Vnwell=3.3 V, Vback = Vpw @ 10 mW/cm$^2$
Epitaxial layer thickness 8 µm




Intrinsic timing resolution: $\sigma_{distortion}$ and $\sigma_{Landau\ noise}$

→ Resolution is **20÷30 ps** for the **50 µm pitch**

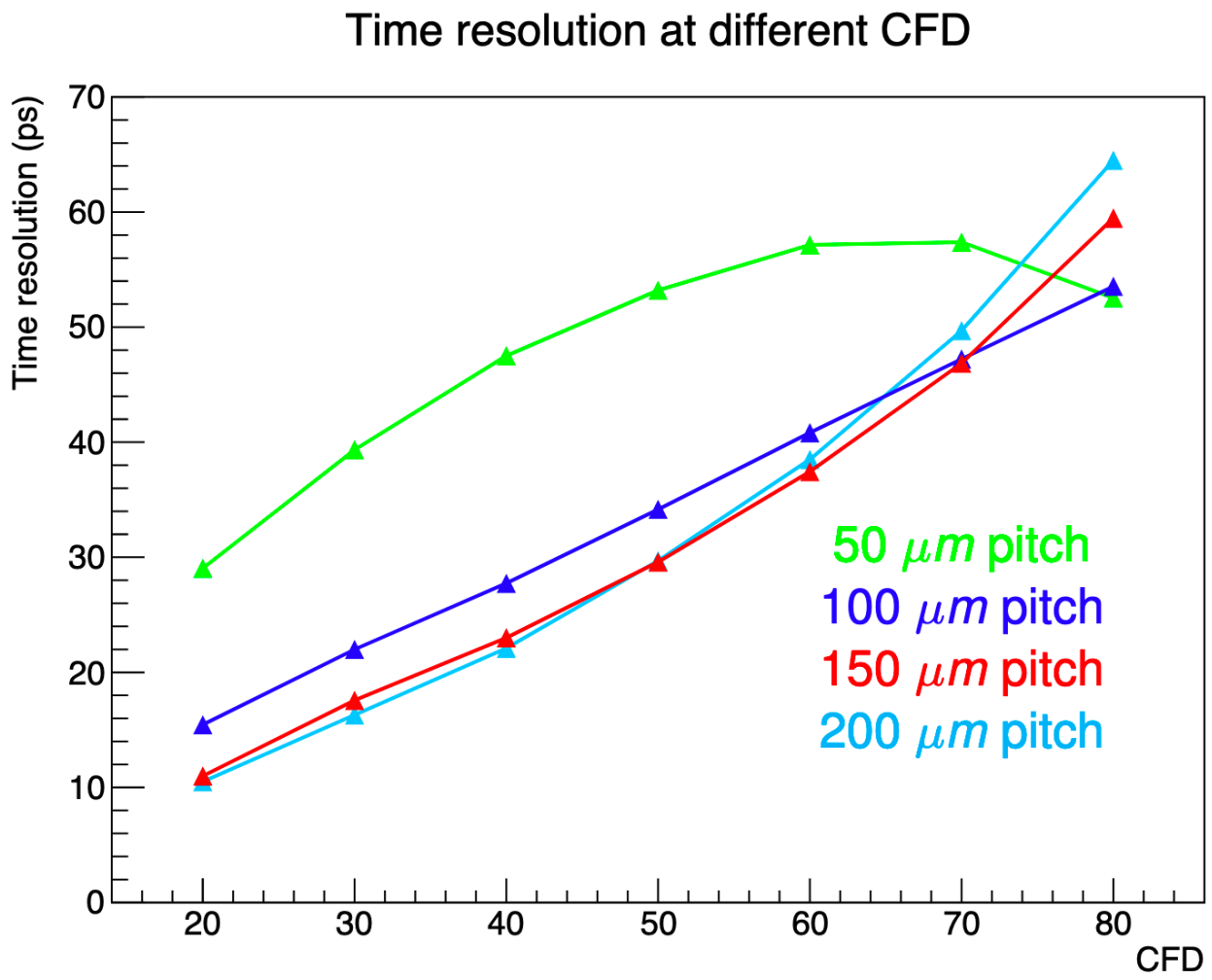
↳ **Larger PAD sizes** allow for a better field uniformity
And better area Efficiency!

→ **Thinner sensors** have a better time resolution
Still, less charge is generated
→ **Increase in the electronics jitter**



IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 67, NO. 6, JUNE 2020

# DEPLETED MAPS 110nm: ARCADIA




Thickness: 50μm

Increasing the pixel pitch for a better time resolution

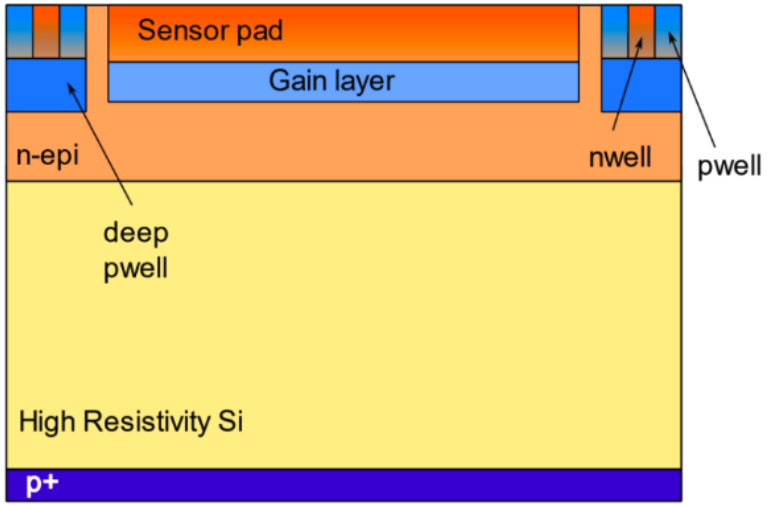
- 150 μm and 200 μm pixel pitches show very close time resolution values

- Add a gain layer to reach 20ps?

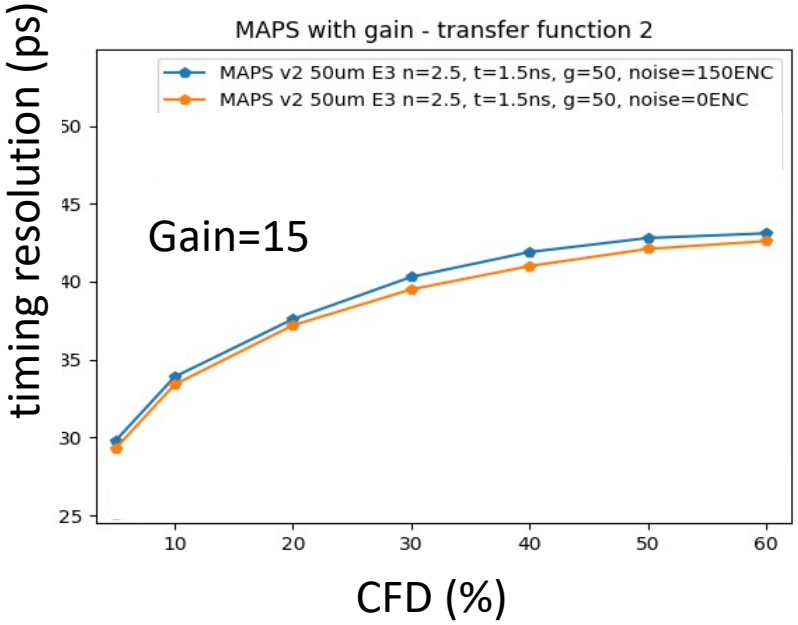
# DEPLETED MAPS with GAIN: larger signal for faster response

ARCADIA engineering run (LFoundry **CMOS 110nm)**

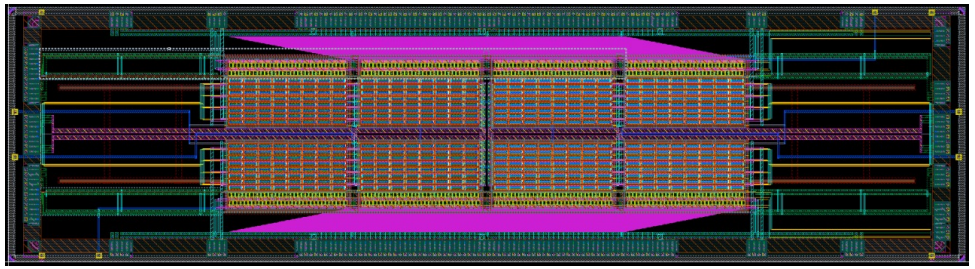
- Gain layer added: expected gain 10-20
- first prototype:
  - pixel size: 250 x 100 $\mu m^2$
  - diode area: 220 x 70 $\mu m^2$
  - sensor capacitance: 127fF
  - electronics size: 280 x 8 $\mu m^2$ on the pixel side
  - active thickness: 50 $\mu m$




noise included in the simulation




- Run submitted in July 2022
- **devices** shipped to INFN TO in **January 2023**



- test beam campaign in summer 2023
- **results available in Q4 2023**

# Conclusions

- Many encouraging results for different developments on MAPS with timing capabilities are now available
- MAPS represent a very attractive solution for very large area 4D tracking or Time of Flight detector systems

but....

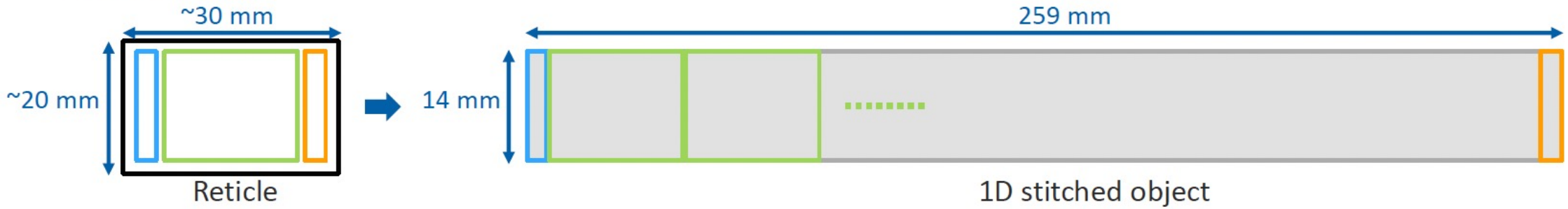
- a lot of work is still needed to reach the ultimate goal of :
  - 10 ps temporal resolution
  - 5 μm spatial resolution
  - low material budget
  - low power

A big thank to Walter Snoeys, Angelo Rivetti, Lucio Pancheri, Stefania Bufalino, Stefano Durando, the ALICE ITS3 team and all the colleagues who helped preparing these slides

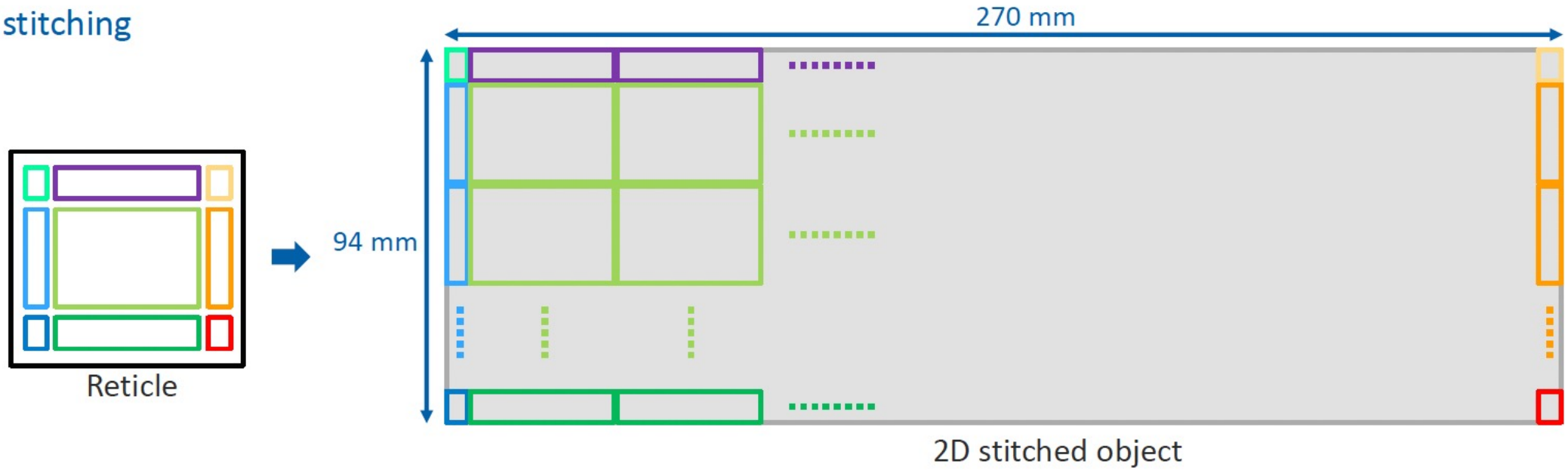
# Back up

# Wafer scale stitched sensors

- 1D stitching




- 2D stitching

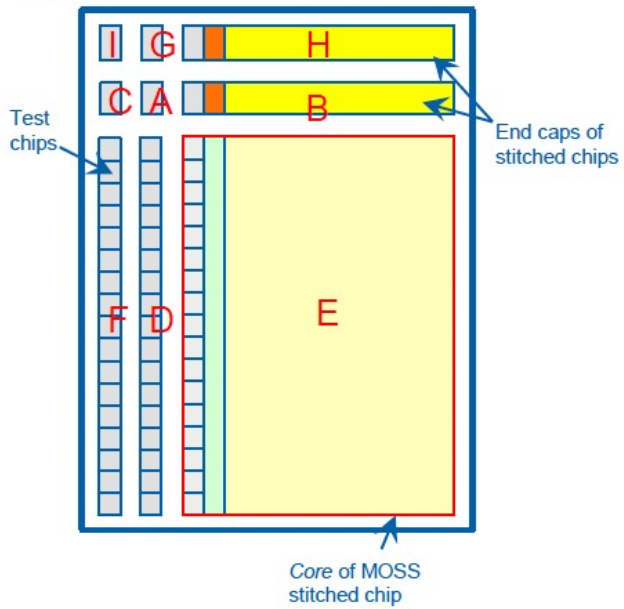


# Wafer scale stitched sensors prototype: MOSS

Technology

- TPSCo 65nm Image Sensor CMOS process
- 300 mm silicon wafer
- Stitching technique
- Full wafer-scale sensor design

**Design reticle**




**Sensor chips on wafer**