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Timespot1: a Fast-Timing, High-Rate Pixel-Matrix ASIC in CMOS 28-nm technology

Vertex detectors being conceived for the next generation of collider experiments will have to operate with an increased number of tracks per event. To cope with this problem, it will be mandatory to operate with pixel sensors and electronics having both high space and time resolutions (tens of μm and tens of ps respectively). Furthermore, high radiation resistance is necessary both for the sensors (around 5×10^{16} 1 MeV neutron equivalent per cm^2) and the electronics side (1-2 Grad). Dedicated development activities have already started in the last years to study possible technical solutions in this respect. The INFN-funded TimeSPOT project aims to produce a small-scale demonstrator, which includes both a pixel sensor with a size of $55 \times 55 \mu\text{m}^2$ and a pixel read-out chip satisfying the above mentioned requirements. This demonstrator includes an ASIC, named Timespot1, which is described in this paper. The chip is being bump-bonded to dedicated 3D silicon sensors, having already shown a time resolution better than 20 ps. Timespot1 is designed in CMOS 28 nm technology. It features a 32×32 -pixel matrix with a pitch of $55 \mu\text{m}$. The ASIC is conceived to be capable to read-out pixels with timing resolution below 50 ps on the full chain (sensor, amplifier, Time-to-Digital-Converter). Each pixel is endowed with a charge amplifier, a discriminator, and a Time-to-Digital Converter with time resolution around 30 ps and maximum read-out rates of 3 MHz per pixel. The timing performance are obtained keeping the power budget of per pixel lower than $40 \mu\text{W}$ per channel. The ASIC has been tested in the laboratory in order to characterize its performance in terms of time resolution, power budget and sustainable rates. The ASIC is being hybridized on a matched 32×32 pixel sensor matrix and will be soon tested under laser beam and Minimum Ionizing Particles in the laboratory and at test beams. In this paper we present a description of the ASIC design, its operation and the results obtained from characterization tests concerning its performance in tracking measurements. A typical time resolution of the order of 30 ps has been achieved. The die size is $2.3 \times 2.6 \text{ mm}^2$. The ASIC layout has been conceived to be easily scalable in area by design, in such a way to read-out larger pixel matrices with the same pitch. This suggest further developments of this first prototype, which are already under consideration by our collaboration. This item will also be addressed in this paper.

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