



A picosecond avalanche detector in SiGe BiCMOS

L. Paolozzi

on behalf of the MONOLITH team



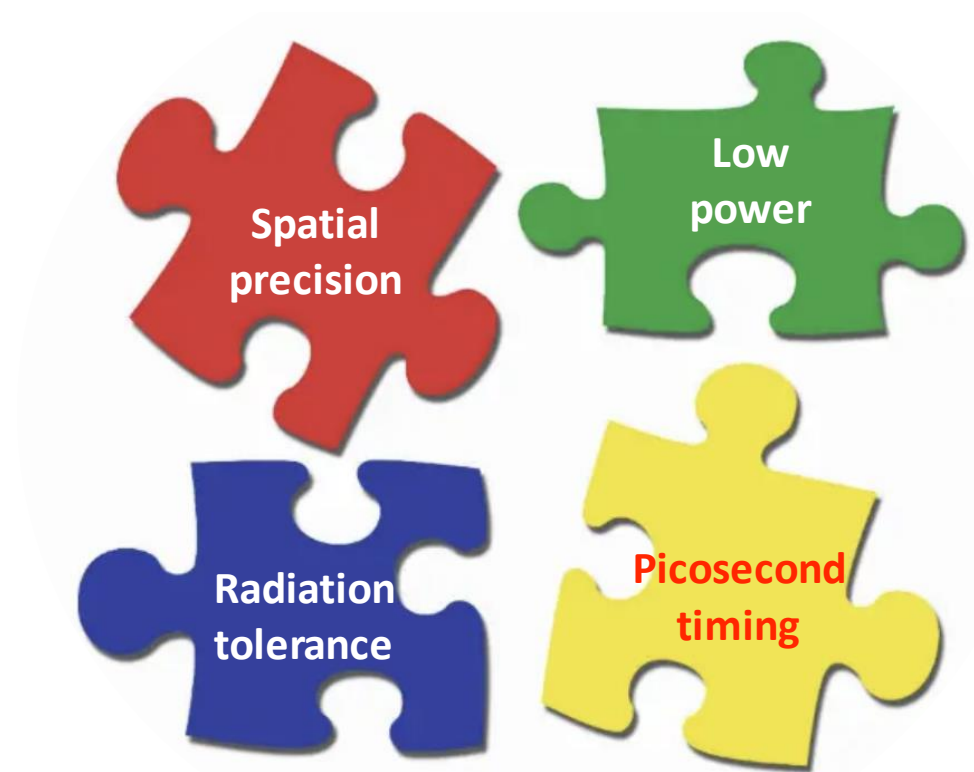
Precise timing with silicon

Timing resolution in silicon pixel detectors mainly determined by:

1. Sensor geometry and fields
2. Charge-collection (Landau) noise
3. Electronic noise
4. Gain by internal charge multiplication

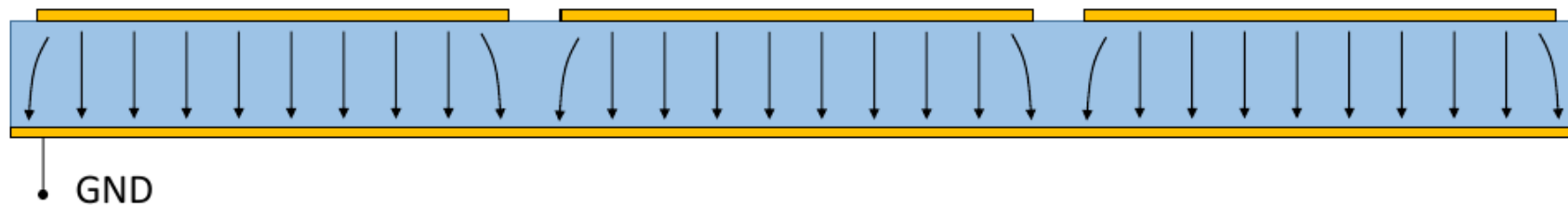
Challenge:

Optimise these parameters for **picosecond timing** while maintaining **other performance requirements**



1. Sensor geometry and fields

Sensor optimization for time measurement means:
Sensor time response **independent** from the particle trajectory



→ **"Parallel plate"** read out: wide pixels w.r.t. depletion region

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i} \cong \boxed{v_{drift}} \boxed{\frac{1}{D}} \sum_i q_i$$

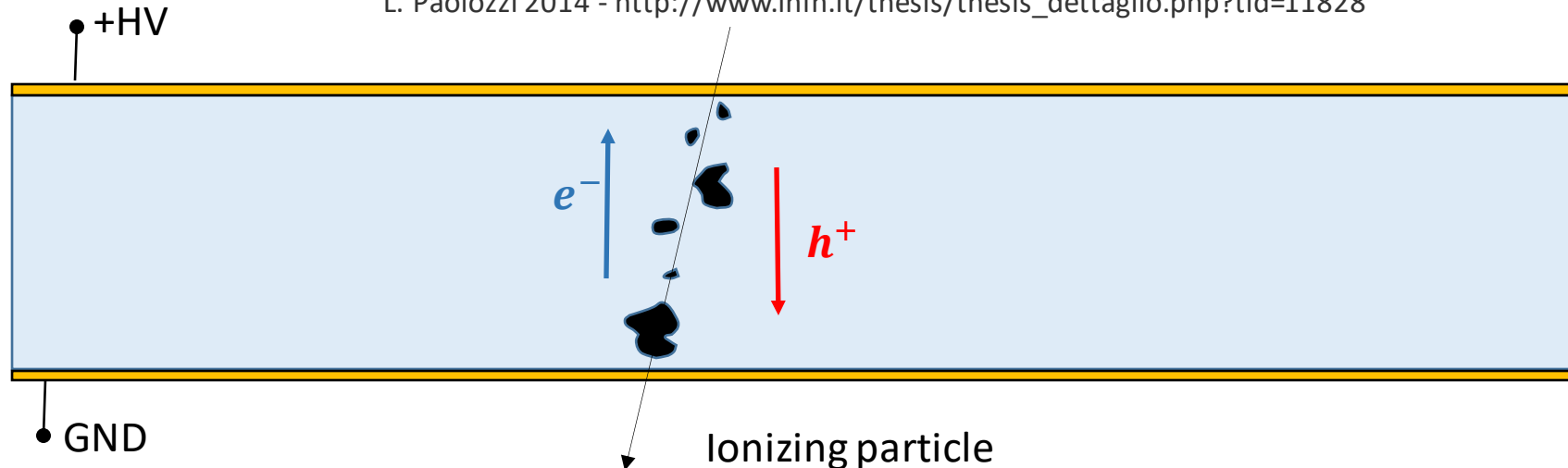
Scalar, saturated Scalar, uniform

Desired features:

- Uniform **weighting field** (signal induction)
- Uniform **electric field** (charge transport)
- Saturated charge **drift velocity** (signal speed)

2. Charge collection noise

L. Paolozzi 2014 - http://www.infn.it/thesis/thesis_dettaglio.php?tid=11828



is produced by the **non uniformity of the charge deposition** in the sensor:

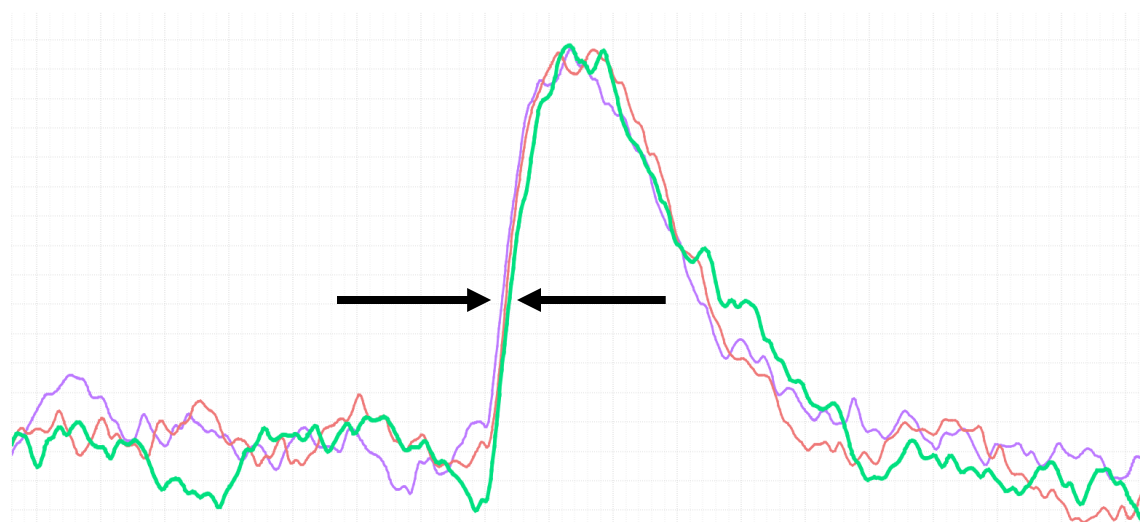
$$I_{ind} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

When **large clusters** are absorbed at the electrodes, their contribution is removed from the induced current. The **statistical origin** of this variability of I_{ind} makes this **effect irreducible in PN-junction sensors**.

3. Electronic noise

Once the geometry has been fixed, the time resolution depends mostly on the **amplifier performance**.

Time jitter

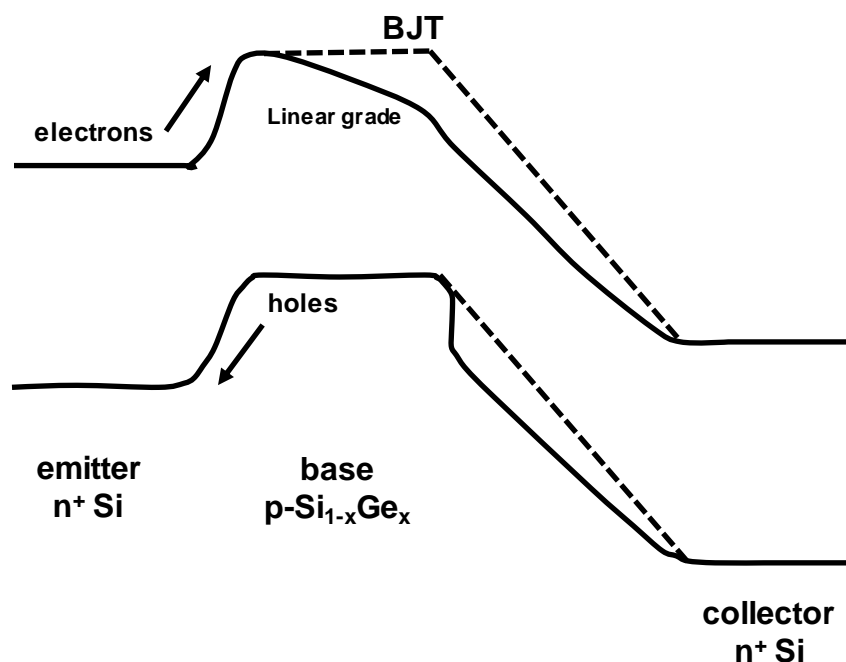


Fast integration

$$\sigma_t = \frac{\sigma_V}{dV/dt} \cong \frac{t_{rise}}{\text{Signal}/\text{Noise}} \cong \frac{ENC}{I_{Ind}}$$

3. Electronic noise

In SiGe Heterojunction Bipolar Transistors (HBT) the **grading** of the bandgap in the Base changes the **charge-transport mechanism** in the Base from **diffusion** to **drift**:



Grading of germanium in the base:

field-assisted charge transport in the Base,
equivalent to introducing an electric field in the Base

⇒ short e^- transit time in Base ⇒ very high β

⇒ smaller size ⇒ reduction of R_b and very high f_t

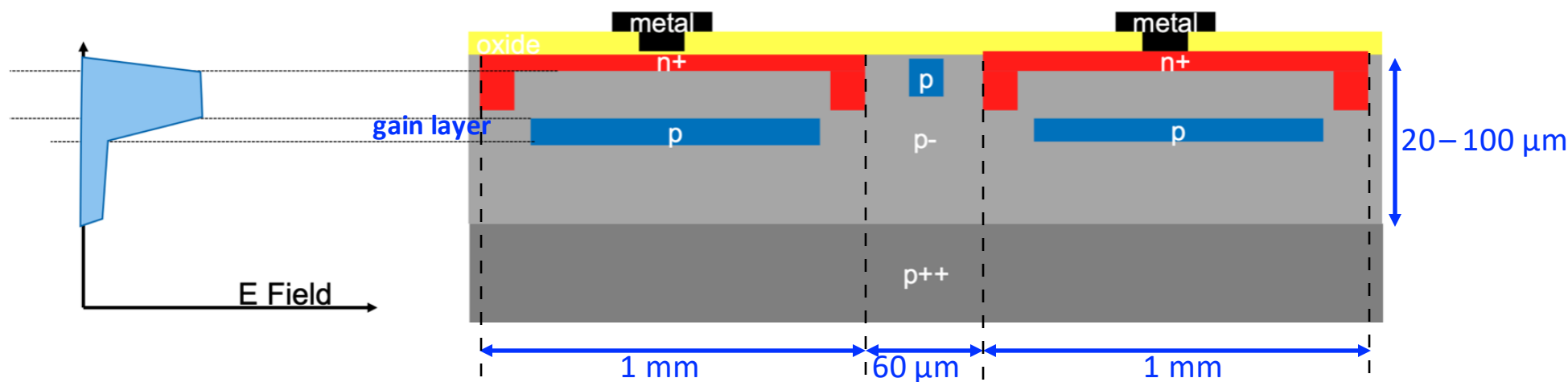
Hundreds of GHz

4. Gain

- A gain layer allows larger signals, and thus, better time resolution

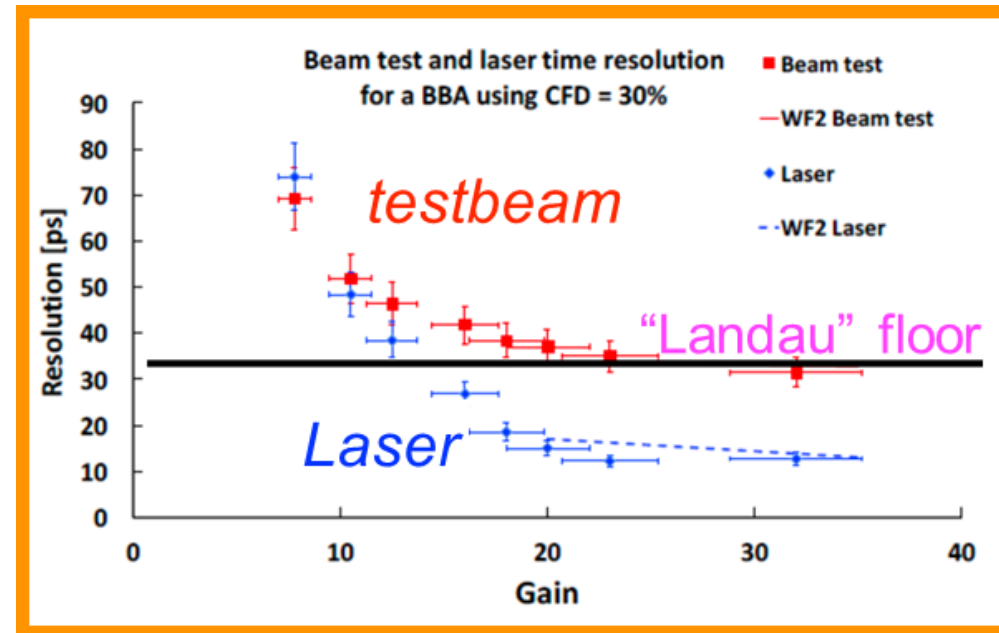
$$\sigma_T \cong \frac{t_{rise}}{\text{Signal/Noise}} \cong \frac{ENC}{I_{Ind}}$$

- This is achieved in the LGADs with a gain layer under the pixel;



- As you will see, we have a different strategy

4. Gain



H. Sadrozinski, A. Seiden and N. Cartiglia, 2018 Rep. Prog. Phys. **81** 026101

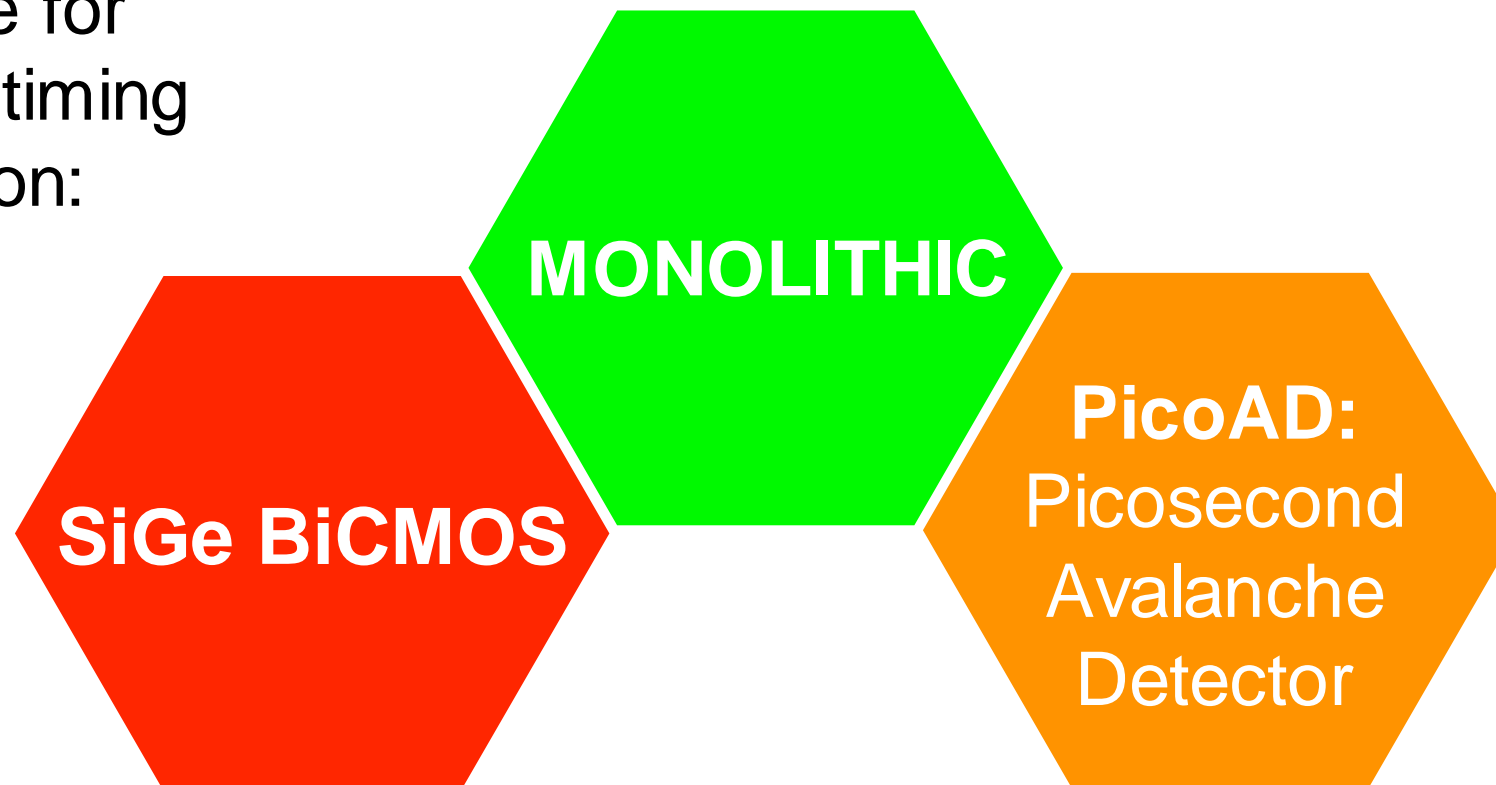
Charge collection noise represents an **intrinsic limit** to the time resolution for a semiconductor PN-junction detector.

~30 ps reached by present LGAD sensors.

Lower contribution from sensors without internal gain

The **MONOLITH** Project

Our recipe for
picosecond timing
with silicon:



The UniGe Silicon Team



Giuseppe Iacobucci

- project P.I.
- System design



Lorenzo Paolozzi

- Sensor design
- Analog electronics



Didier Ferrere

- System integration
- Laboratory test



Sergio Gonzalez-Sevilla

- System integration
- Laboratory test



Thanushan Kugathasan

- Lead chip design
- Digital electronics



Magdalena Munker

- Sensor design
- Laboratory test



Yannick Favre

- Board design
- RO system



Stéphane Débieux

- Board design
- RO system



Roberto Cardella

- Sensor design
- Laboratory test



Stefano Zambito

- Laboratory test
- Data analysis



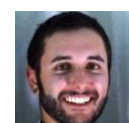
Mateus Vicente

- System integration
- Laboratory test



Fulvio Martinelli

- Chip design
- Firmware



Matteo Milanesio

- Laboratory test
- Data analysis



Théo Moretti

- Laboratory test
- Data analysis



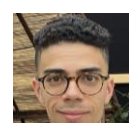
Antonio Picardi

- Chip design
- Firmware



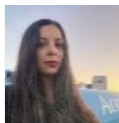
Chiara Magliocca

- Laboratory test
- Data analysis



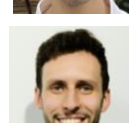
Jihad Saidi

- Laboratory test
- Data analysis



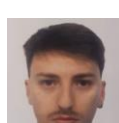
Raffaella Kotitsa

- Sensor simulation



Carlo Alberto Fenoglio

- Chip design
- Firmware



Luca Iodice

- Chip design
- Firmware

Main research partners:



Roberto Cardarelli
INFN Rome2 & UNIGE



Holger Rücker
IHP Mikroelektronik



Marzio Nessi
CERN & UNIGE



Matteo Elviretti
IHP Mikroelektronik

Funded by:



Swiss National
Science Foundation



European Research Council
Established by the European Commission



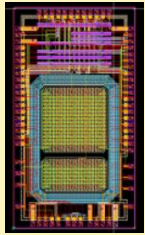
UNITEC

Monolithic SiGe BiCMOS for timing



Monolithic prototypes with SiGe BiCMOS (without internal gain layer)

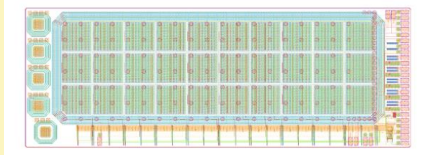
2016



200ps

- 1 and 0.5 mm² pixels
- Discriminator output

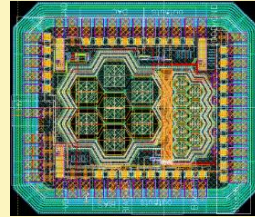
2017



110ps

- 30 pixels 500x500μm²
- 100ps TDC +I/O logic

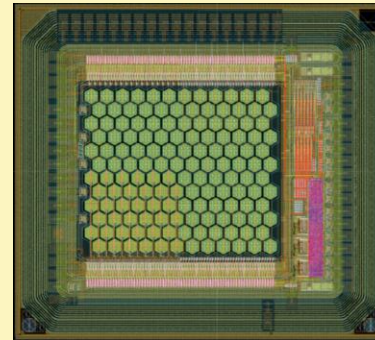
2018



50ps

- Hexagonal pixels 65μm and 130μm side
- Discriminator output

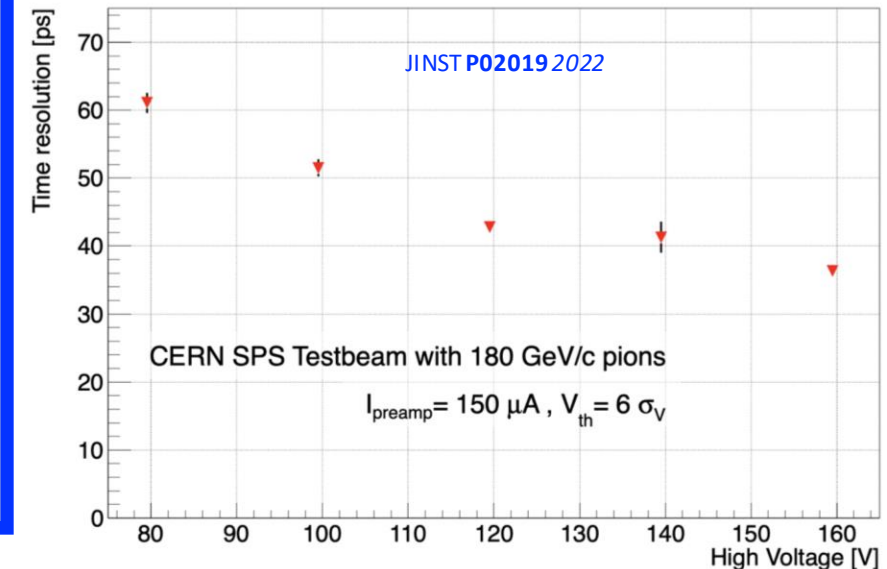
2019



36 ps

- Hexagonal pixels 65μm side
- 30ps TDC +I/O logic
- Analog channels

Test beam results of 2019 prototype



Sensor with no gain test beam results: JINST **P02019 2022**

PicoAD Sensor Concept



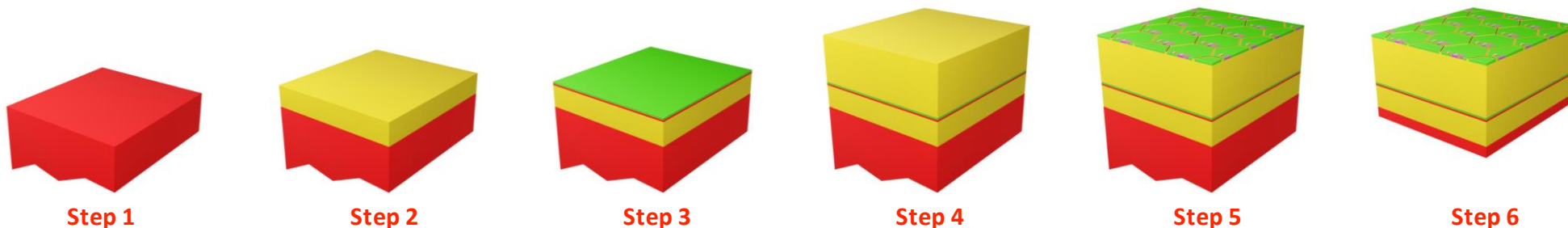
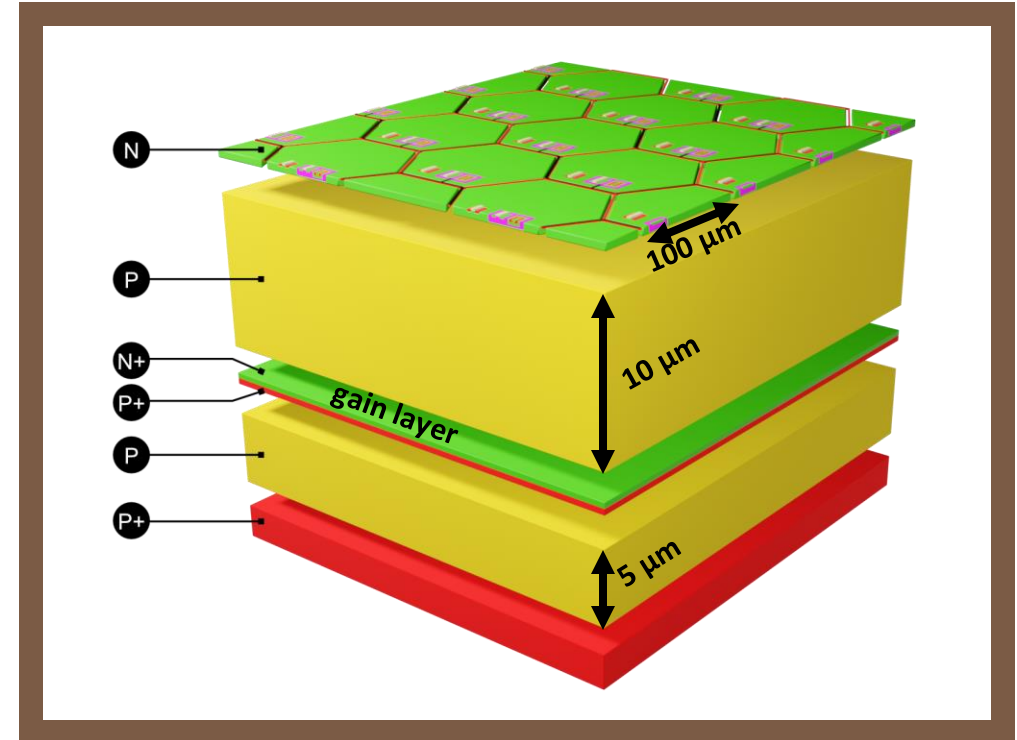
© G. Iacobucci, L. Paolozzi and P. Valerio. Multi-junction pico-avalanche detector;
European Patent EP3654376A1, US Patent US2021280734A1, Nov 2018

Multi-Junction Picosecond-Avalanche Detector[©]

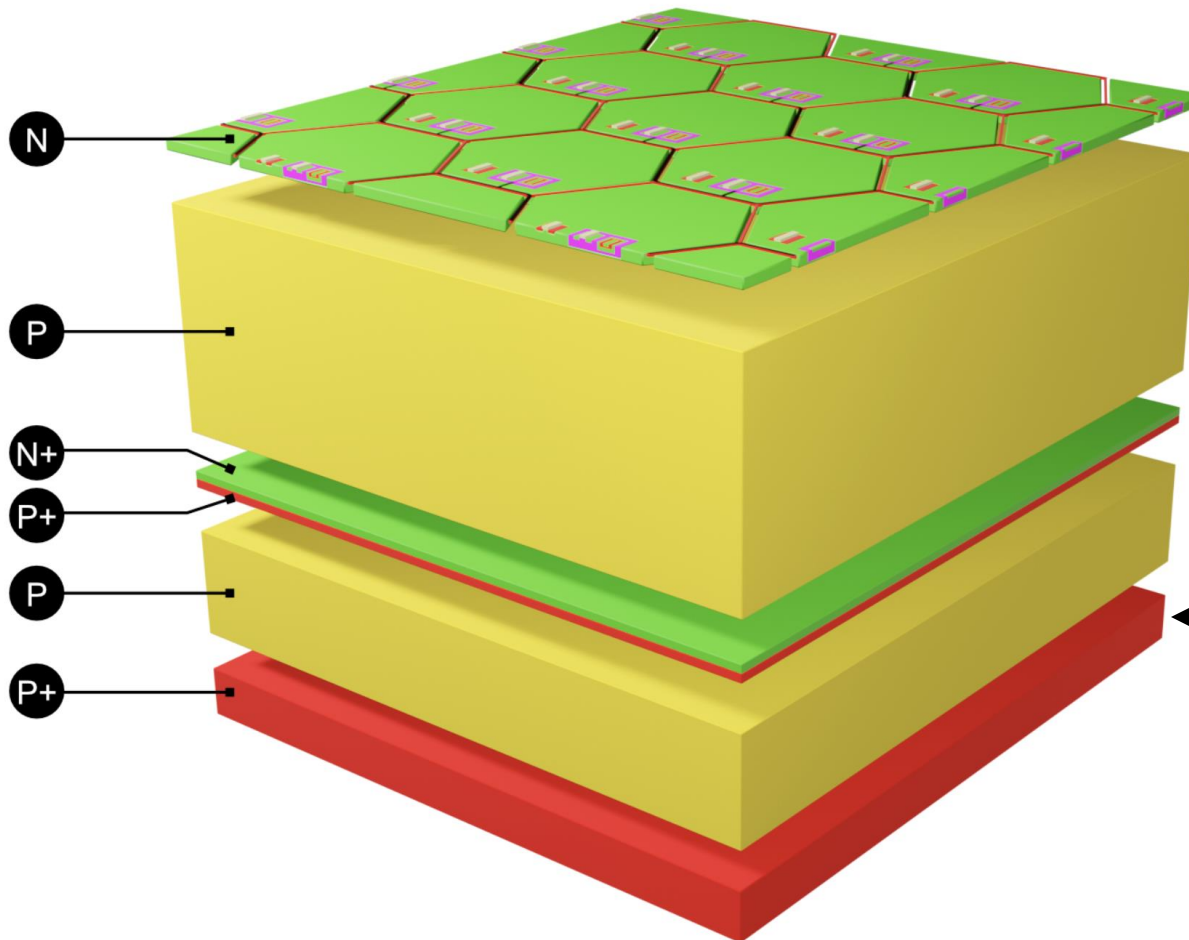
with continuous and deep gain layer:

- De-correlation from implant size/geometry
→ **high pixel granularity and full fill factor**
(high spatial resolution)
- Only small fraction of charge gets amplified
→ **reduced charge-collection noise**
(enhance timing resolution)

$$\sigma_T \cong \frac{t_{rise}}{Signal/Noise} \cong \frac{ENC}{I_{Ind}}$$



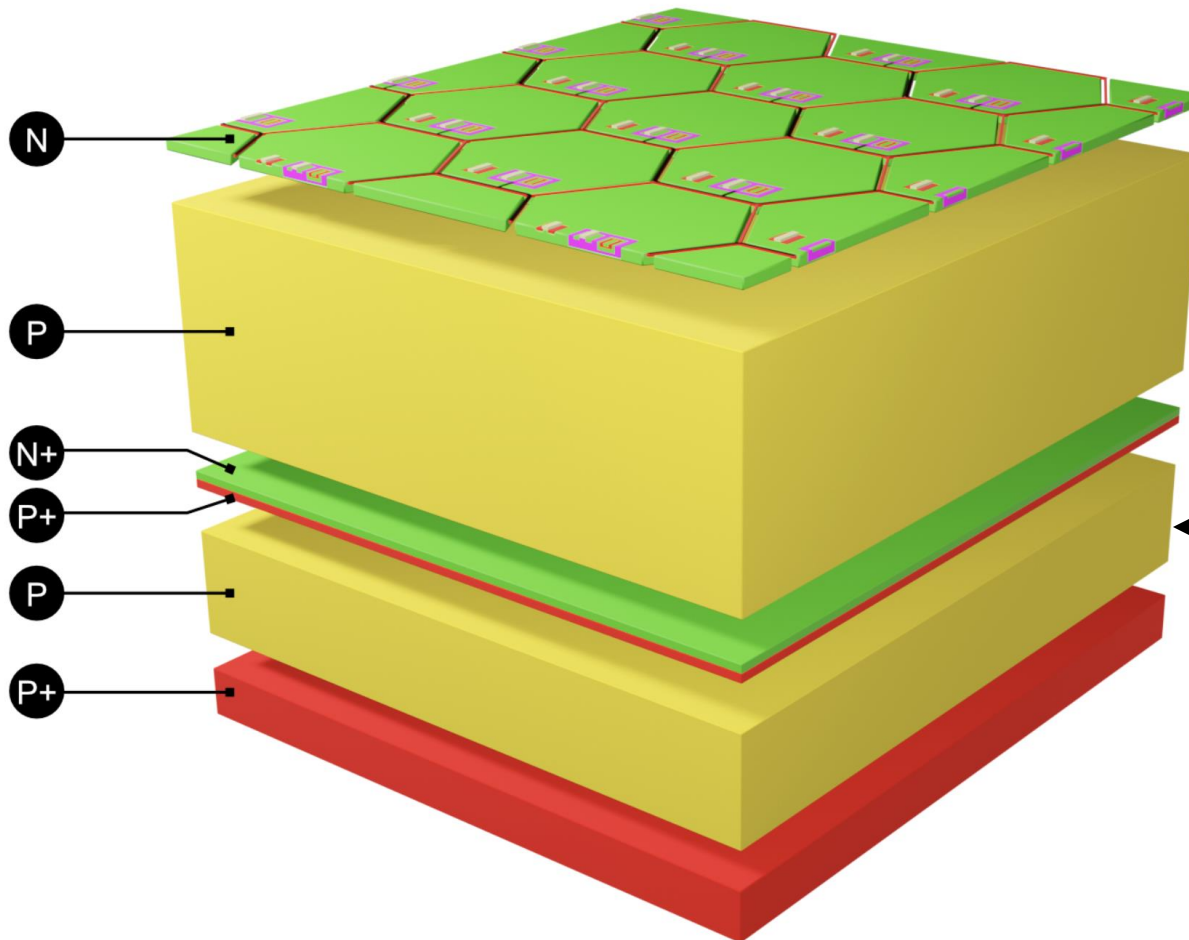
PicoAD Sensor Concept



Sensor growth on low resistivity wafers:

1. **No dedicated backside processing** needed
2. Low resistivity important to end depleted active region of sensor and minimise coupling to FE integrated in pixel

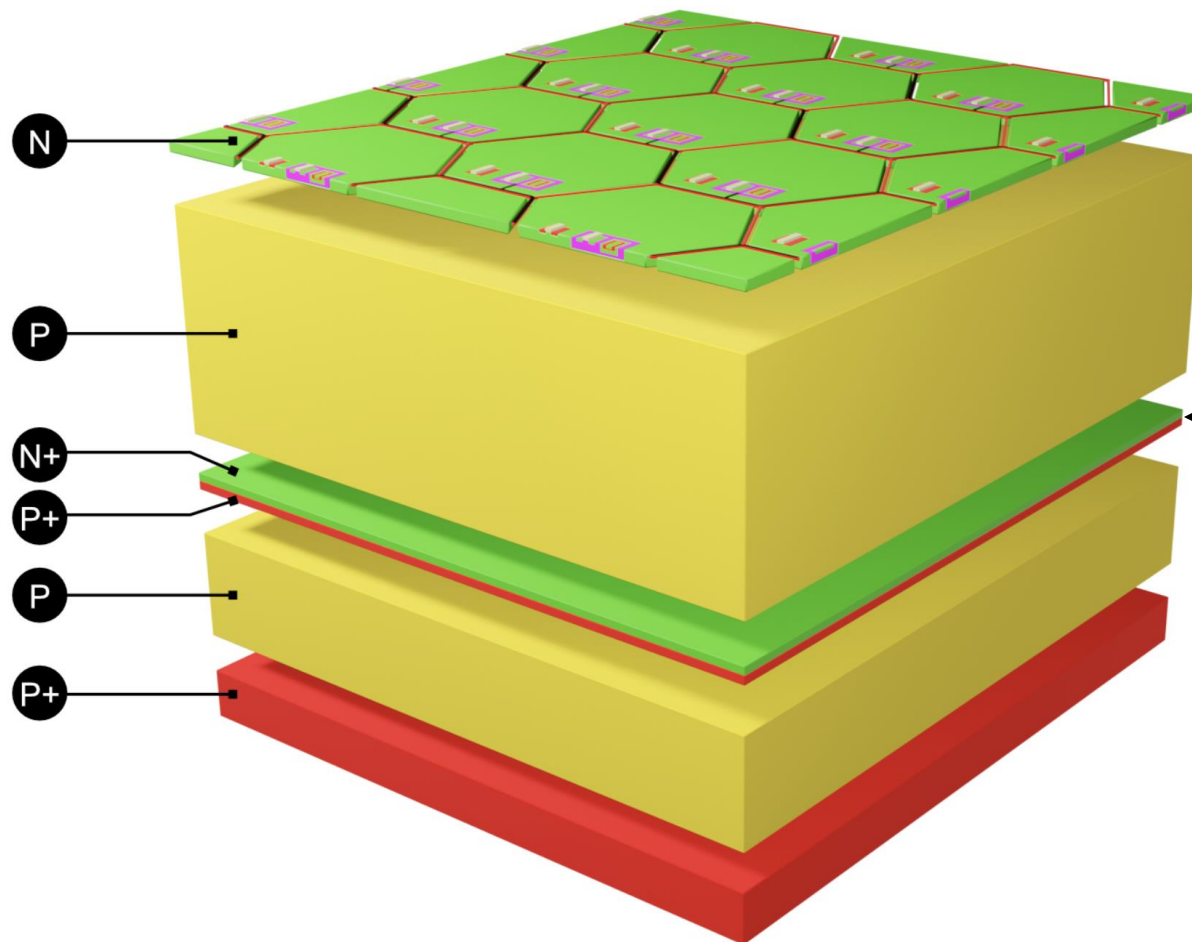
PicoAD Sensor Concept



Thin 'absorption region', 1st epitaxial layer:

1. Region where primary charge drifting towards topside gets amplified is produced
2. Thin layer ($\sim 5\mu\text{m}$) to **minimise charge collection noise**

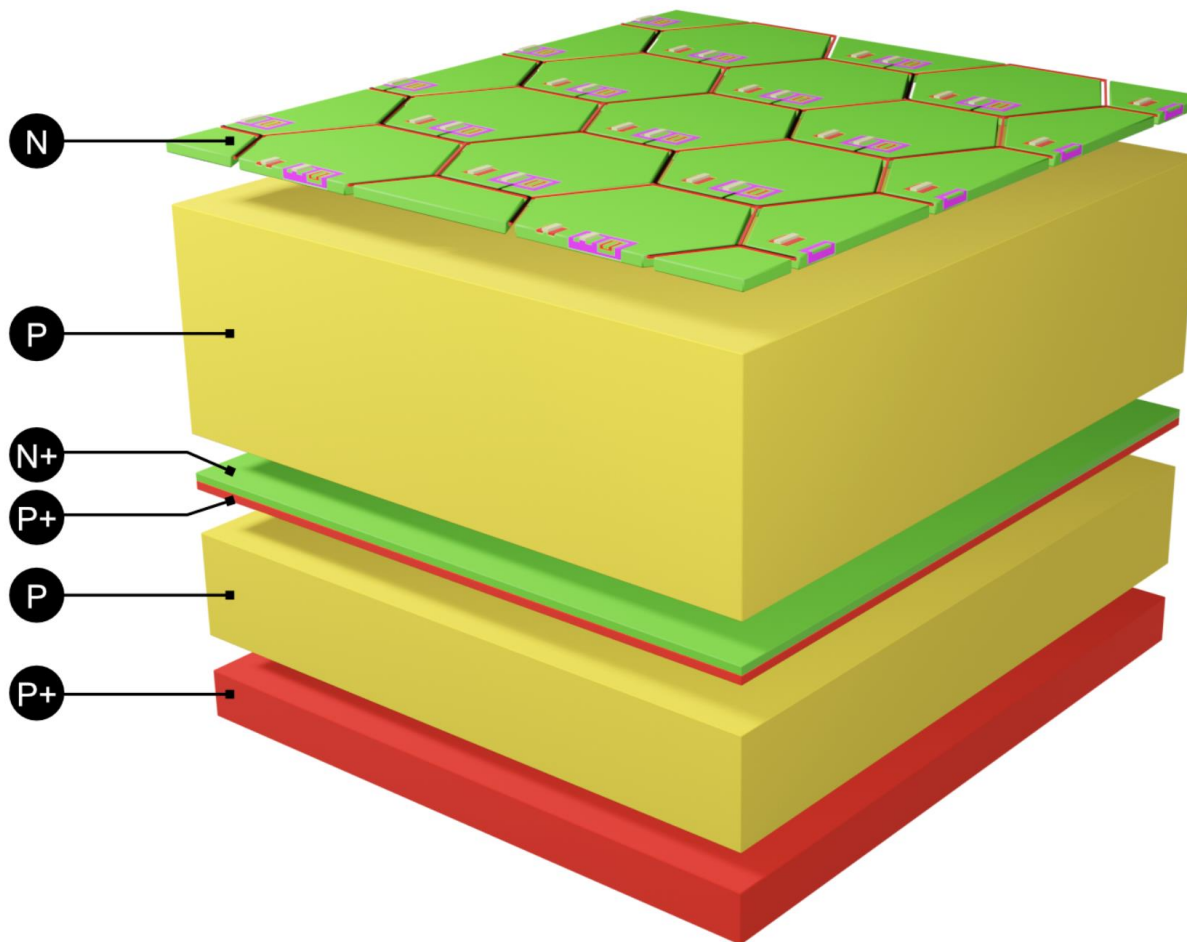
PicoAD Sensor Concept



Thin and uniform deep gain layer:

- Same doping of gain layer over full pixel cell (full 'fill-factor'):
 - **Uniform gain** and minimisation of pixel edge effects
- Gain layer physically separated from pixel implant:
 - Can decrease absorption region to minimise charge collection noise without increasing sensor capacitance (coupling to backside substrate p+)
 - Can integrate FE electronics inside pixel implant (**fully monolithic CMOS**)

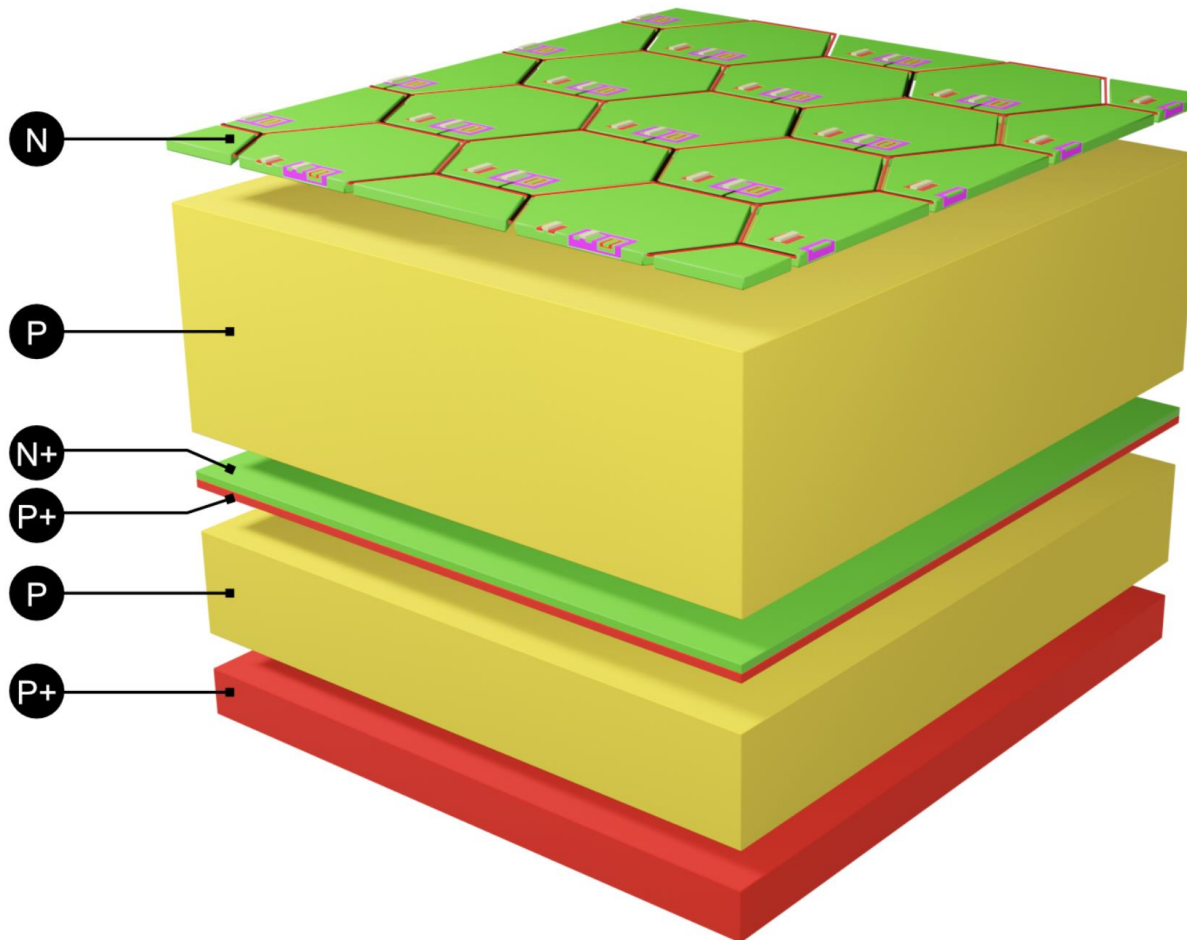
PicoAD Sensor Concept



Thicker 'drift region', 2nd epiaxial layer:

- Constrains:
 - Not too thick:
 - Maximise weighting field ($\propto 1/\text{depletion}$)
 - Maximise drift field
 - Not too thin:
 - Minimize capacitance
 - Minimize impact of pixel implants on gain layer uniformity

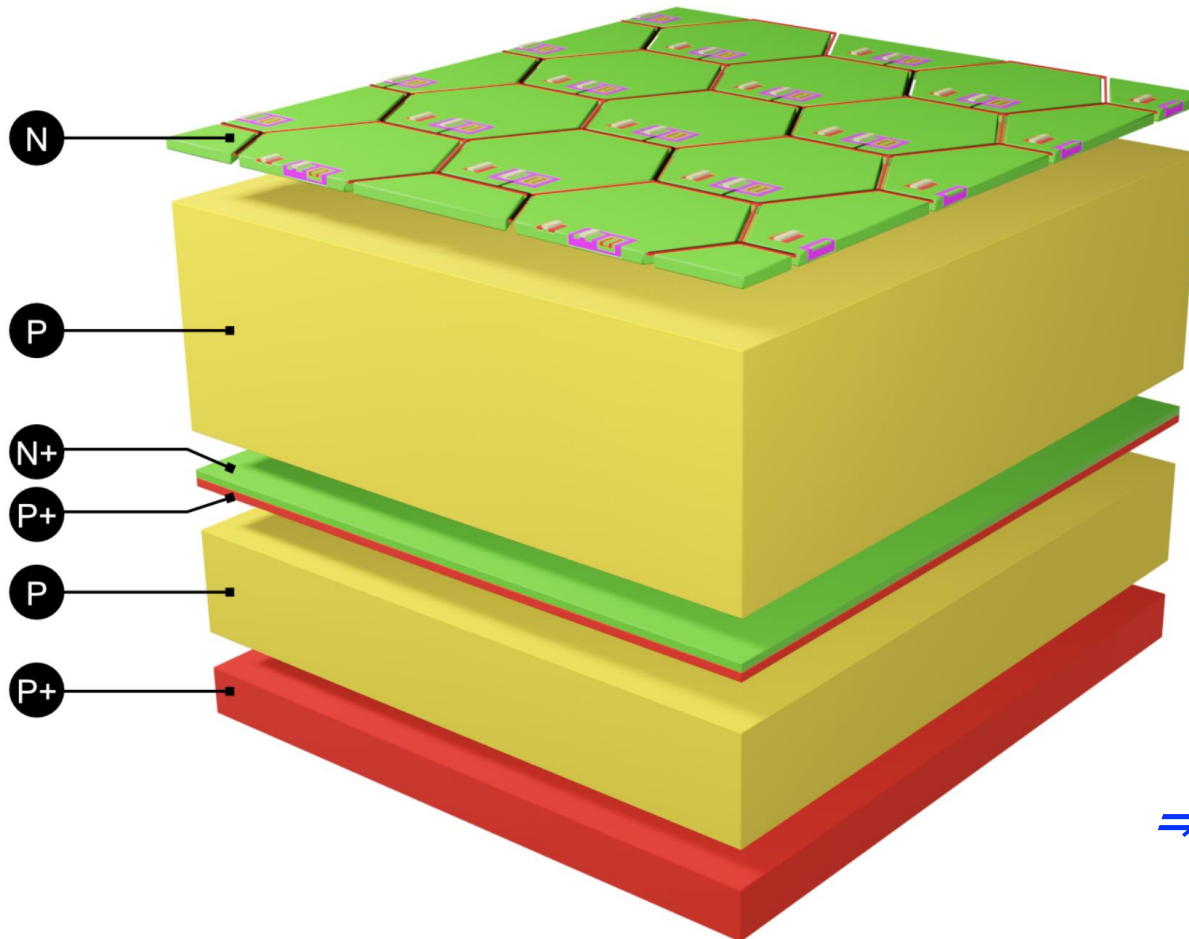
PicoAD Sensor Concept



Fully monolithic CMOS processing:

- Implemented in **large collection electrode design to maximise weighting** field over full pixel cell
- **Pixel implant size can be minimised** while maintaining gain layer uniformity!
- **Hexagonal design to minimise edge effects** (impact on gain layer + high field breakdown between pixels)

PicoAD Sensor Concept



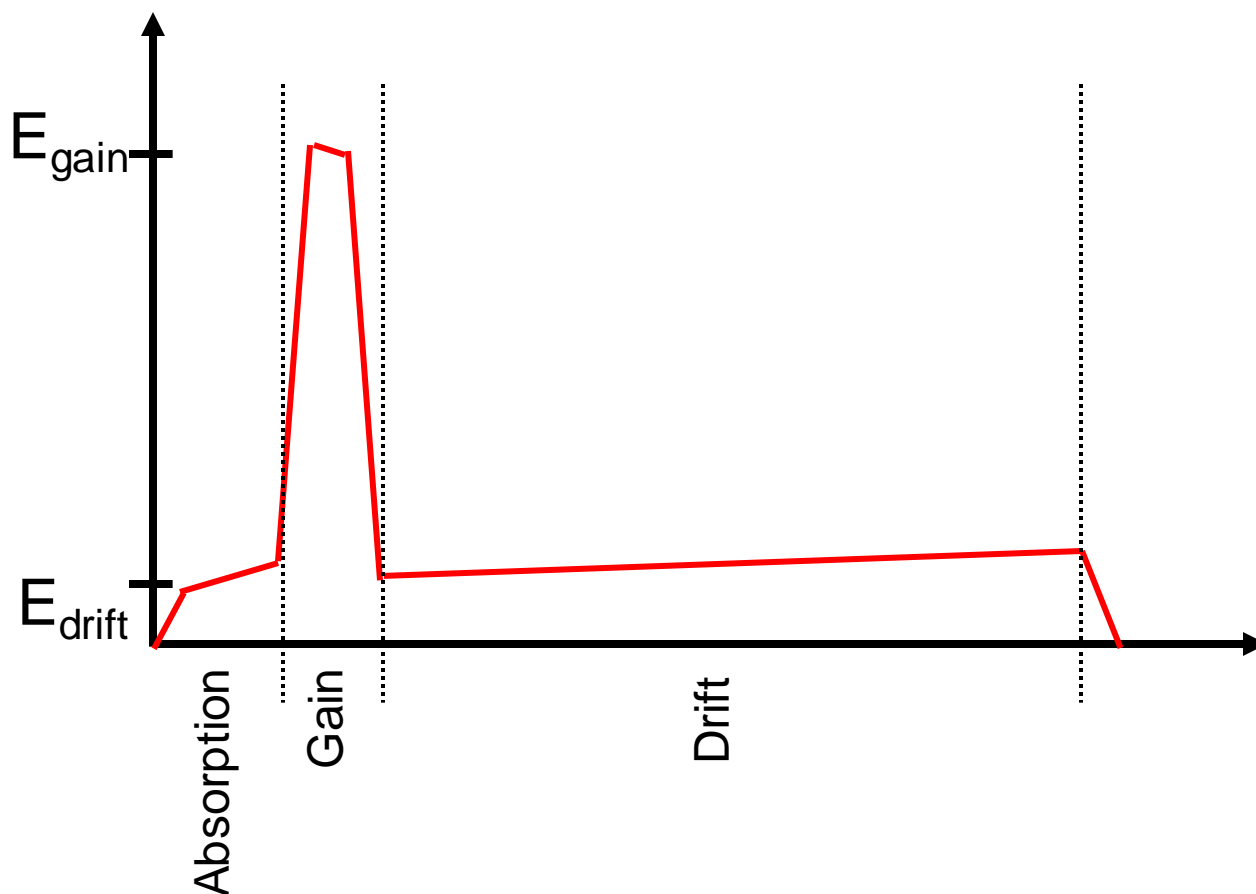
⇒ PicoAD concept provides **simultaneously**:

- Reduced charge collection noise
 - Reduced sensor capacitance
 - Improved weighting field
 - Small pixel size
 - Fully monolithic CMOS design
- } Pico-second sensor timing

⇒ *Sensor optimised for picosecond timing in fully monolithic small pixel design*

PicoAD Sensor Concept

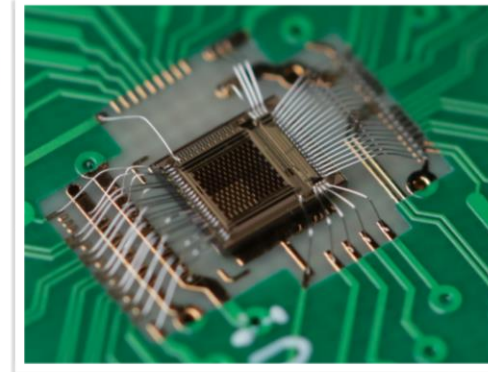
Picosecond Avalanche Detector (PicoAD): EU Patent EP18207008.6



- The introduction of fully-depleted multi-pn junctions allows to **engineer the electric field**.
- New device with unique timing and reliability performance.
- Gain with 100% fill-factor.
- Geant4 + Cadence simulations estimate **~2ps time resolution** contribution from the sensor.
- Requires low-noise, ultra fast electronics to be fully exploited.

PicoAD monolithic proof-of-concept prototype

The proof-of-concept monolithic ASIC was produced by IHP in their SG13G2 SiGe BiCMOS process using the existing 2019 prototype design.

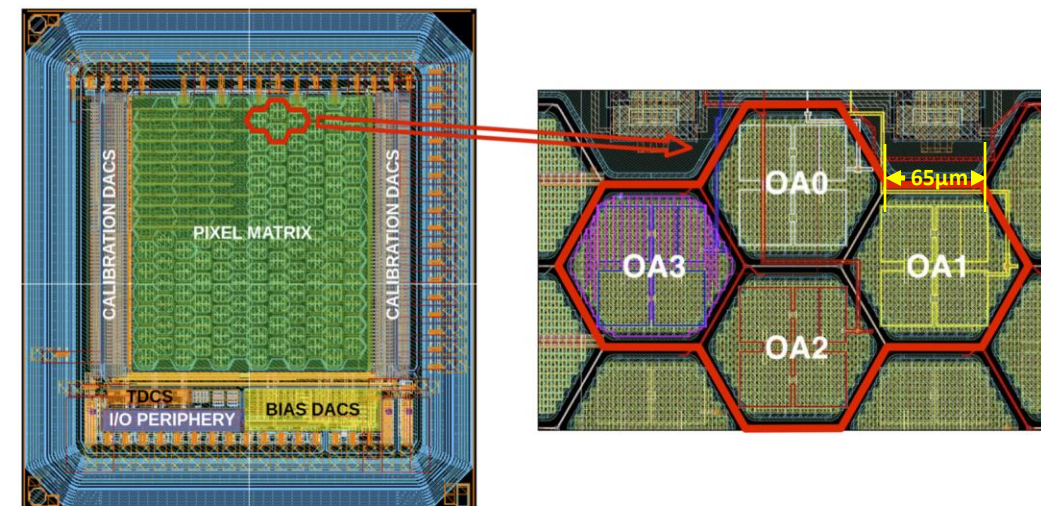


The ASIC contains:

- **Four matrices** of **hexagonal pixels** with $\approx 100\mu\text{m}$ pitch
 - with different electronics configurations
- **Four analog pixels**
 - tested with ^{55}Fe source and in testbeam

IHP also produced **PicoAD special wafers** with **four different gain-layer implant doses**

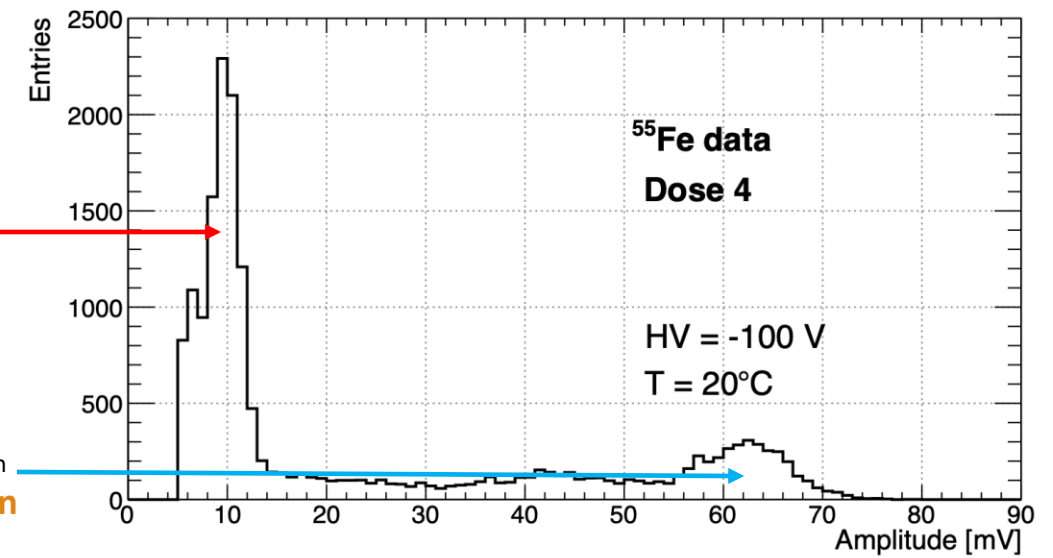
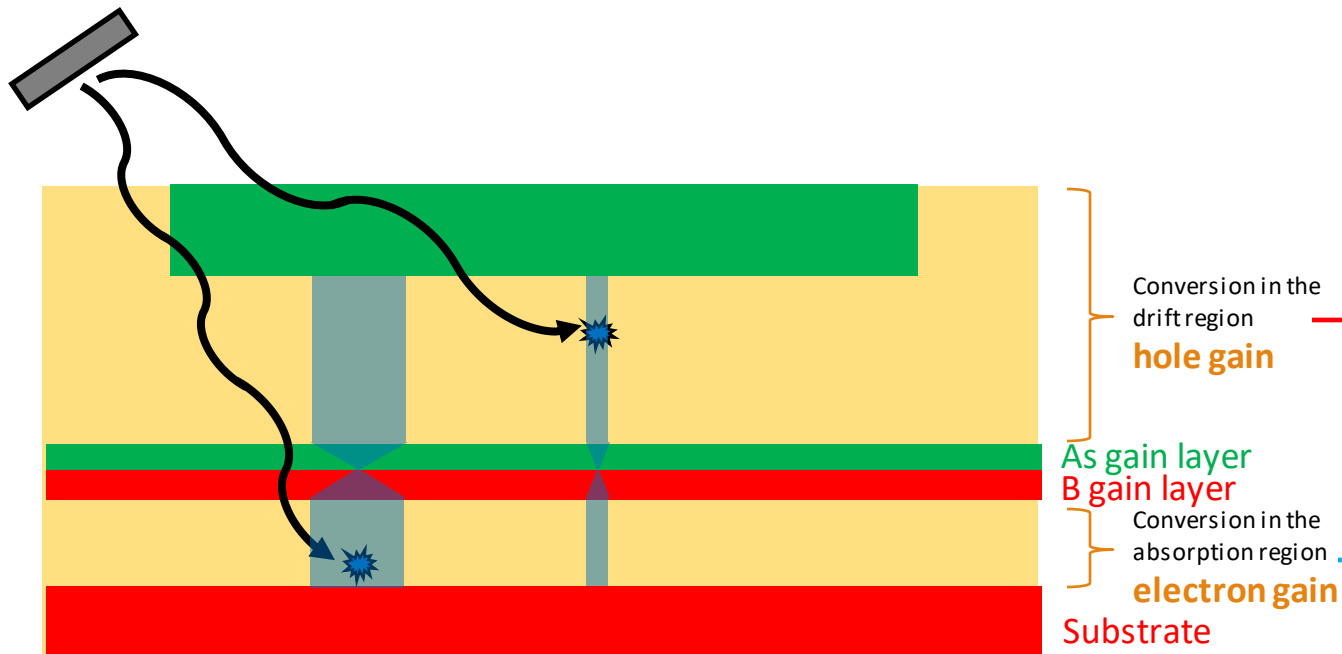
PicoAD Proof-Of-Concept Prototype (2021)



Gain Measurement with ^{55}Fe source

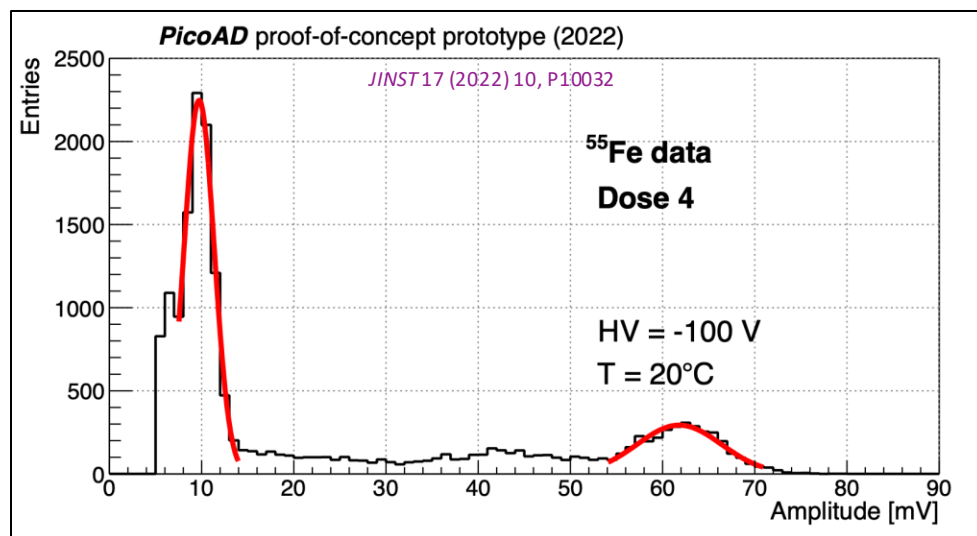


Fe-55 X-ray source: point-like charge deposition inside the sensor



Gain Measurement with ^{55}Fe source

Average amplitudes of h^+ and e^- gains
extracted via gaussian fit around local maxima

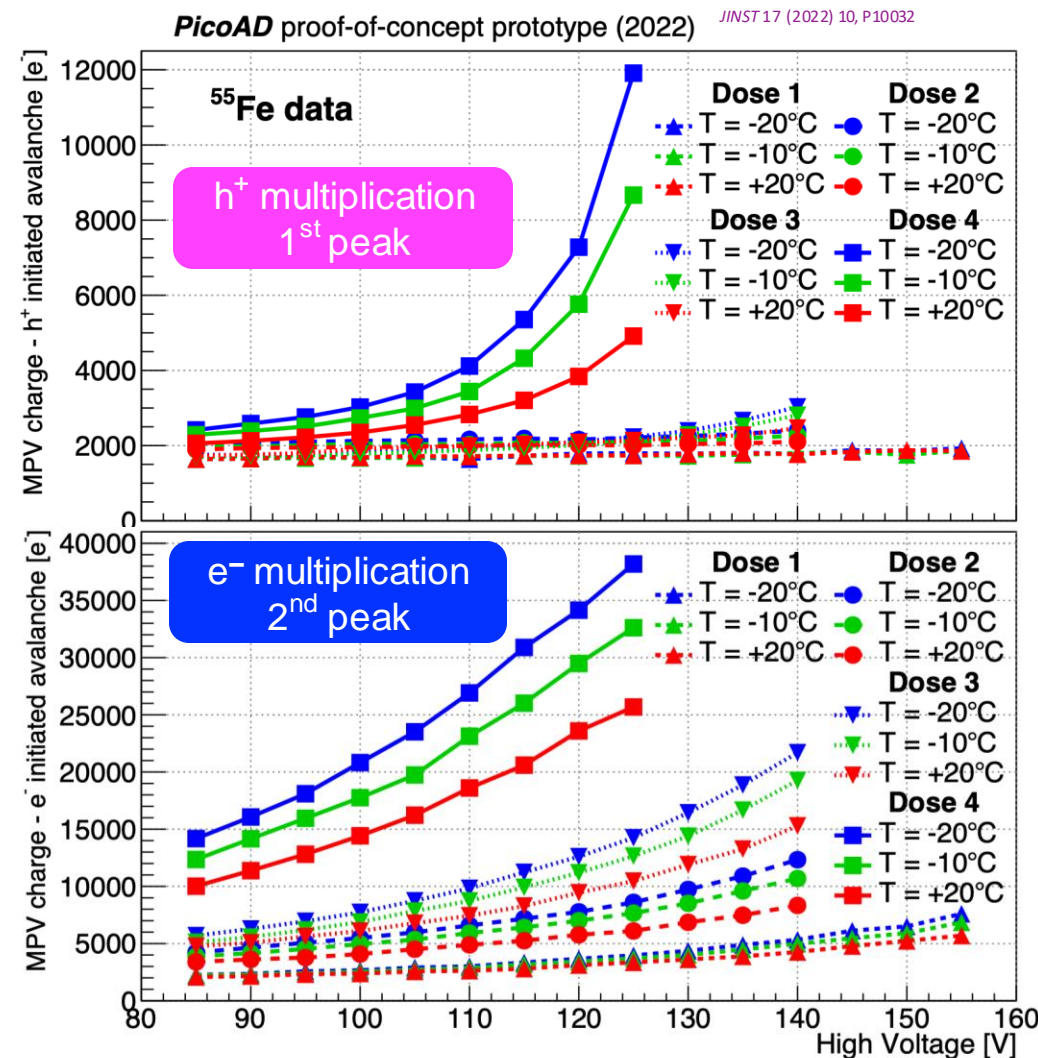


Assumption of no gain multiplication when:

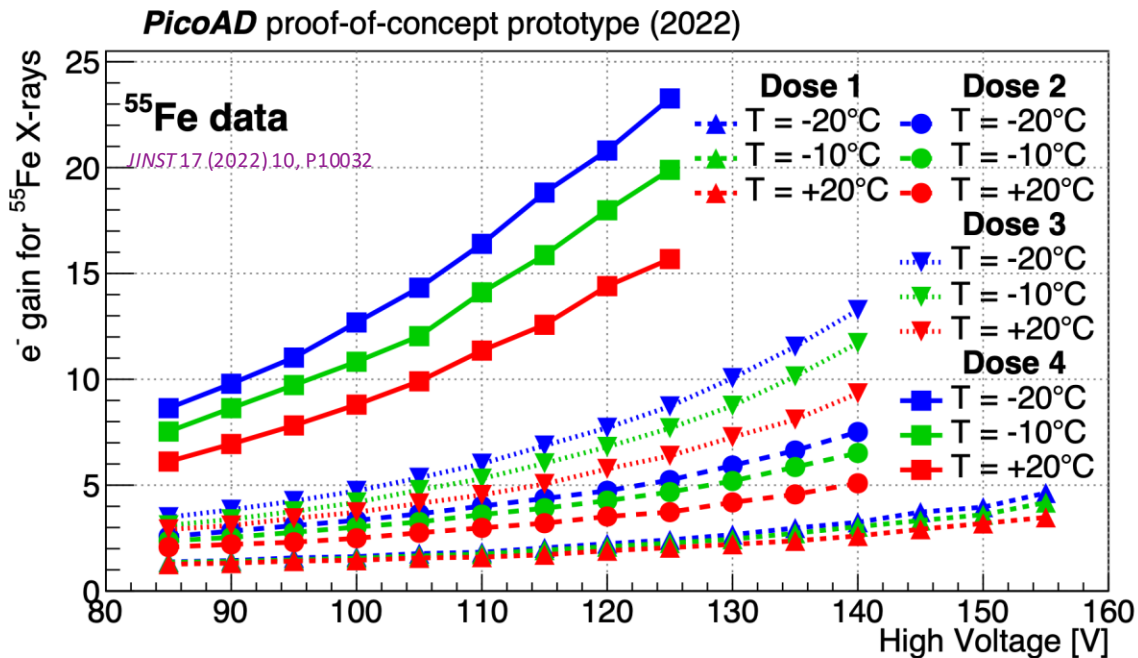
- photon absorbed in drift region
- lowest voltage (85 V)
- lowest dose (dose 1)



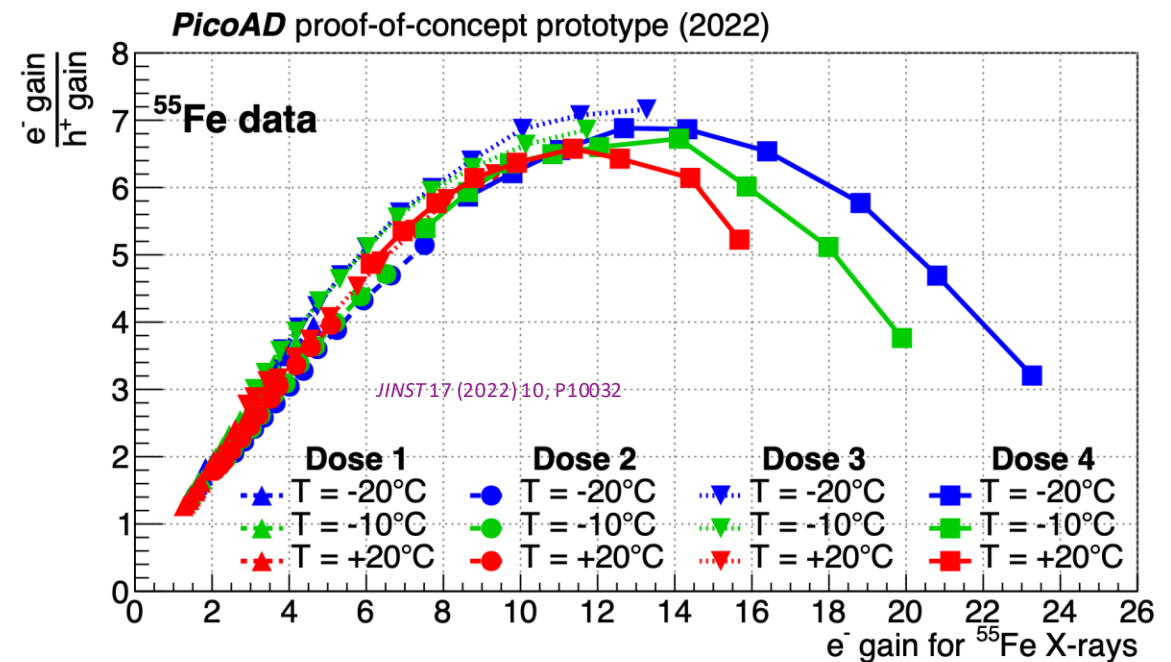
**normalization
value**



Gain Measurement with ^{55}Fe source



A gain up to ≈ 20 for ^{55}Fe X-rays
obtained at HV = 120 V and $T = -20^\circ\text{C}$



Evidence for **gain suppression** due
to space-charge effects
in the case of ^{55}Fe X-rays

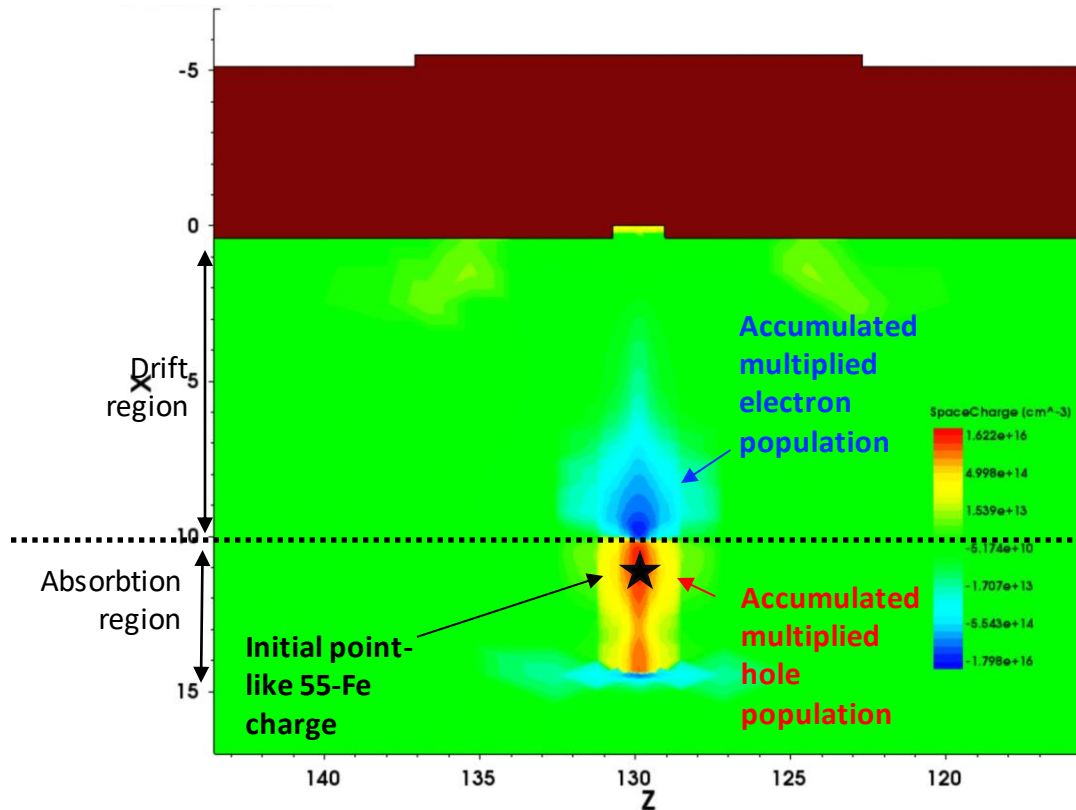
We estimated that ^{55}Fe gain of ≈ 23 corresponds to **gain 60–70 for a MIP**

Transient space charge

Transient 3D TCAD simulation of point like 55-Fe charge deposition in absorption layer:

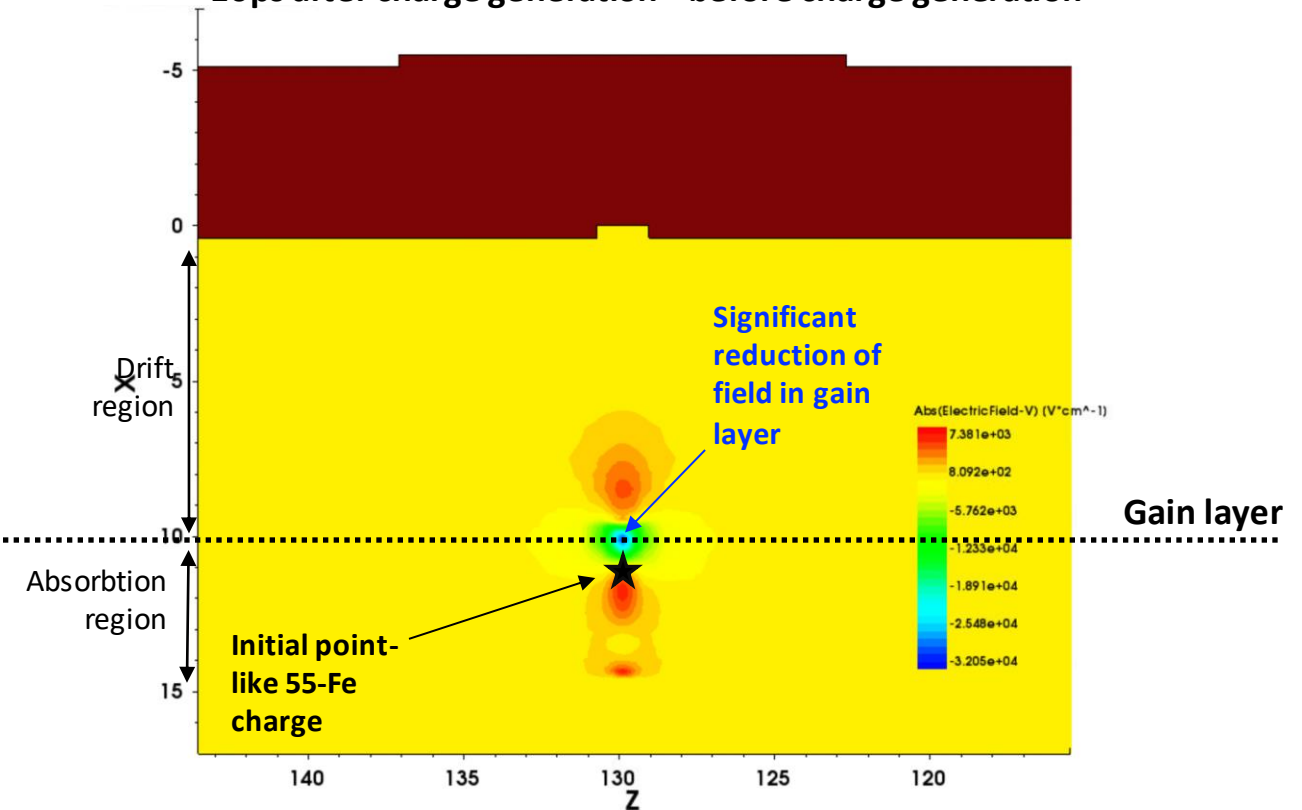
Space charge:

10ps after charge generation – before charge generation:



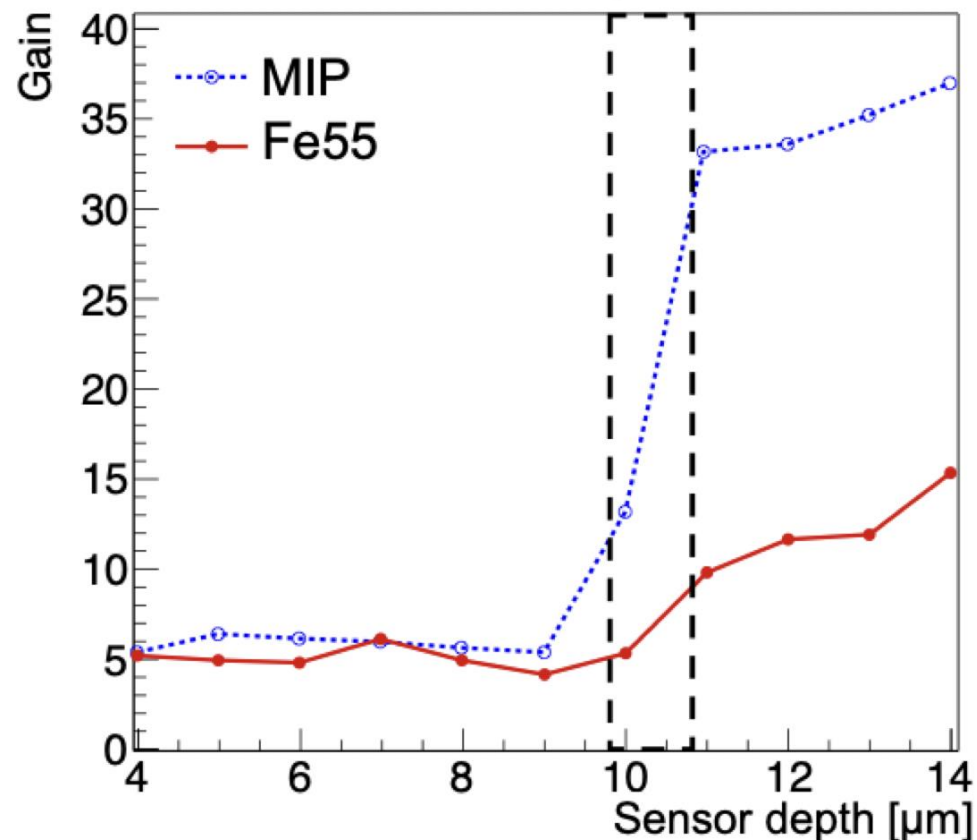
Electric field:

10ps after charge generation – before charge generation



Transient space charge

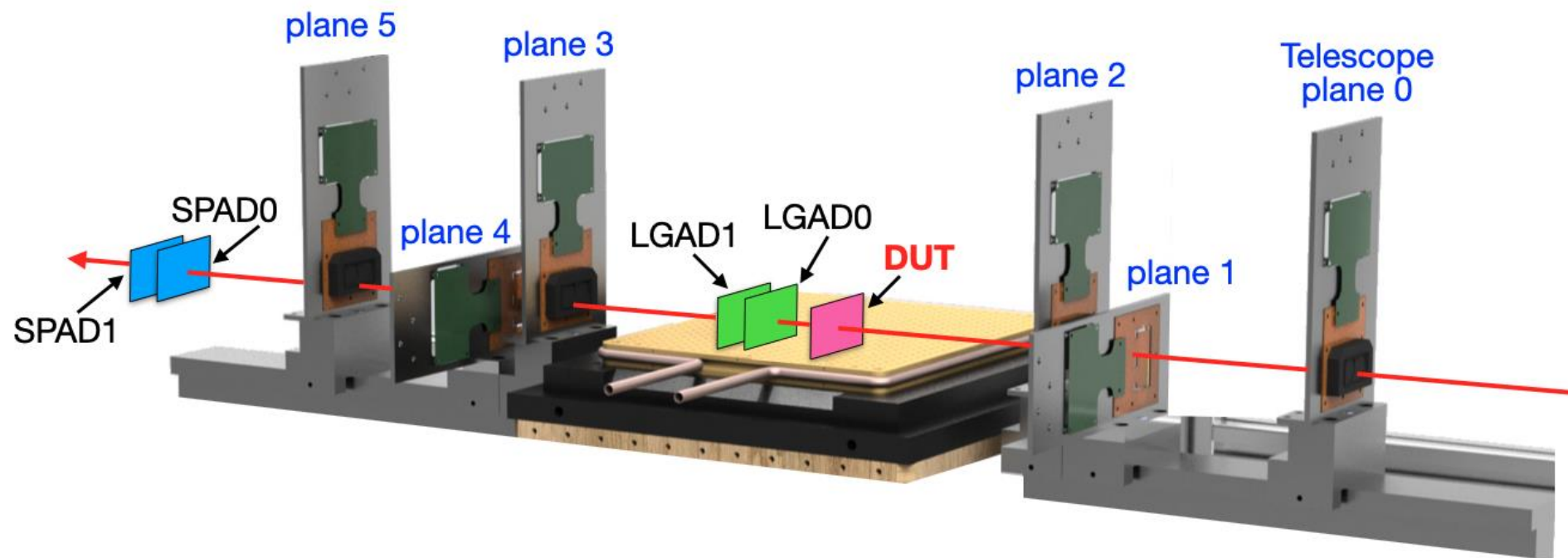
Gain as function of sensor depth for different primary charge carrier densities:



- For high charge carrier densities (Fe55) the electron gain is suppressed compared to lower charge carrier densities (MIPs).
- Simulated suppression factor of Fe55 w.r.t. MIP charge compatible to calculation of compression factor from test-beam and Fe55 measurements.
- Measured gain for Fe55 significantly suppressed by transient space charge effect.
- Need of fully self consistent transient TCAD simulations.

Test Beam: Experimental Setup

CERN SPS Testbeam with 180 GeV/c pions to measure **efficiency** and **time resolution**

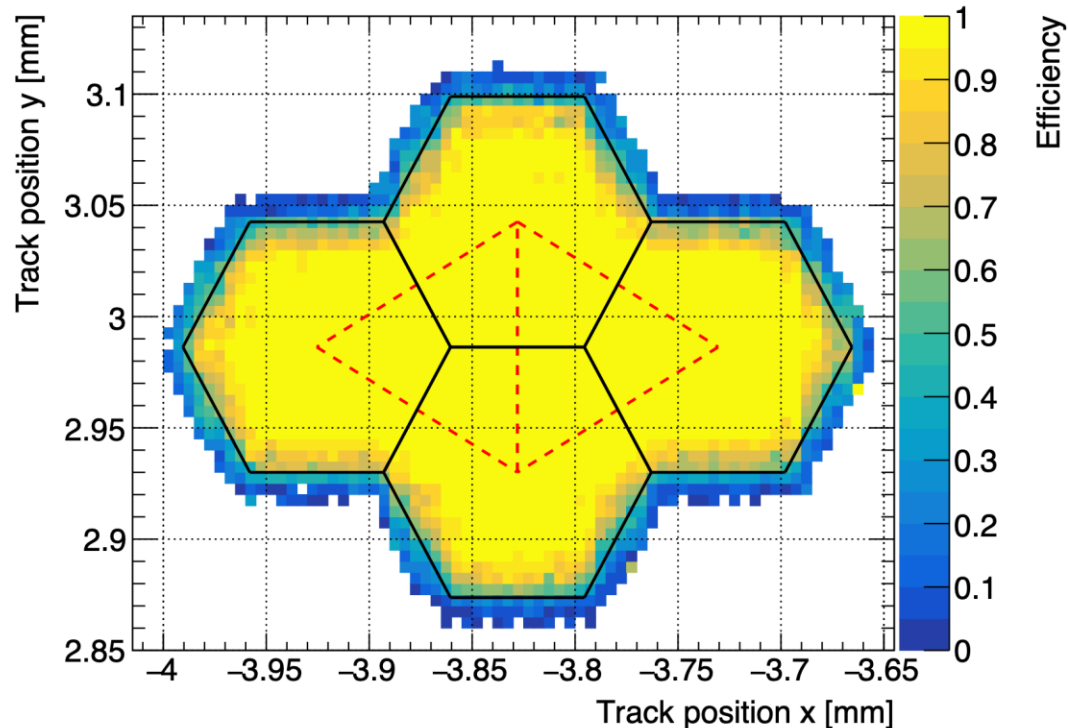


UNIGE FE-I4 telescope to provide spatial information ($\sigma_{x,y} \approx 10 \mu\text{m}$)

Two LGADs ($\sigma_t \approx 35 \text{ ps}$) to provide the timing reference (and **two SPADs** with $\sigma_t \approx 20 \text{ ps}$)

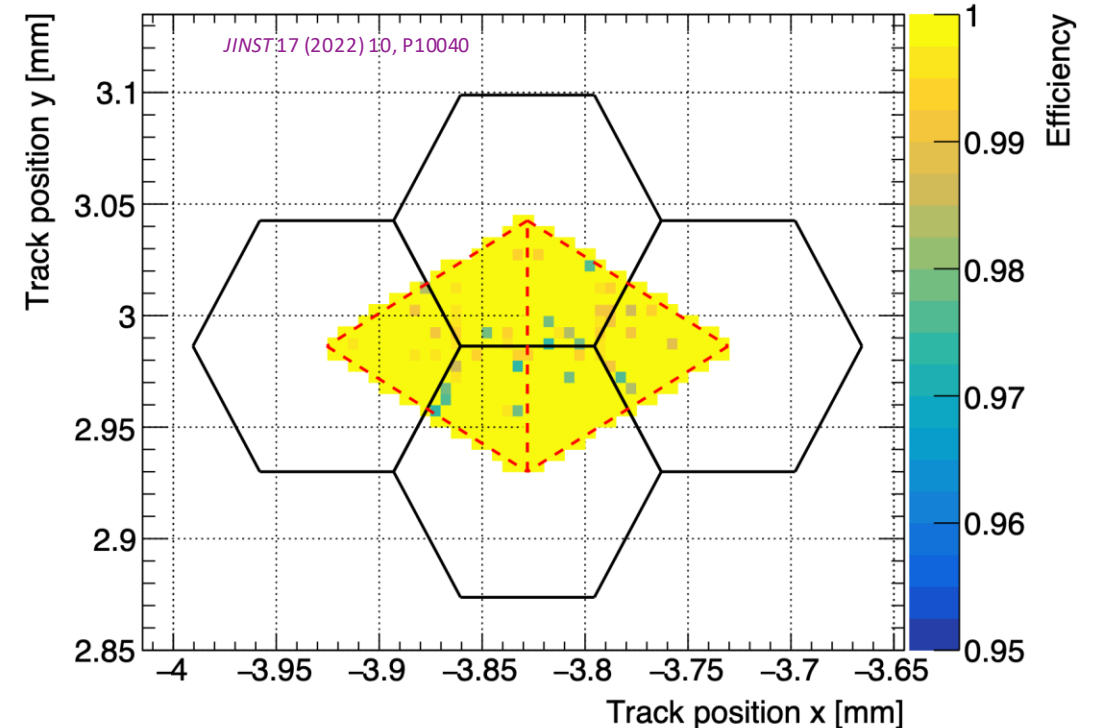
Testbeam results: Efficiency

PicoAD proof-of-concept prototype (2022)

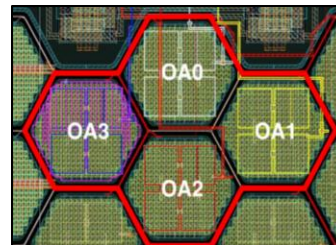


CERN SPS Testbeam: 180 GeV/c pions

$V_{th} = 4$ mV ; HV = 125 V ; Power = 2.7 W/cm²



Apparent degradation at the external edges of the four pixels is due to the telescope pointing resolution of ≈ 10 μ m

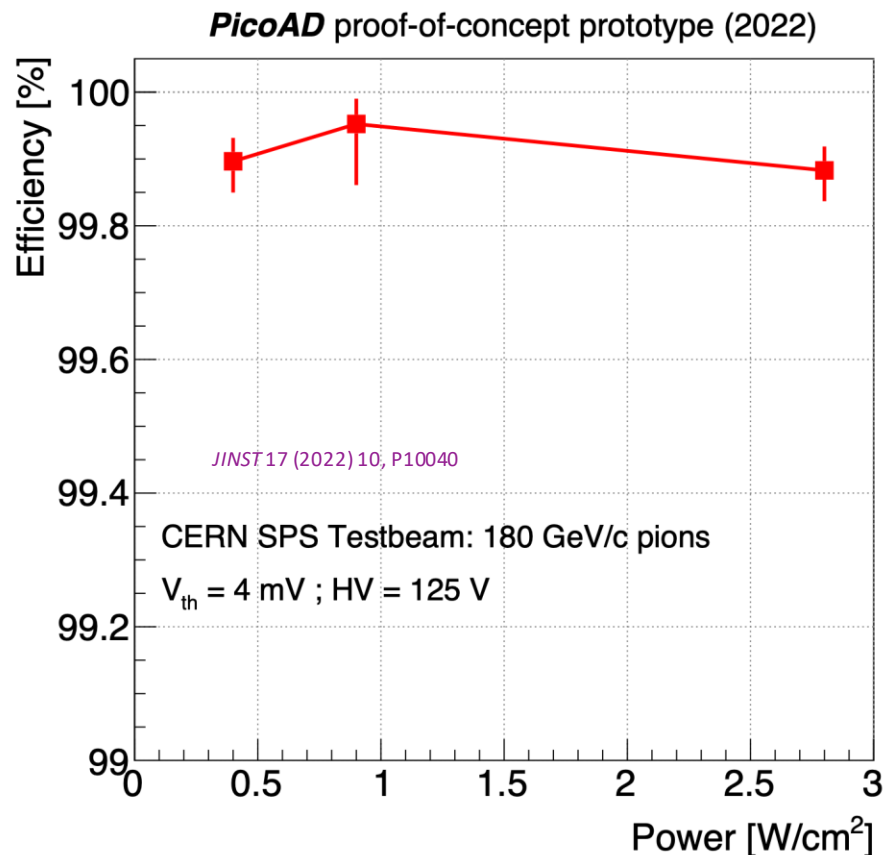


Selection of two **triangles**:

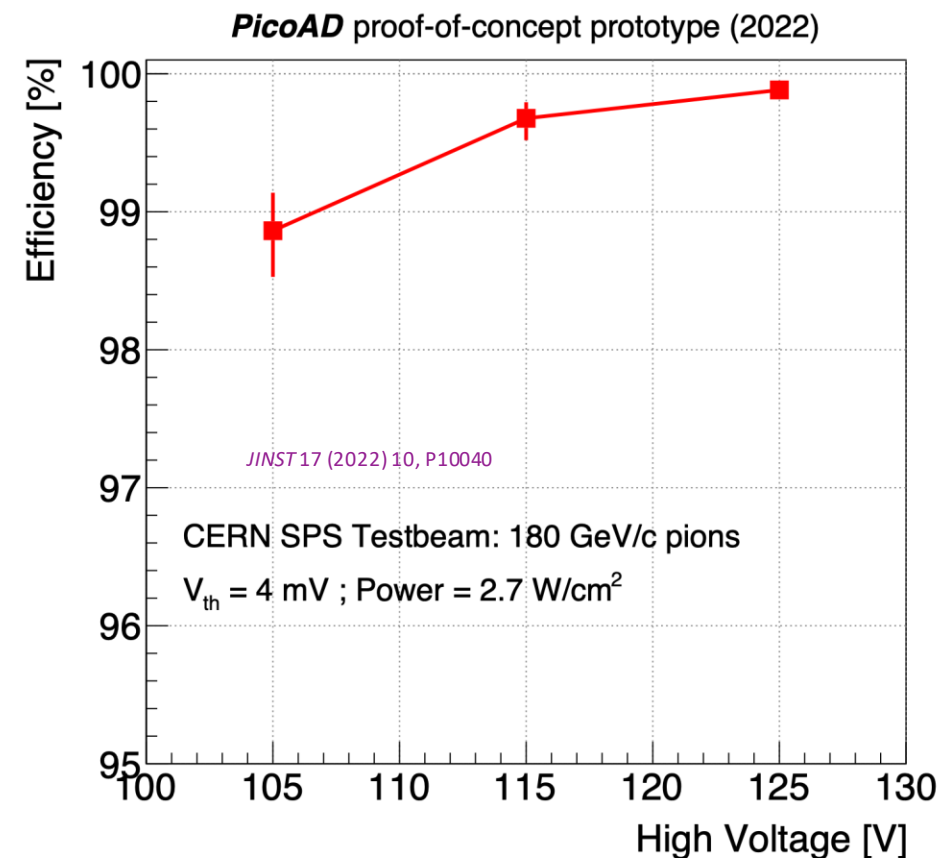
- representative of a whole pixel
- **unbiased** by telescope resolution

Testbeam results: Efficiency

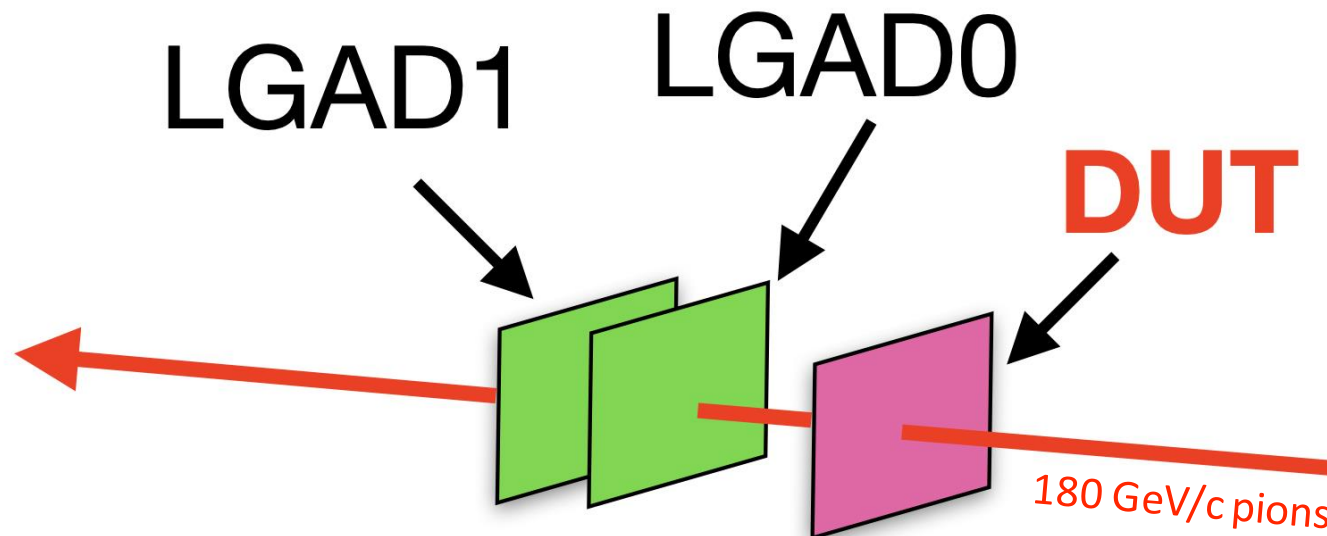
99.9% for all power consumptions



Drops to 99% for HV=105 V



Time Resolution

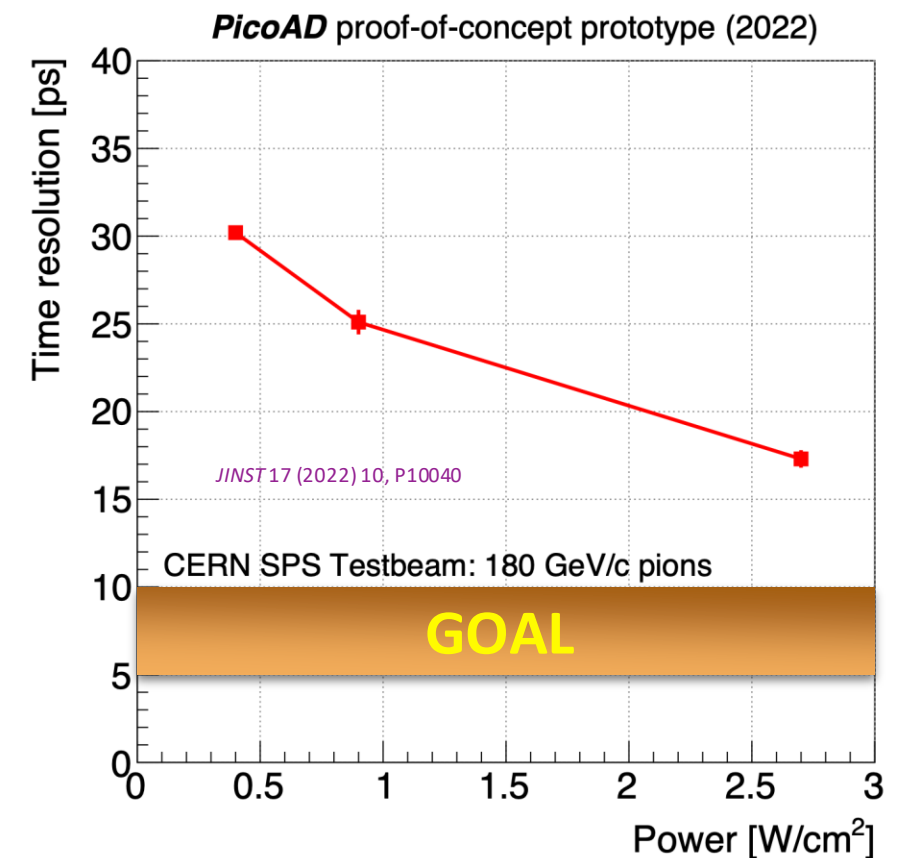
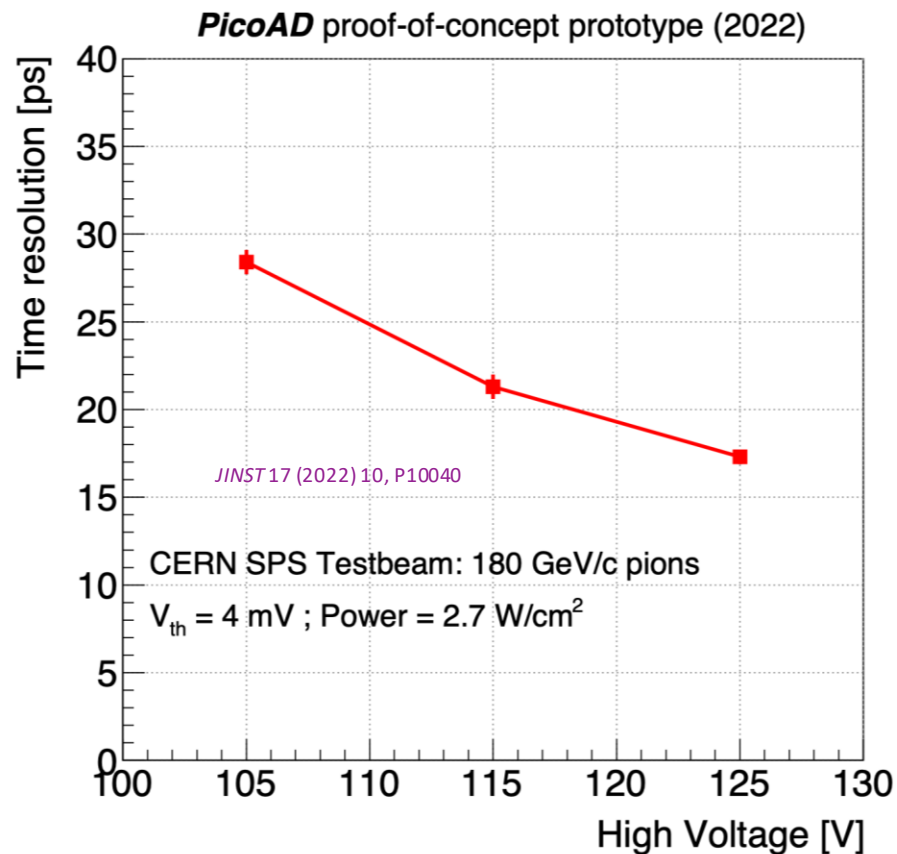


Results were also verified using **two SPADs** (but with much smaller statistics)

Testbeam results: Time Resolution

Best performance: **(17.3 ± 0.4) ps**
for HV=125 V and Power = **2.7 W/cm^2**

Timing resolution of **30 ps** even
at power consumption of **0.4 W/cm^2**



PicoAD uniformity of response

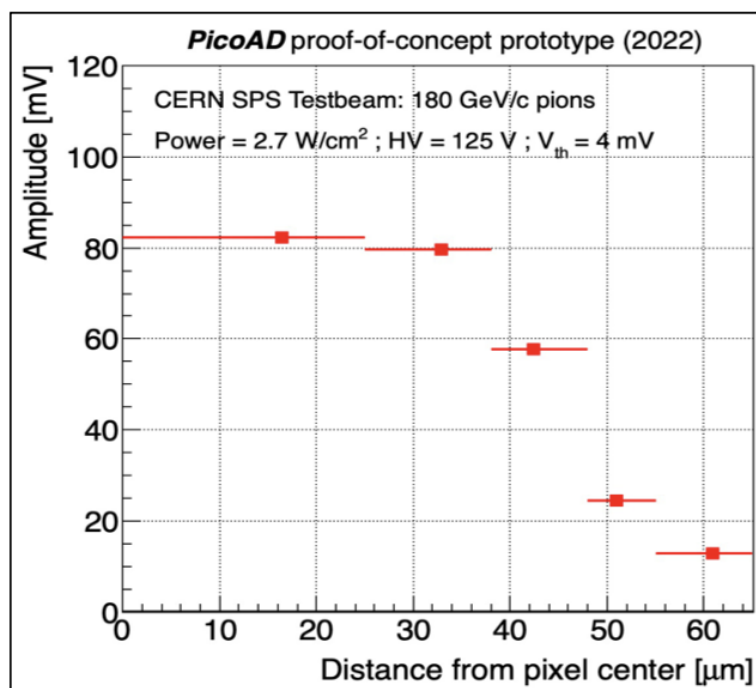
Testbeam Results of the Picosecond Avalanche Detector Proof-Of-Concept Prototype,
G. Iacobucci et.al, arXiv:2208.11019v1, submitted to JINST



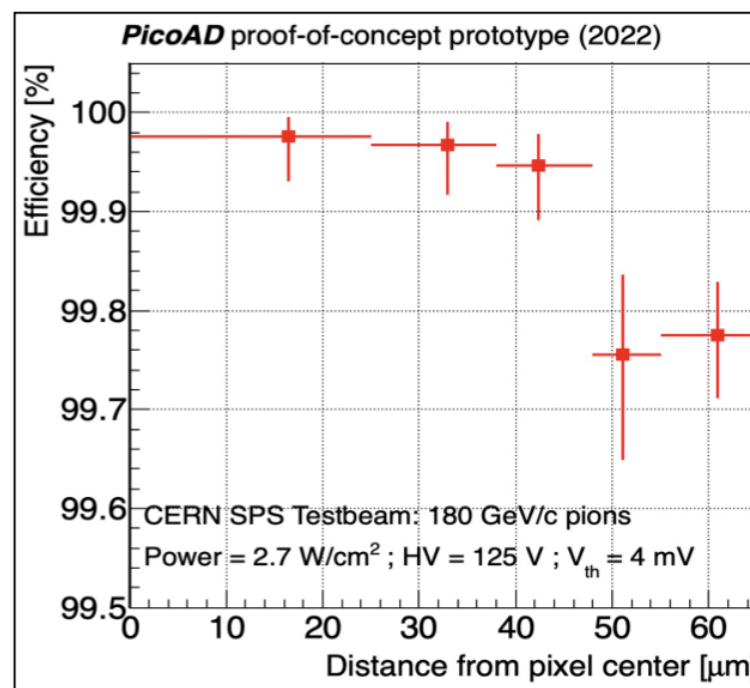
FACULTY OF SCIENCE
Department of Nuclear and
Particle Physics



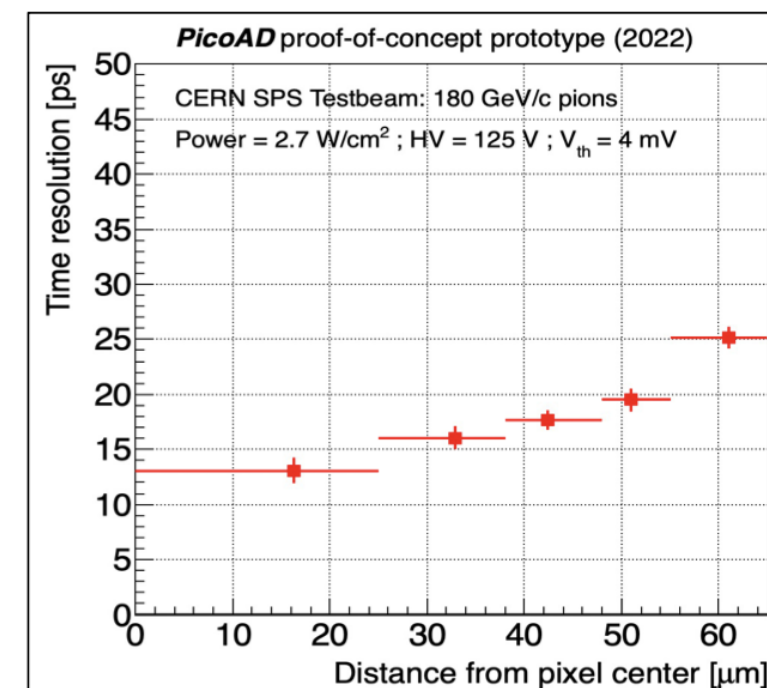
Amplitude vs. distance pixel center:



Efficiency vs. distance pixel center:



Time resolution vs. distance pixel center:

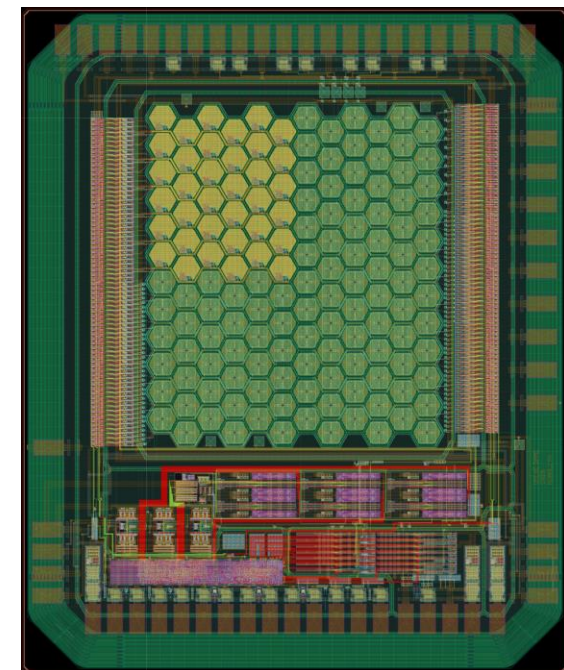


- Small degradation of the performance towards the edge of the pixel
- Effect of the finite resolution of the telescope convoluted with the real degradation
- The best timing resolution is **13.2 ± 0.8 ps within 25 μm from the pixel center**

2022 prototype – No gain layer

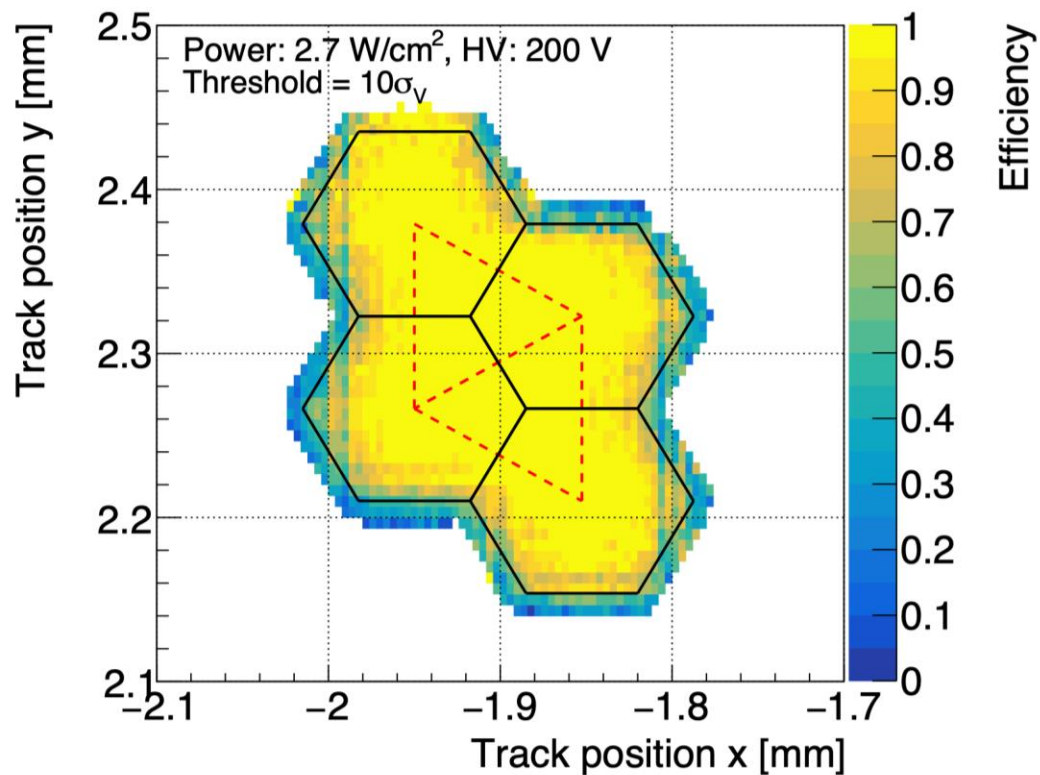
Same matrix configuration as previous, but:

- Substrate: $50\Omega\text{cm}$ \rightarrow $350\Omega\text{cm}$ epilayer, $50\mu\text{m}$ thick on low-res ($1\Omega\text{cm}$) substrate.
 - Smaller pixel capacitance
 - **Depletion $26\mu\text{m} \rightarrow 50\mu\text{m}$**
 - Can operate sensor with v_{drift} **saturated** everywhere
- Preamp and driver voltage decoupled:
 - Increased amplifier gain
 - **Removed cross-talk**
- Differential output, optimized FE layout, high-frequency cables:
 - **Better rise time ($600\text{ps} \rightarrow 300\text{ps}$)**
- **NO GAIN LAYER**
 - A picoAD version of the 2022 prototype is still being manufactured.



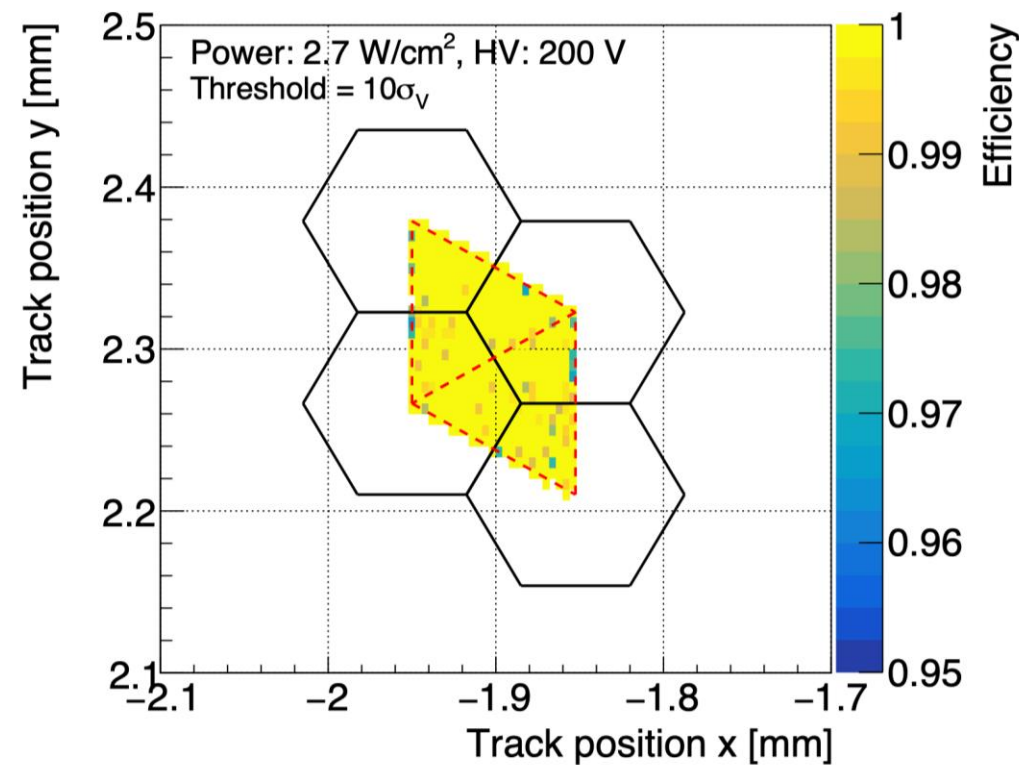
2022 prototype — no gain layer

MONOLITH prototype (2022) — no gain layer



Efficiency at the external edges affected by the telescope resolution of 10 μm

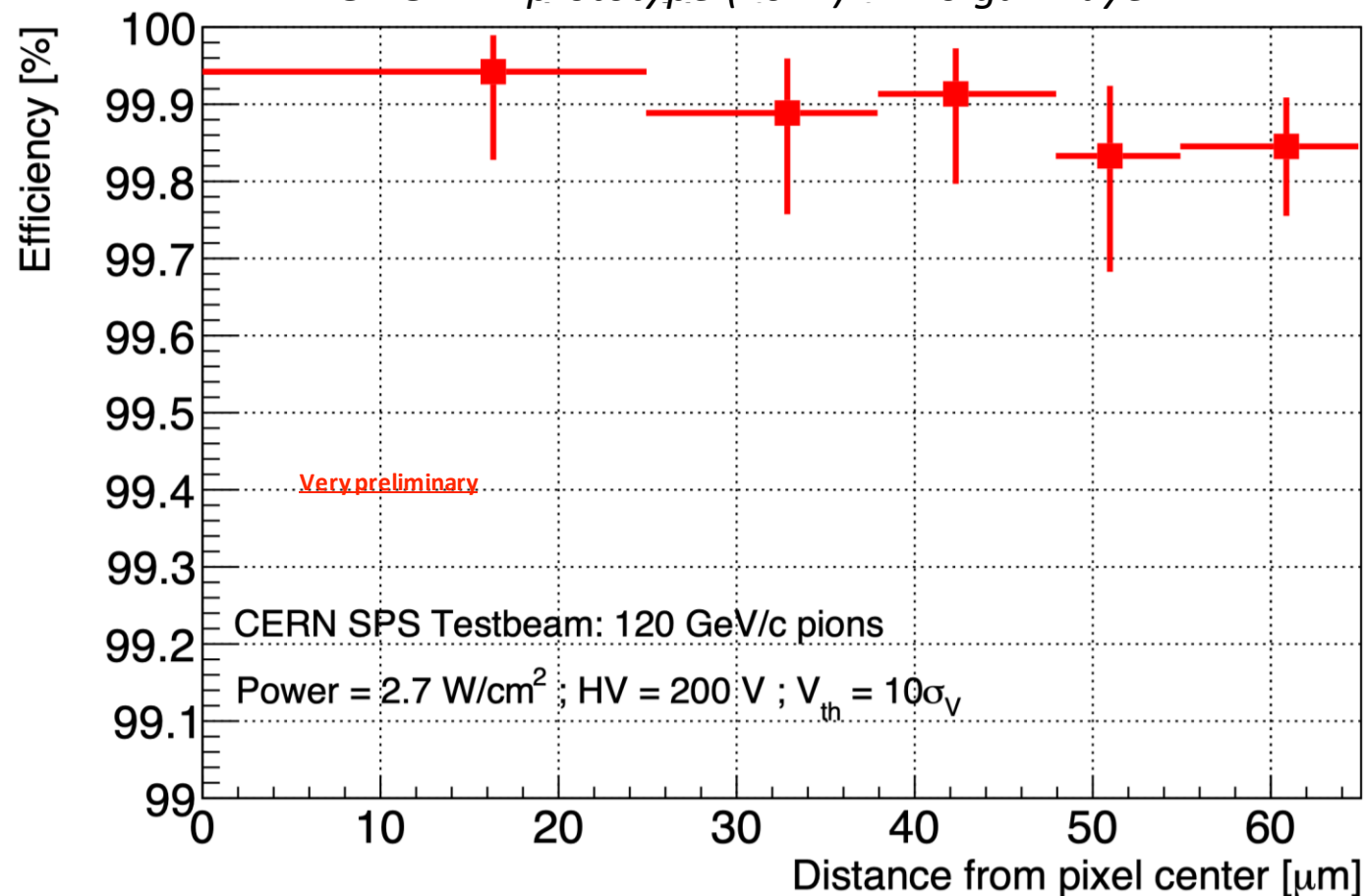
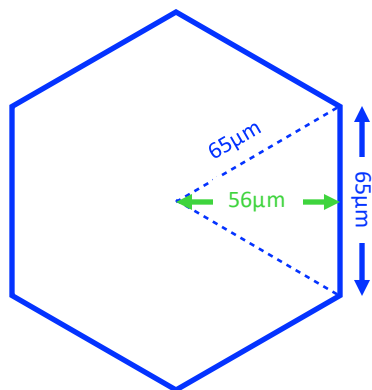
MONOLITH prototype (2022) — no gain layer



Full efficiency (yellow is 99.8%) in the two triangles unaffected by telescope resolution

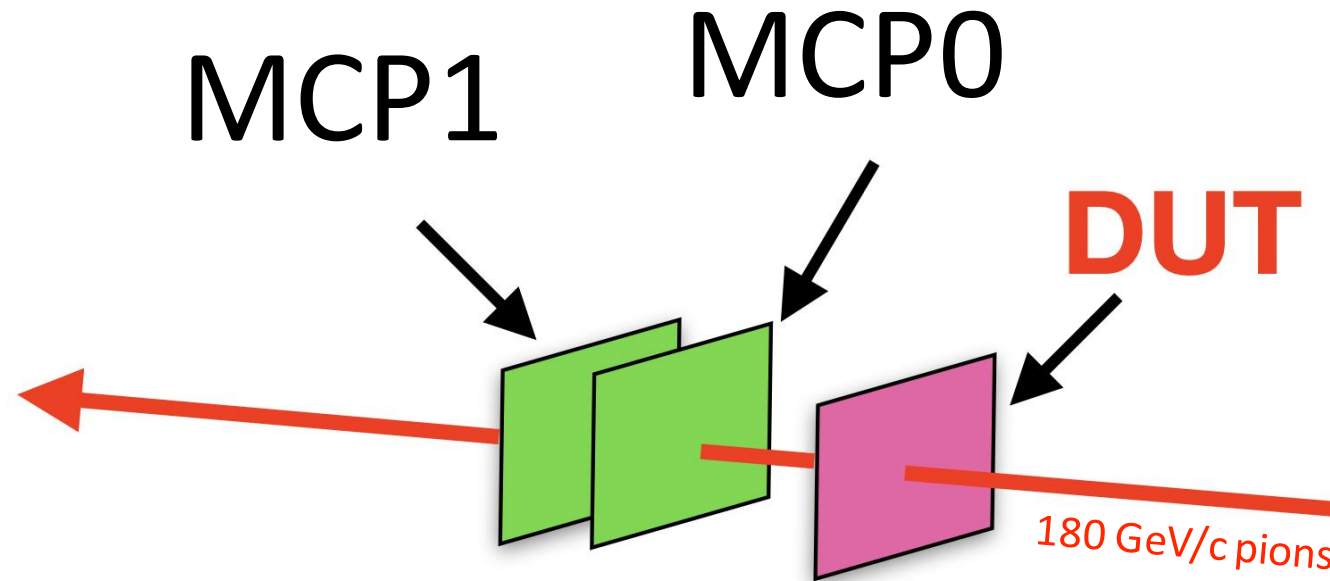
2022 prototype — no gain layer

MONOLITH prototype (2022) — no gain layer

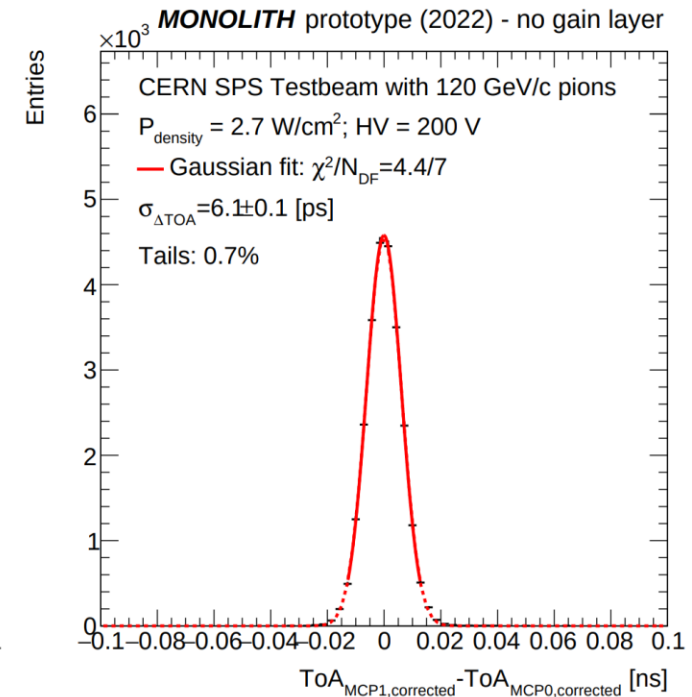
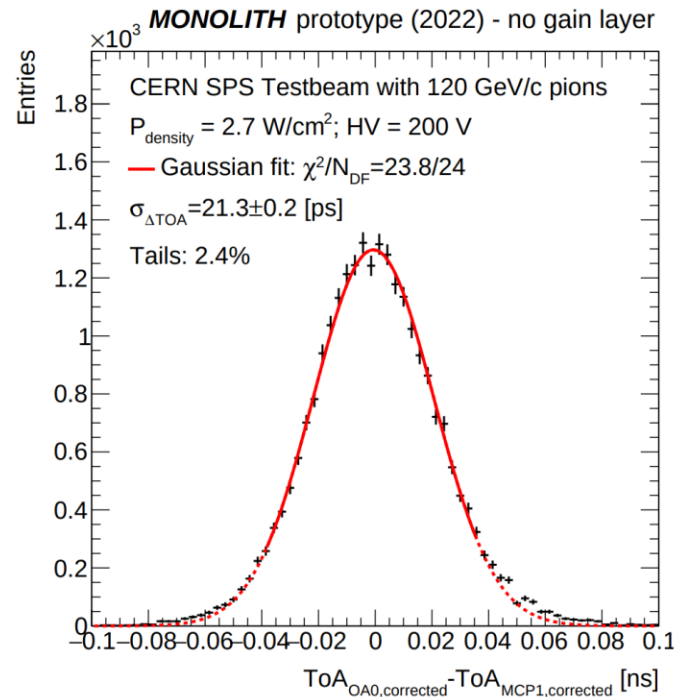
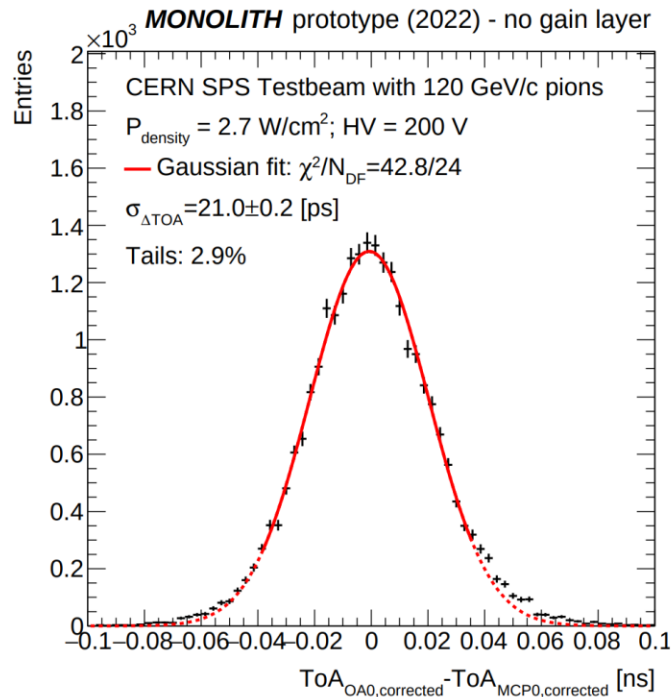


Efficiency $\approx 99.9\%$ even in the inter pixel region.

2022 prototype — no gain layer



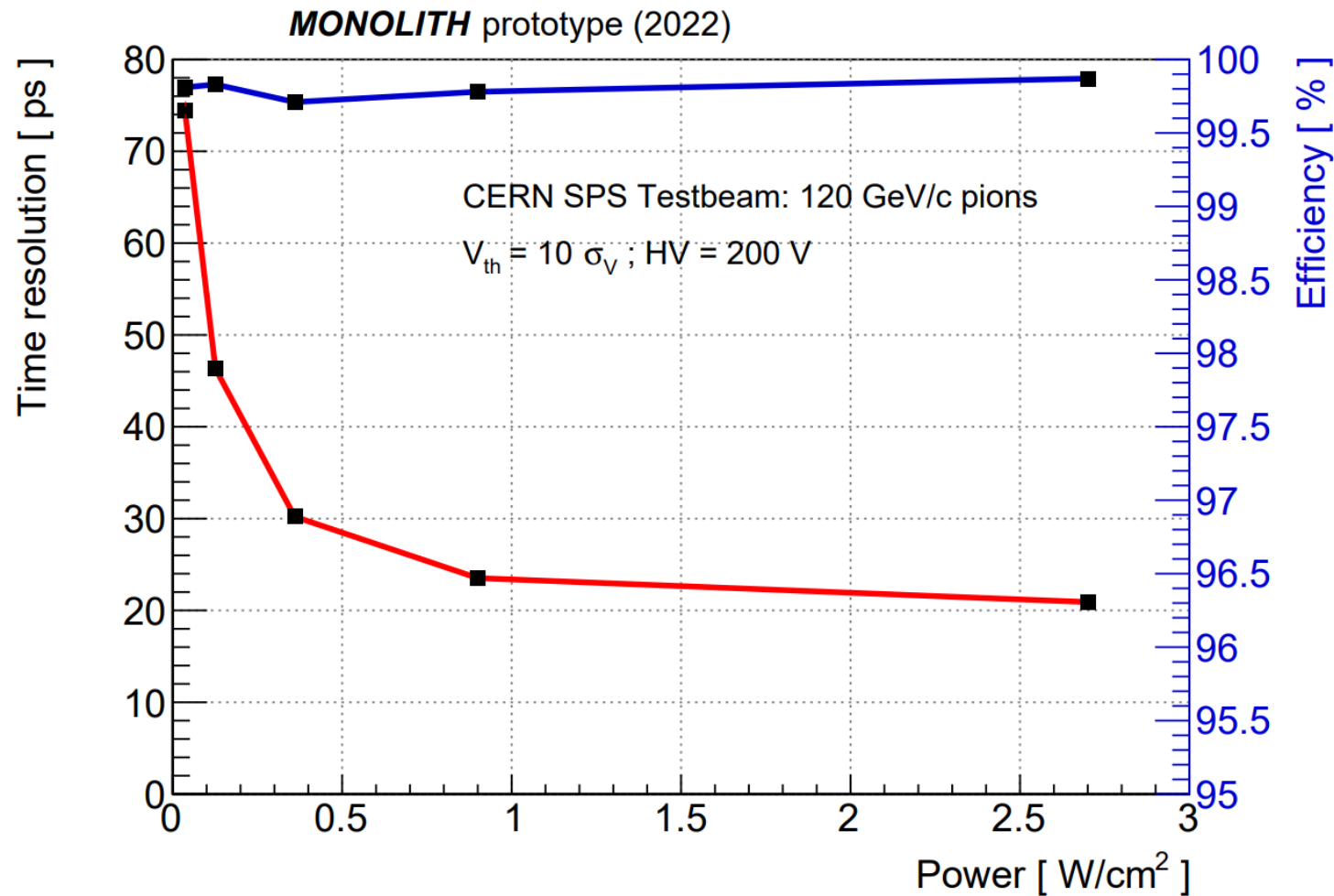
2022 prototype — no gain layer



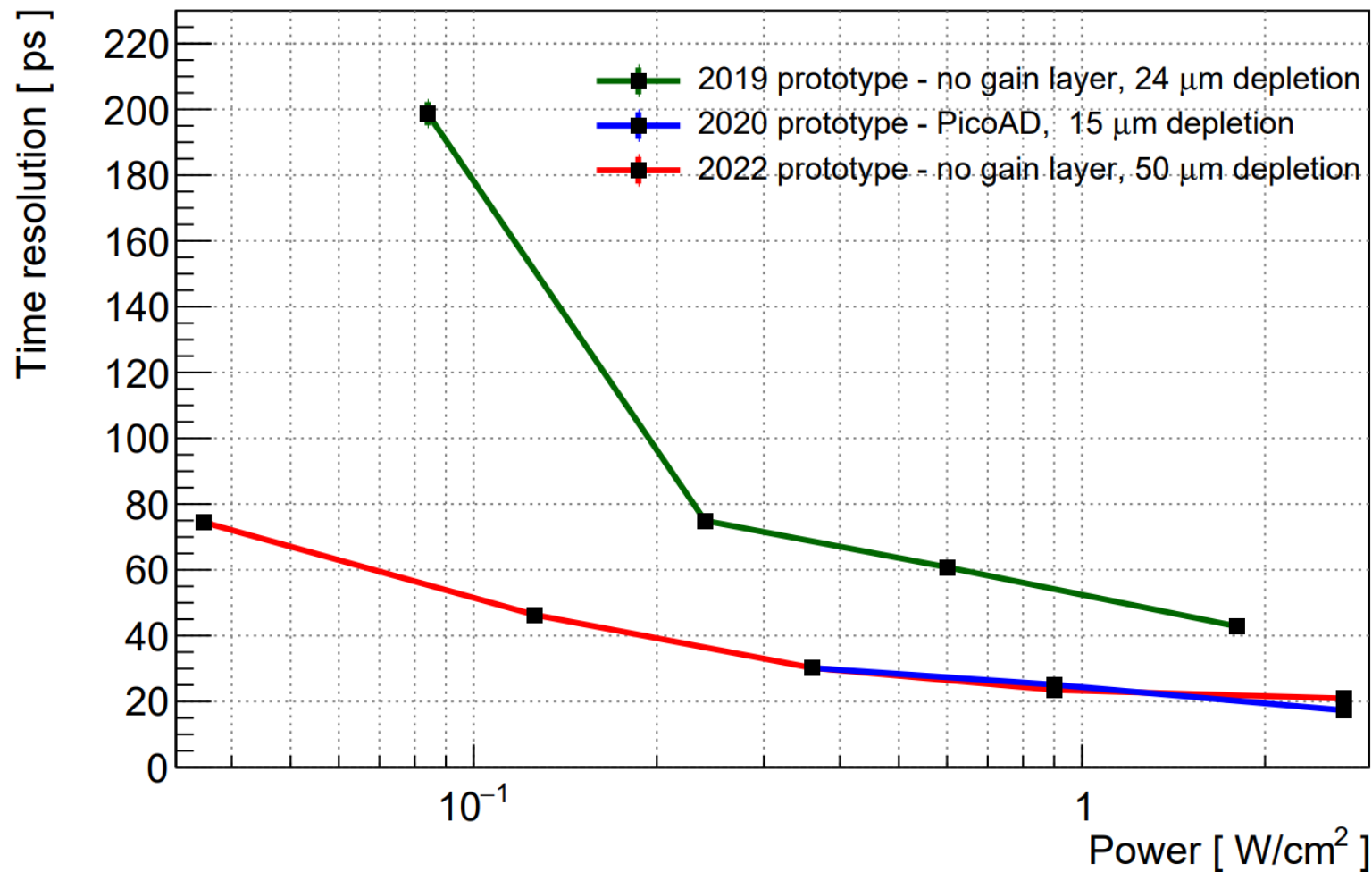
System results: MCP0 $\sigma_T = (3.6 \pm 1.5) \text{ ps}$
MCP1 $\sigma_T = (5.0 \pm 1.1) \text{ ps}$

$\sigma_T = (20.7 \pm 0.3) \text{ ps}$
with non-Gaussian tails of <3%

2022 prototype — no gain layer



Comparison between prototypes

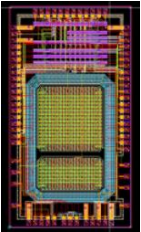


Monolithic SiGe BiCMOS for timing



Monolithic prototypes with SiGe BiCMOS

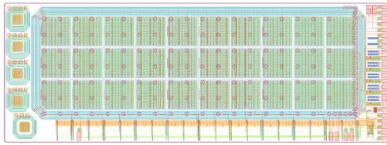
2016



200ps

- 1 and 0.5 mm² pixels
- Discriminator output

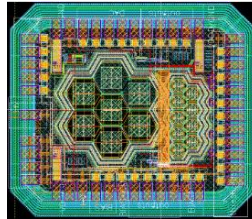
2017



110ps

- 30 pixels 500x500μm²
- 100ps TDC +I/O logic

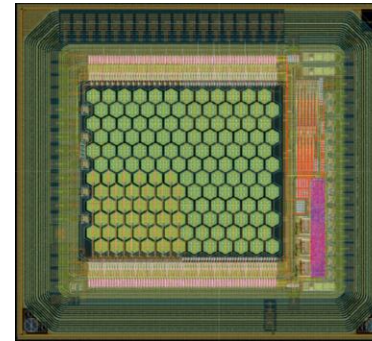
2018



50ps

- Hexagonal pixels 65μm and 130μm side
- Discriminator output

2019



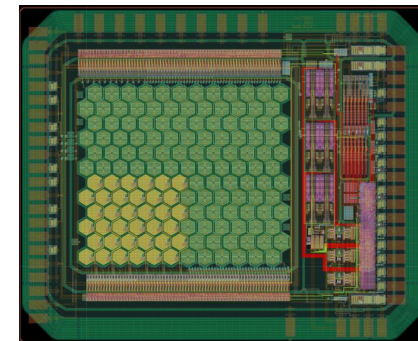
36 ps

- Hexagonal pixels 65μm side
- 30ps TDC +I/O logic
- Analog channels



PicoAD version
17 ps

2022



21 ps

- Hexagonal pixels 65μm side
- improved electronics
- 50μm epitaxial layer (350Ωcm)



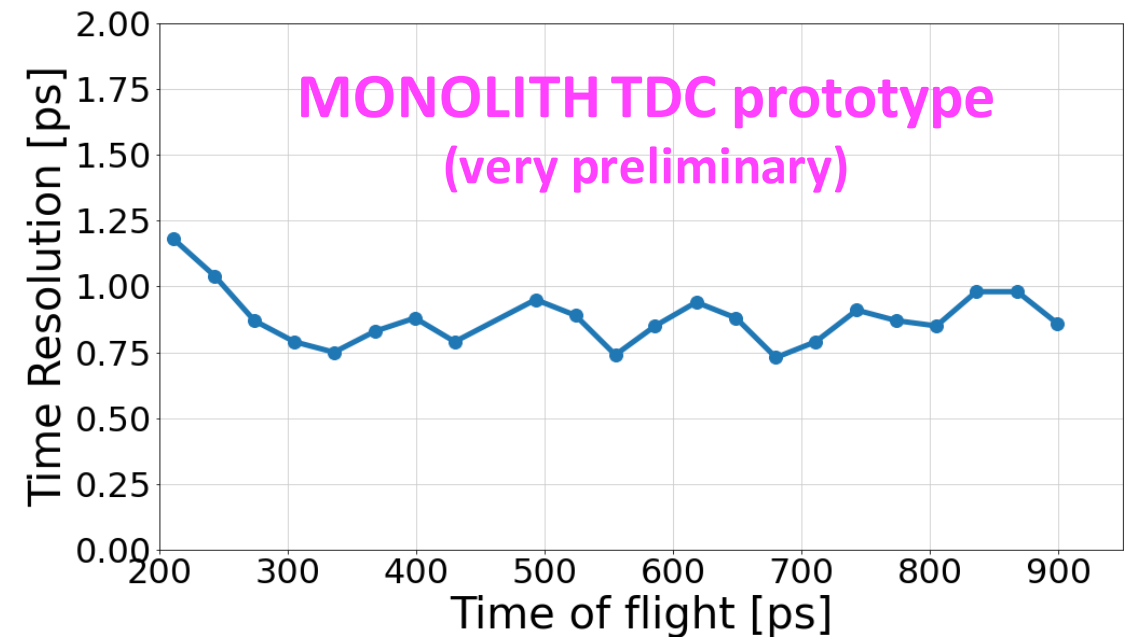
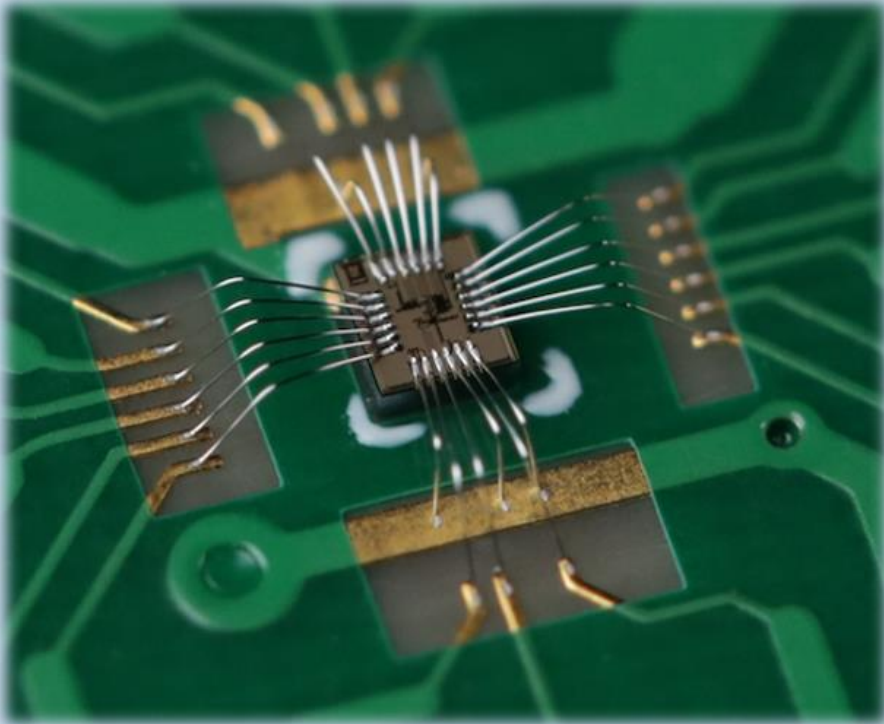
PicoAD version
In production

Sub-picosecond TDC

We are developing a sub-picosecond TDC based on a novel design (our patent[©] & more):



© R. Cardarelli, L. Paolozzi, P. Valerio and G. Iacobucci, European Patent Application / Filing - UGKP-P-001-EP, Europe Patent EP 18181123.3. 2 July 2018.



Standalone prototype still under test at UNIGE.
Integrated in MONOLITH 2022 monolithic ASIC.



Summary & Outlook

The **PicoAD[©]** Monolithic proof-of-concept prototype **works**. Testbeam provided:

- **Gain ≈ 20** for ^{55}Fe X-rays (space-charge effects); gain ≈ 60 -70 for mips.
- **Efficiency = 99.9 %** including inter-pixel regions
- **Time resolution $\sigma_t = (17.3 \pm 0.4)$ ps : 13 ps** at center and **25 ps** at pixel edge (although sensor not yet optimized for timing)

Ongoing activities include:

- Data analysis of 2nd prototype without gain layer: **(20.7 ± 0.3) ps**
- Optimization for timing of the PicoAD sensor design with TCAD to **achieve $\lesssim 10$ ps** (smaller pixel pitch; thicker drift layer; improved inter-pixel region)
- Development of **picosecond TDC** for fully monolithic chip
- Radiation hardness studies started in 2023 together with IHP and KEK

Deliverable of MONOLITH ERC project:

- Full-reticle chip in **Summer 2025** with 50 μm pitch and sub-10ps timing

Relevant papers



2019 prototype (no gain) testbeam:

<https://iopscience.iop.org/article/10.1088/1748-0221/17/02/P02019>

PicoAD proof of concept:

<https://iopscience.iop.org/article/10.1088/1748-0221/17/10/P10032>

2019 prototype + PicoAD testbeam:

<https://iopscience.iop.org/article/10.1088/1748-0221/17/10/P10040>

2022 prototype (no gain) testbeam:

<https://arxiv.org/abs/2301.12244>

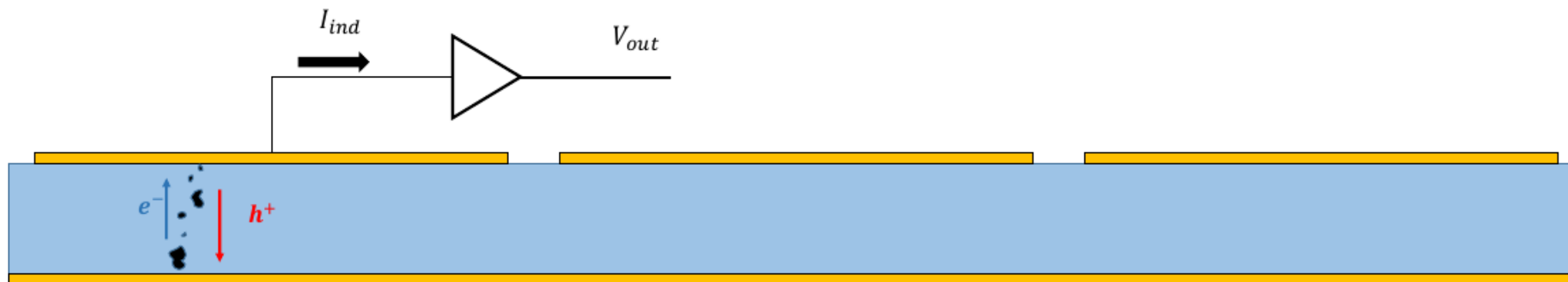
Backup

Precise timing with silicon

What are the main parameters that determine the time resolution of semiconductor detectors?

Induced current from the Shockley-Ramo's theorem:

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i}$$



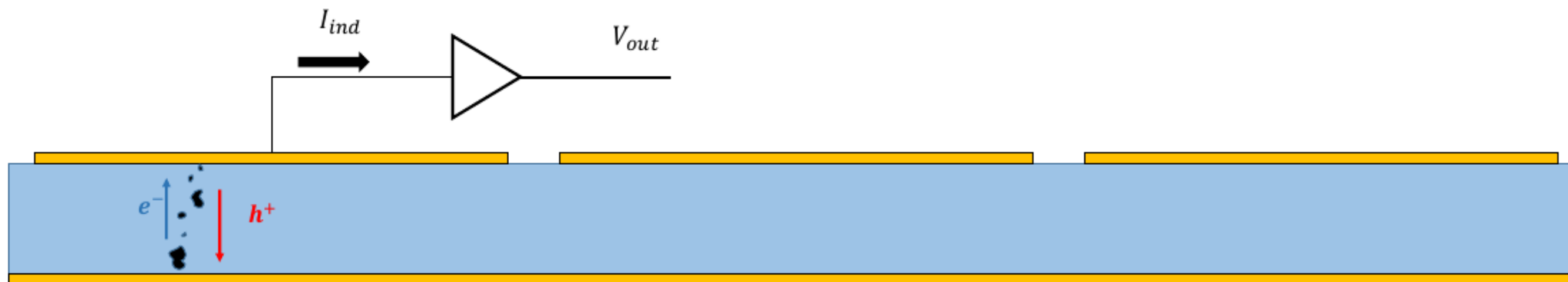
Precise timing with silicon

What are the main parameters that determine the time resolution of semiconductor detectors?

- Geometry and fields

Induced current from the Shockley-Ramo's theorem:

$$I_{ind} = \sum_i q_i \vec{v}_{drift,i} \cdot \vec{E}_{w,i}$$



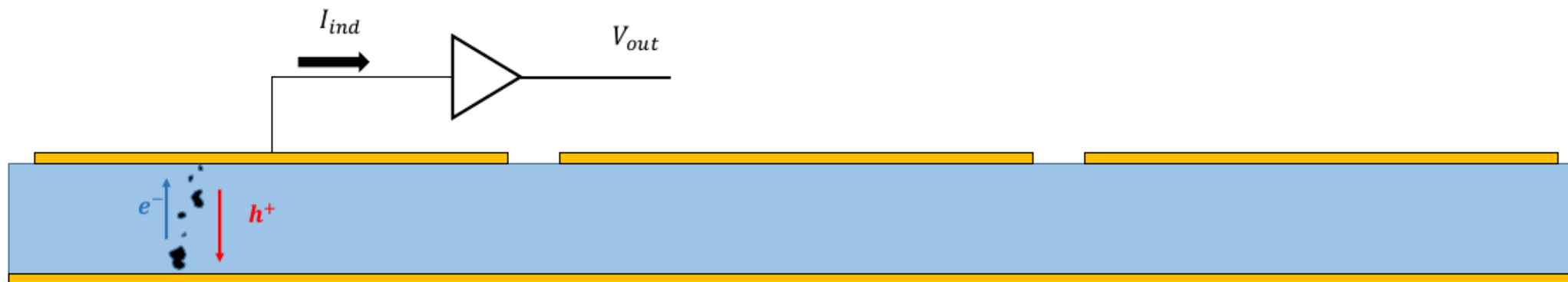
Precise timing with silicon

What are the main parameters that determine the time resolution of semiconductor detectors?

- Geometry and fields
- Charge collection noise

Induced current from the Shockley-Ramo's theorem:

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i}$$



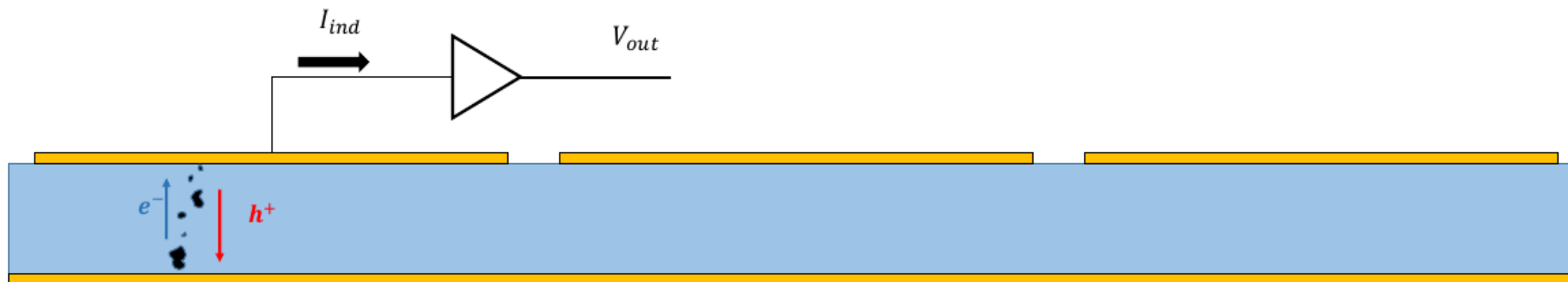
Precise timing with silicon

What are the main parameters that determine the time resolution of semiconductor detectors?

- Geometry and fields
- Charge collection noise
- Electronic noise

Induced current from the Shockley-Ramo's theorem:

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i}$$



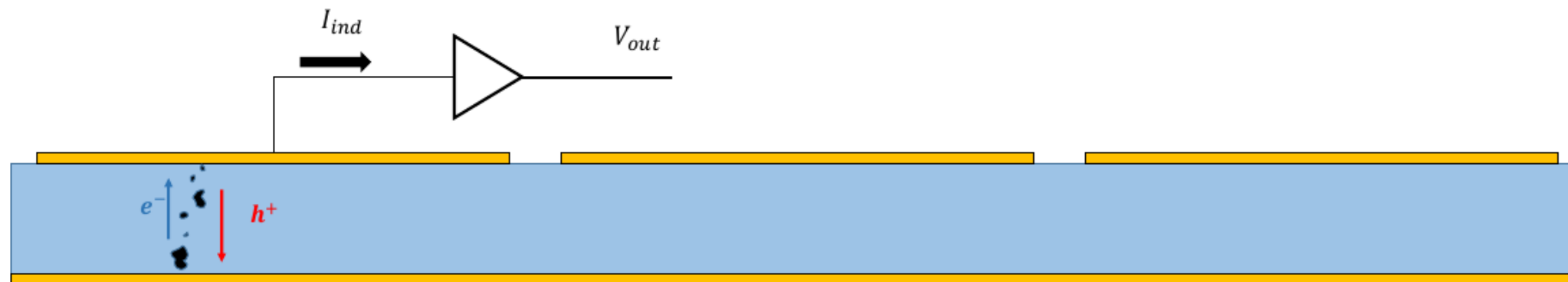
Precise timing with silicon

What are the main parameters that determine the time resolution of semiconductor detectors?

- Geometry and fields
- Charge collection noise
- Electronic noise
- Gain

Induced current from the Shockley-Ramo's theorem:

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i}$$



Title here

- Time Of Arrival (TOA) as a **time at constant fraction**
- Distributions after **time-walk correction**
- Distributions are **Gaussian**: only $\approx 2\text{-}4\%$ of entries in non-gaussian tails
- Simultaneous fit to extract time resolutions of the DUT, LGAD0, LGAD1

