4D Tracking – ASIC

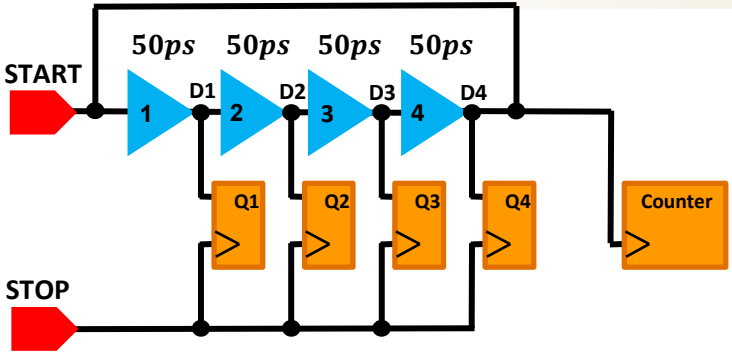
01/12/2022

Bojan Markovic

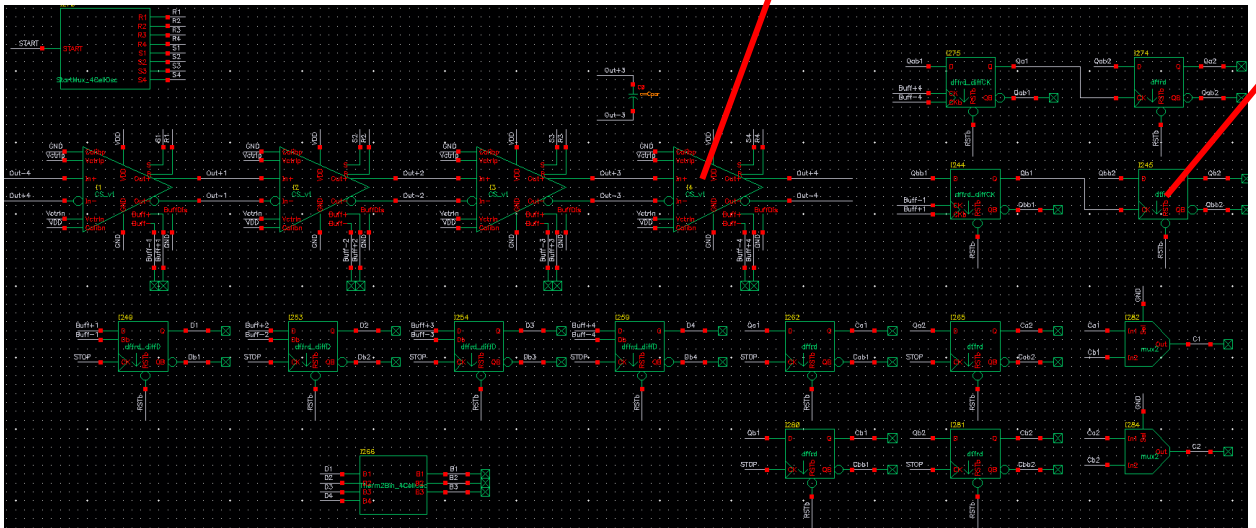
U.S. DEPARTMENT OF ENERGY
Office of Science

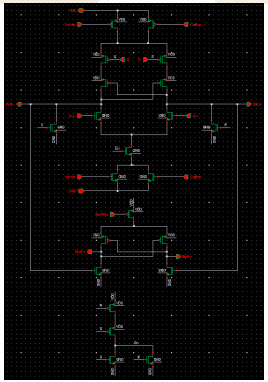
SLAC NATIONAL ACCELERATOR LABORATORY

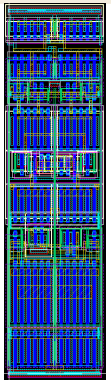
28nm TDC Initial Evaluation



- Schematic & Layout done (v1):



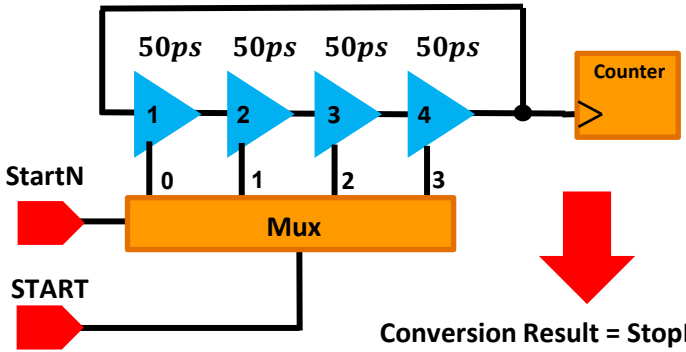




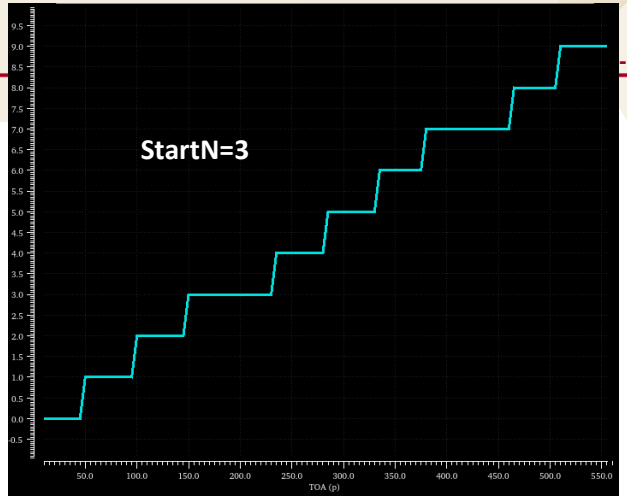
- Ideal/Code (VerilogA) Elements:

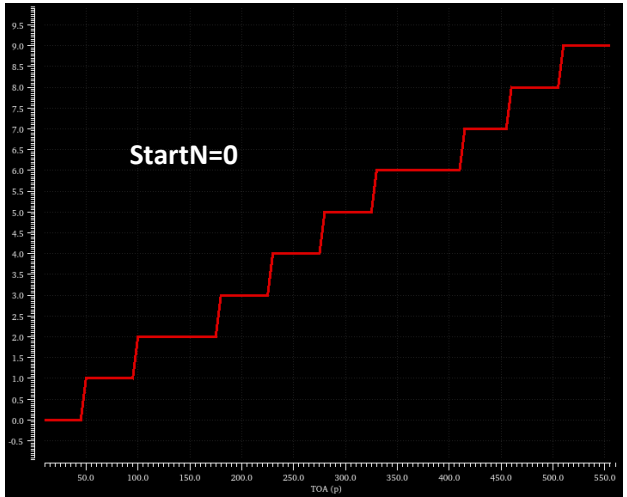
```
module dffrd(Q, QB, CK, D, RSTb);

inout Q; electrical Q;      // Q output
inout QB; electrical QB;  // Q bar output
input CK; voltage CK;  // Clock input (falling edge triggered)
input D; voltage D;          // D input
input RSTb; voltage RSTb;  // Reset input (immediately forces Q output low) (active low)

parameter real VDD = 0.9;                // voltage level of logic 1 (V)
parameter real VSS = 0;                  // voltage level of logic 0 (V)
parameter real vth = (VDD+VSS)/2;        // logic threshold level (V)
parameter real td = 5p from [0:inf);  // delay to start of output transition
parameter real Tr = 5p from [0:inf);  // rise time of output signals
parameter real Tf = 5p from [0:inf);  // fall time of output signals
parameter real ro = 1k from [0:inf);   // output resistance (ohm)

real out, outb;
electrical Qi, QBi;

analog begin
    @(initial_step) begin
        out = VSS;
        outb = VDD;
    end
    @(cross(V(CK) - vth, -1)) begin
        if (V(D) > vth && V(RSTb) > vth) begin
            out = VDD;
            outb = VSS;
        end else begin
            out = VSS;
            outb = VDD;
        end
    end
    @cross(V(RSTb) - vth);
    if (V(RSTb) < vth) begin
        out = VSS;
        outb = VDD;
    end
    V(Qi) <+ transition( out, td, Tr, Tf );
    V(QBi) <+ transition( outb, td, Tr, Tf );
    V(Q,Qi) <+ I(Q,Qi)*ro;
    V(QB,QBi) <+ I(QB,QBi)*ro;
end
endmodule
```

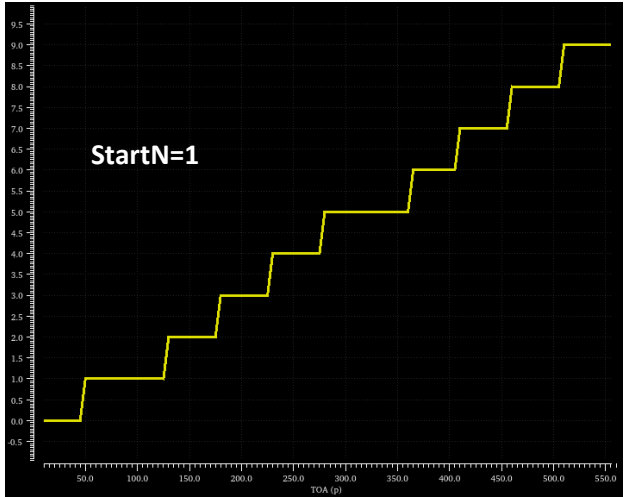
28nm TDC Initial Evaluation



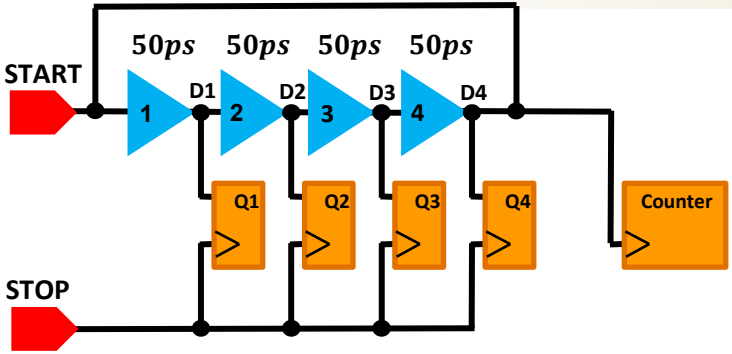
Conversion Result = StopBin - StartN







Counter Metastability/Timing Issue



1 1 0 0

Thermometric to Binary

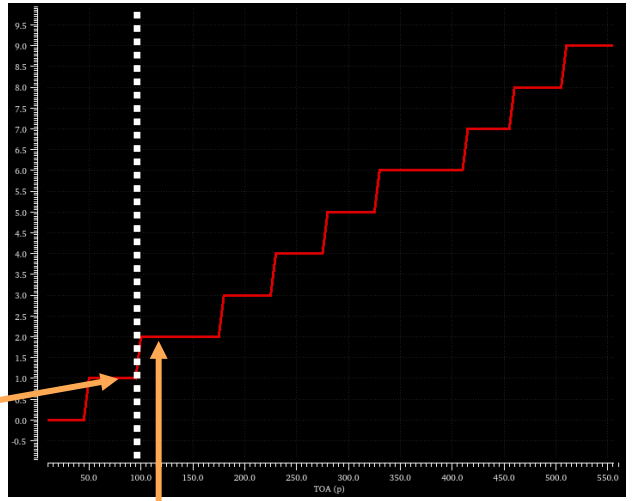
100

00

Binary to Dec

10000

1



1 1 1 0

Thermometric to Binary

010

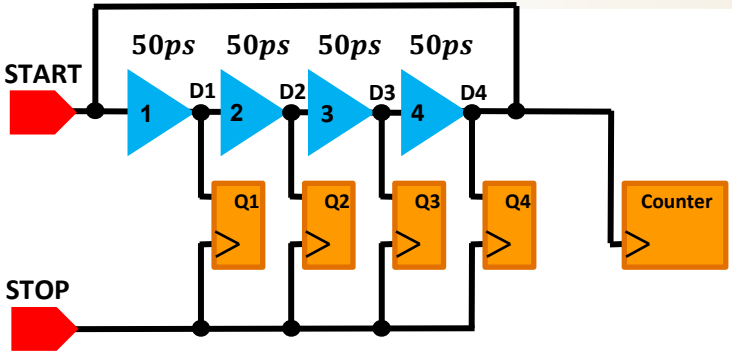
00

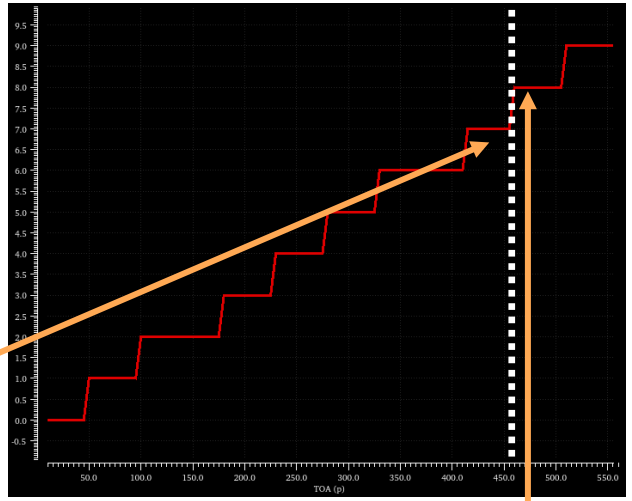
Binary to Dec

01000

2

Counter Metastability/Timing Issue





0 0 0 1 00

Thermometric to Binary

111

Binary to Dec

11100 → 7

0 0 0 0 10

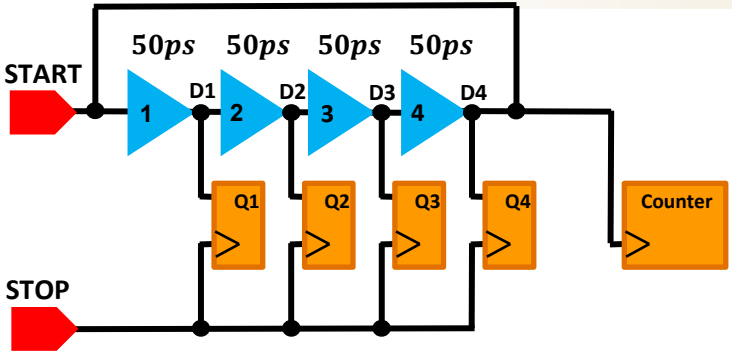
Thermometric to Binary

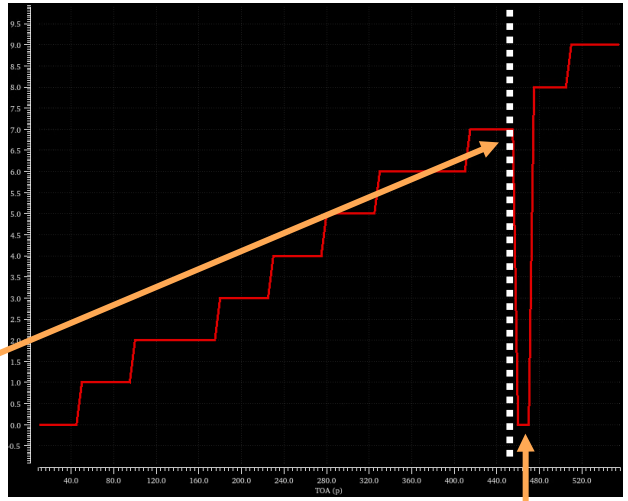
000

Binary to Dec

00010 → 8

Counter Metastability/Timing Issue





0 0 0 1 00

Thermometric to Binary

111

Binary to Dec

11100 → 7

0 0 0 0 00

Thermometric to Binary

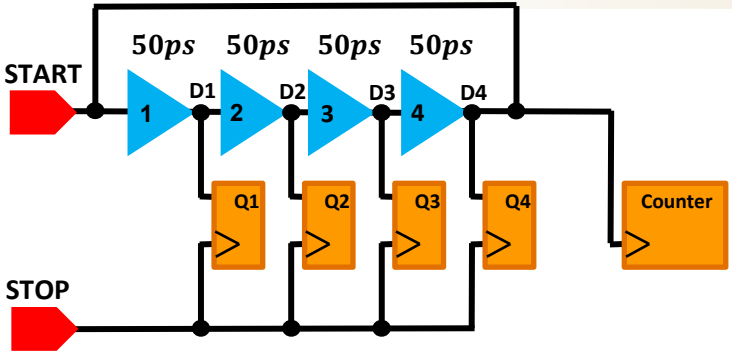
000

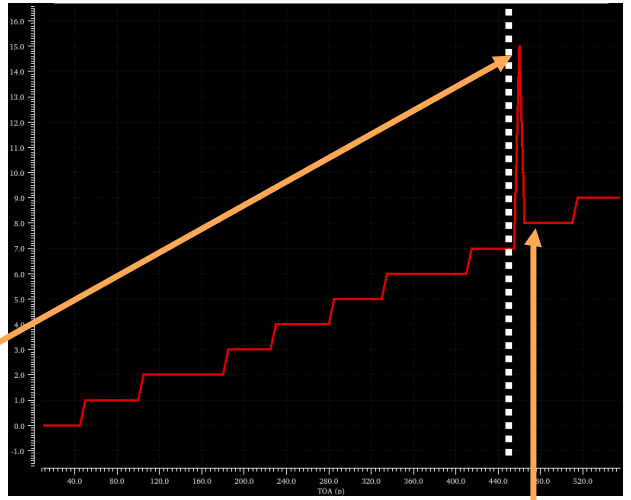
Binary to Dec

00000 → 0

Counter Metastability/Timing Issue

TID-ID SLAC





0 0 0 1 10

Thermometric to Binary

111

Binary to Dec

11110 → 15

0 0 0 0 10

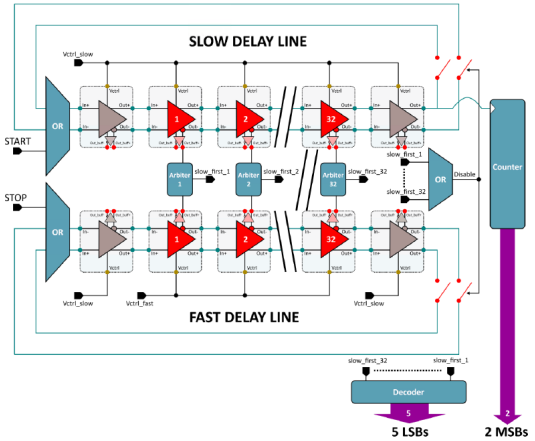
Thermometric to Binary

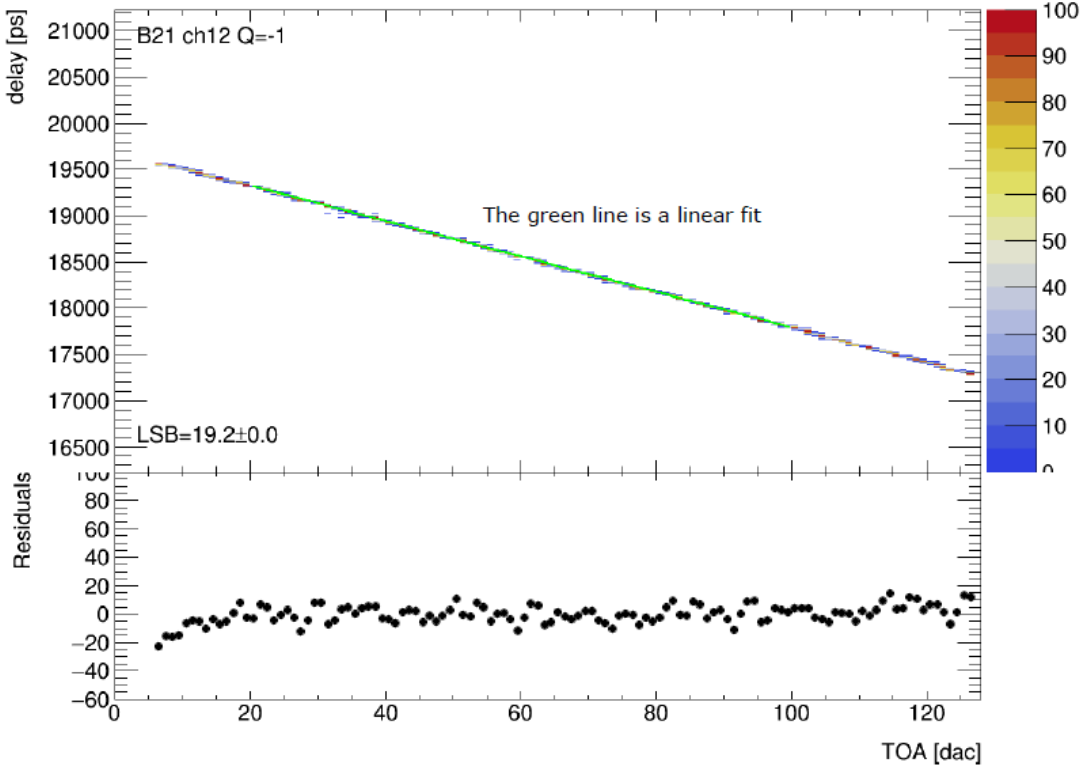
000

Binary to Dec

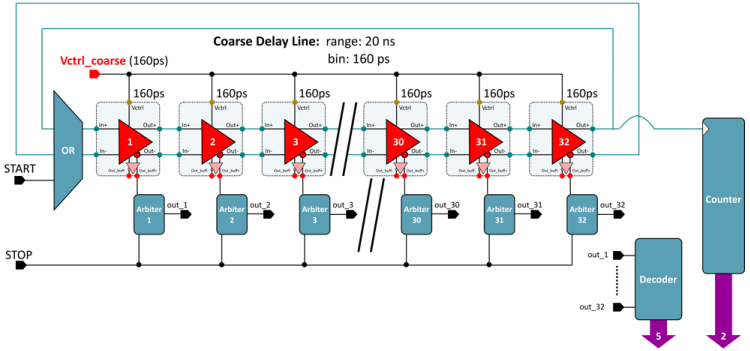
00010 → 8

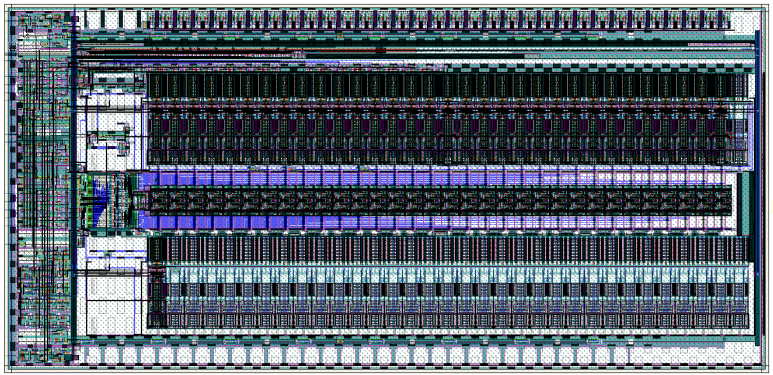
HGTD Altiroc TOA Non-Linearity

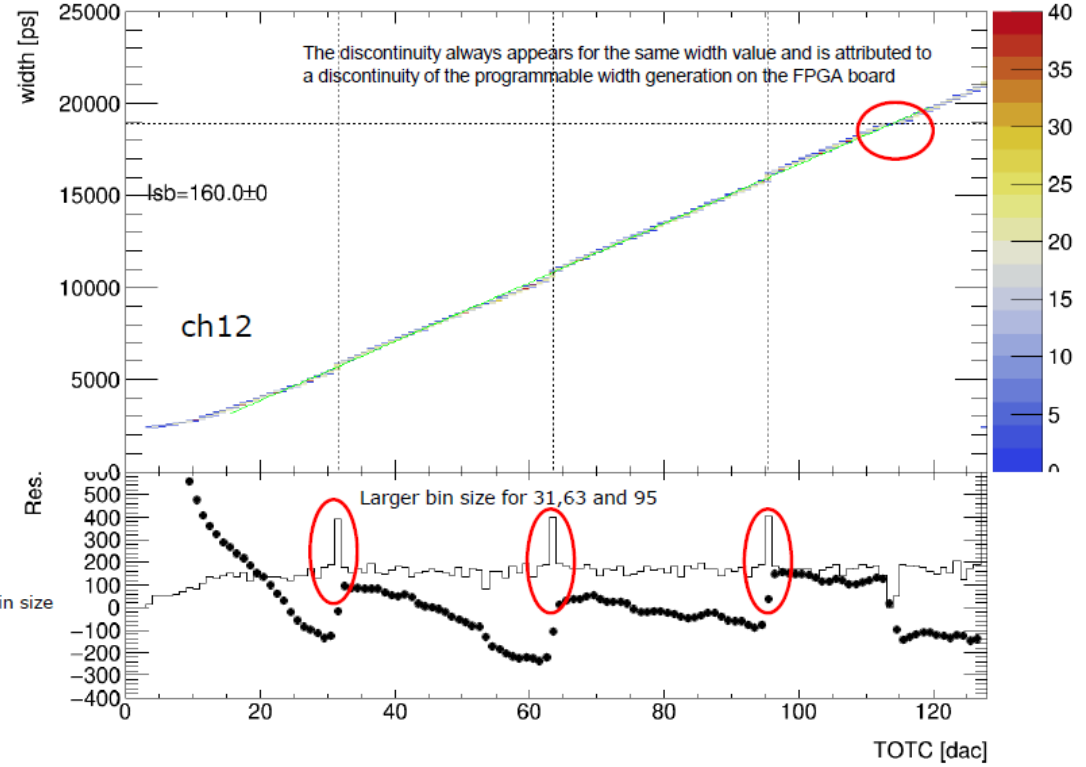




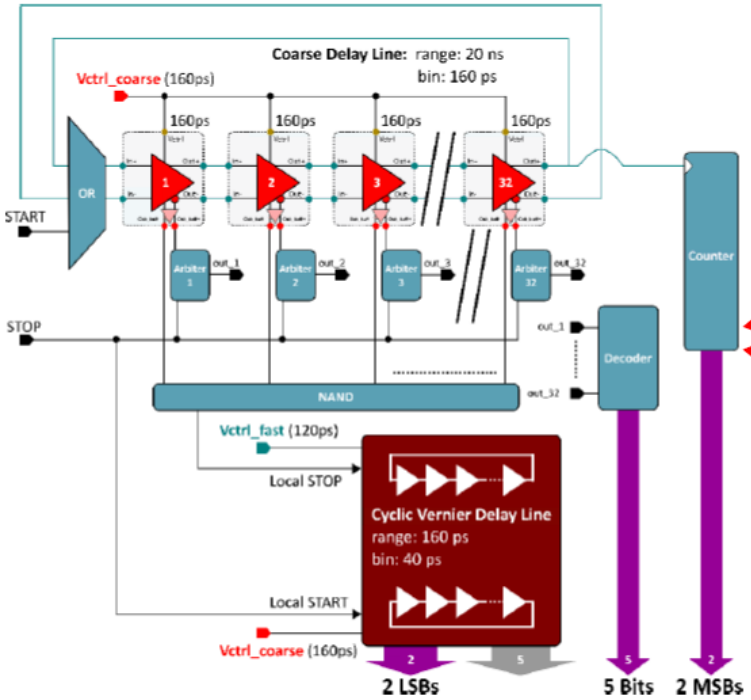
HGTD Altiroc TOT Non-Linearity

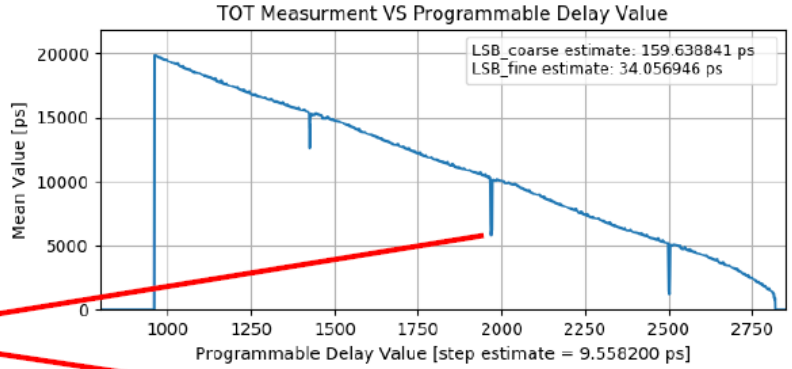






HGTD Altiroc TOT – Counter Issue

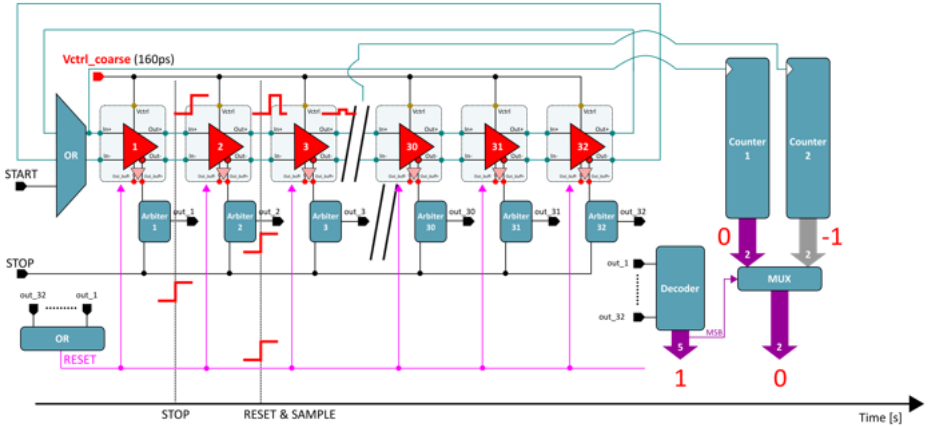


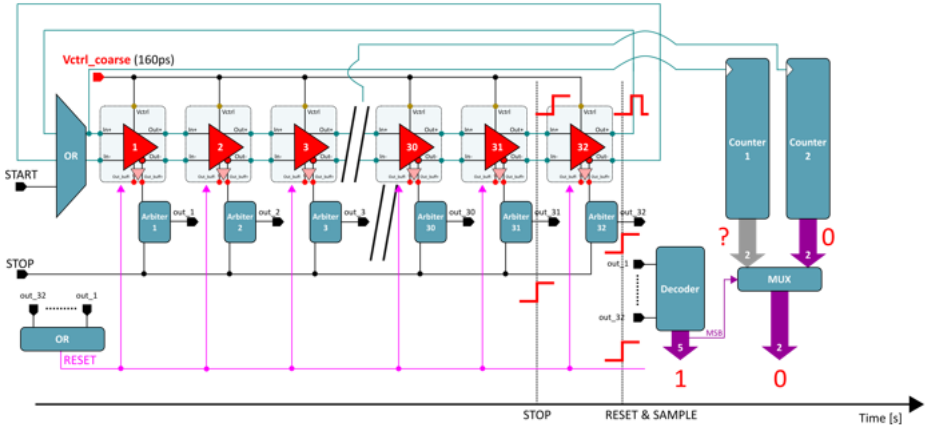


- Due to counter not finishing the counting of the pulse / metastability

Fixed in the new version

Altiroc Counter Issue: Two Counters Solution





- Issue is present when START signal circulating within the delay line is close to the counter when STOP signal arrives;
- The delay line sampling decoder provides the position of the START signal within the delay line in the instant of STOP arrival.

- With two counters positioned at the beginning and at the middle of delay line, and leveraging the knowledge of the START signal position provided by the delay line sampling, it is possible to avoid sampling the counter at risk of metastable behavior.
- Two counter solution implemented both in the coarse delay line and Vernier delay line TDC.