4D Tracking – ASIC

12/08/2021

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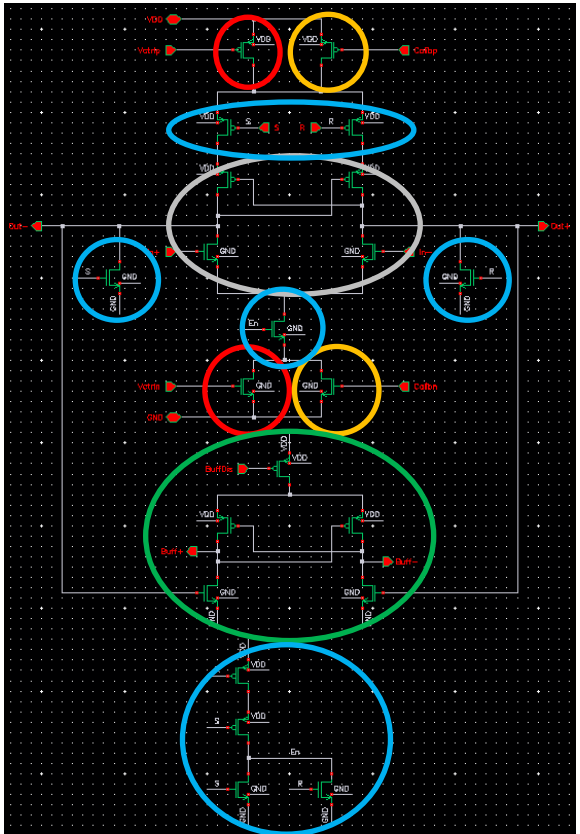
Office of Science

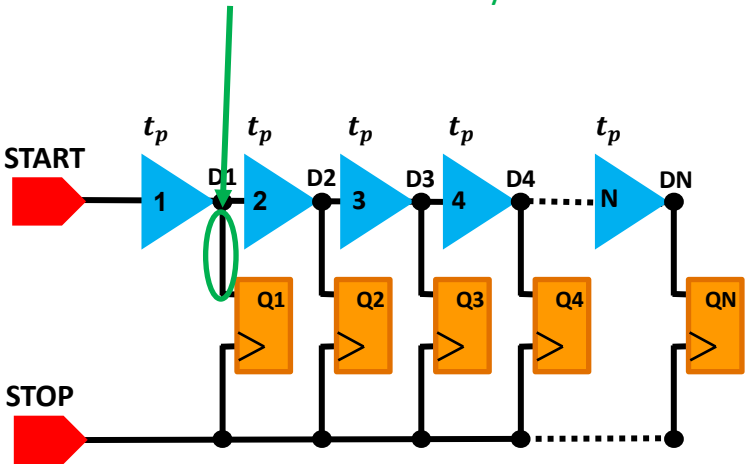
SLAC NATIONAL ACCELERATOR LABORATORY

Voltage-Controlled Delay Cell

- Current-Starved Delay Cell:



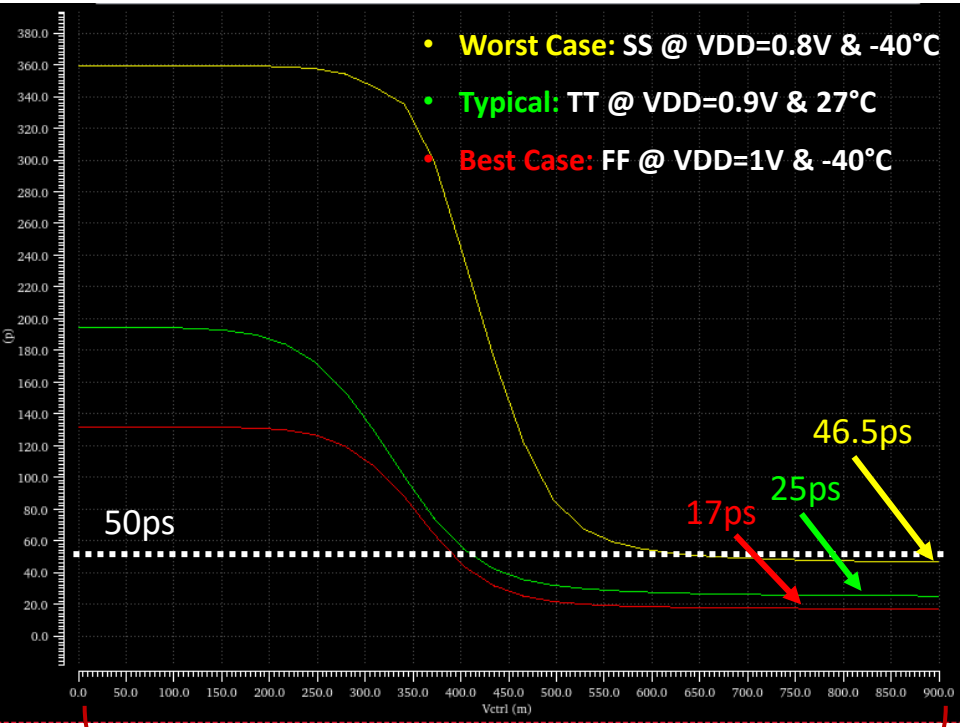
- DCVSL core transistors
- Voltage Controlled Delay
- Calibration / Trimming
- Cell Logic Controls (Disable; Set; Reset)
- Output Buffers for access to the delay line state



Voltage-Controlled Delay Cell

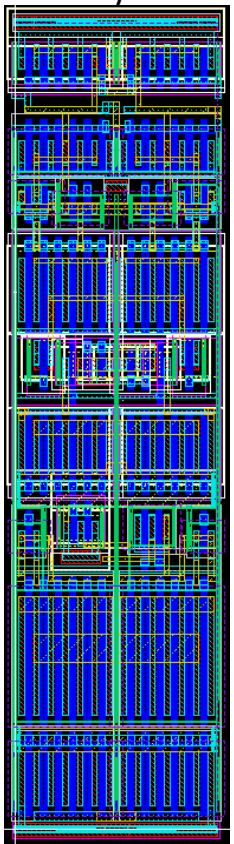
TID-ID SLAC

- Layout Parasitics Extracted (RCX) Simulation:

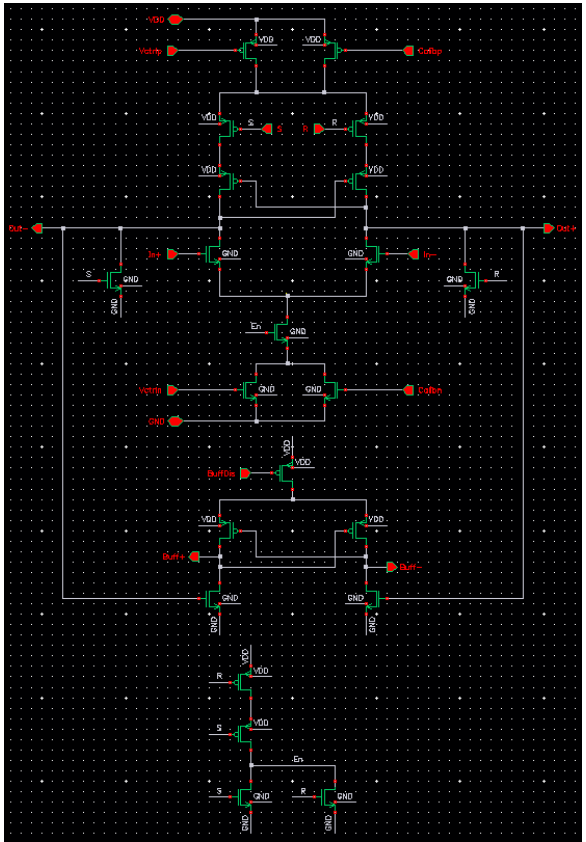


Delay-Control Voltage

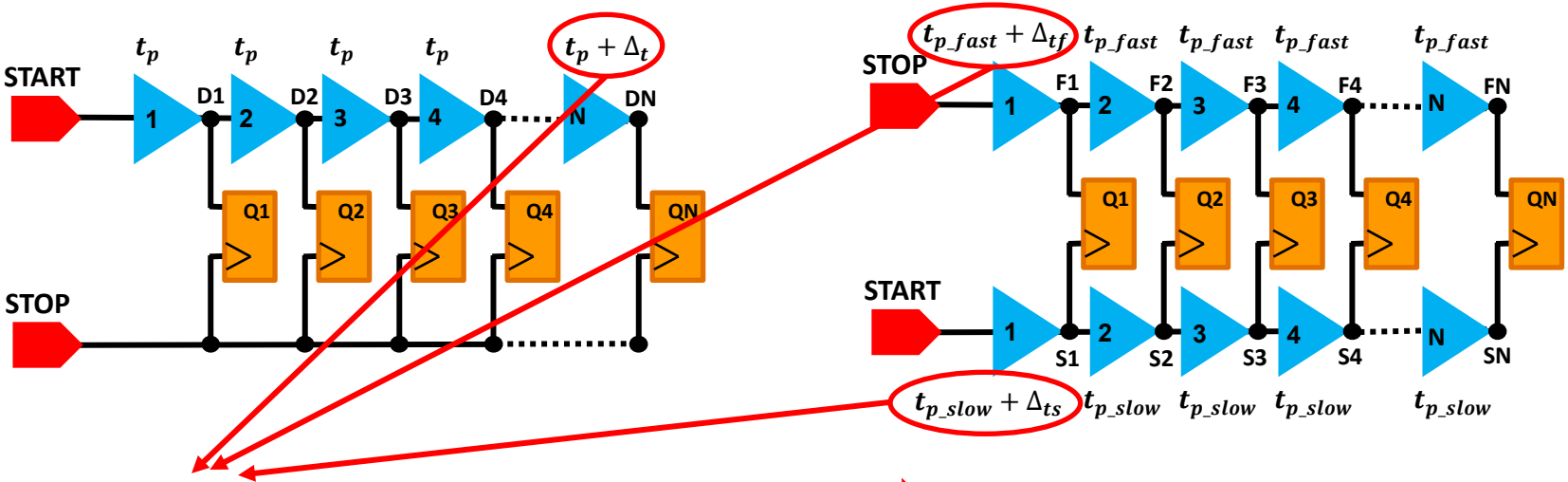
- Layout:



- Schematic:



Delay Line Non-Linearity



Actual delay of each cell differs from the nominal value

Non-Linearity of TDC conversion characteristics

- ❑ Statistical Mismatch
- ❑ Systematic Mismatch

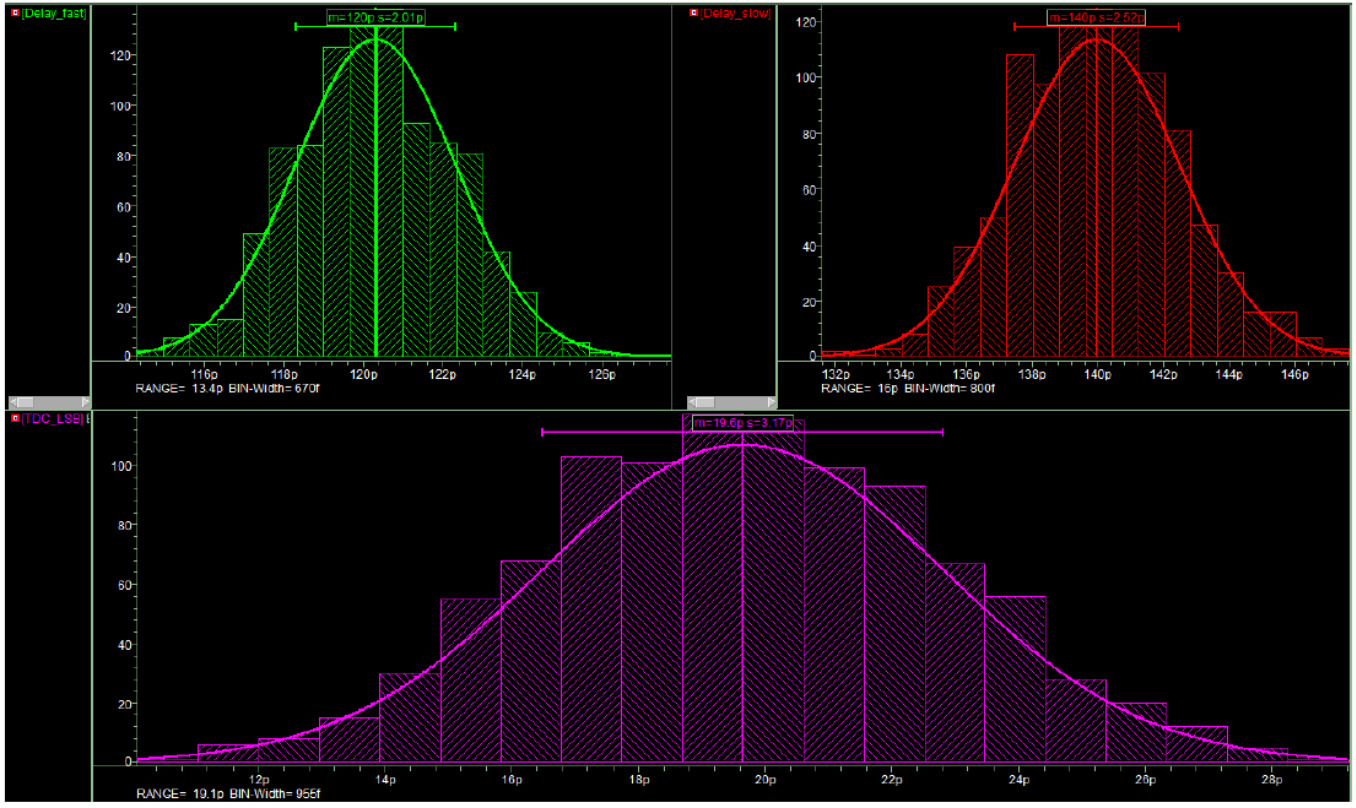
Ideal Converter:

Real Converter:

Statistical Mismatch

TID-ID SLAC

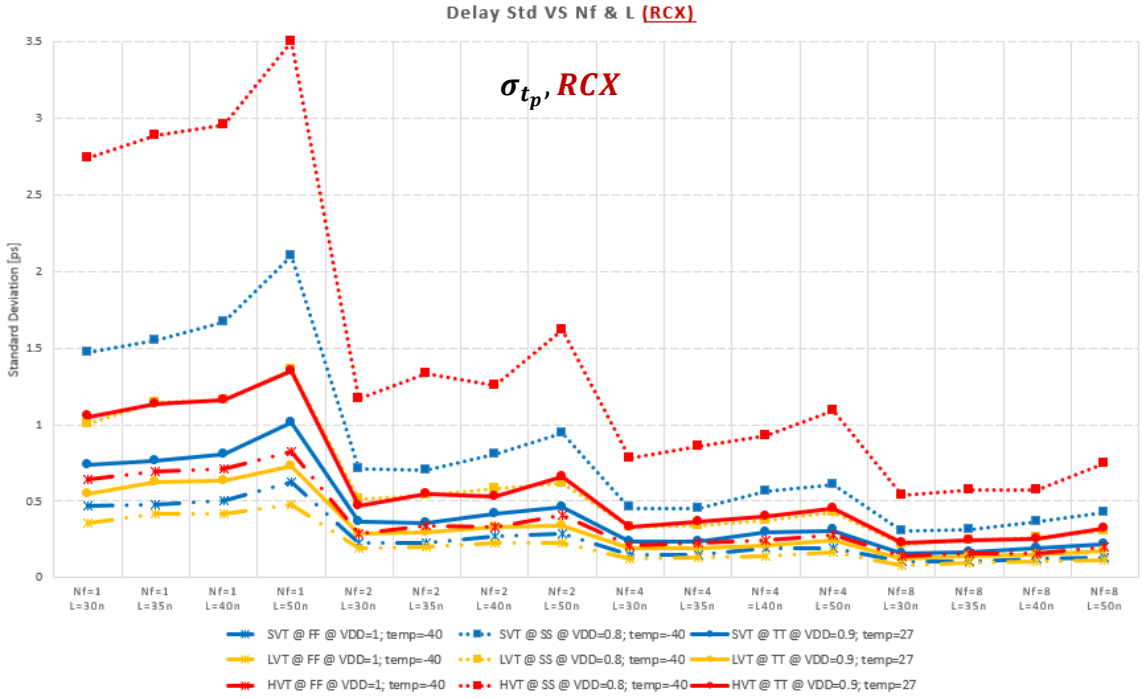
Mismatch (Monte Carlo Simulation): HGTD Altiroc (130nm)

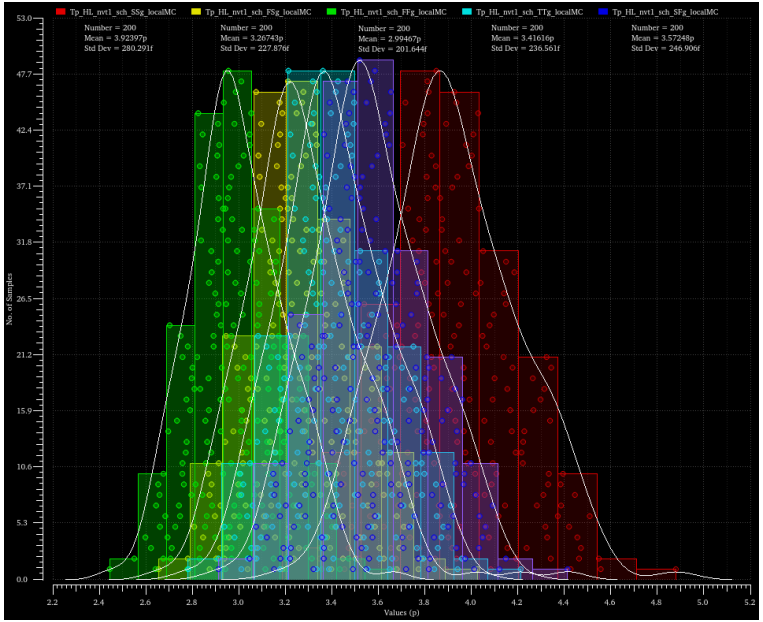


Statistical Mismatch

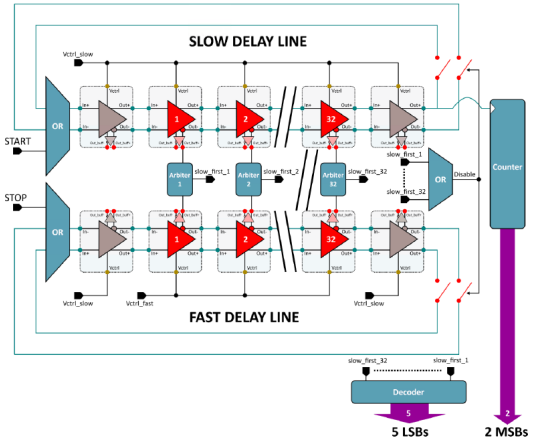
TID-ID SLAC

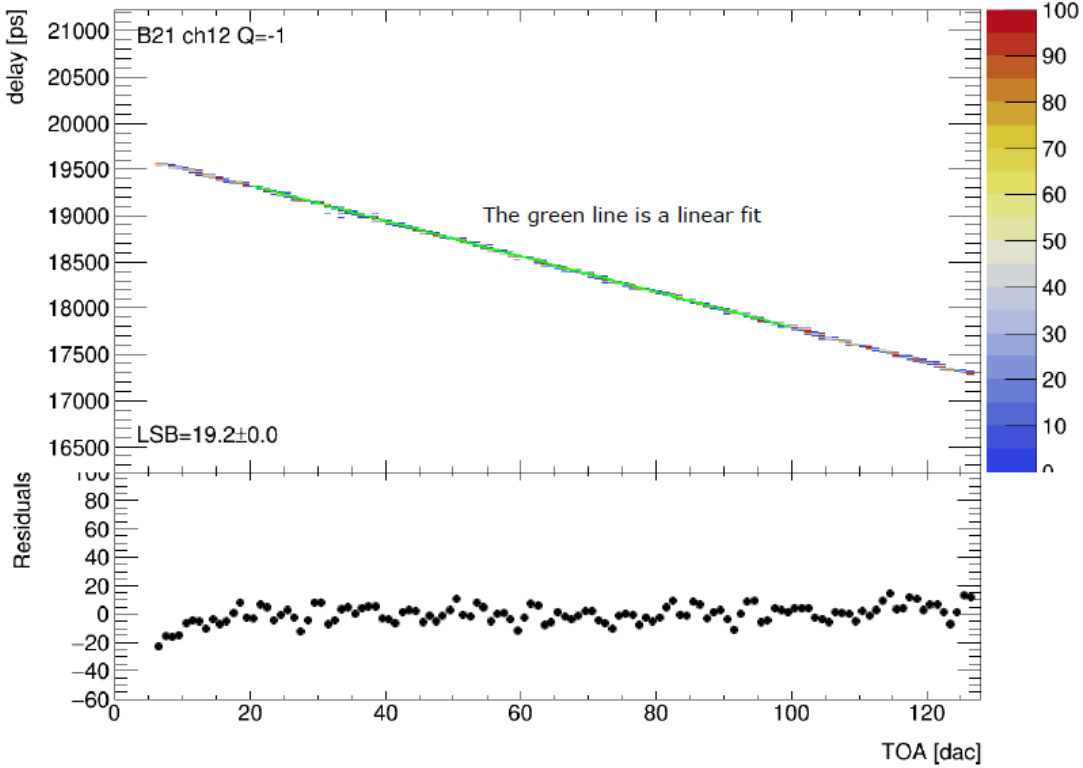
Mismatch (Monte Carlo Simulation): 28nm



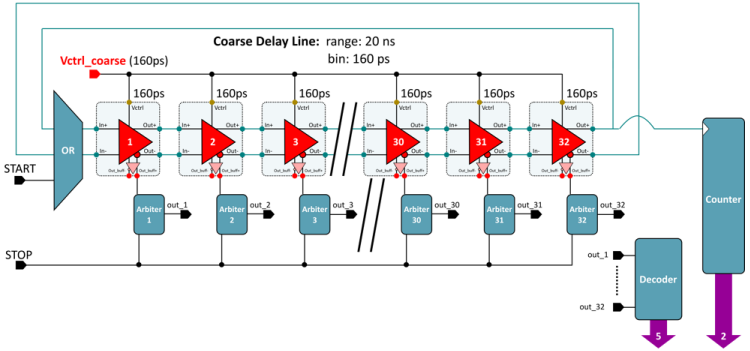


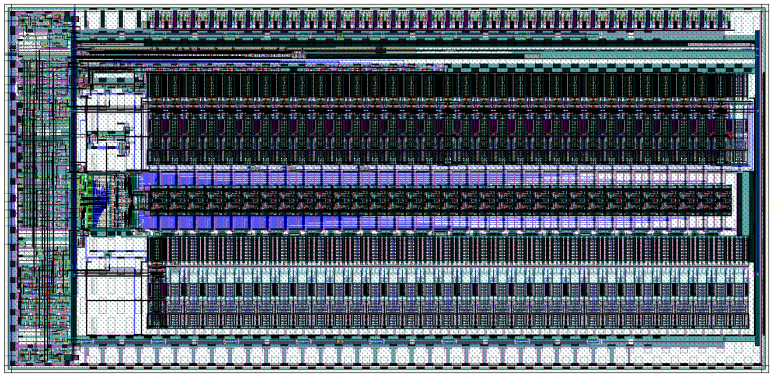
HGTD Altiroc TOA Non-Linearity

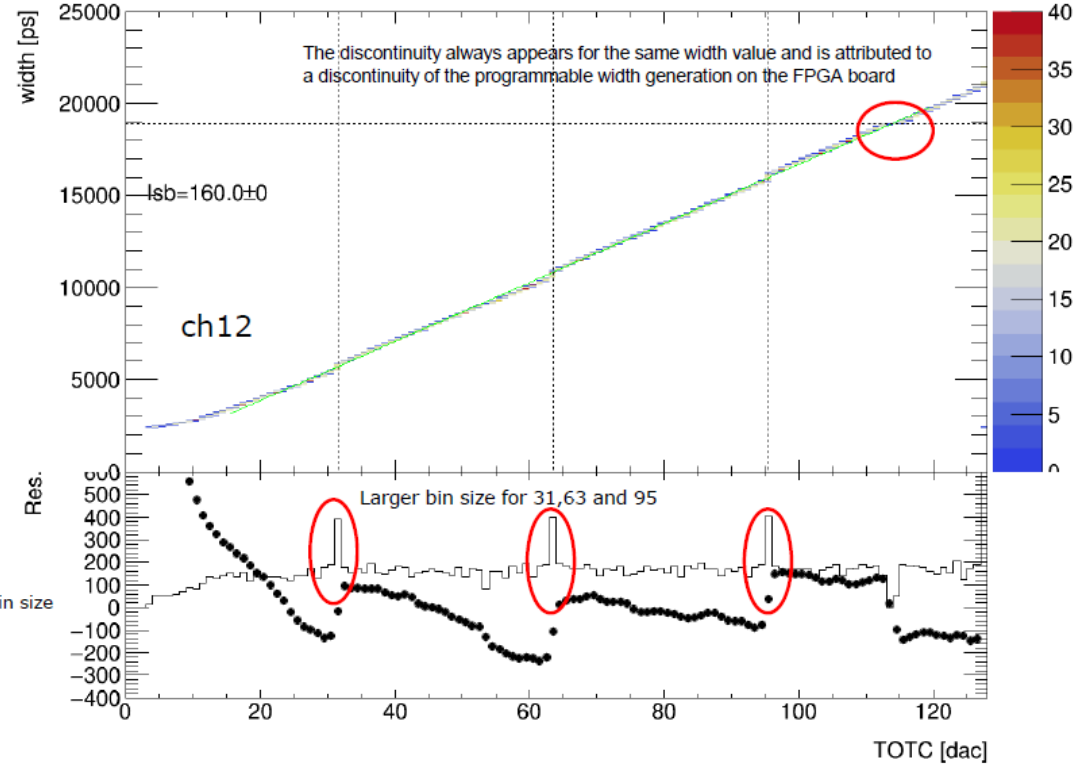




HGTD Altiroc TOT Non-Linearity



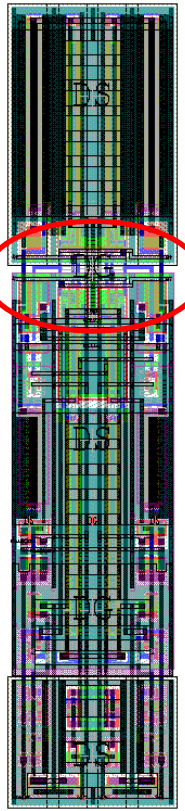


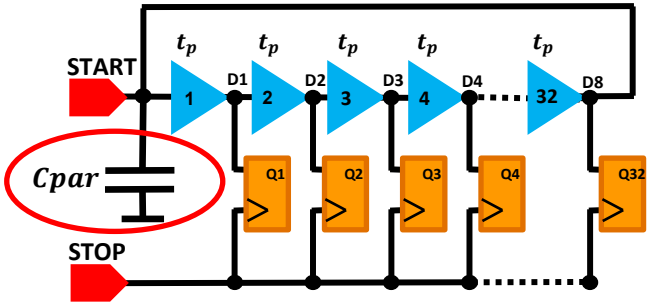


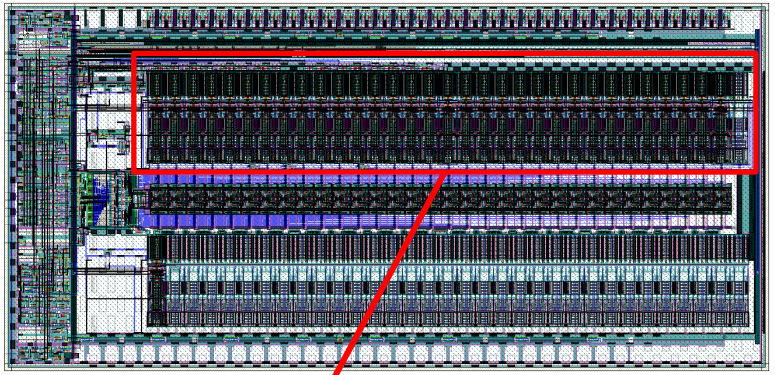
HGTD Altiroc TOT Non-Linearity – Systematic Mismatch

TID-ID SLAC

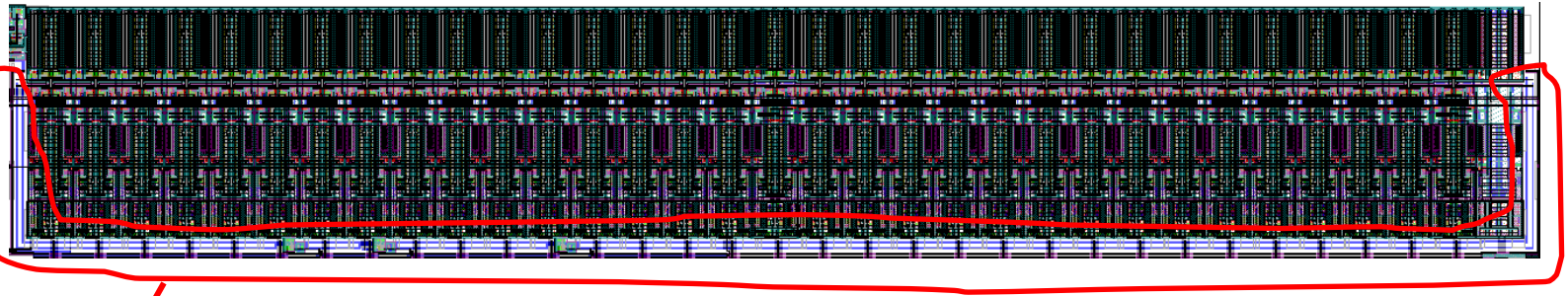
Delay Cell Layout:







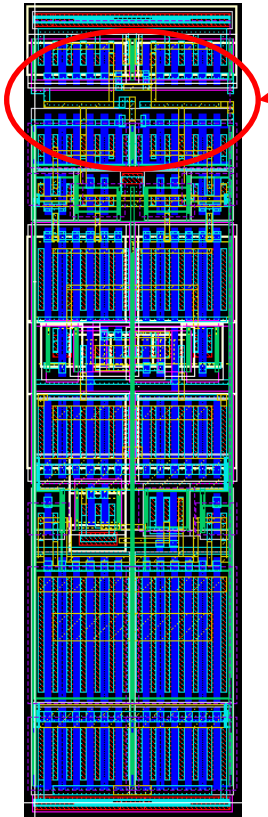
Core Transistors



Cell 32 (last Cell) has a higher load (parasitic capacitance) than other cells in the delay line

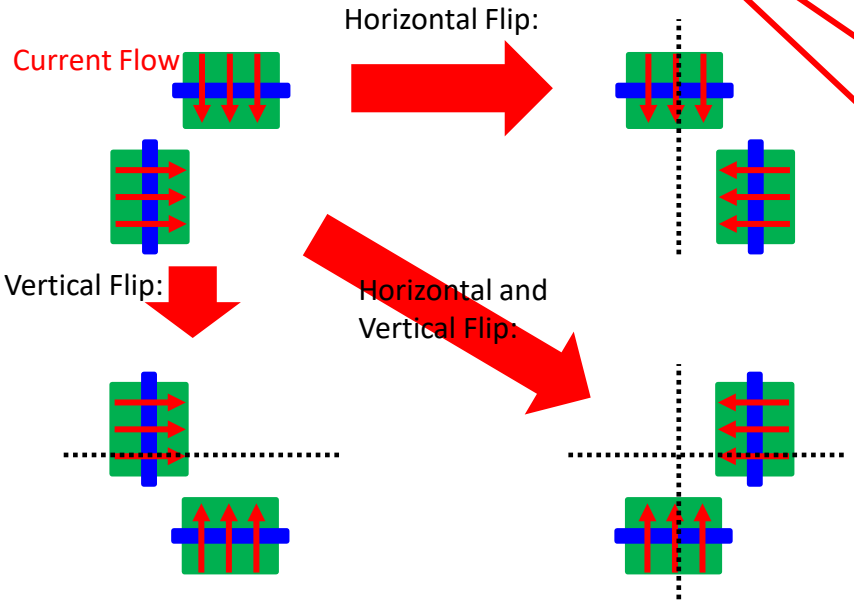
28nm Delay Cell Layout

Delay Cell Layout:

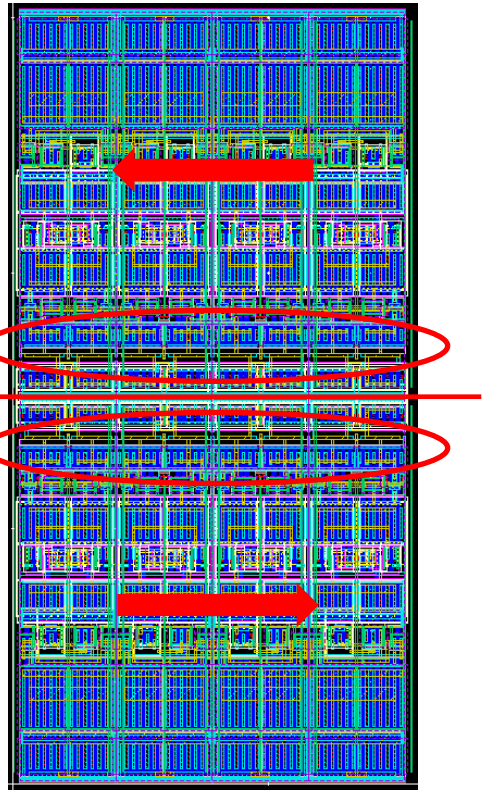


Cell Layout Optimized to minimize systematic mismatch:

- ❑ Core Transistors at the top edge
- ❑ All transistor with vertical gates (horizontal current flow)
- ❑ All transistor with number of fingers multiple of 2

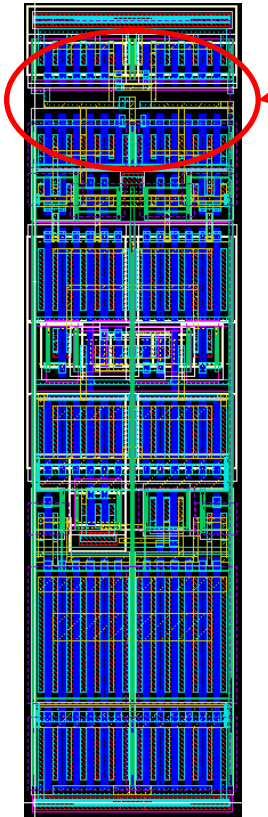


8 Cell Delay Line Layout Draft:



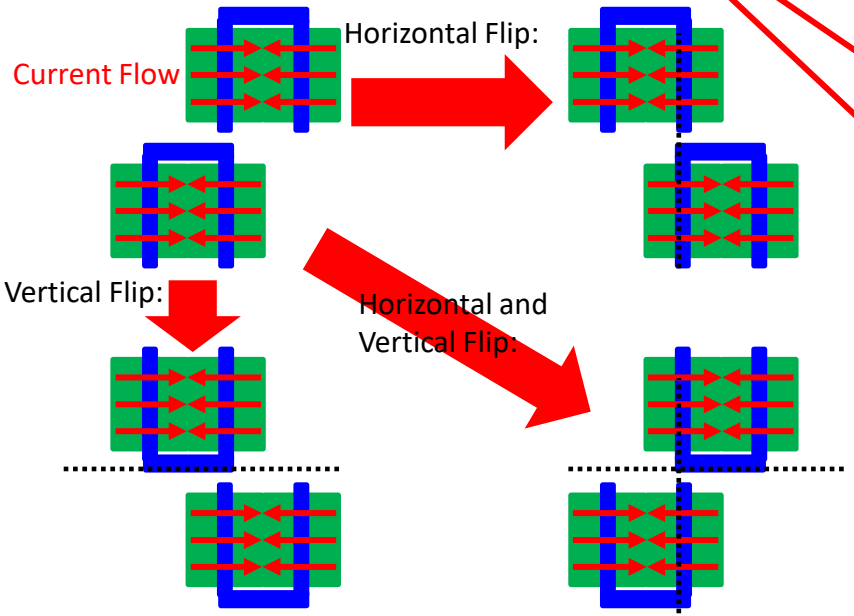
28nm Delay Cell Layout

Delay Cell Layout:

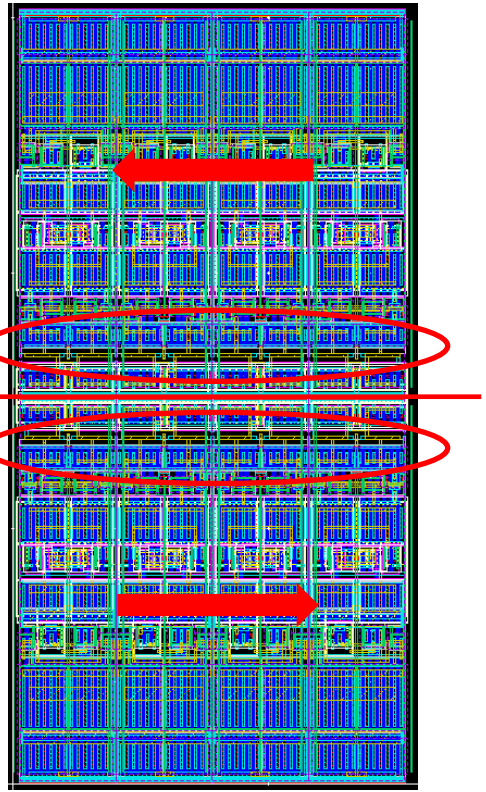


Cell Layout Optimized to minimize systematic mismatch:

- ❑ Core Transistors at the top edge
- ❑ **All transistor with vertical gates (horizontal current flow)**
- ❑ **All transistor with number of fingers multiple of 2**

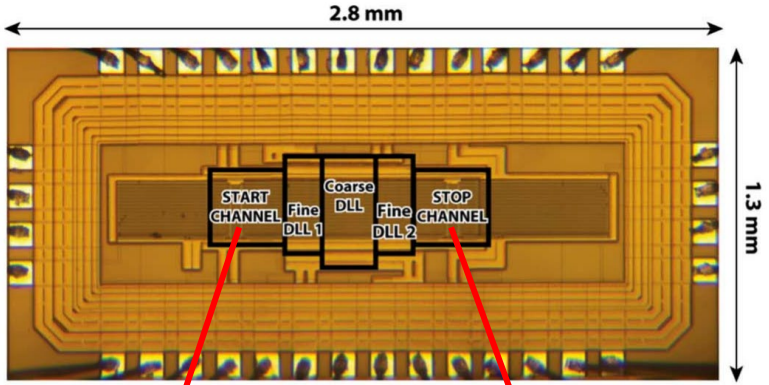


8 Cell Delay Line Layout Draft:

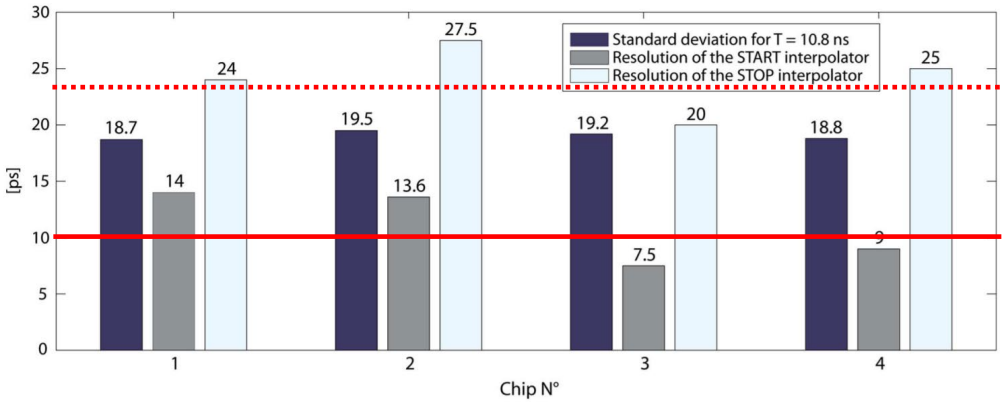


350nm TDC

B. Markovic, S. Tisa, F. A. Villa, A. Tosi and F. Zappa, "A High-Linearity, 17 ps Precision Time-to-Digital Converter Based on a Single-Stage Vernier Delay Loop Fine Interpolation," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 3, pp. 557-569, March 2013, doi: 10.1109/TCSI.2012.2215737.



❑ 10ps Nominal Resolution

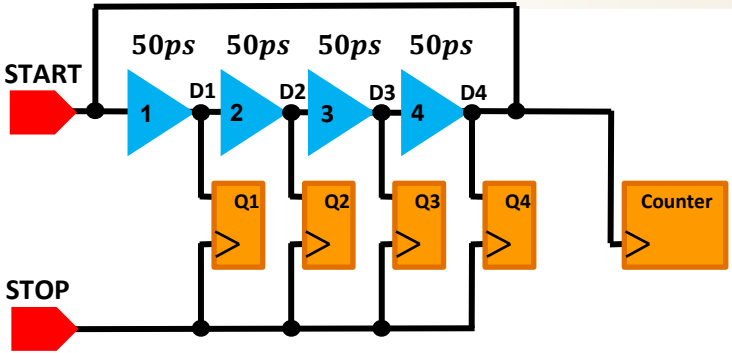


START Channel orientation same as bias DLLs

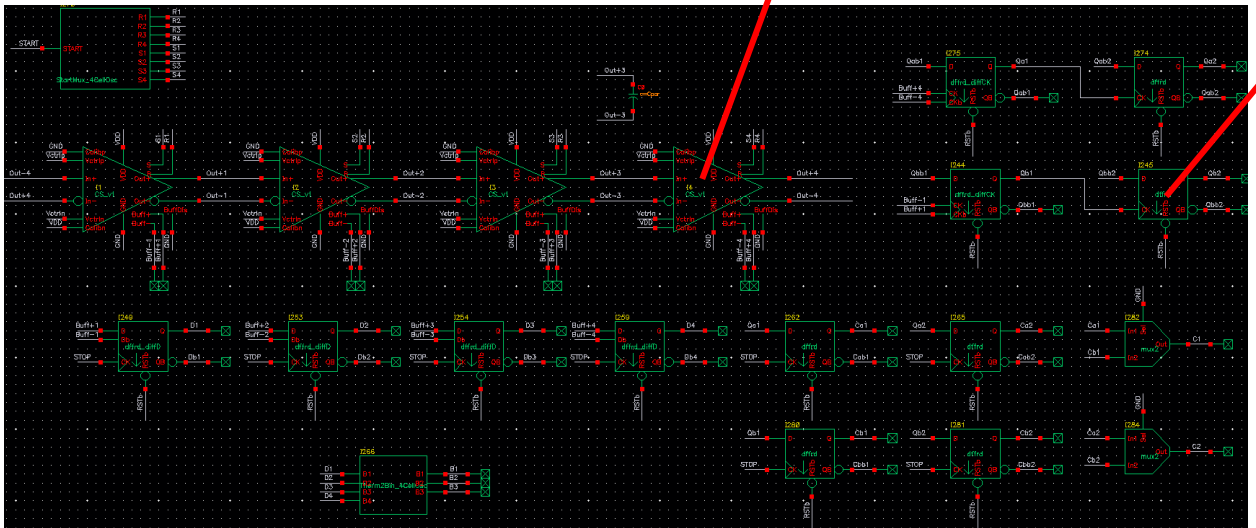
STOP Channel orientation vertically mirrored compared to bias DLLs

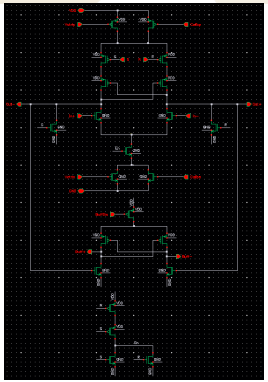
→ Systematic Mismatch

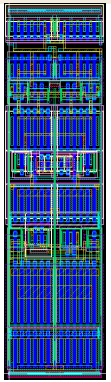
28nm TDC Initial Evaluation



- Schematic & Layout done (v1):



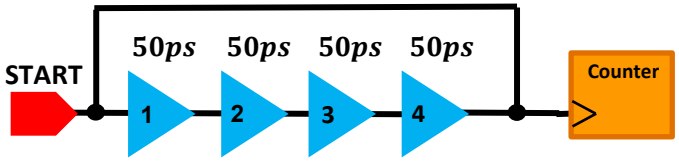


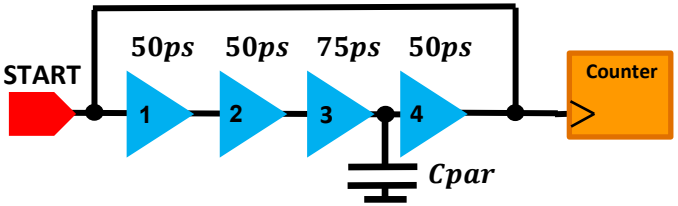


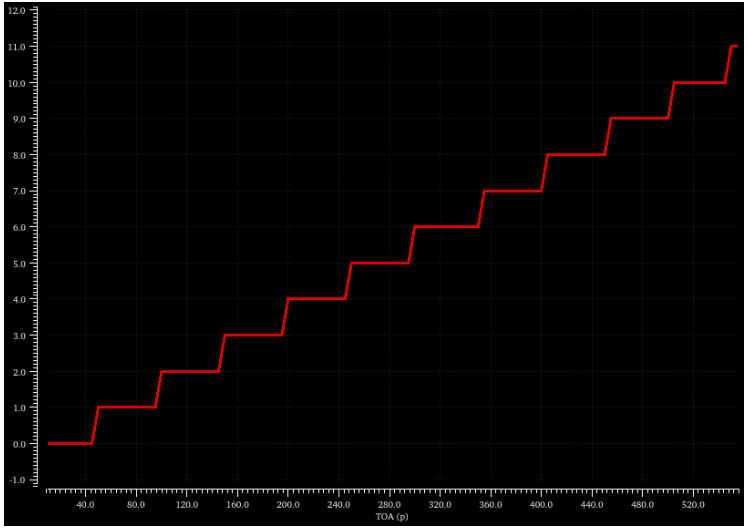
- Ideal/Code (VerilogA) Elements:

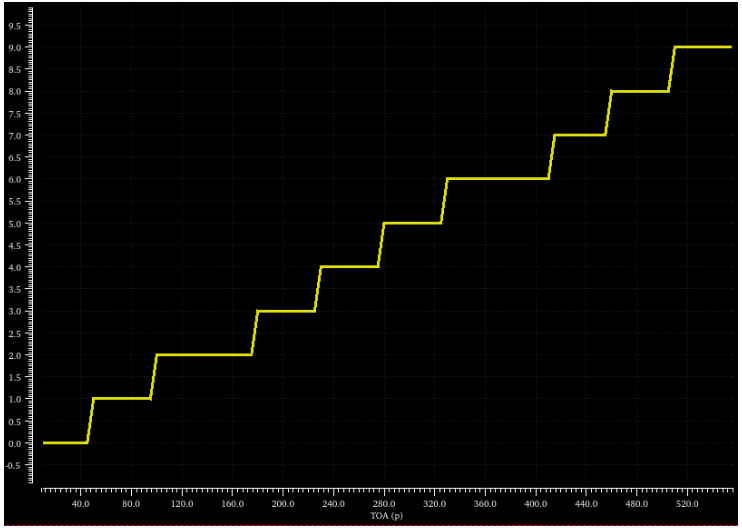
```
module dffrd(Q, QB, CK, D, RSTb);

inout Q; electrical Q;      // Q output
inout QB; electrical QB;  // Q bar output
input CK; voltage CK;  // Clock input (falling edge triggered)
input D; voltage D;          // D input
input RSTb; voltage RSTb;  // Reset input (immediately forces Q output low) (active low)

parameter real VDD = 0.9;                // voltage level of logic 1 (V)
parameter real VSS = 0;                  // voltage level of logic 0 (V)
parameter real vth = (VDD+VSS)/2;        // logic threshold level (V)
parameter real td = 5p from [0:inf);  // delay to start of output transition
parameter real Tr = 5p from [0:inf);  // rise time of output signals
parameter real Tf = 5p from [0:inf);  // fall time of output signals
parameter real ro = 1k from [0:inf);   // output resistance (ohm)

real out, outb;
electrical Qi, QBi;

analog begin
    @(initial_step) begin
        out = VSS;
        outb = VDD;
    end
    @(cross(V(CK) - vth, -1)) begin
        if (V(D) > vth && V(RSTb) > vth) begin
            out = VDD;
            outb = VSS;
        end else begin
            out = VSS;
            outb = VDD;
        end
    end
    @cross(V(RSTb) - vth);
    if (V(RSTb) < vth) begin
        out = VSS;
        outb = VDD;
    end
    V(Qi) <+ transition( out, td, Tr, Tf );
    V(QBi) <+ transition( outb, td, Tr, Tf );
    V(Q,Qi) <+ I(Q,Qi)*ro;
    V(QB,QBi) <+ I(QB,QBi)*ro;
end
endmodule
```

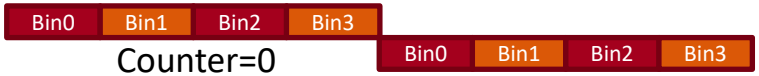
28nm TDC Initial Evaluation

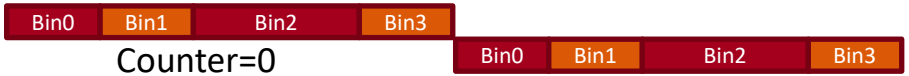










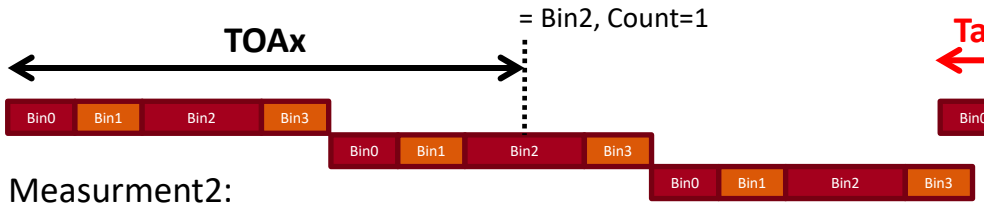


28nm TDC Initial Evaluation

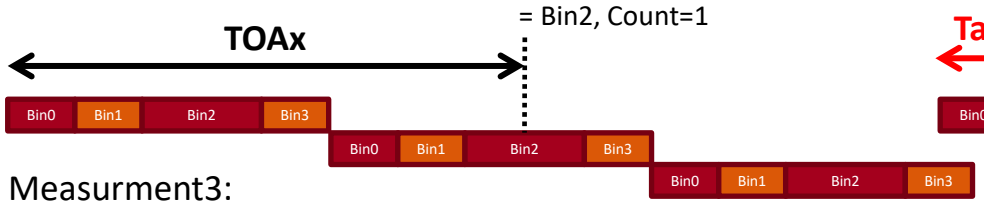
[1] C. Cottini, E. Gatti, and V. Svelto, “A new method for analog to digital conversion,” Nucl. Instr. Meth., vol. 24, p. 241, Aug. 1963.
[2] E. Gatti, P. F. Manfredi, and D. Marino, “Analysis and characterization of cyclic-scale compensated analog-to-digital converters,” Nucl. Instrum. Methods, vol. 165, no. 2, pp. 225–230, Oct. 1979.

- Regular Converter:

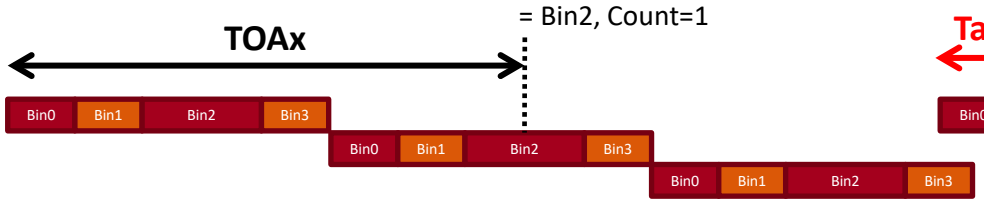
Measurment1:



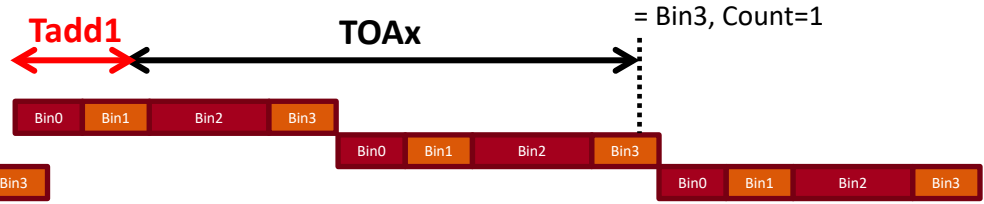
Measurment2:

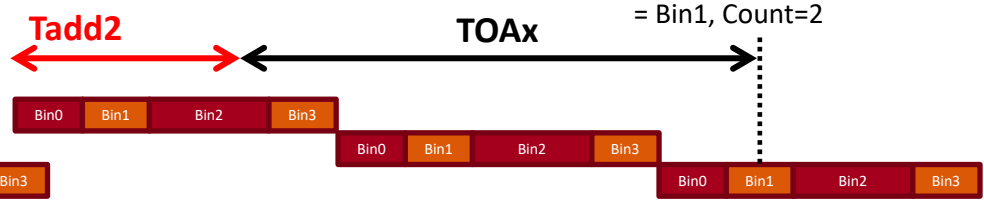


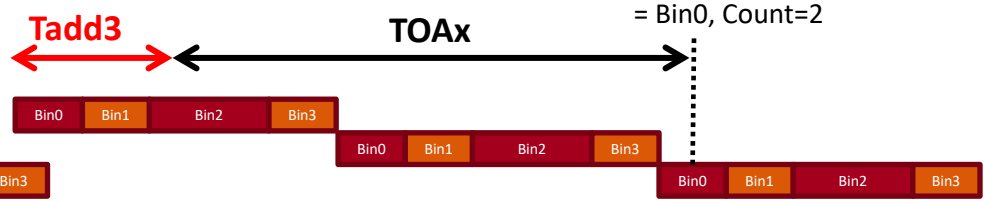
Measurment3:



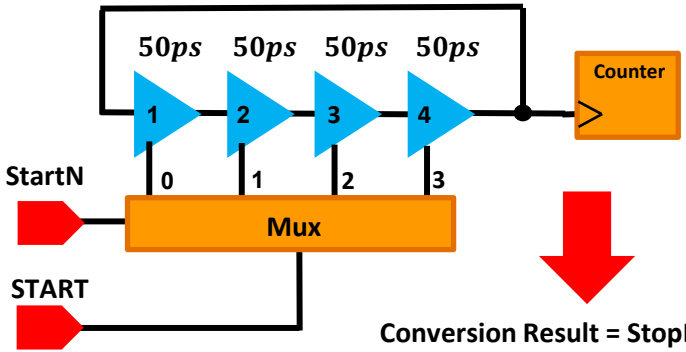
- Sliding Scale [1][2] / Dithering:







28nm TDC Initial Evaluation



Conversion Result = StopBin - StartN