4D Tracking – ASIC

11/17/2021

Bojan Markovic

U.S. DEPARTMENT OF ENERGY
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

Towards 4D tracking and calorimetry in deep submicron technologies

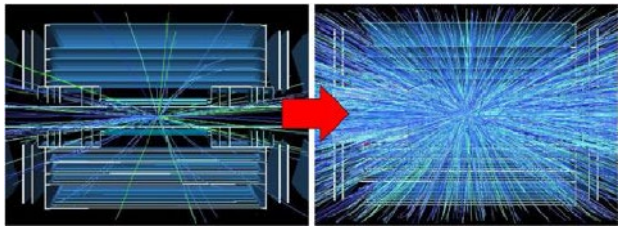
TID-ID SLAC

SOLUTION/IMPACT

- Research 4D (space and time) architectural front-end solutions in 28nm and 22nm FinFET for next generation trackers and calorimeters
- Enables higher spatial resolution and sub-bunch timing resolution, while sustain higher radiation doses
- Critical for resolving pile-ups in future high luminosity colliders operating in extreme radiation environments

COCNEPT

High Luminosity implications



Highly segmented hybrid pixel detectors with precision timing (28nm)
+
Fast sensors (LGADs)

→ **4D tracking and calorimetry**

RESOURCES

- PI B. Markovic (TID), Co-PI A. Pena Perez (TID)
- Co-Is: Kenney (TID), A. Schwartzman (FPD), Su Dong (FPD), C. Vernieri (FPD)
- Resources from TID-ID IC & Sensors
- **5 months FTE ($200k)**
- **M&S ($40k)**
- Long term R&D (scope defined for Q2-Q4 2022)

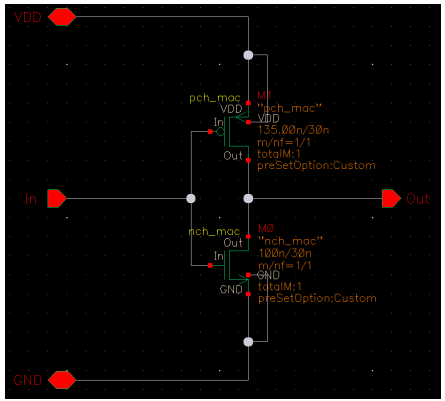
DELIVERABLES

- Continue engaging with the broader community collaboration around 28nm and 22nm (CERN, LBNL, FNAL)
- Establish 28nm and 22nm FinFET design flows (mostly done)
- Continue the design and layout test structures for technology characterization
- Continue the design and layout prototype of pixel timing blocks and ADCs
- Fab a first 28nm prototype (opportunity for joint fab run with LBNL and FNAL)

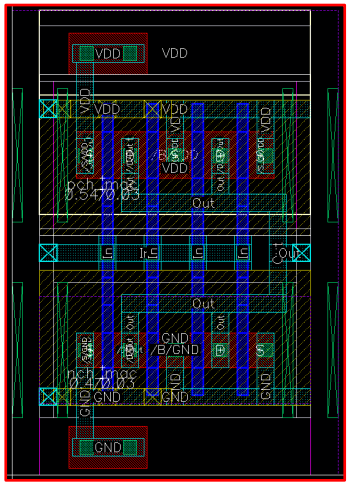
Propagation Delay: Inverter

TID-ID SLAC

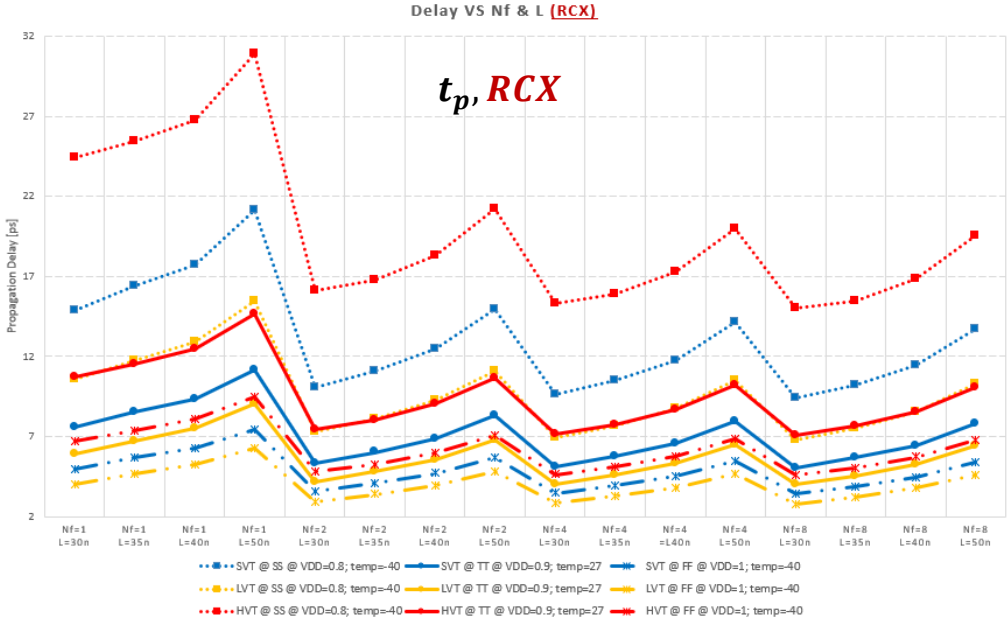
- Inverter:
  - Schematic:



  - Layout:



Propagation Delay
$\times \sim 2$

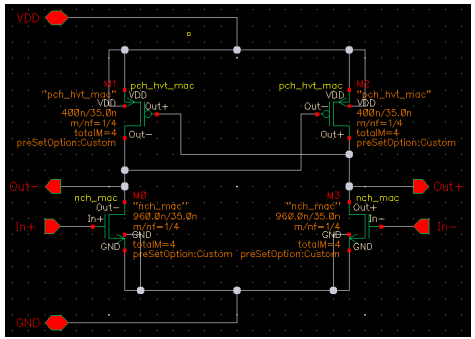


$t_{pRCX} \sim 12 - 25ps$

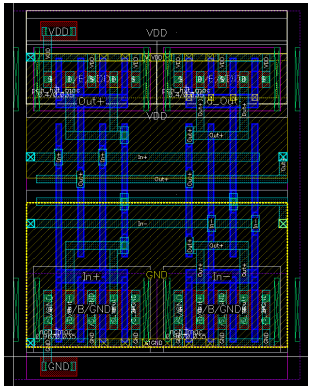
*A Buffer is made of 2 inverters thus the corresponding delay would be 24-50ps

DCVSL Delay Cell

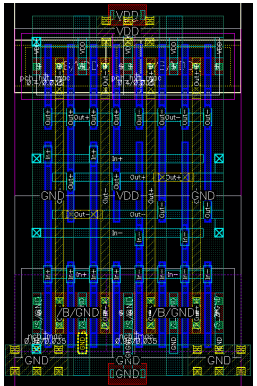
- Differential Cascode Voltage Switch Logic (DCVSL) Implementation:



- Layout 1:

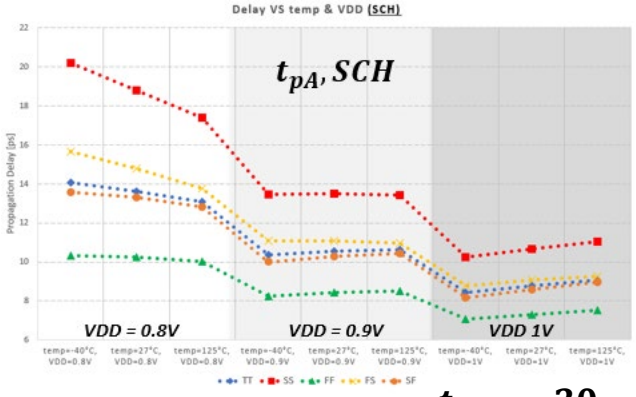


- Layout 2:



Layout 1:

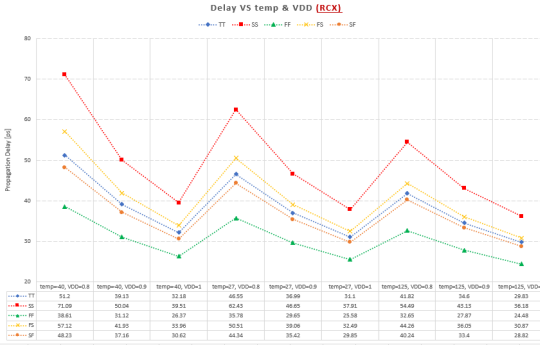
$\times \sim 3.5$



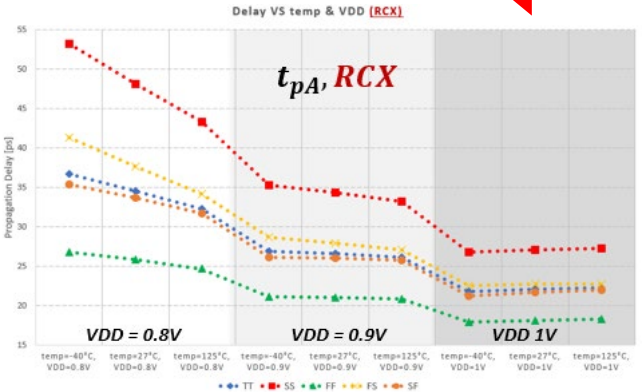
Layout 2:

$\times \sim 2.5$

$t_{pRCX} \sim 40 - 70ps$

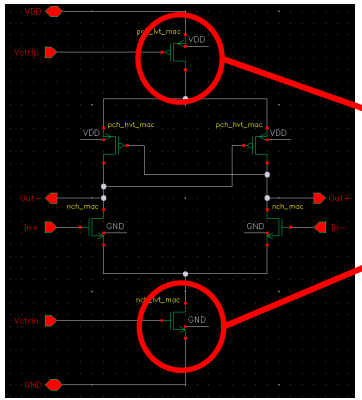


$t_{pRCX} \sim 30 - 50ps$



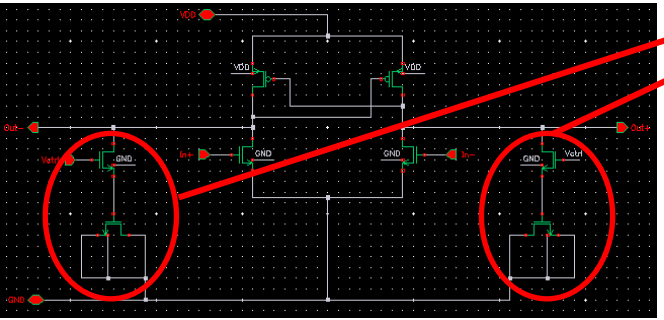
Voltage-Controlled Delay Cells

- Current-Starved Delay Cell:

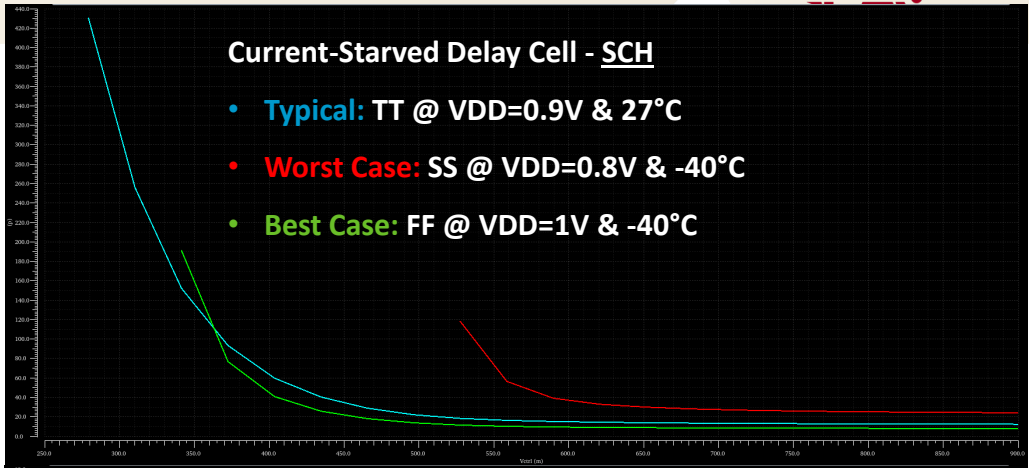


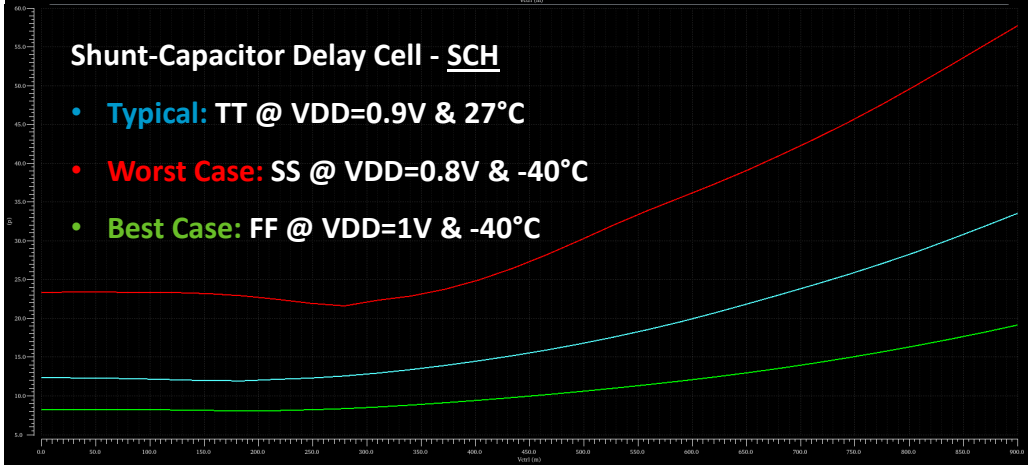
Delay controlled thro current

- Shunt-Capacitor Delay Cell:



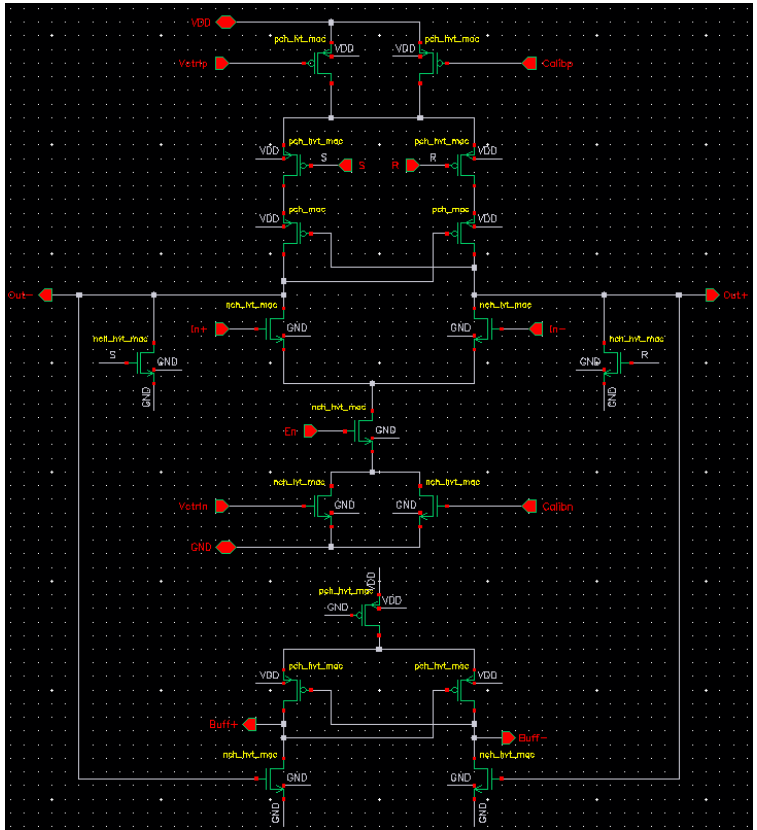
Delay controlled thro load



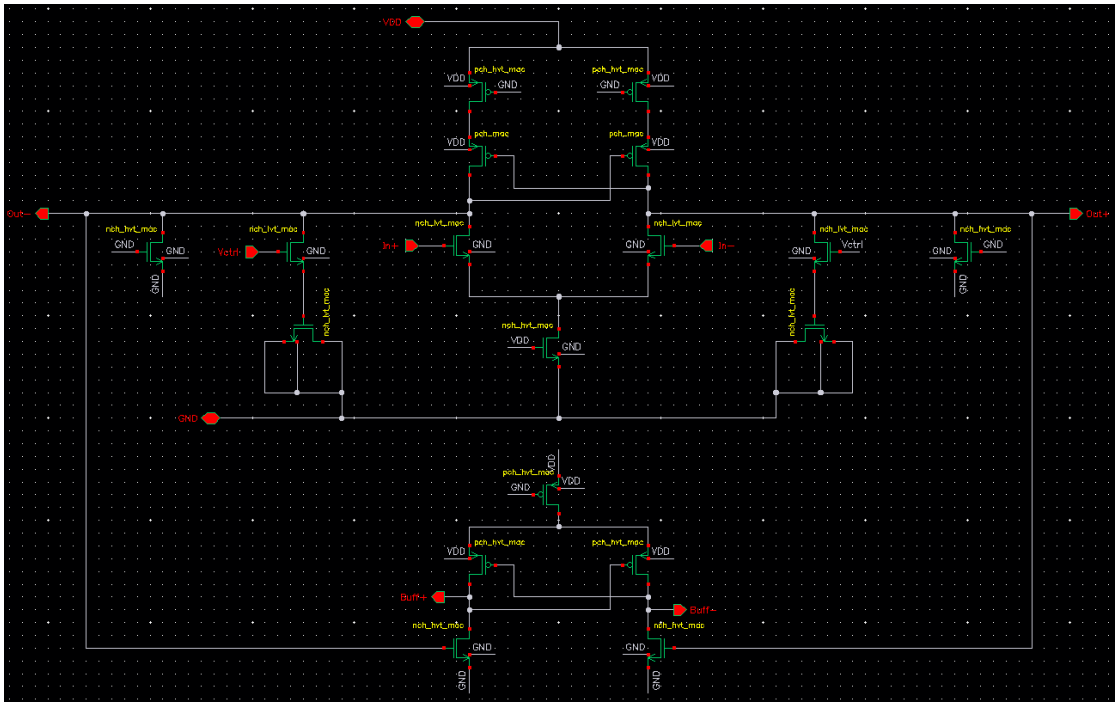


Voltage-Controlled Delay Cells

- Current-Starved Delay Cell:

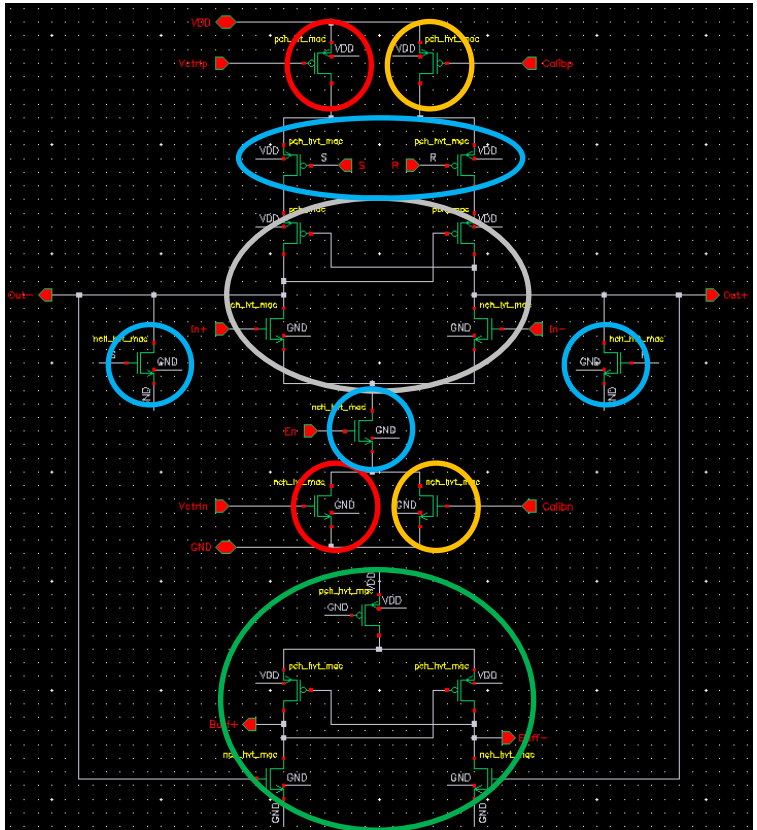


- Shunt-Capacitor Delay Cell :

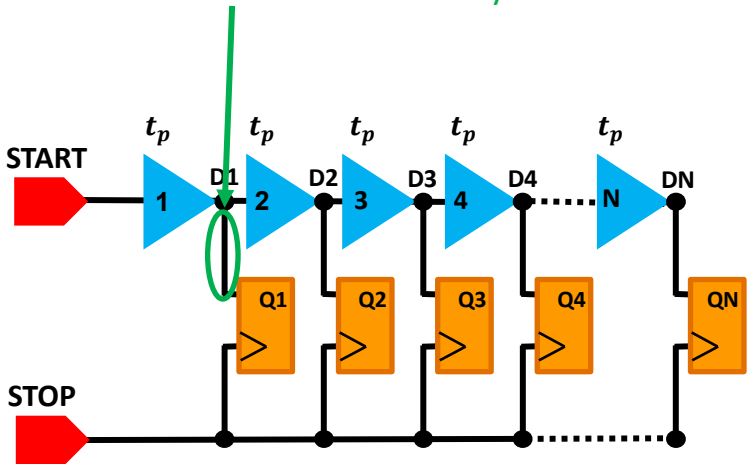


Voltage-Controlled Delay Cell

- Current-Starved Delay Cell:



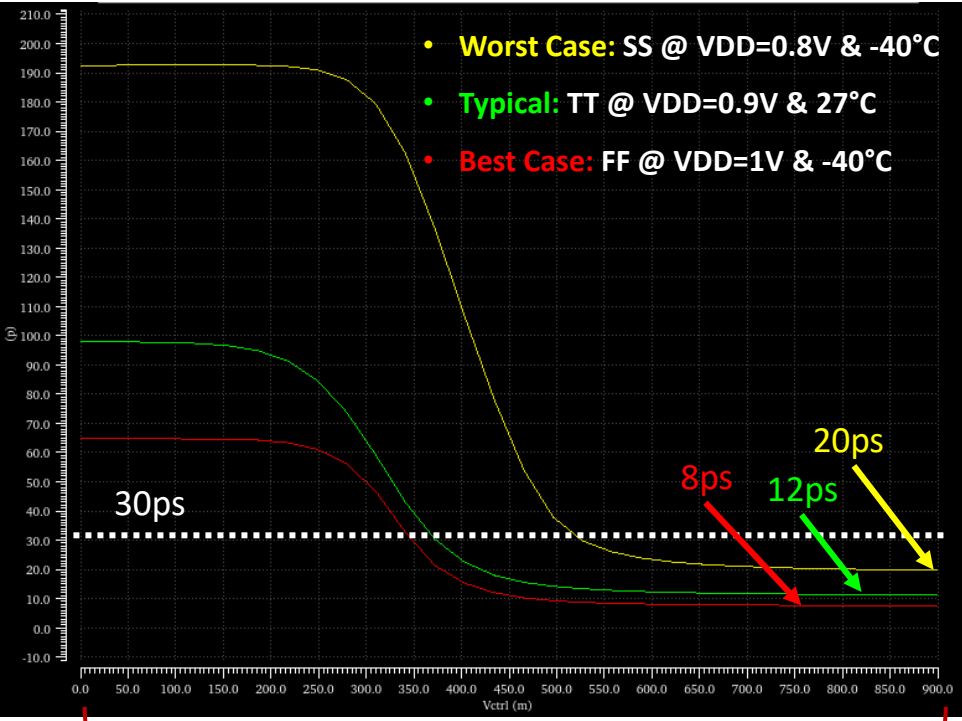
- DCVSL core transistors
- Voltage Controlled Delay
- Calibration / Trimming
- Cell Logic Controls (Disable; Set; Reset)
- Output Buffers for access to the delay line state



Voltage-Controlled Delay Cells

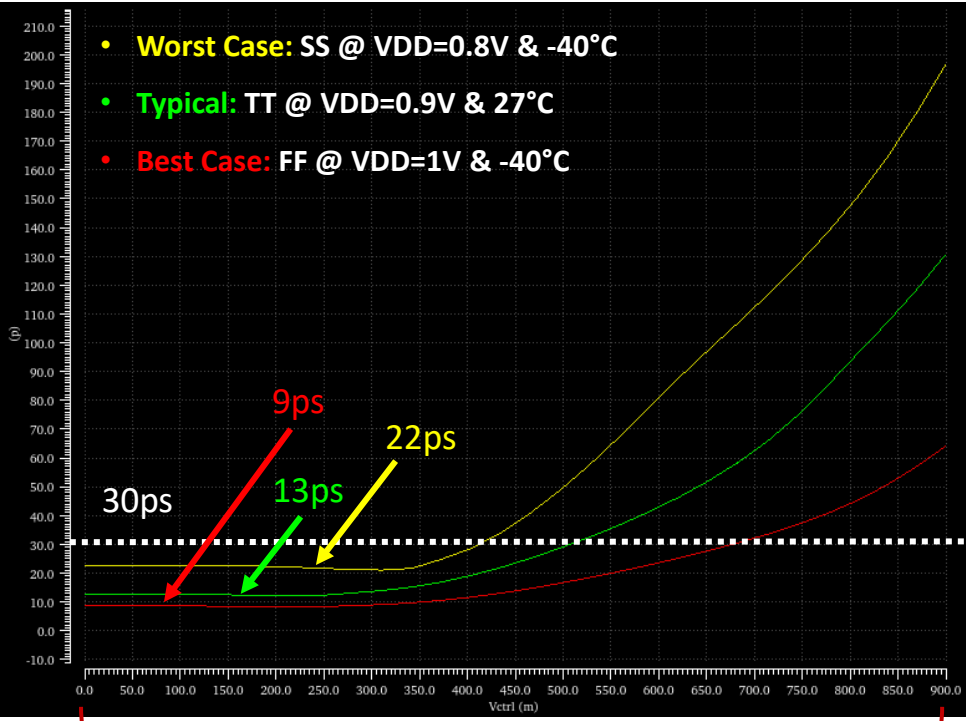
TID-ID SLAC

- Current-Starved Delay Cell:



Delay-Control Voltage

- Shunt-Capacitor Delay Cell :

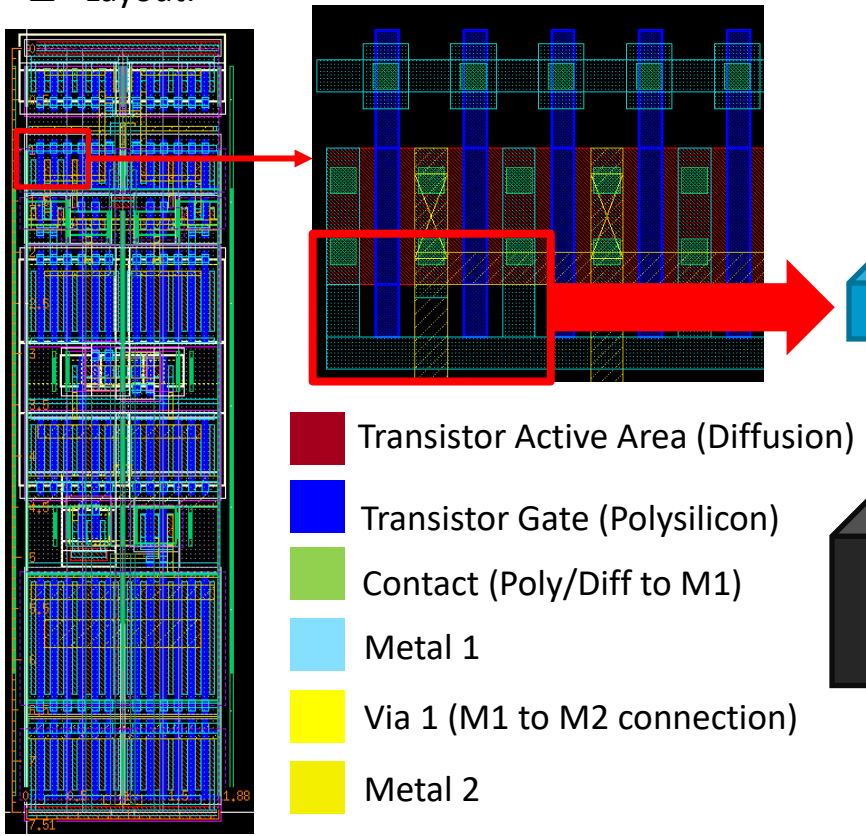


Delay-Control Voltage

Layout

TID-ID SLAC

- Layout:



Transistor Active Area (Diffusion)

Transistor Gate (Polysilicon)

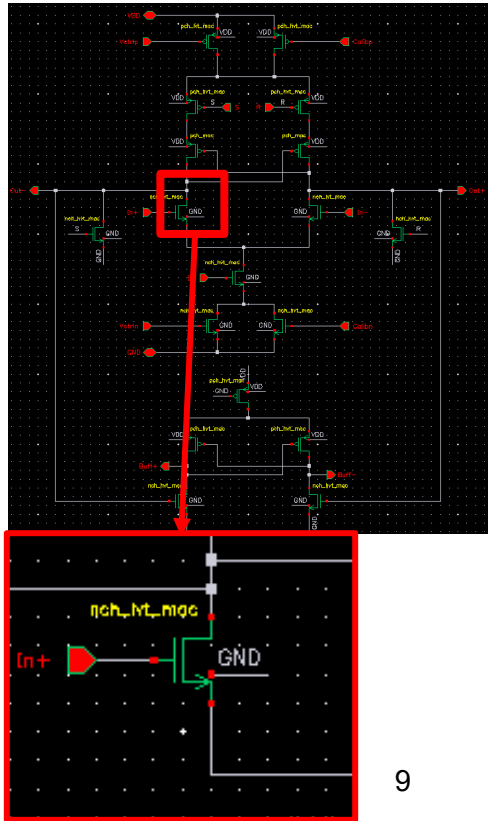
Contact (Poly/Diff to M1)

Metal 1

Via 1 (M1 to M2 connection)

Metal 2

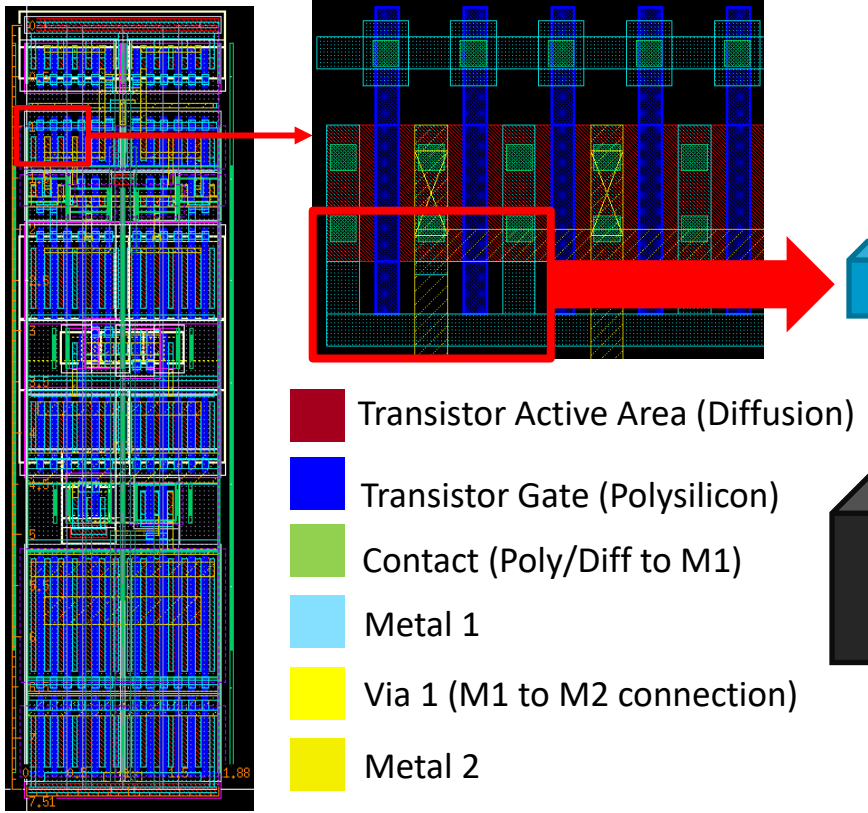
- Schematic:



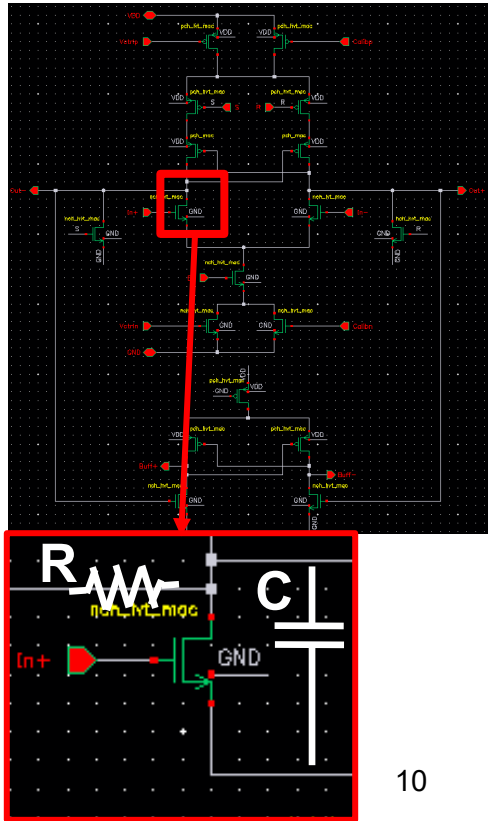
Layout: Parasitics

TID-ID SLAC

- Layout:

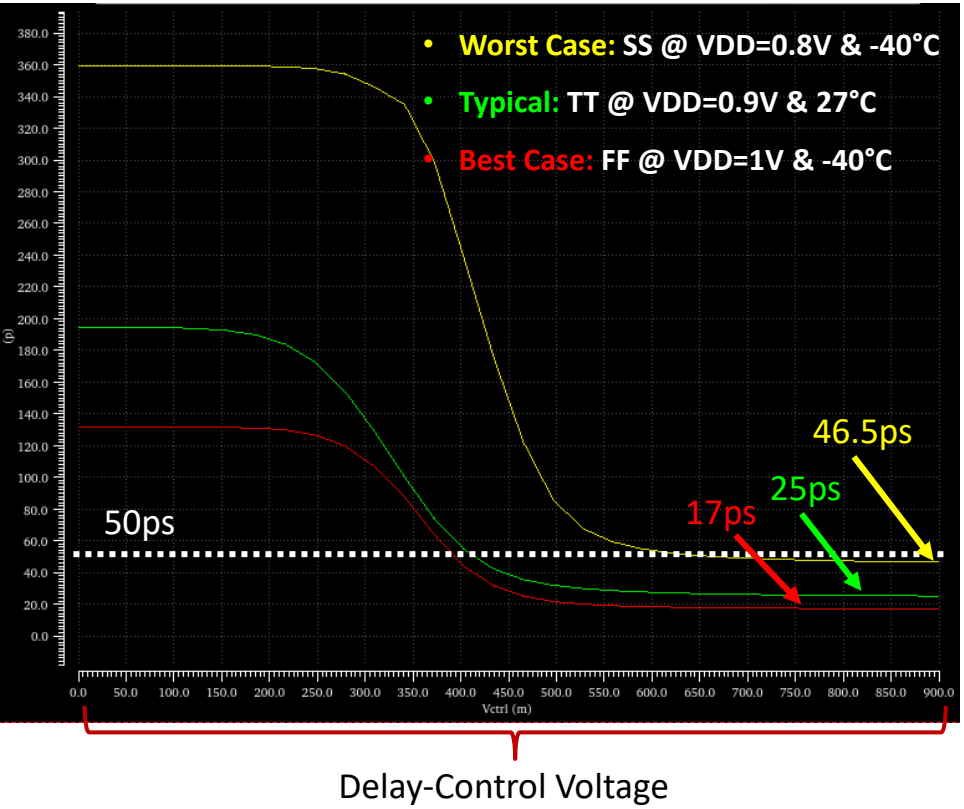


- Schematic:

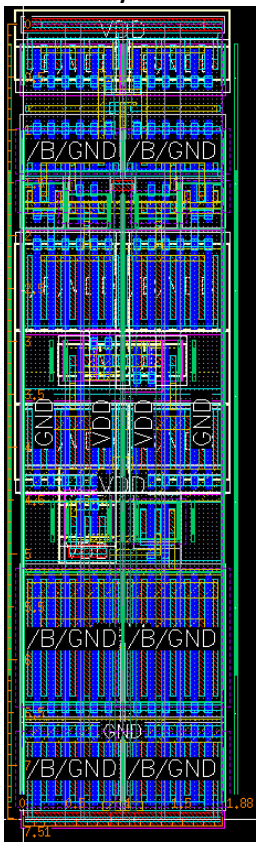


Voltage-Controlled Delay Cell

- Layout Parasitics Extracted (RCX) Simulation:



- Layout:



- Schematic: