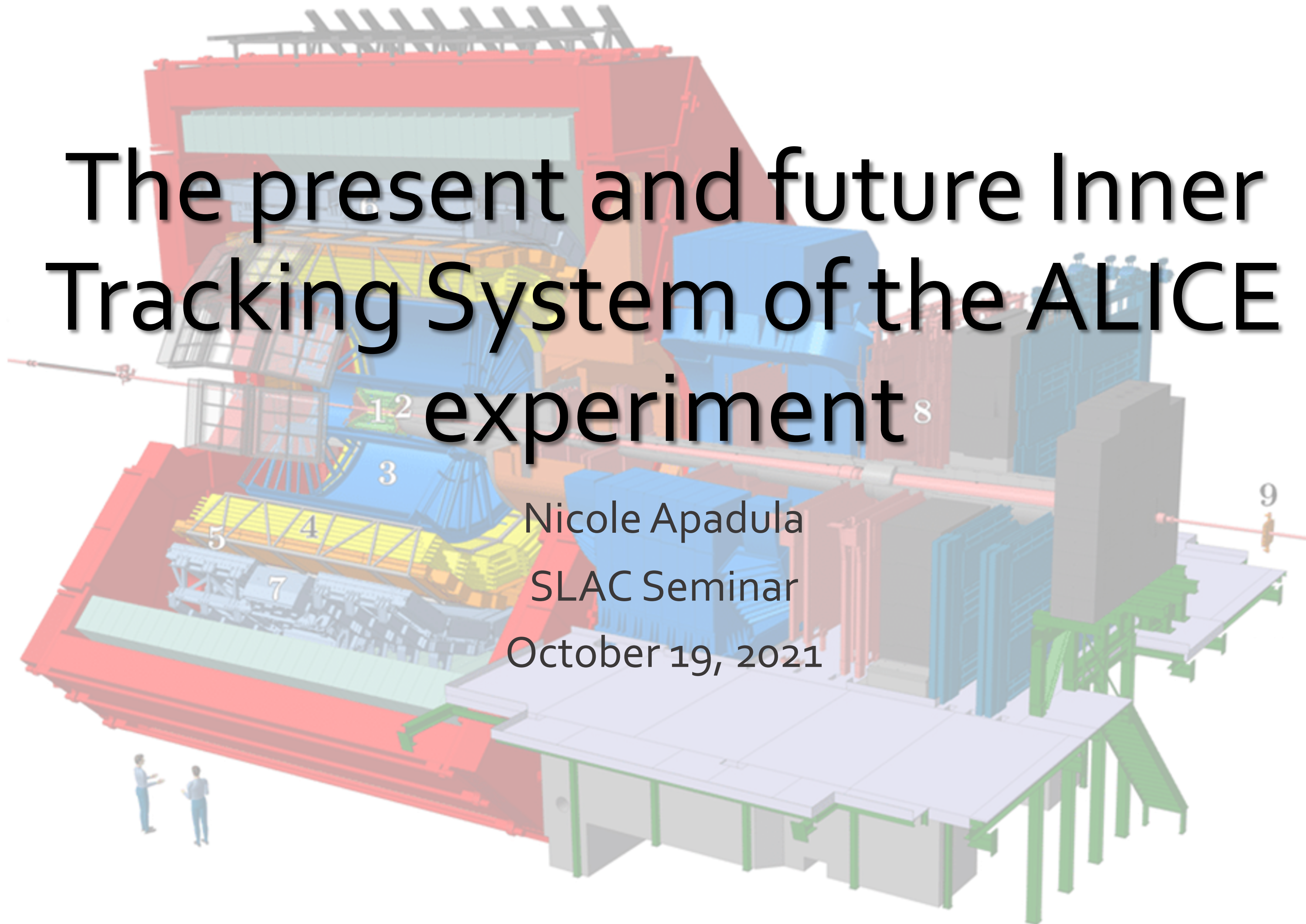



ALICE

BERKELEY LAB

# The present and future Inner Tracking System of the ALICE experiment

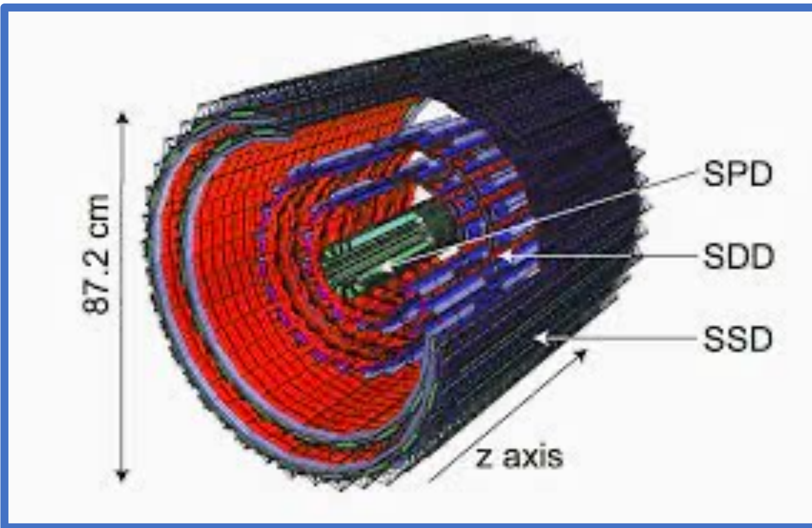
Nicole Apadula

SLAC Seminar

October 19, 2021

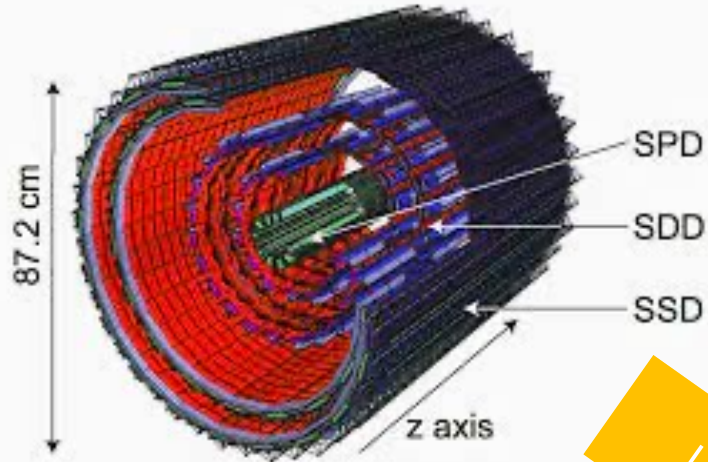
NicoleApadula@lbl.gov

# Evolution of the ALICE Inner Tracking System (ITS)




ALICE ITS1
2009 – 2019
Thickness of 1st layer: 1.14% $X_0$

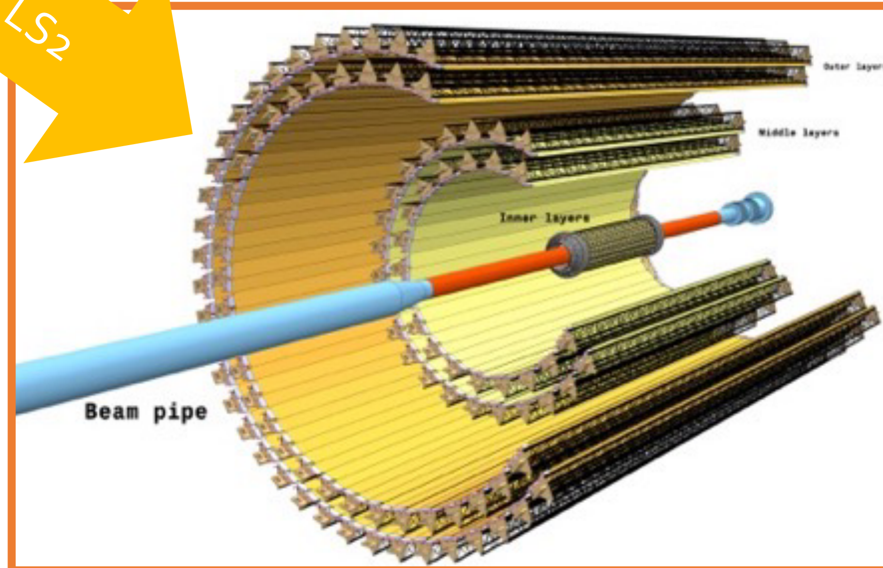
# Evolution of the ALICE Inner Tracking System (ITS)




ALICE ITS1
2009 – 2019
Thickness of 1st layer: 1.14% $X_0$

LS2

ALICE ITS2
2021+
Thickness of IB layers: 0.35% $X_0$



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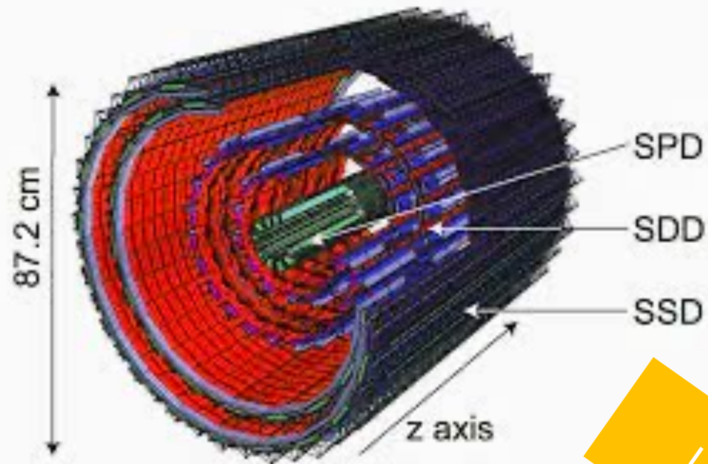


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2009 – 2019
Thickness of $1^{st}$ layer: 1.14% $X_0$

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2021+
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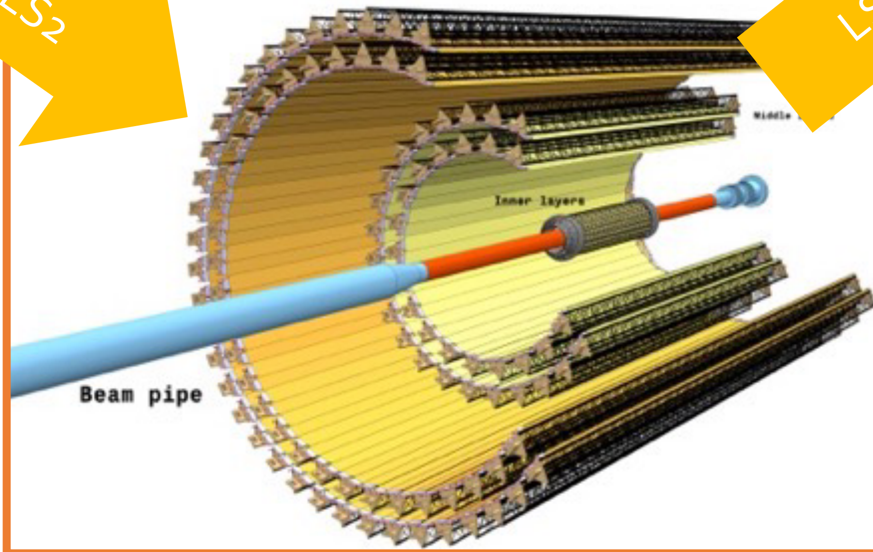
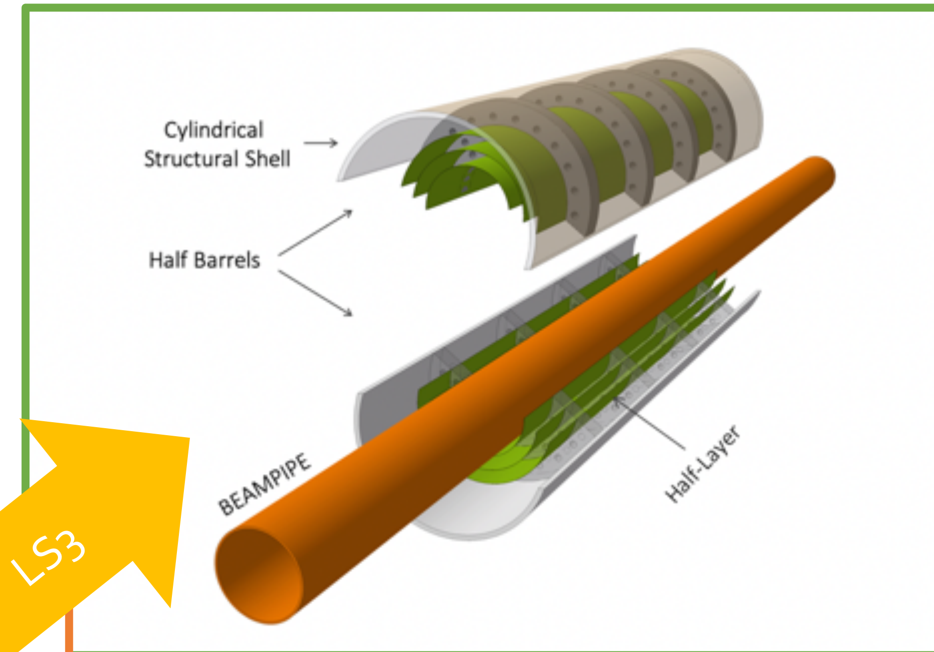


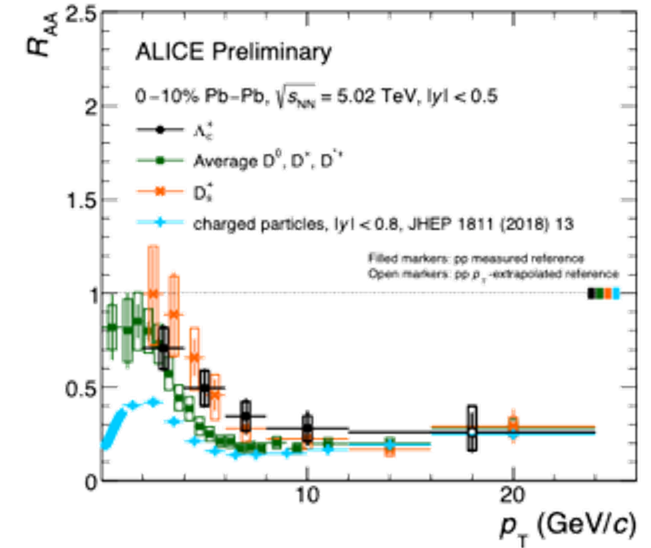

LS3

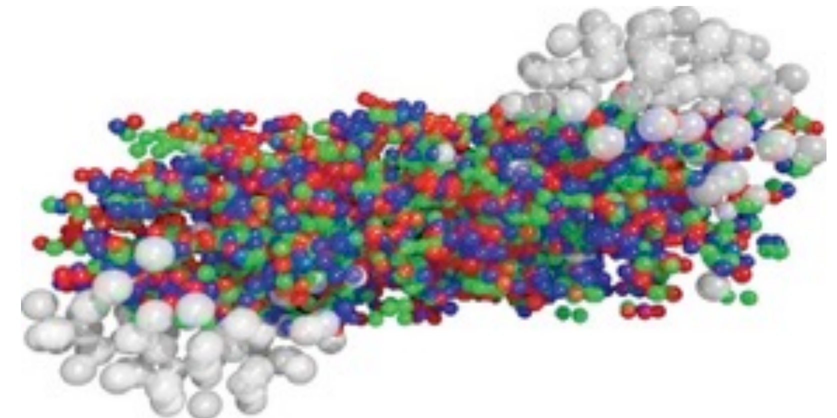



ALICE ITS3
Replacement of ITS2 inner layers
2026+
Thickness of layers: 0.05% $X_0$

# Motivation & Needs

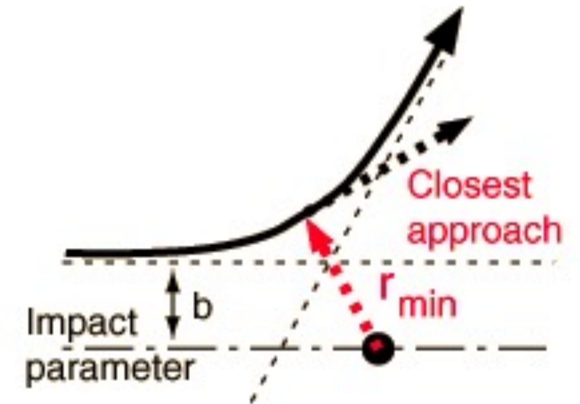
- Motivation:  QGP precision study
  - High precision measurement of heavy-flavor hadrons
    - Large range of $p_T$ & rapidity, centrality & reaction plane binned
- Requirements:
  - Excellent tracking efficiency & resolution at low $p_T$
  - Large statistics with MB trigger
- Strategy:
  - Readout all Pb-Pb interactions at 50 kHz
  - Improve vertexing & tracking capabilities



# Design Requirements: ITS2

- Improve impact parameter resolution (factor of 3 in $r\phi$, 5 in $z$)
  - Reduce beam-pipe diameter
    - 29 mm → 17.2 mm
  - Minimize distance between beam axis and first detector layer
    - 39 mm → 21 mm
  - Reduce pixel size
    - 50 μm x 425 μm → ~30 μm x 30 μm



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    - 39 mm → 21 mm
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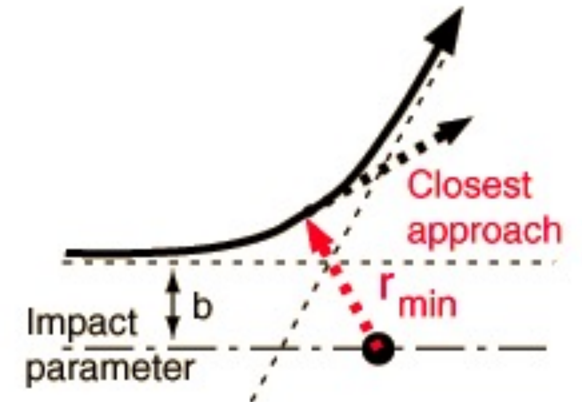
    - 50 μm x 425 μm → ~30 μm x 30 μm
- Increase tracking efficiency at low $p_T$ (60% at 100 MeV/c)
  - Reduce material budget (sensors, power, cooling)
    - > 1% $X_0$ → < 0.5% $X_0$ inner layers
  - Added layer of silicon detectors



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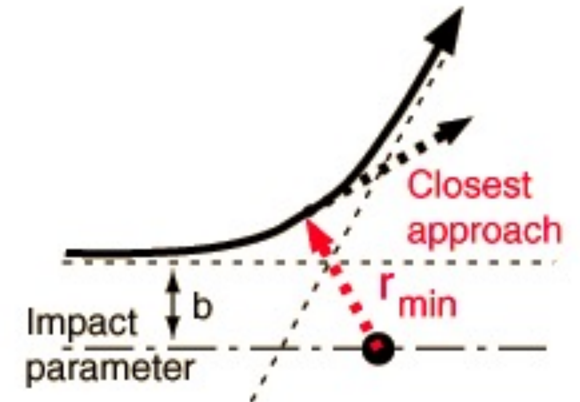
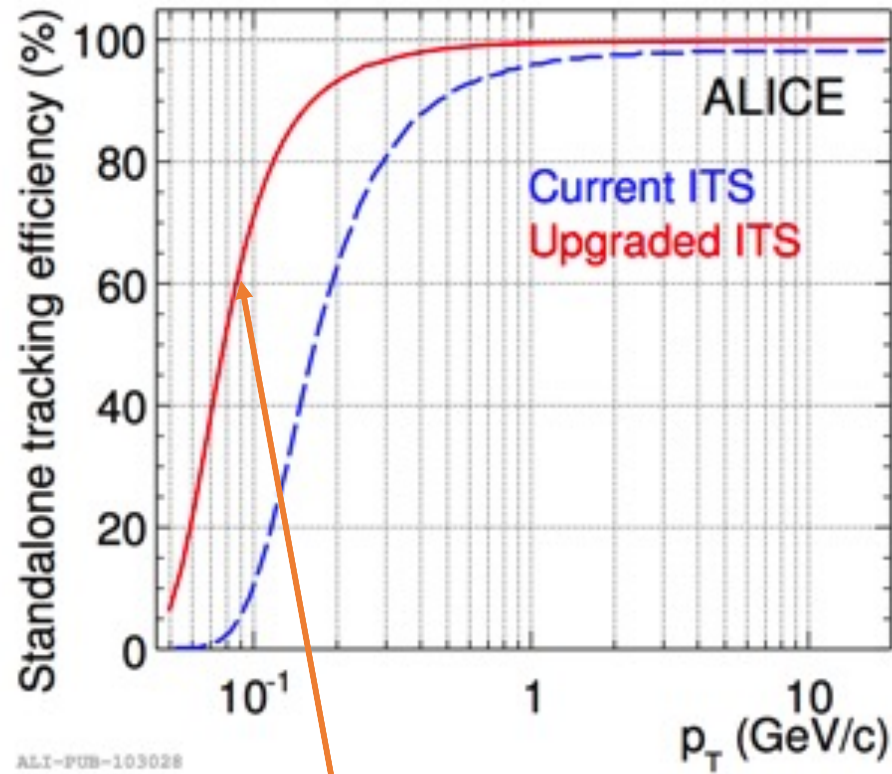
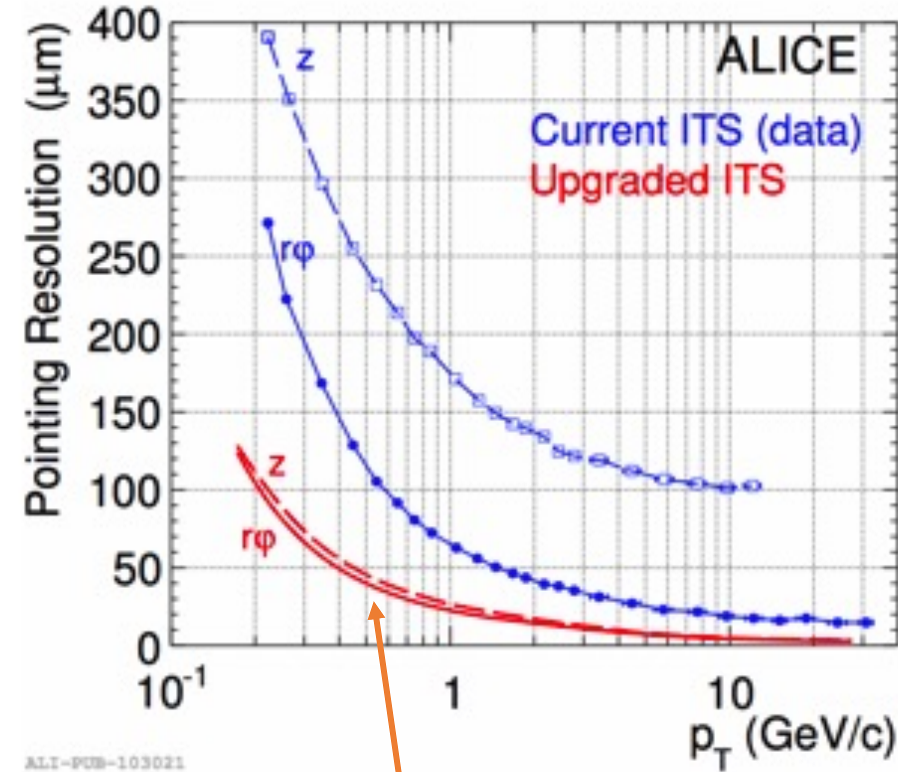
  - Reduce material budget (sensors, power, cooling)
    - > 1% $X_0$ → < 0.5% $X_0$ inner layers
  - Added layer of silicon detectors
- More statistics
  - Faster read-out (100 kHz for p+p collisions) for increased luminosity (10 $nb^{-1}$)



# ITS2 Projected Performance

ITS1
ITS2



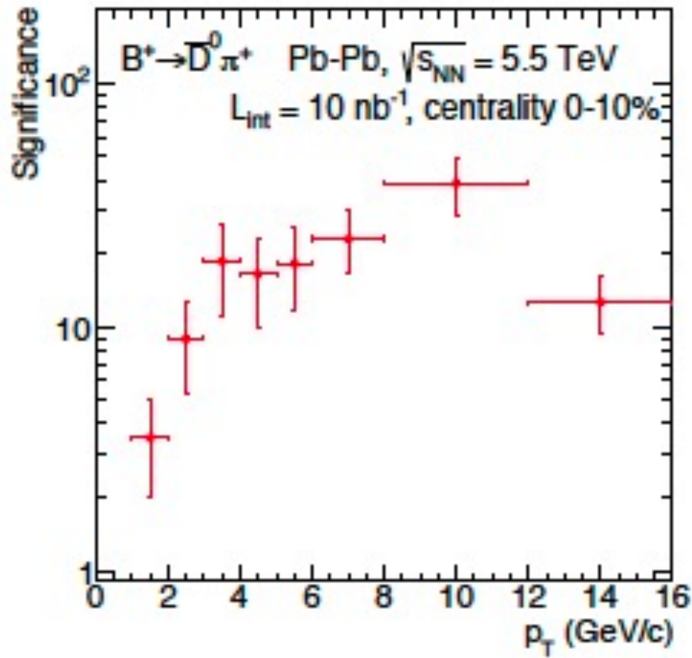



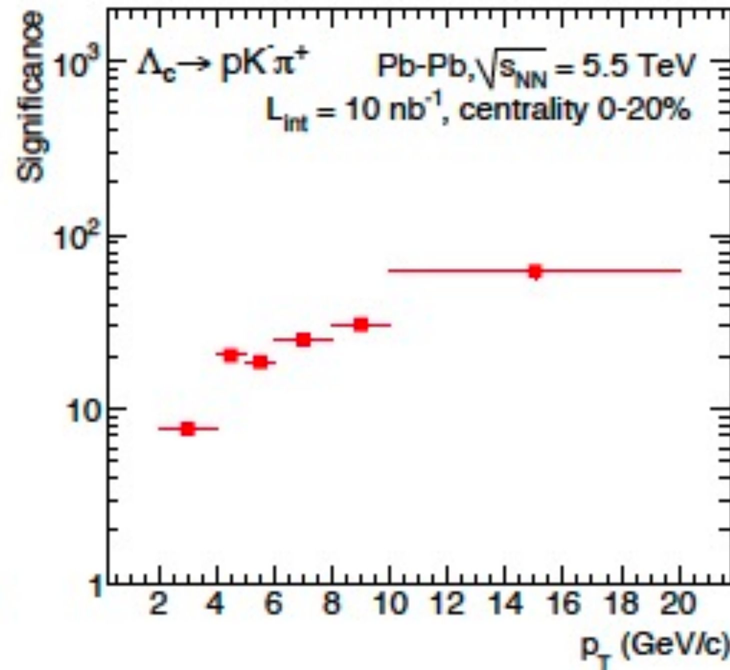

~60% at $p_T$ = 100 MeV/c

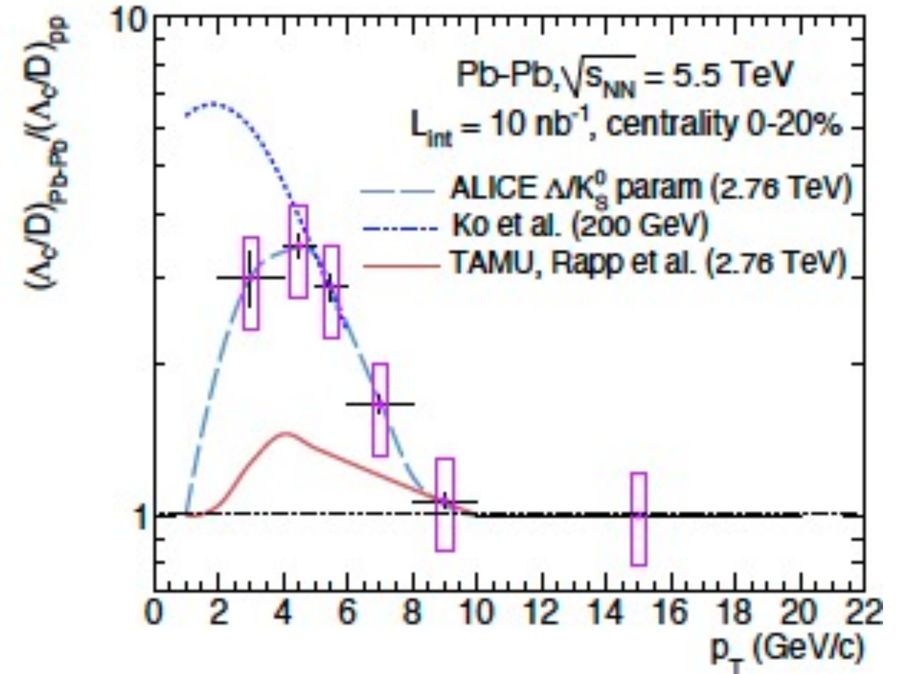
< 50 µm at $p_T$ = 500 MeV/c

J.Phys. G41 (2014) 087002 / CERN-LHCC-2013-024

# ITS2 Physics: Heavy Flavor Examples



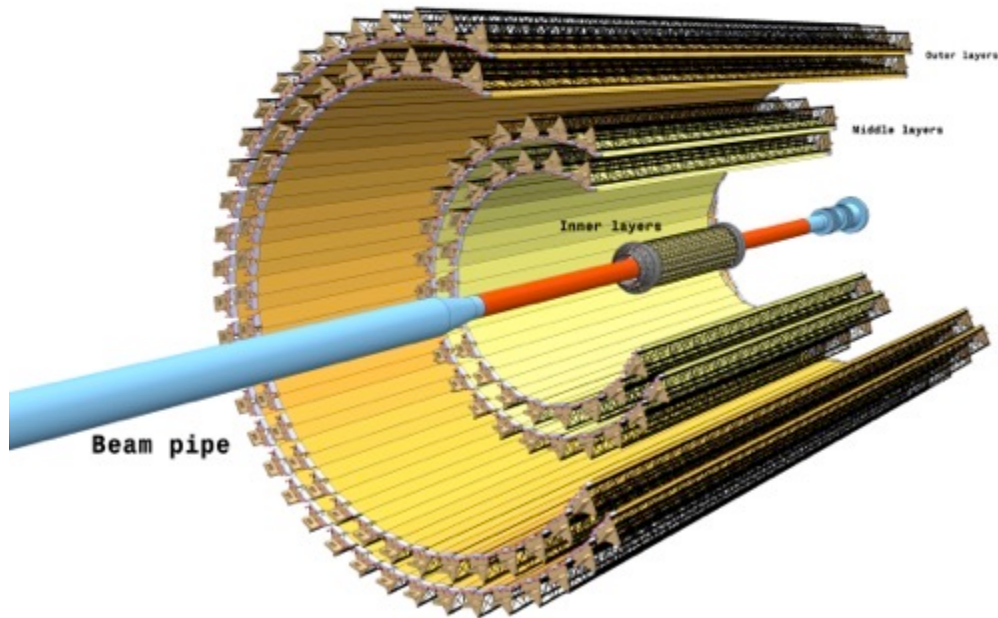



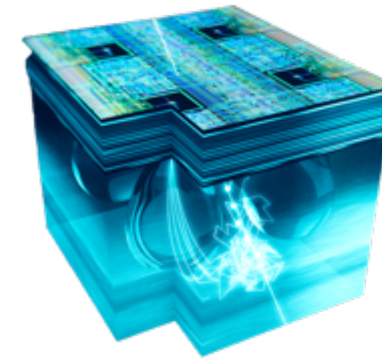

- Full reconstruction of B meson down to 1 GeV/c
- $\Lambda_c$ baryon in Pb+Pb down to 2 GeV/c
- Access to the charmed baryon/meson ratio

J.Phys. G41 (2014) 087002 / CERN-LHCC-2013-024

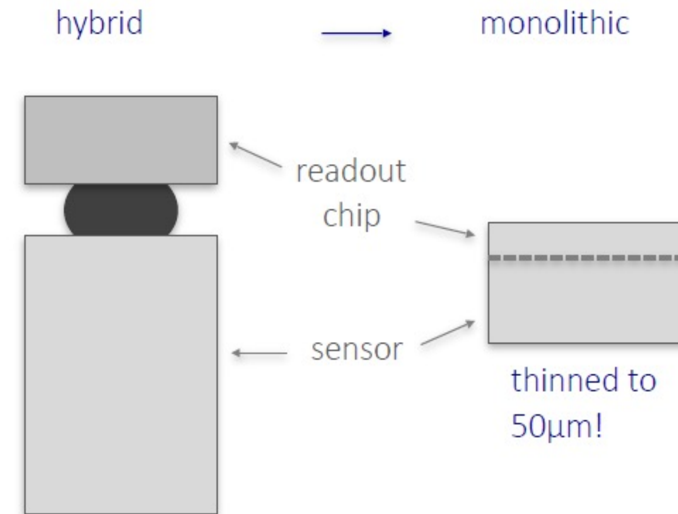
# ITS2 Structure

7 layer barrel geometry,
fully equipped (~24000 chips) with dedicated **MAPS:**
**ALice PIxel DEtector (ALPIDE)**
r-coverage: 23 – 400 mm
η coverage: |η| ≤ 1.3



**Monolithic Active Pixel Sensors**




Material /layer : 0.3% $X_0$ (IB), 1% $X_0$ (OB)

12.5 G-pixel camera (~10 $m^2$ active Si)
Binary read–out

# ALPIDE Sensor

180 nm CMOS Imaging Process

28 μm

collection electrode

2 x 2 pixel volume

*Artistic view of a SEM picture of ALPIDE cross section*

$C_{in} \approx 5$ fF

$Q_{in}$ (MIP) ≈ 1300 e ⇨ V ≈ 40mV

NWELL DIODE

NMOS TRANSISTOR

PMOS TRANSISTOR

PWELL

PWELL

NWELL

DEEP PWELL

Epitaxial Layer P-

Substrate P++

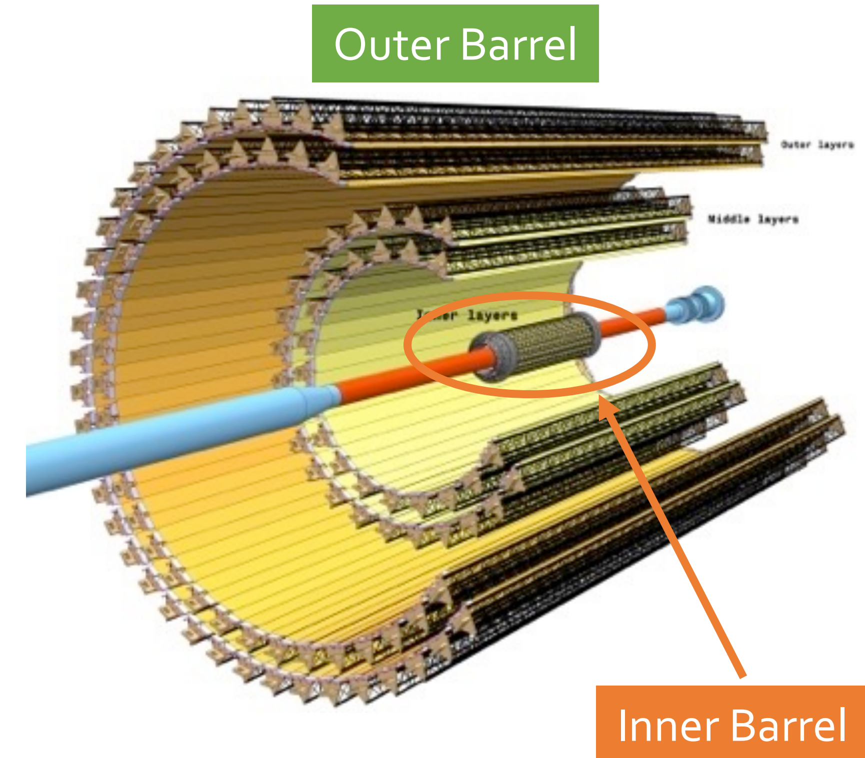
- In-pixel amplification, shaping, discrimination, Multi-Event Buffers (MEB)
- Moderate reverse bias (down to -6V) → Increases depletion region to collect more charge by drift
- Deep PWELL to shield  NWELL of PMOS transistors

# ALPIDE Requirements

Sensor requirements for the ALICE ITS Upgrade for Inner Barrel (IB) and Outer Barrel (OB) [1].

| Parameter | IB | OB |
|---|---|---|
| Sensor thickness (μm) | 50 | 100 |
| Spatial resolution (μm) | 5 | 10 |
| Dimensions ($mm^2$) | 15 × 30 | 15 × 30 |
| Power density ($mW\ cm^{-2}$) | 300 | 100 |
| Time resolution (μs) | 30 | 30 |
| Detection efficiency (%) | 99 | 99 |
| Fake hit rate[a] | $10^{-5}$ | $10^{-5}$ |
| TID radiation hardness[b] (krad) | 2700 | 100 |
| NIEL radiation hardness[b] ($1\ MeV n_{eq}/cm^2$) | $1.7 \times 10^{13}$ | $10^{12}$ |

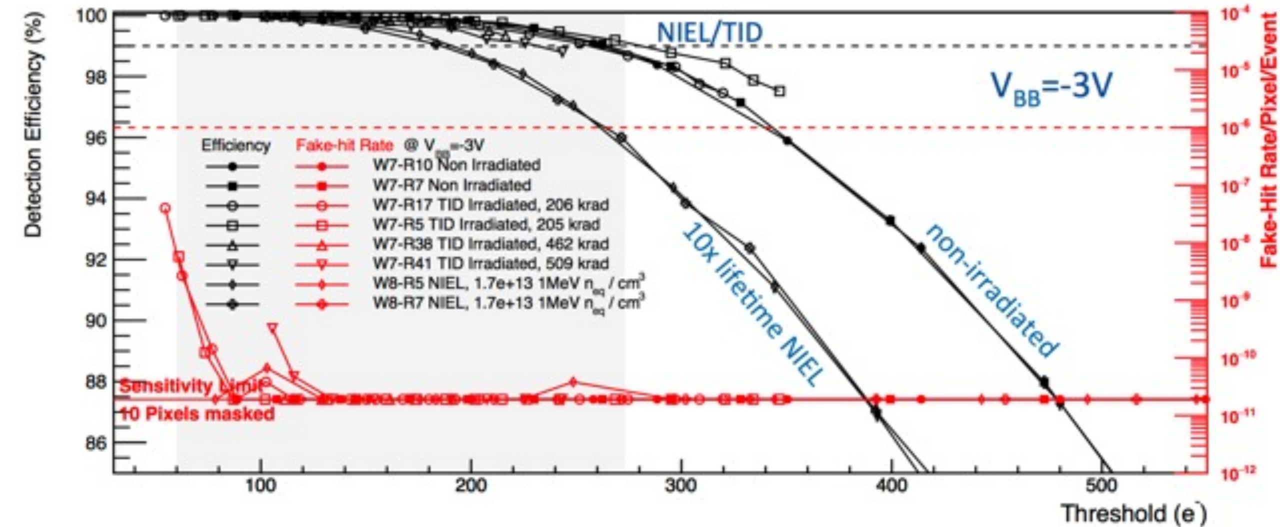
[a] Per pixel and readout.
[b] Including a safety factor of 10, revised numbers w.r.t. TDR.

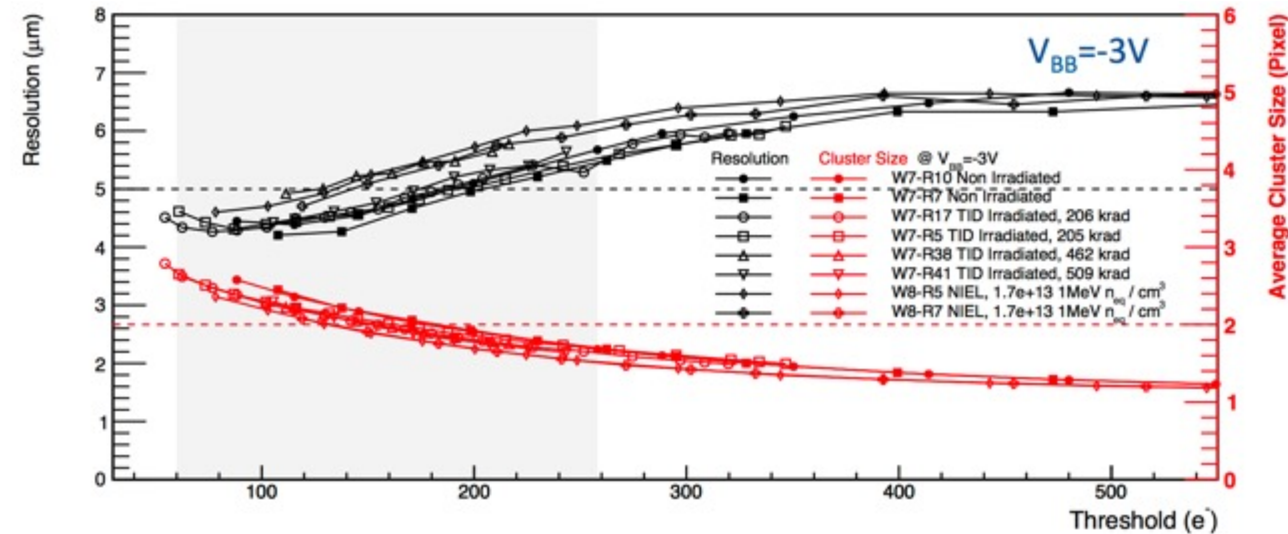


# ALPIDE Performance

- Tested at 10x lifetime NIEL level
- Performance similar before and after irradiation
- Chip-to-chip fluctuations negligible
- Fake hit rate
  - << $10^{-5}$ hits/pixel/event
- Resolution
  - 4-6 μm in operating range

Operating threshold ~ 110 $e^-$

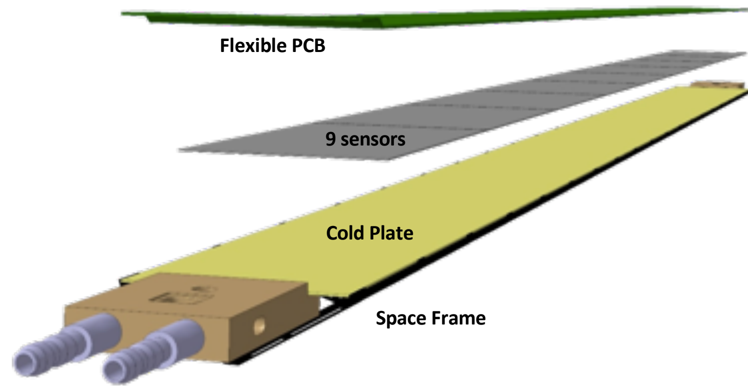



6 GeV/c $\pi^-$

# ALICE ITS2 Construction & Assembly

## Inner Barrel

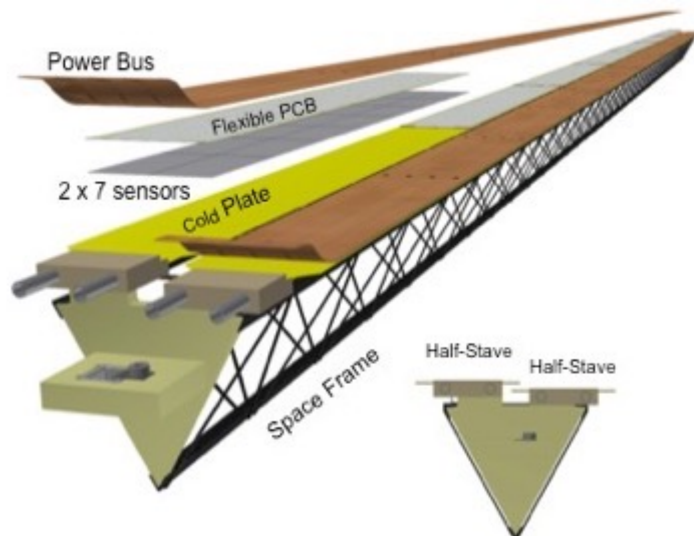



All inner barrel staves made at CERN

sensors thinned to 50 μm

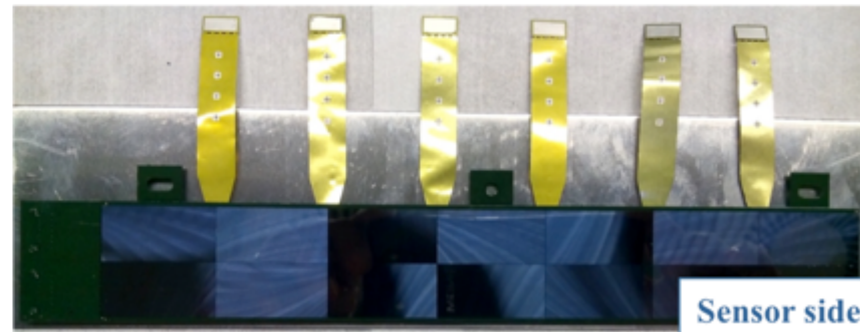
9 chips, stave length ~450 mm

## Outer Barrel

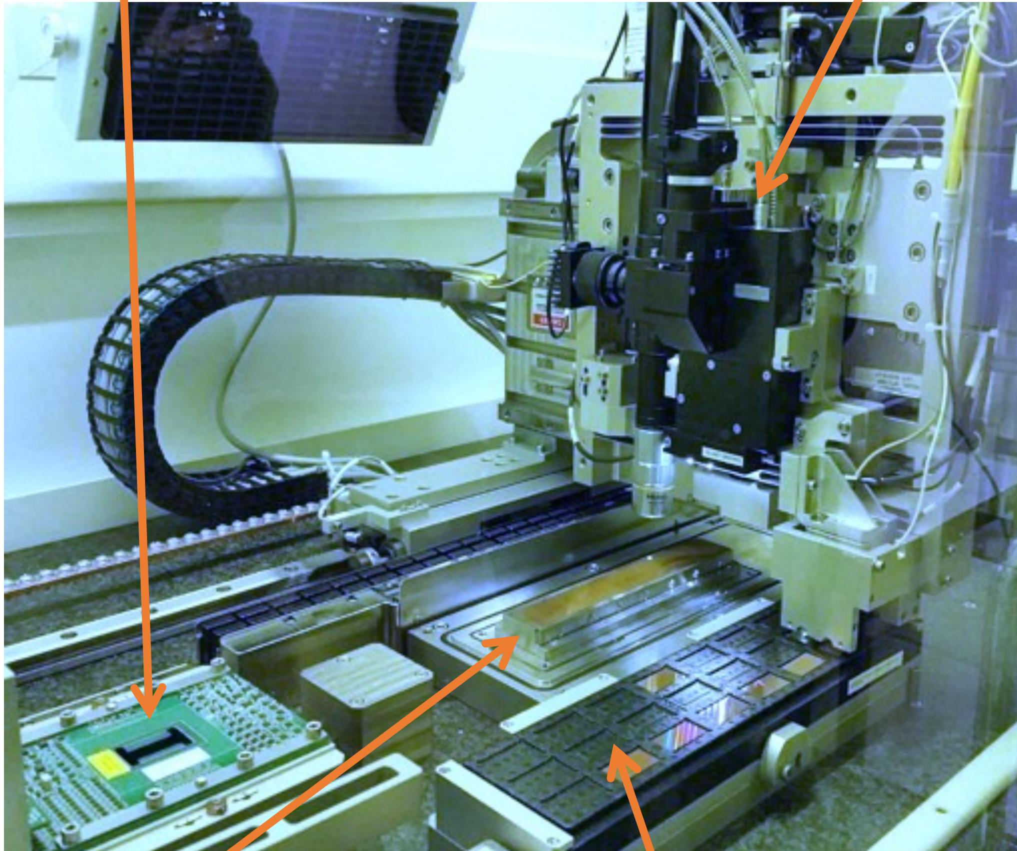


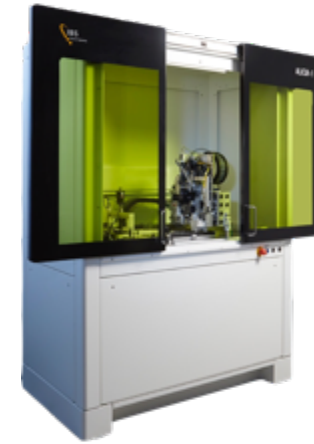

x-cables for connection to power bus

2x7 chips
Module length ~245 mm



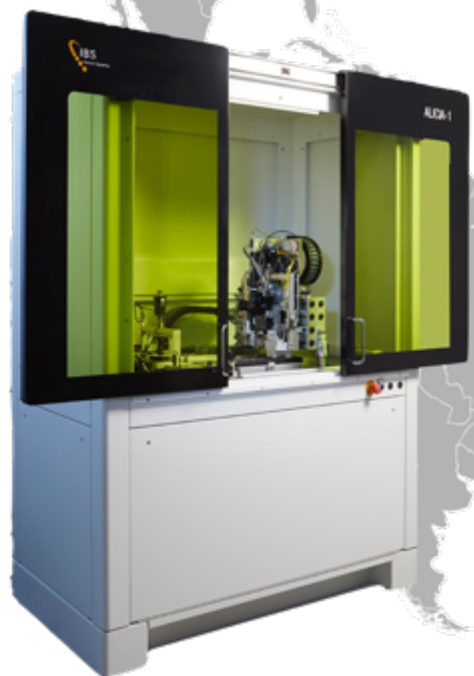
# OB Module Production



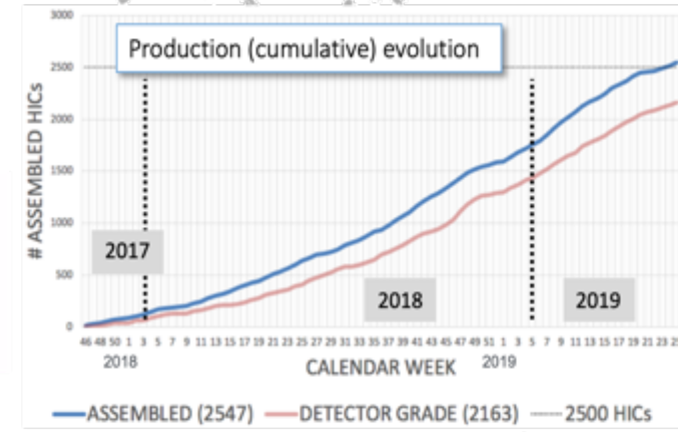
- Modules assembled with custom machine (ALICIA)
  - Aligned chips with +/- 5 μm precision
  - Can probe & automatic visual inspection
- Produced at 5 sites worldwide
  - Strasbourg, Bari, Liverpool, Pusan, Wuhan

# ALICE ITS2 Construction:
## Module assembly

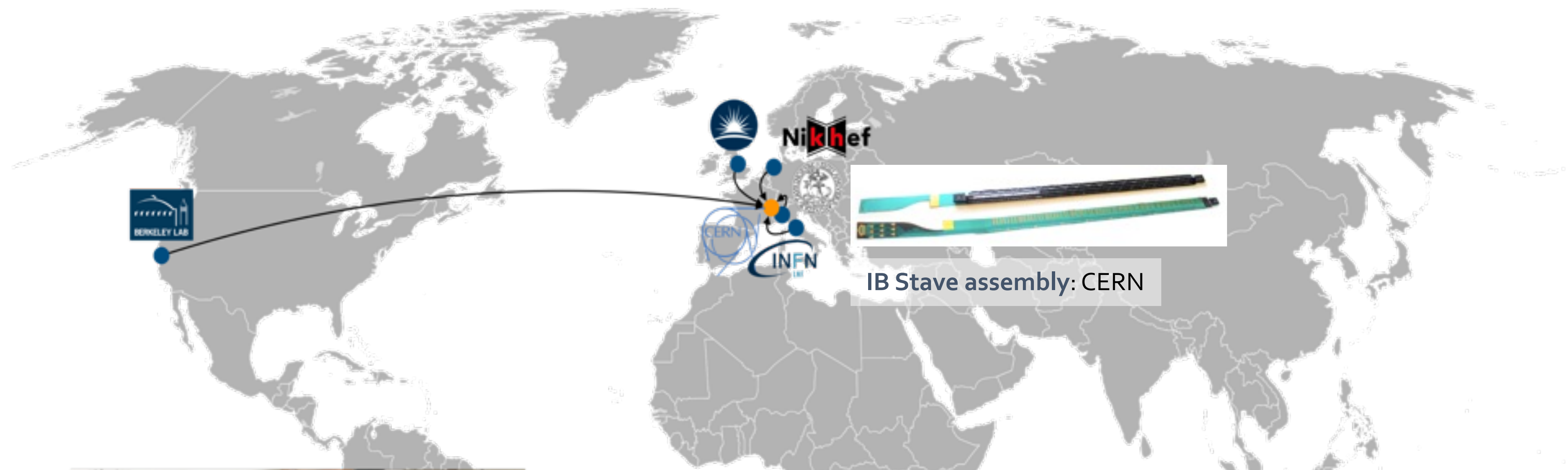


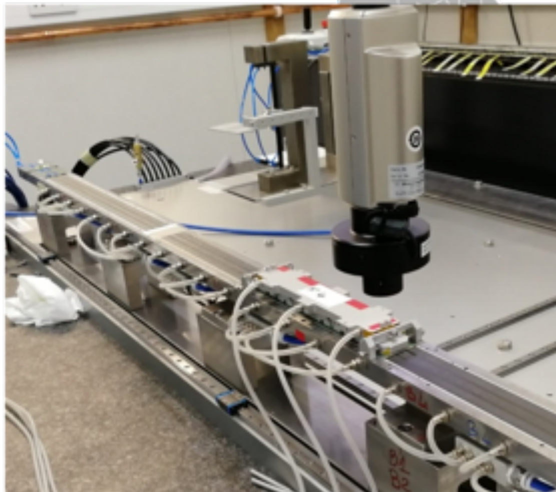
**Module assembly and distribution** (100 µm)
at Bari, Pusan, Liverpool, Strasbourg, Wuhan
done

**Stave assembly**



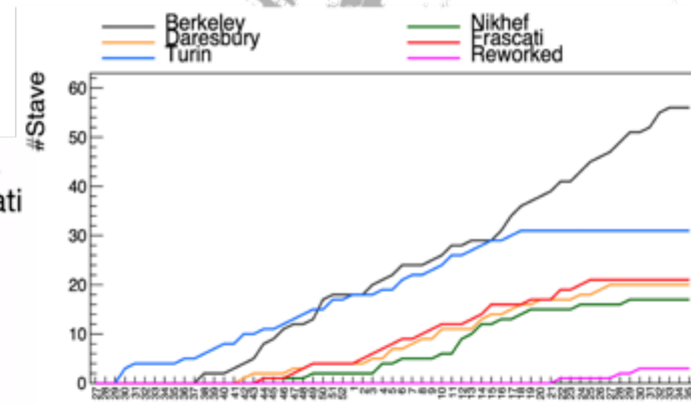
# ALICE ITS2 Construction:
## Stave assembly, detector integration



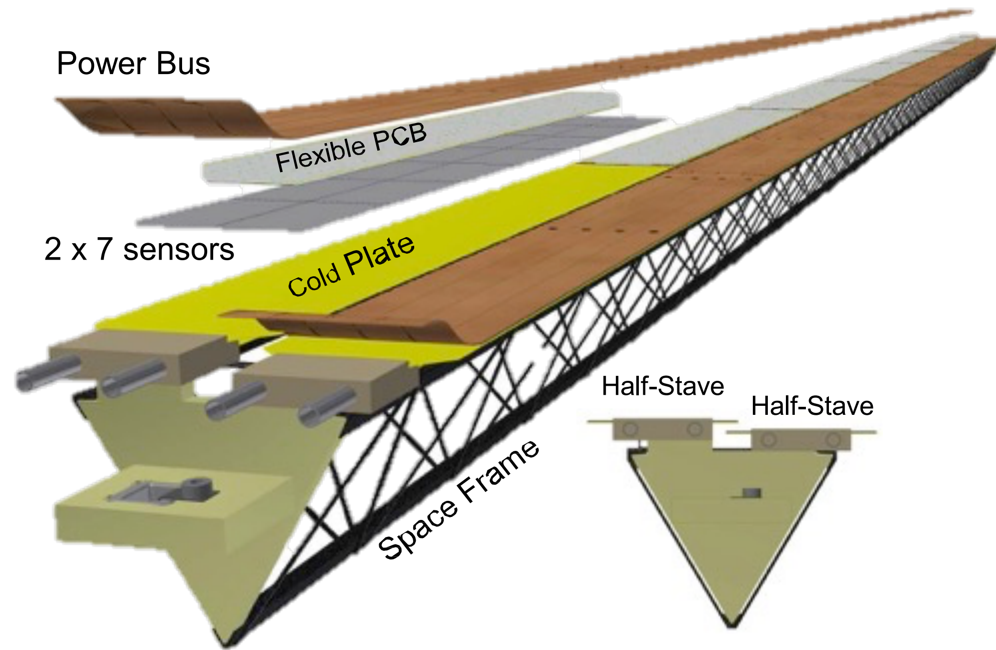
**Stave assembly**
at Berkley, Nikhef, Daresbury, Torino, Frascati
done

**Detector integration**
at CERN
done, to be installed at P2




Magnus Mager (CERN) | 6th Annual MT Meeting | 17.06.2020 |

# ITS Outer Barrel Stave Structure



Outer Barrel (OB)

**LBL built Middle Layers in Red**

<radius> (mm): **194, 247**, 353, 405

Nr. staves: **24, 30**, 42, 48

Nr. Chips/layer: **6048 (ML)**, 17740 (OL)

Power density < 100 mW / cm²

Length (mm): **900 (ML)**, 1500 (OL)

Nr. modules/stave: **4 (ML)**, 7 (OL)

Material thickness: ~ 1% $X_0$

Throughput (@100kHz): < 3Mb/s × $cm^{-2}$

# Stave Assembly Requirements

- OL (4 sites): 30 staves per site, 1 stave every 2 weeks
- ML (LBNL): 60 staves, 1 per week
- > 90% production yield
  - > 10 assembly steps → each must have ~99% yield
- Within 1 mm tolerance for planarity
  - Clearance for neighboring staves
- Noisy pixel rate below $10^{-5}$

# Stave Assembly Dependencies

- Each Stave takes ~5-6 days to complete
  - 1 per week requirement for ML
- Modules arriving from 5 different sites
- Carbon Fiber Cold Plates & Space Frames from CERN
- Power & Bias Bus shipped through CERN

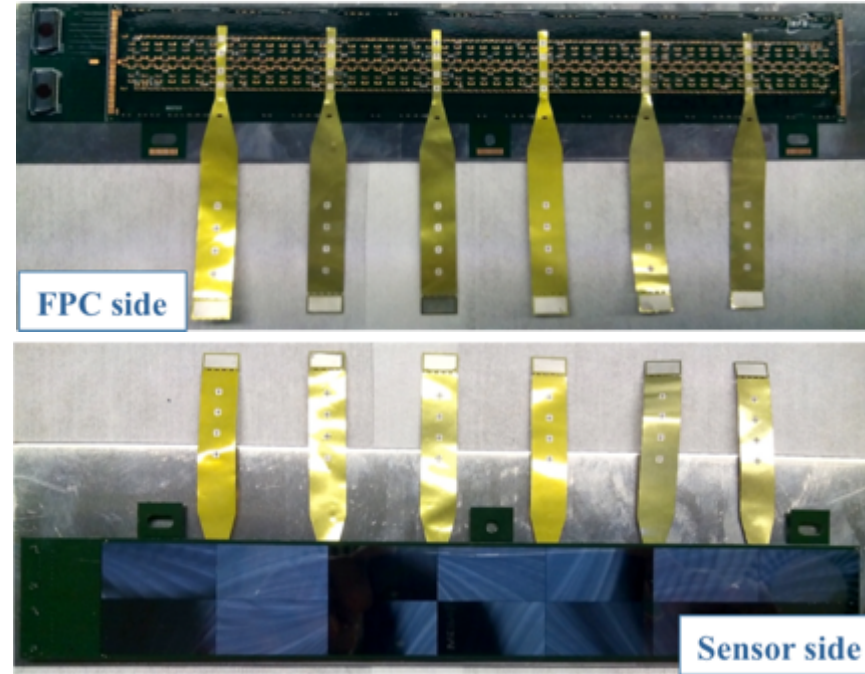
| | | 9:00 | 9:30 | 10:00 | 10:30 | 11:00 | 11:30 | 12:00 | 12:30 | 13:00 | 13:30 | 14:00 | 14:30 | 15:00 | 15:30 | 16:00 | 16:30 | 17:00 | 17:30 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DAY 1 | CMM BASE STATION | HSR METR. | | CP PLANARITY | | | | | | | HSL ASSEMBLY | | | | | | GLUE DRYING | | |
| | HS TEST STATION | | | HSR SOLDERING | | | | TEST | UARM GLUING | | TEST | | | | | | | | |
| | CMM SPACE FRAME | | | | | | | | | | | | | | | | | | |
| | CMM METROLOGY | | | | | | | | | | | | | | | | | | |
| | STAVE TEST STATION | | | | | | | | | | | | | | | | | | |
| DAY 2 | CMM BASE STATION | HSL METR. | | | | | | | | | HSR TO SF | | | | | | | | |
| | HS TEST STATION | | | HSL SOLDERING | | | | TEST | UARM GLUING | | TEST | | | | | | | | |
| | CMM SPACE FRAME | | | | | | | | | | | | HSR TO SF | | GLUE DRYING | | | | |
| | CMM METROLOGY | | | | | | | | | | | | | | | | | | |
| | STAVE TEST STATION | | | | | | | | | | | | | | | | | | |
| DAY 3 | CMM BASE STATION | HSL TO SF | | | | CP PLANARITY | | HSR ASSEMBLY | | | | | | GLUE DRYING | | | | | |
| | HS TEST STATION | | | | | | | | | | | | | | | | | | |
| | CMM SPACE FRAME | | | HSL TO SF | | GLUE DRYING | | | | | | | | | | | | | |
| | CMM METROLOGY | | | | | | | | | | | | | | | | | | |
| | STAVE TEST STATION | | | | | | | | | | | | | | | | | | |
| DAY 4 | CMM BASE STATION | HSR METR. | | | | | | CP PLANARITY | | | HSL ASSEMBLY | | | | | | GLUE DRYING | | |
| | HS TEST STATION | | | HSR SOLDERING | | | | TEST | UARM GLUING | | TEST | | | | | | | | |
| | CMM SPACE FRAME | | | | | | | | | | | | | | | | | | |
| | CMM METROLOGY | | | STAVE METROLOGY | | | | | | | | | | | | | | | |
| | STAVE TEST STATION | | | | | | | PB/BB/FB SOLDERING | | | | STAVE TEST | | | | | | | |
| DAY 5 | CMM BASE STATION | HSL METR. | | | | | | | | | HSR TO SF | | | | | | | | |
| | HS TEST STATION | | | | | | | | | | | | HSR TO SF | | GLUE DRYING | | | | |
| | CMM SPACE FRAME | | | HSL SOLDERING | | | | TEST | UARM GLUING | | TEST | | | | | | | | |
| | CMM METROLOGY | | | | | | | | | | | | | | | | | | |
| | STAVE TEST STATION | PB FOLDING & U-ARM GLUING | | | | | | | | | | STAVE TEST | | | | | | | |

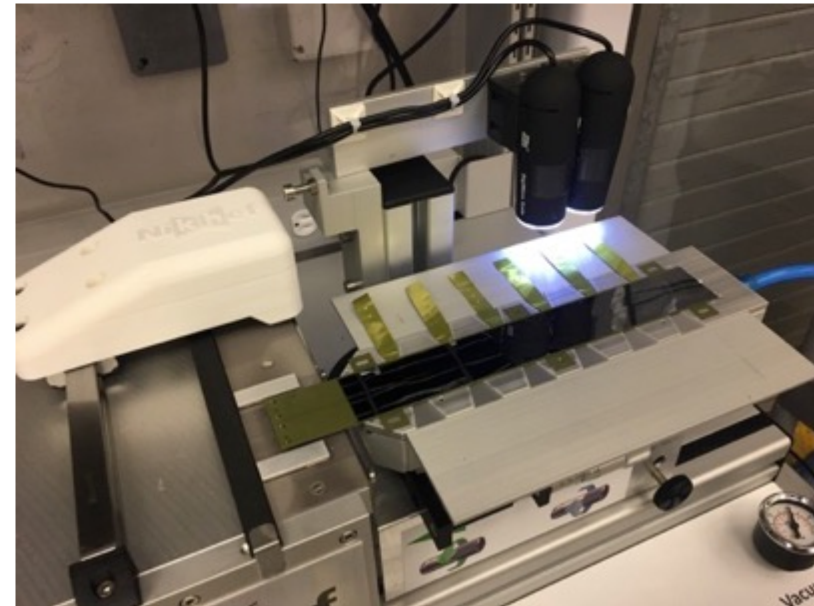
# Infrastructure for Stave Assembly

- 3 separate spaces
  - Module testing (small)
  - HS assembly
  - Stave completion

# ITS ML Assembly at LBL

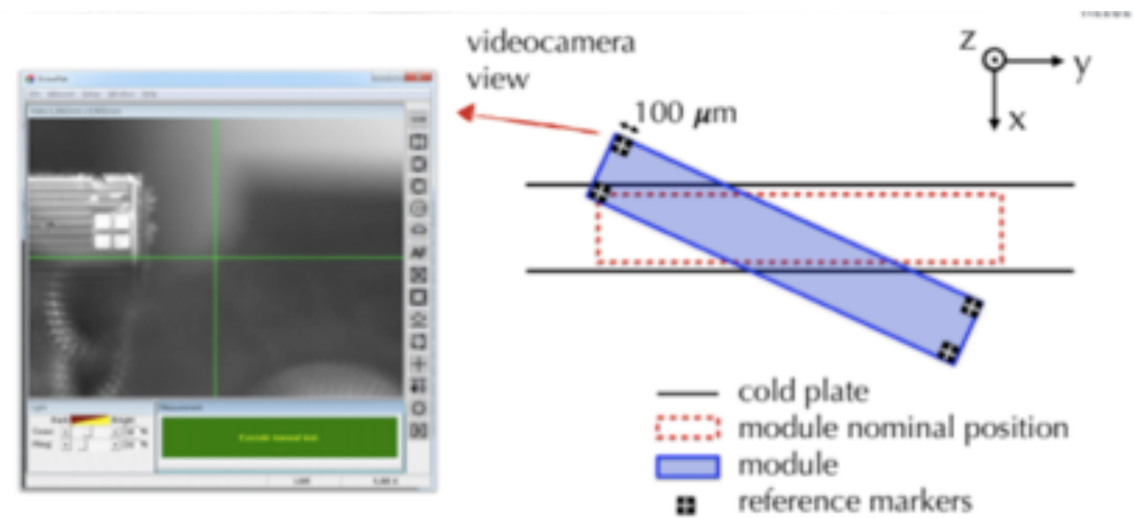
- HIC arrives
  - Tested and tab cut

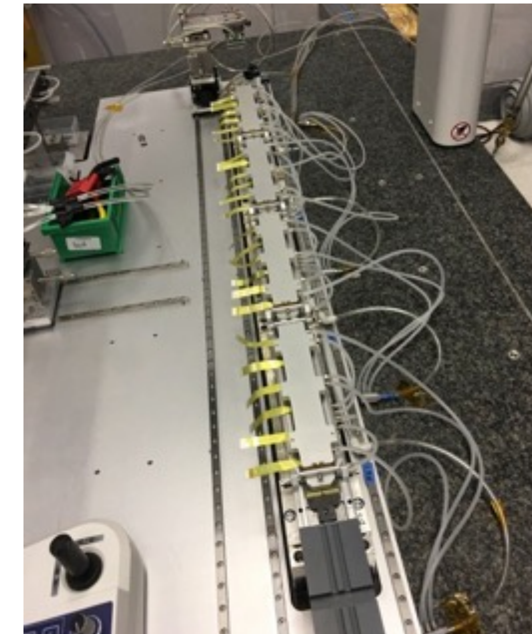


# ITS ML Assembly at LBL

- HIC arrives
  - Tested and tab cut
- 4 HICs glued to CP (1 HS)
  - Aligned within 20 μm of nominal



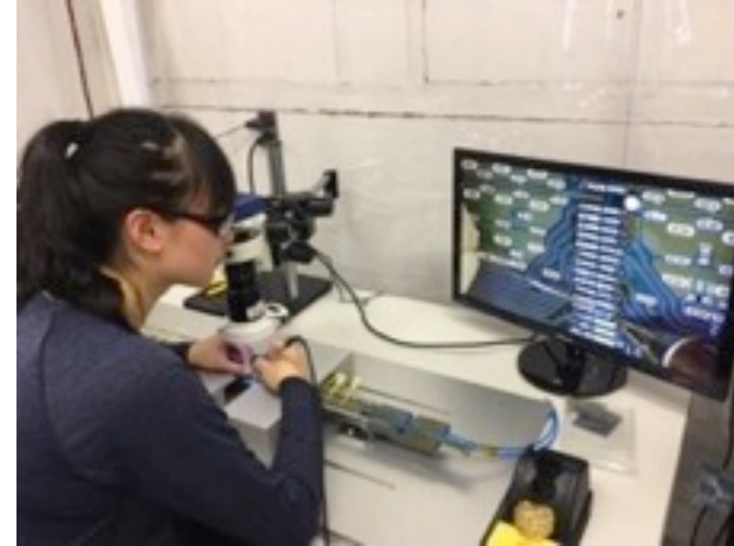



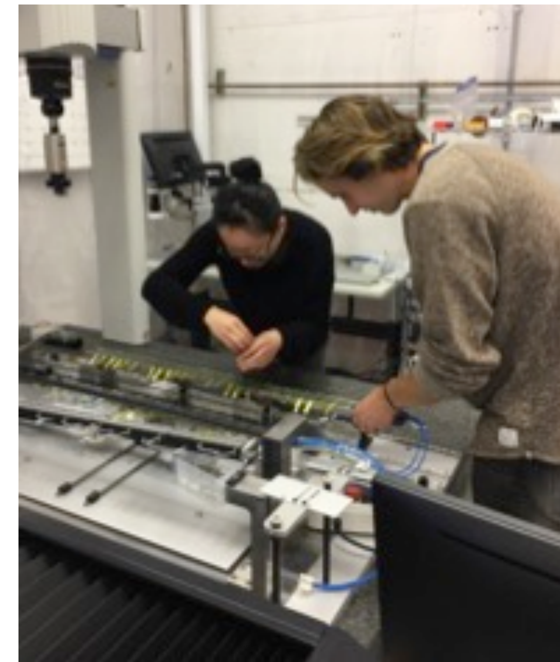
# ITS ML Assembly at LBL

ALICE

BERKELEY LAB

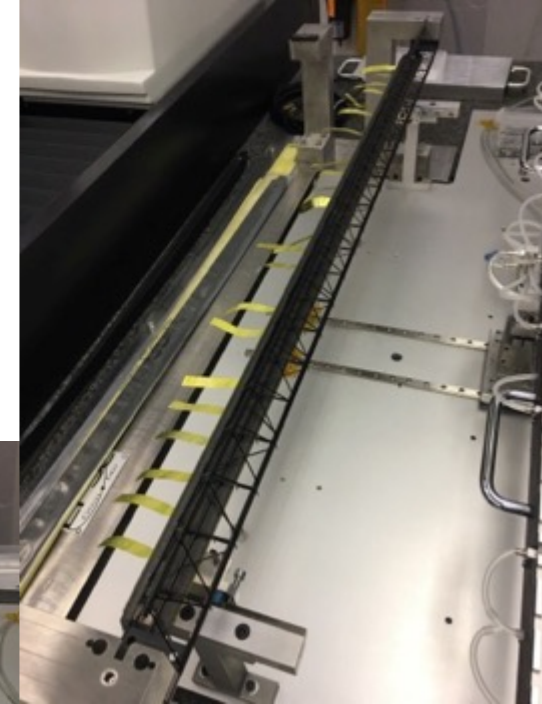
- HIC arrives
  - Tested and tab cut
- 4 HICs glued to CP (1 HS)
  - Aligned within 20 μm of nominal
- HS soldered & tested

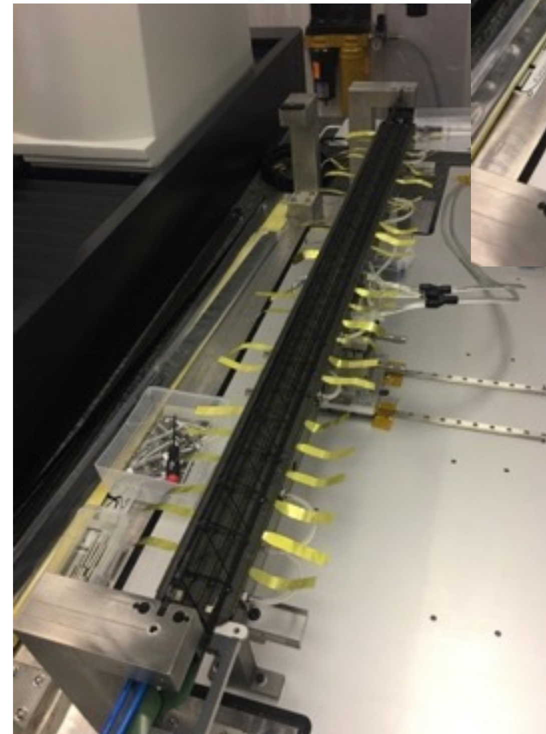




# ITS ML Assembly at LBL

- HIC arrives
  - Tested and tab cut
- 4 HICs glued to CP (1 HS)
  - Aligned within 20 μm of nominal
- HS soldered & tested
- HS aligned & glued under SF



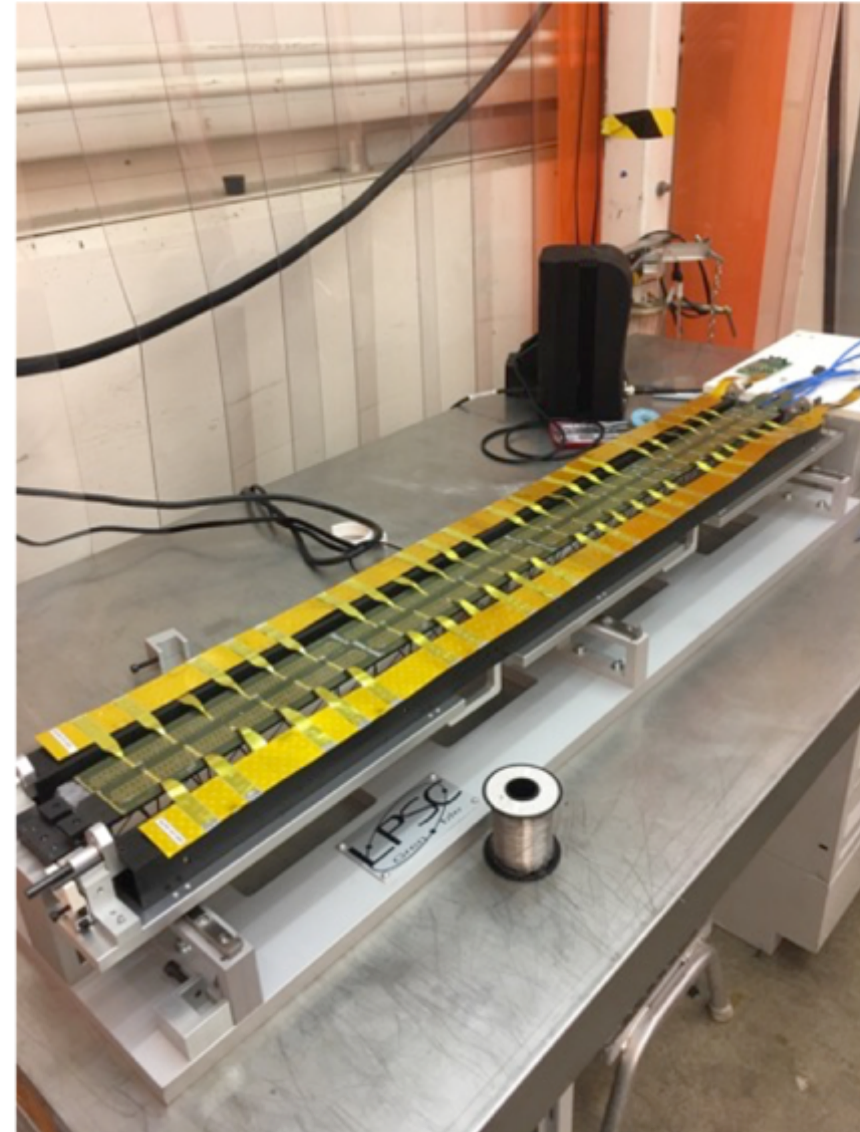


# ITS ML Assembly at LBL

- HIC arrives
  - Tested and tab cut
- 4 HICs glued to CP (1 HS)
  - Aligned within 20 μm of nominal
- HS soldered & tested
- HS aligned & glued under SF
- Stave gets final metrology

# ITS ML Assembly at LBL

- HIC arrives
  - Tested and tab cut
- 4 HICs glued to CP (1 HS)
  - Aligned within 20 μm of nominal
- HS soldered & tested
- HS aligned & glued under SF
- Stave gets final metrology
- PB soldered to Stave & tested



# ITS ML Assembly at LBL

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- HIC arrives
  - Tested and tab cut
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- HS soldered & tested
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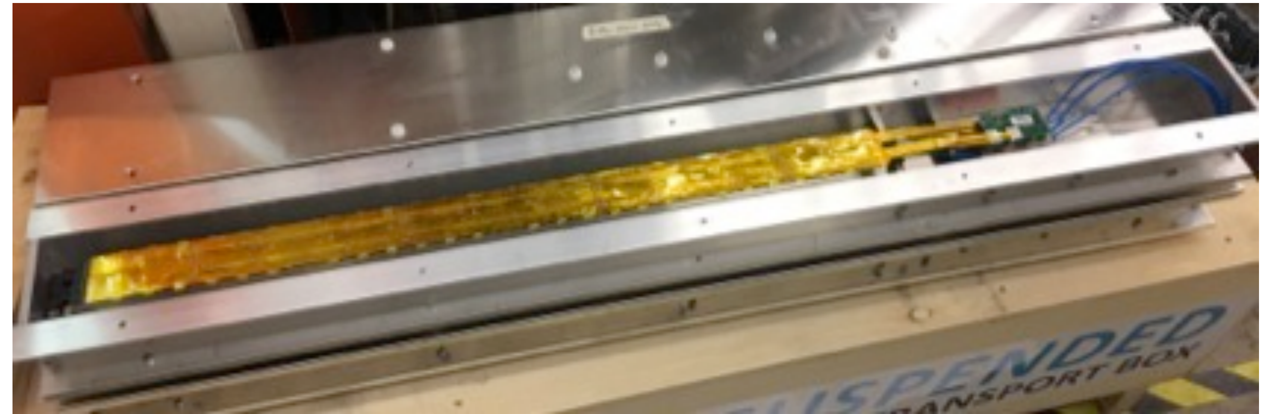
- Stave is folded & tested

# ITS ML Assembly at LBL

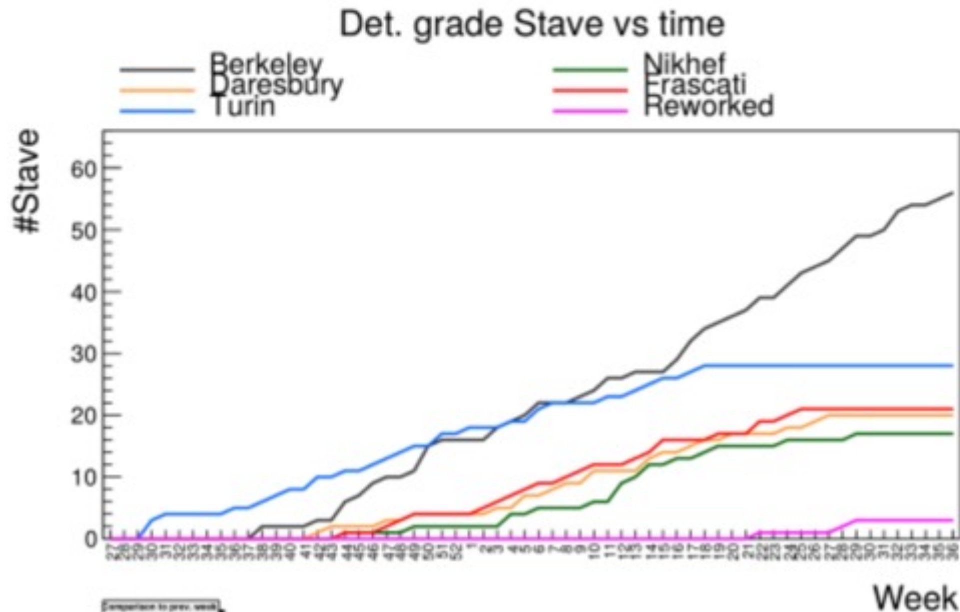
- HIC arrives
  - Tested and tab cut
- 4 HICs glued to CP (1 HS)
  - Aligned within 20 μm of nominal
- HS soldered & tested
- HS aligned & glued under SF
- Stave gets final metrology
- PB soldered to Stave & tested
- Stave is folded & tested
- Stave is boxed & stored/shipped to CERN

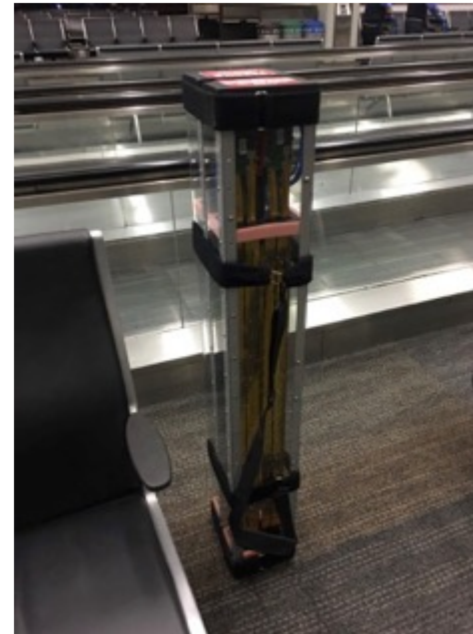
**Production completed in October '19**

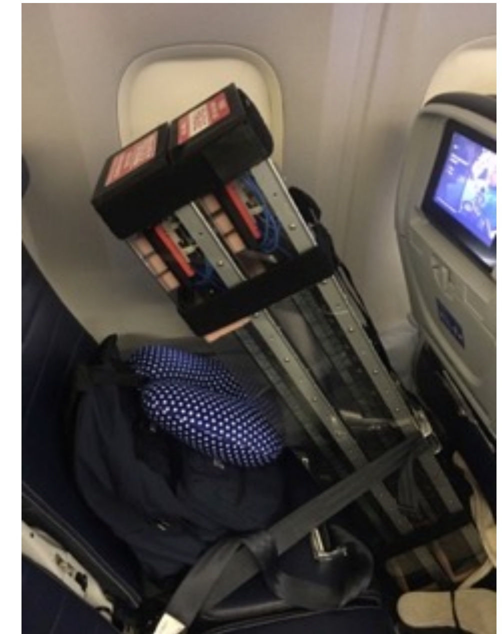


# ITS ML Assembly at LBL

- Planned deliverables: 60 staves (54 + 6 spares)
  - Constructed 68 staves, 64 detector grade (no more than 1 dead chip per HS)
  - Rate ~1/week
- 17 trips made – delivered 4 at a time
  - Last trip made October 2019



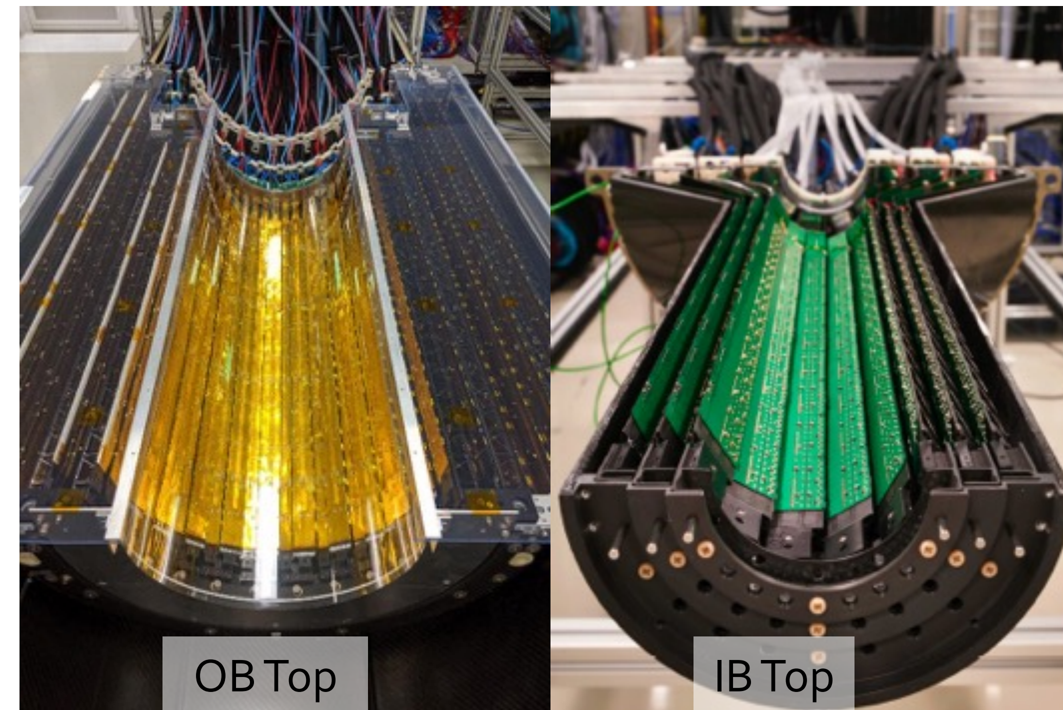





https://newscenter.lbl.gov/2019/09/19/how-to-get-a-particle-detector-on-a-plane/

# ALICE ITS2 Half Barrel Assembly

- All half barrels complete by end of 2019
- Commissioning began mid 2019 – 2021 (before installation into cavern)




~72000 chips (65% yield)
~2600 modules (85% yield)
~280 staves (95% yield)

# ALICE ITS2 Commissioning

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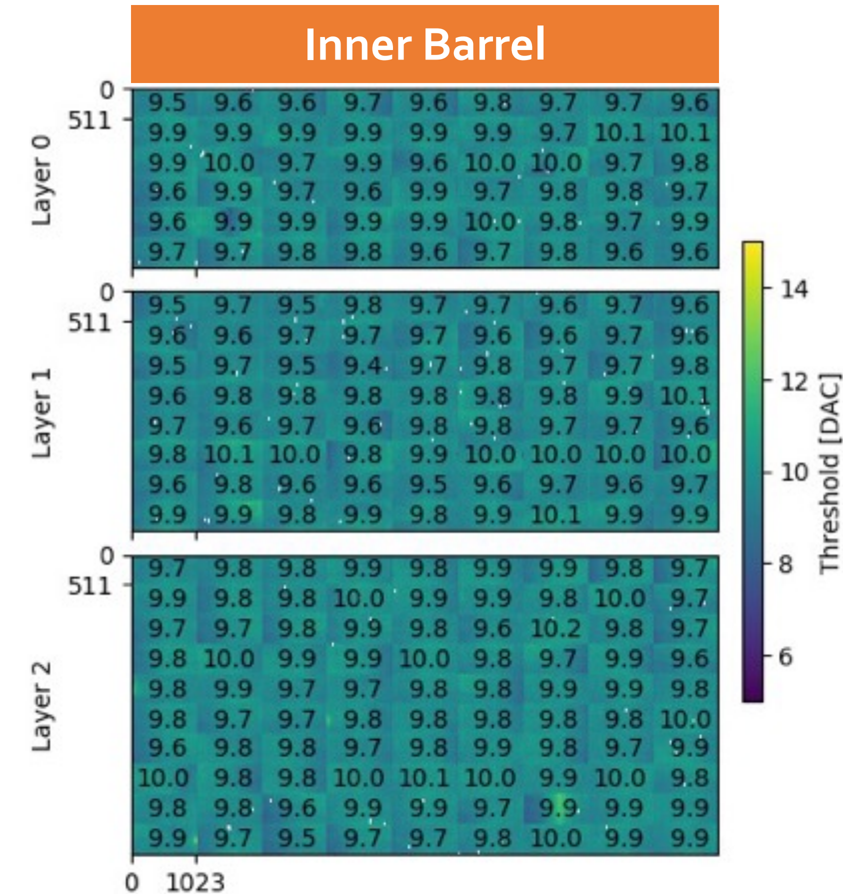
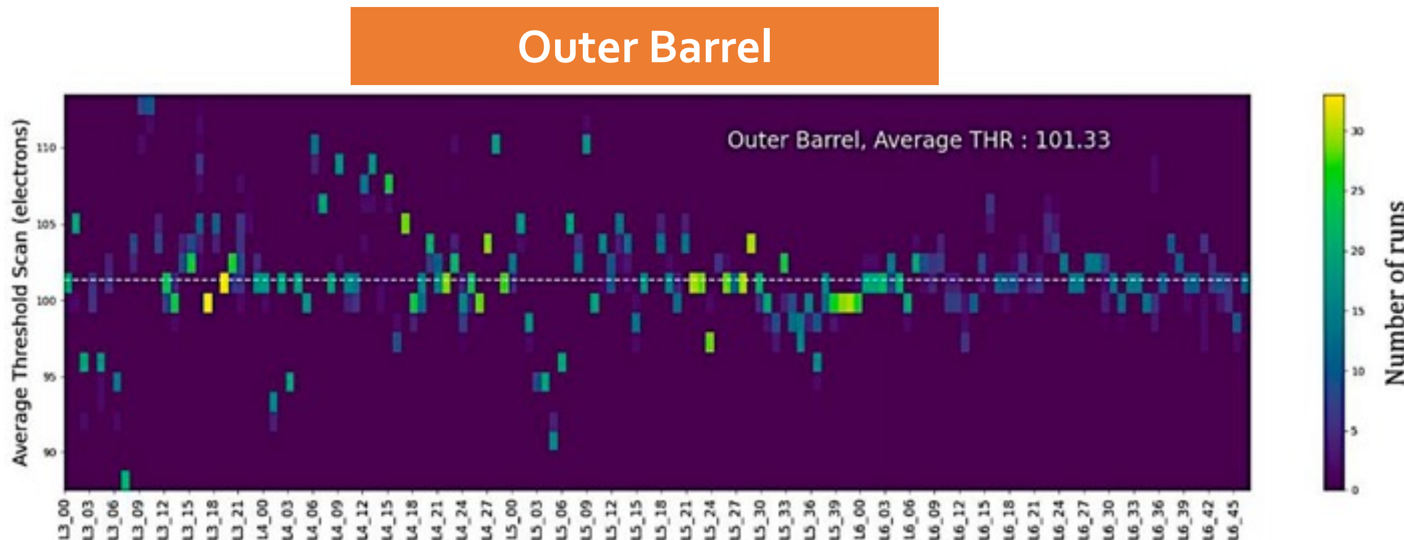
- On-surface commissioning
  - 24/7 from July 2019 – December 2020
  - Verification of detector performance and stability
    - Monitor voltage, current, temperature
    - Threshold scans, fake-hit rate runs, readout tests

# ALICE ITS2 Commissioning

- On-surface commissioning
  - 24/7 from July 2019 – December 2020
  - Verification of detector performance and stability
    - Monitor voltage, current, temperature
    - **Threshold scans**, fake-hit rate runs, readout tests

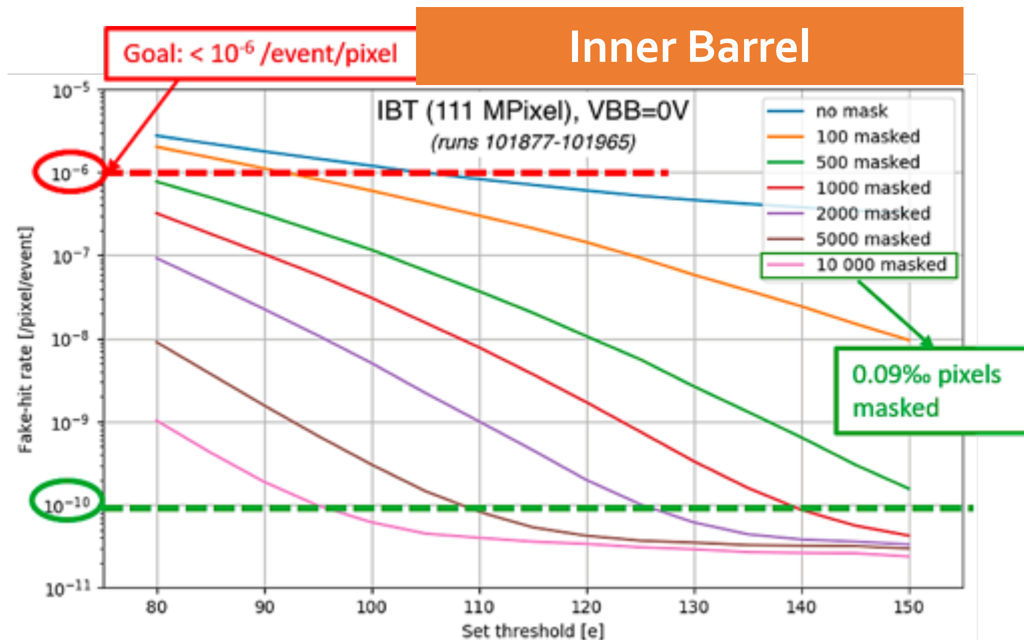


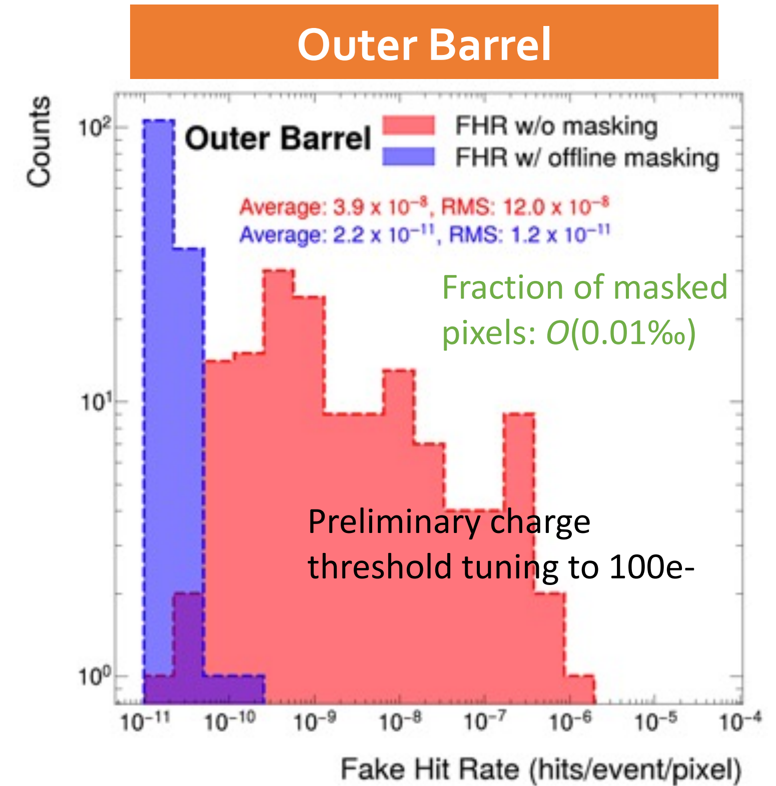




Threshold tuning is effective
Good uniformity
< 1000 dead pixels in IB

# ALICE ITS2 Commissioning

- On-surface commissioning
  - 24/7 from July 2019 – December 2020
  - Verification of detector performance and stability
    - Monitor voltage, current, temperature
    - Threshold scans, **fake-hit rate runs**, readout tests



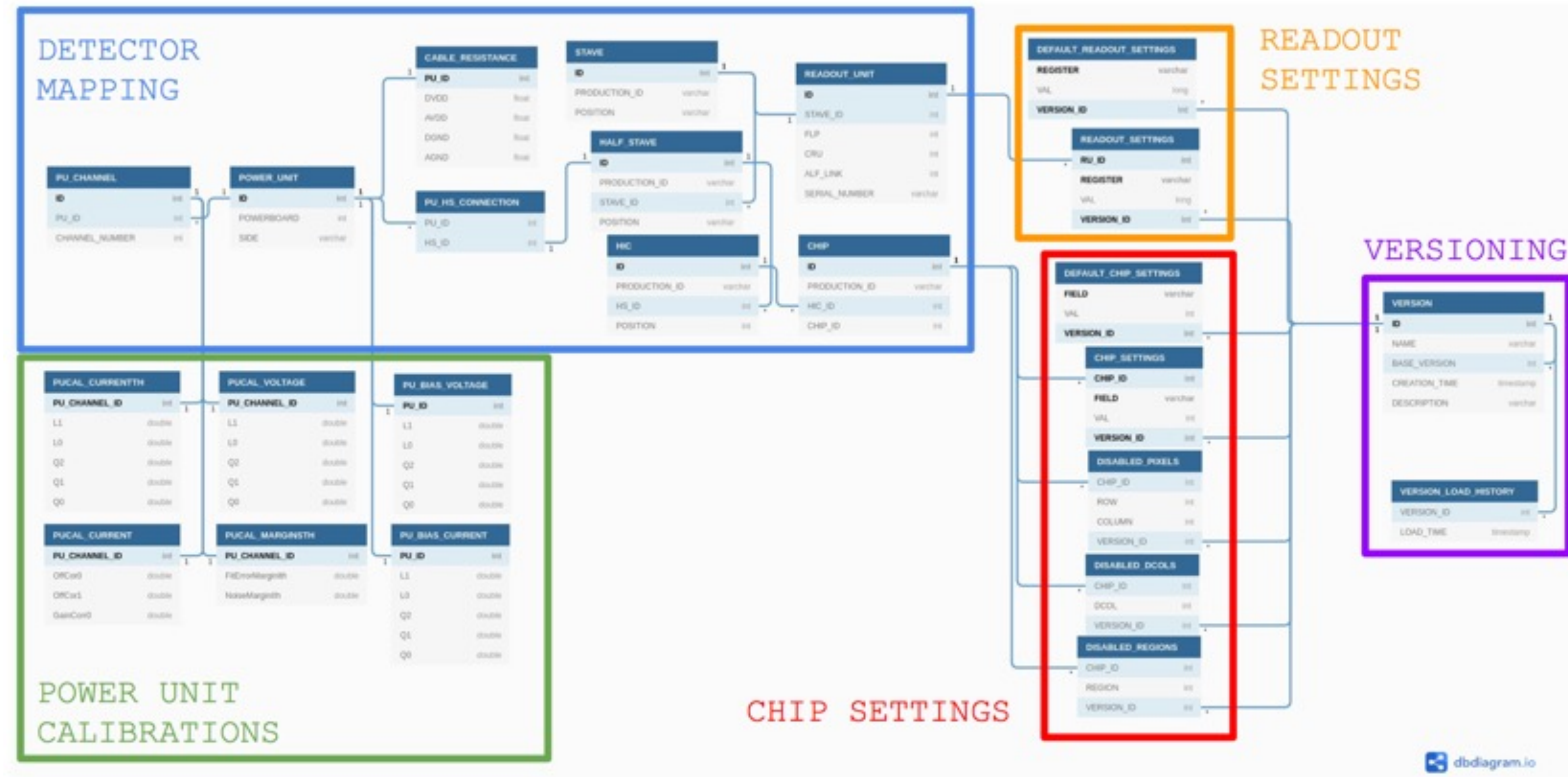

Fraction of masked pixels < 0.1 % for IB & OB

Fake-hit rate < $10^{-10}$/pixel/event

Very quiet detector!

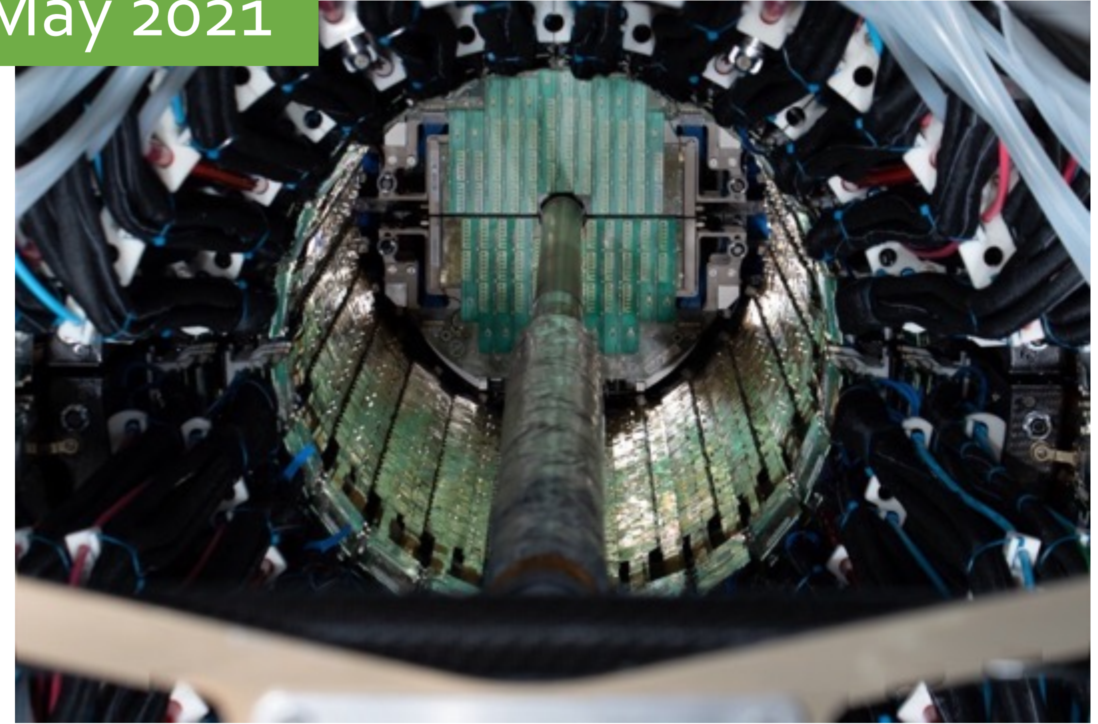
# ALICE ITS Configuration Database

- Creation & maintenance LBNL responsibility
- Oracle (i.e. SQL)
  - Standard for CERN databases
- Relational db
- Tools to get information in and out
  - Python, sql, c++, wincc



# ITS2 into the cavern

OB installed April 2021
IB installed May 2021

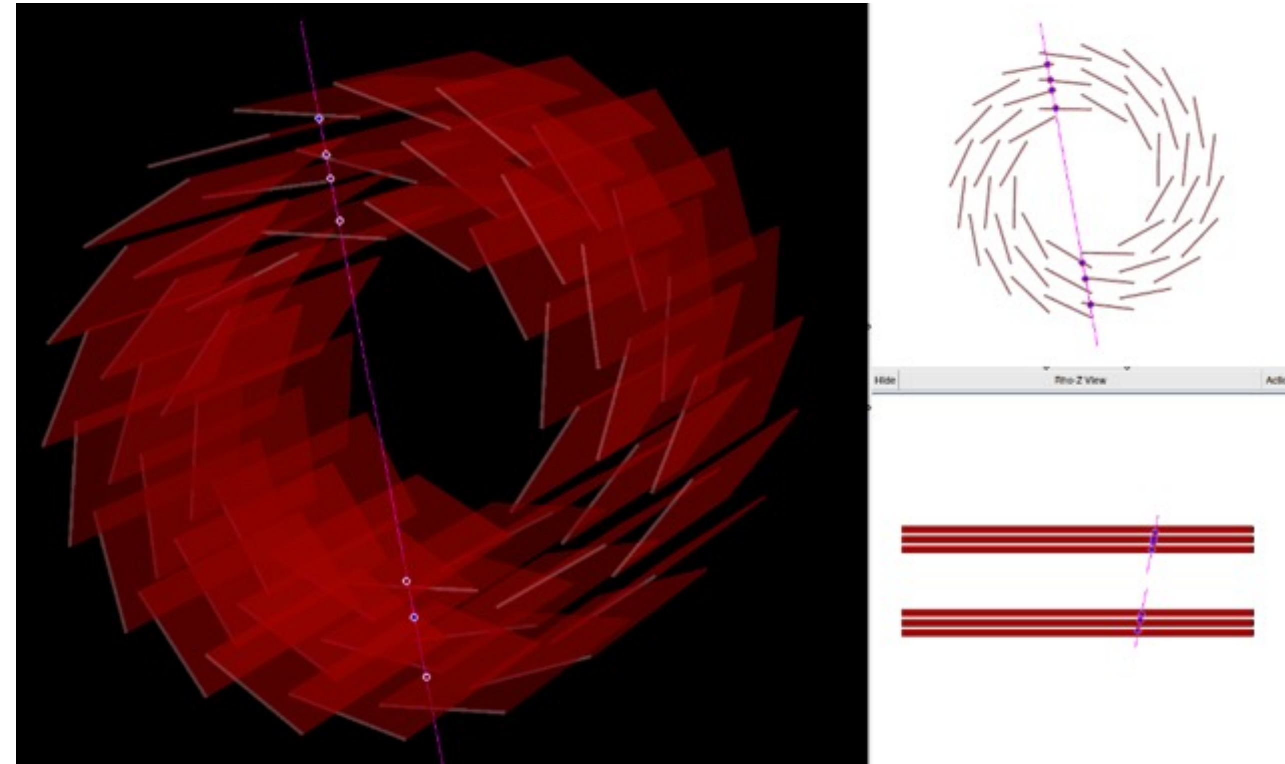


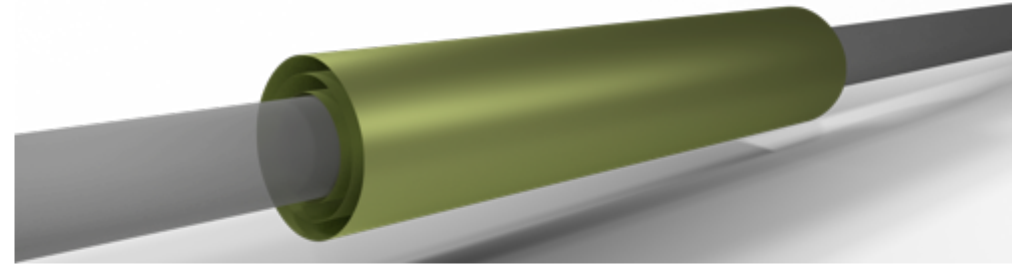
Commissioning ongoing – will be ready for data taking when LHC turns back on

# ALICE ITS2 Commissioning

- In cavern commissioning
  - Standalone (April – June 2021)
    - Similar to on-surface commissioning
      - Detector monitoring, scans
    - Central system integration
  - Global (July – December 2021)
    - Validation/finalization of online data processing/monitoring
    - Detector alignment & calibration
    - Technical & physics runs

Cosmic Track from the full IB





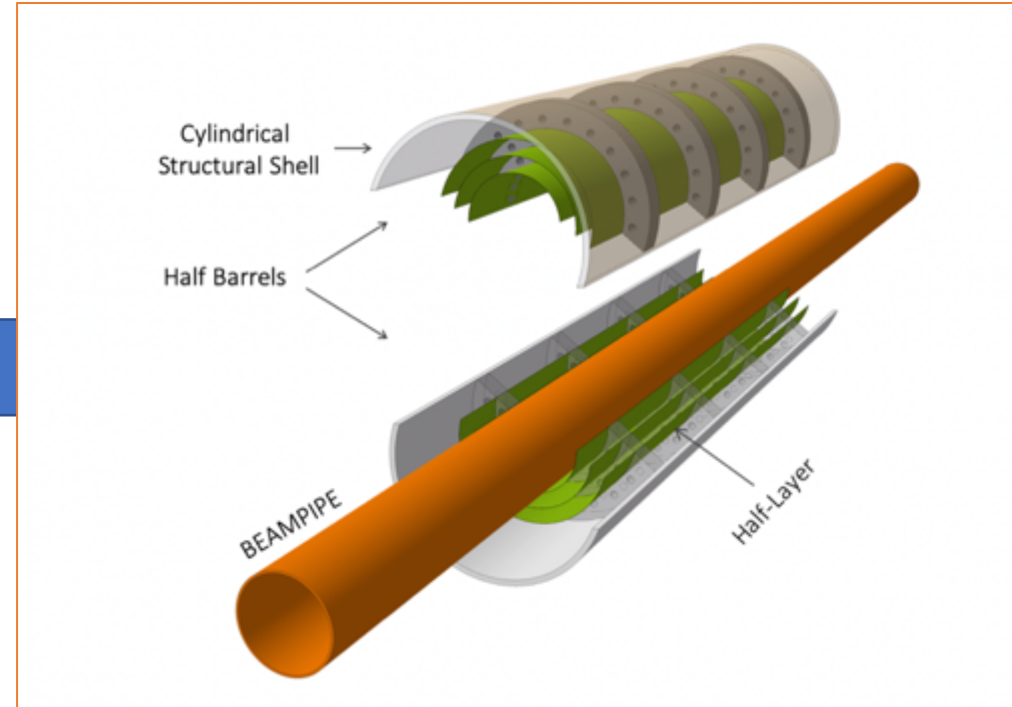
# What comes next?

ITS3: Thinner & closer to the beam pipe

# ITS3 Detector Layout

Replace

with



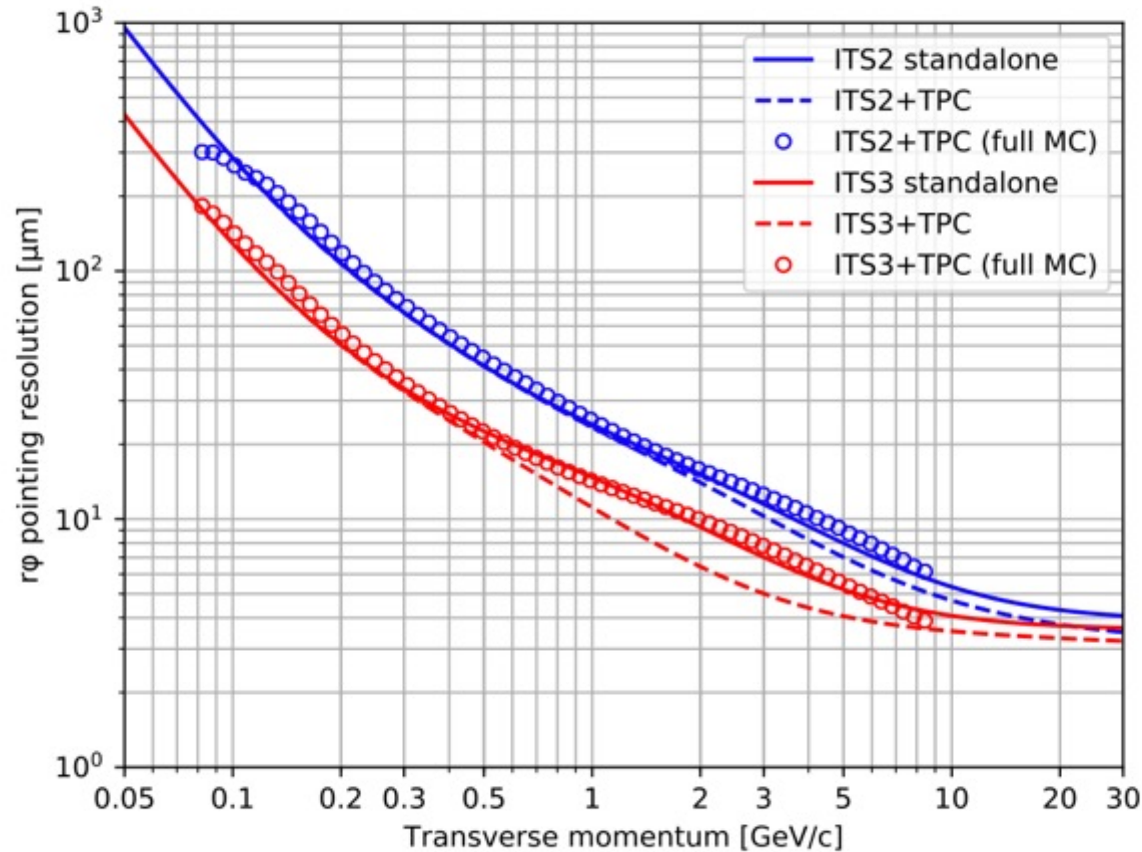

during LS3

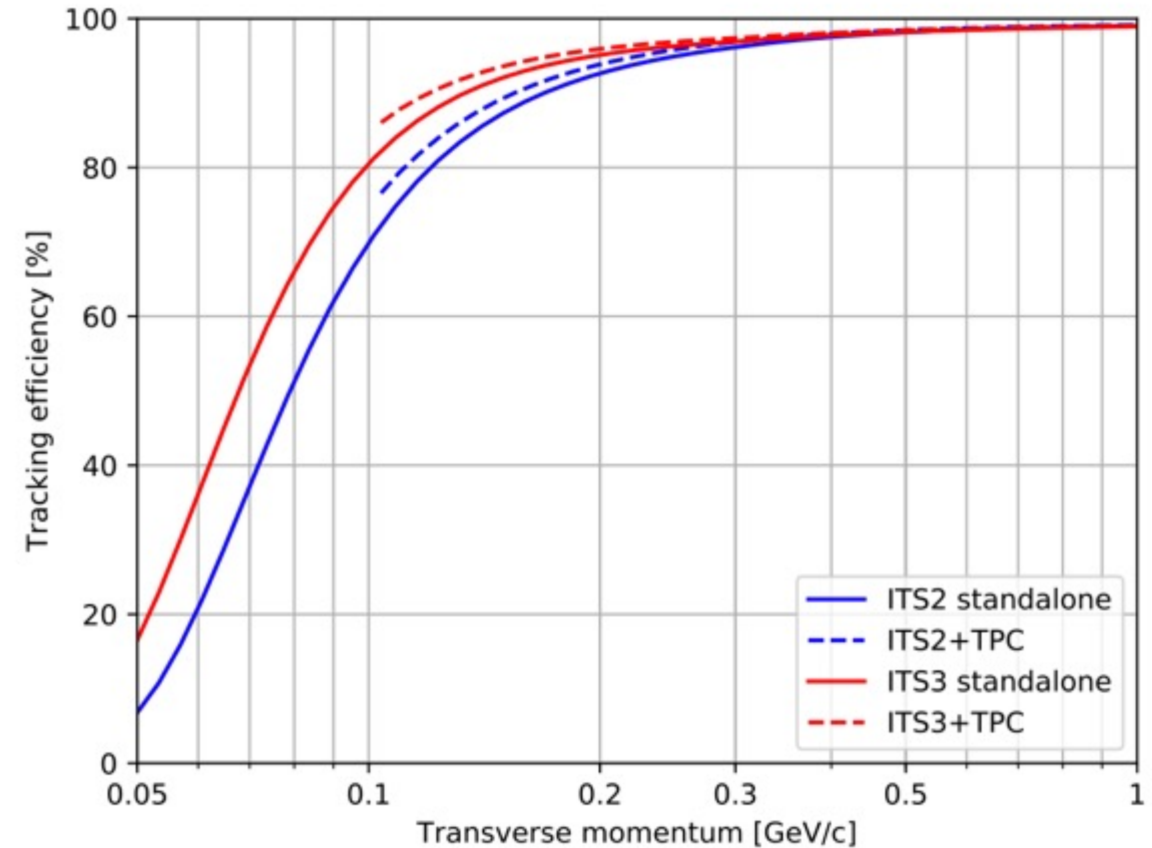
Improve pointing resolution
- Closer to the beam pipe: 23 mm → 18 mm

Better tracking resolution (especially at low $p_T$)
- Less material: 0.3% $X_0$ → ~0.03% $X_0$

MAPS sensors
- Wafer-scale (up to ~28 x 10 cm)
- Ultra-thin (20 – 40 μm)
- Bent (R = 18, 24, 30 mm)

# Improvement with ITS3 over ITS2



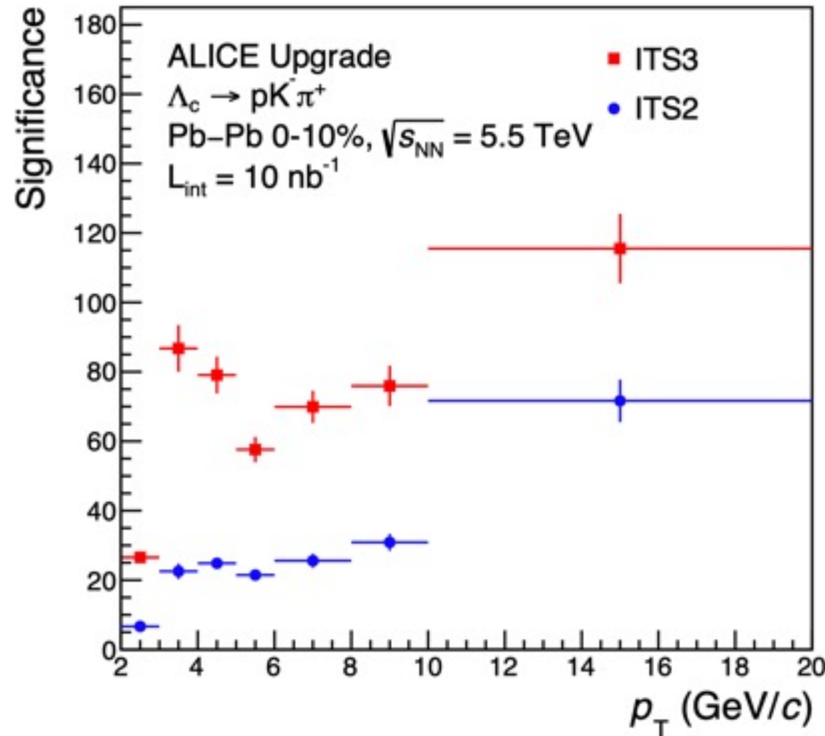



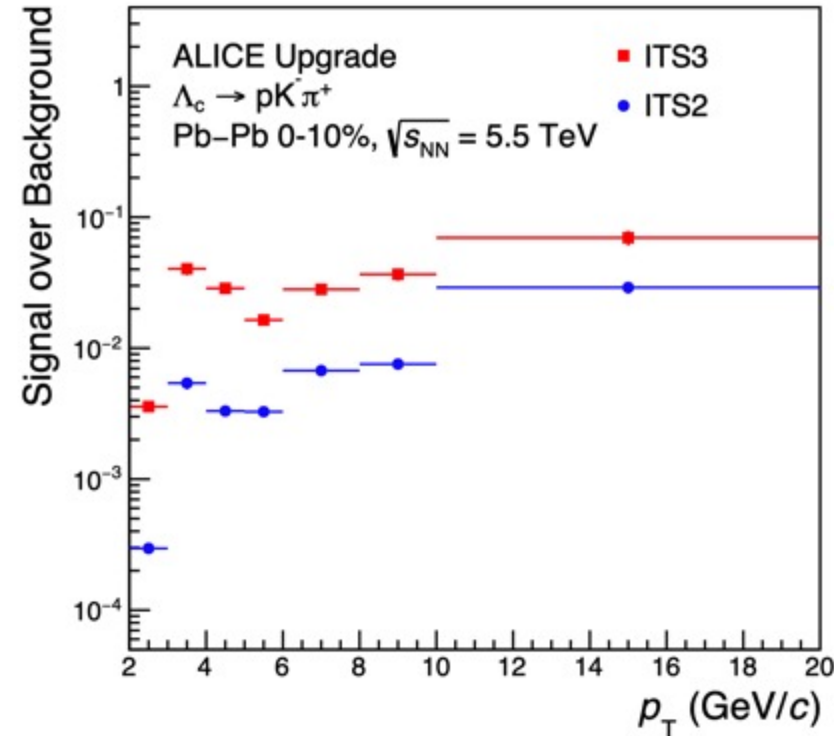

ALICE-PUBLIC-2018-013

Pointing Resolution 2x better

Improved tracking efficiency for low $p_T$

# ITS3 Physics: $\Lambda_c$ improvement

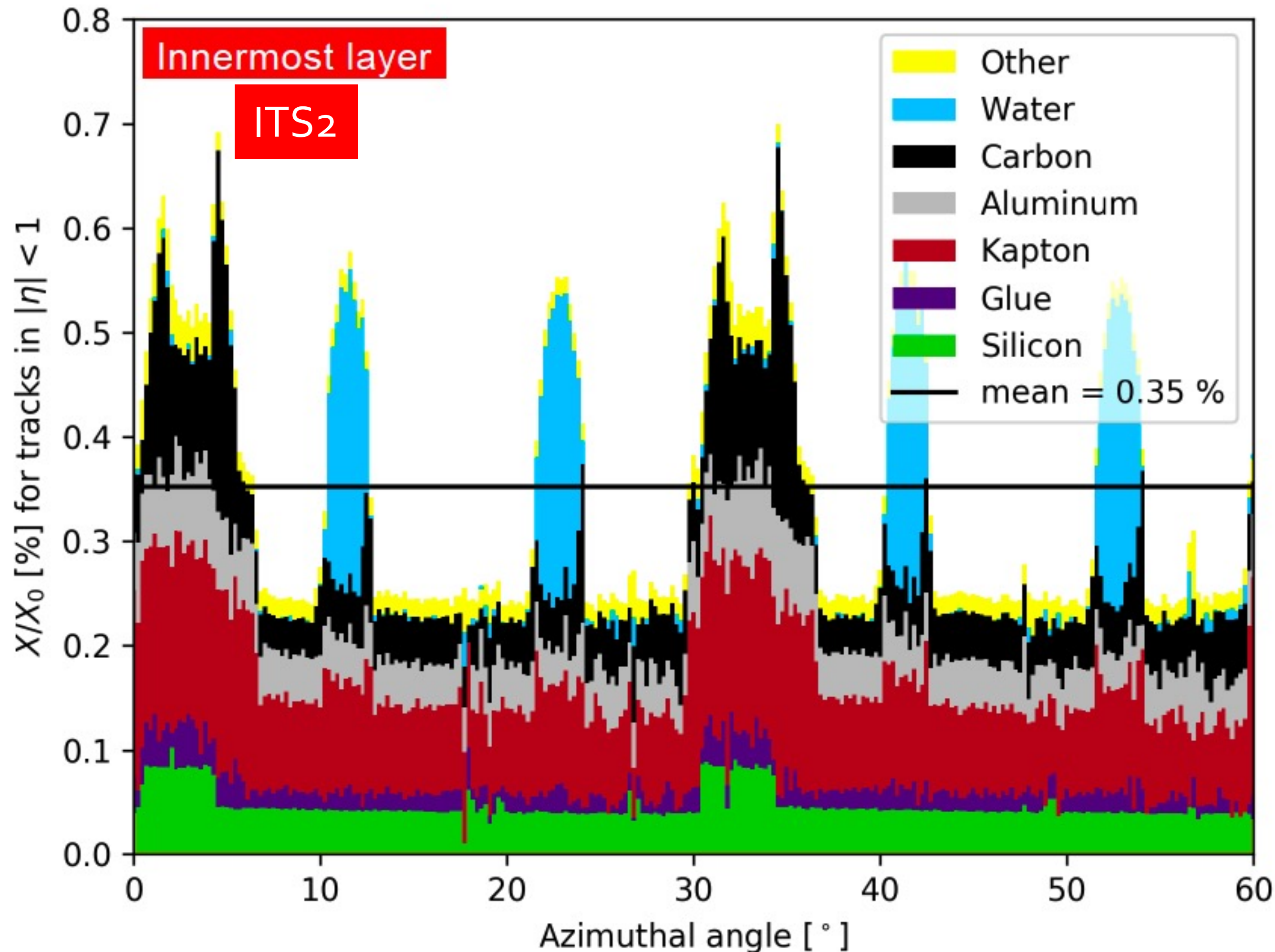



- Helped by improved pointing resolution
- Measurement in 0-10% centrality (0-20% with ITS2)
- Crucial for refining the total charm cross section measurement

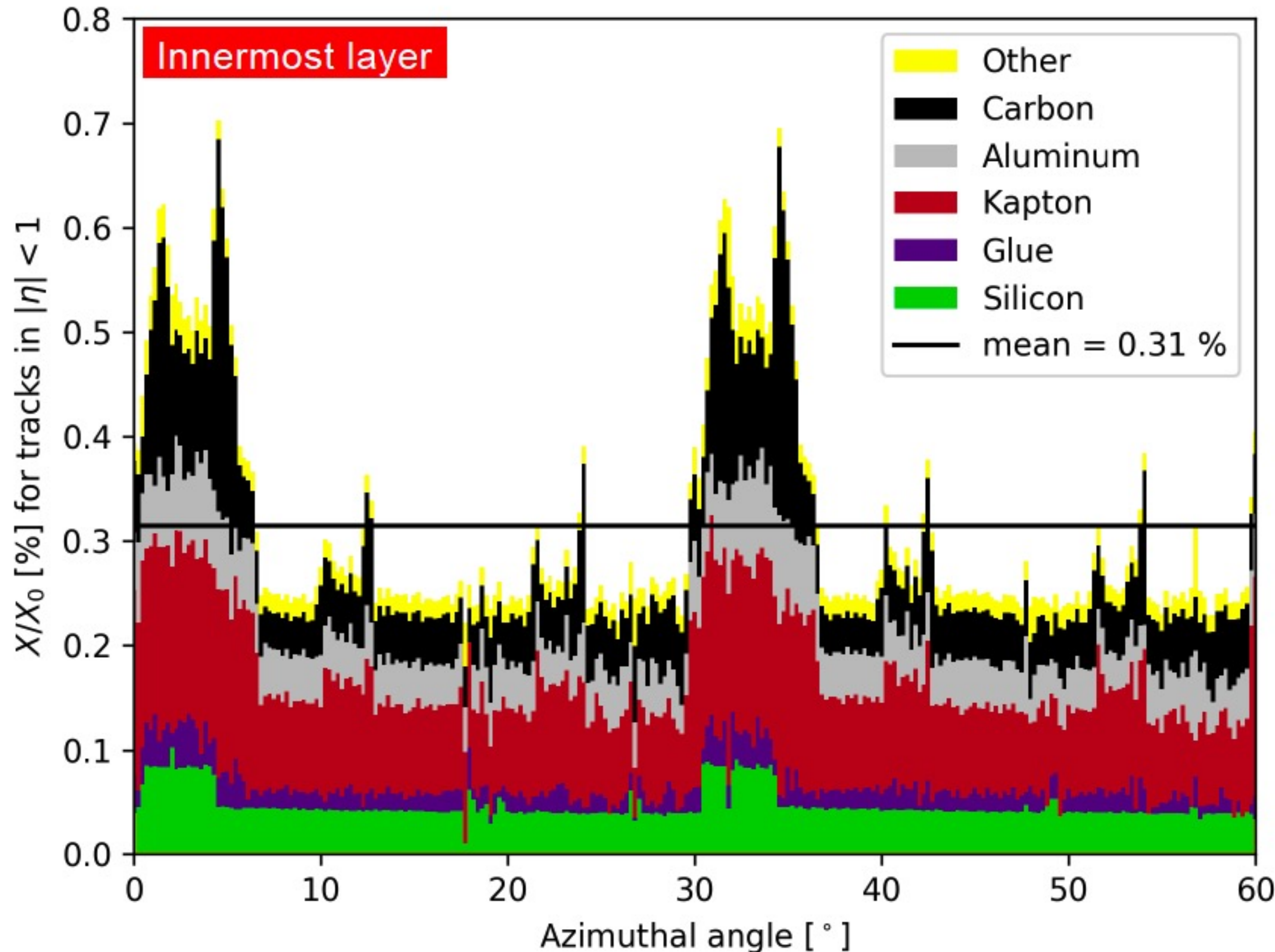
EoI for an ALICE ITS Upgrade in LS3, ALICE-PUBLIC-2018-013

# How?→Reduce Material Budget



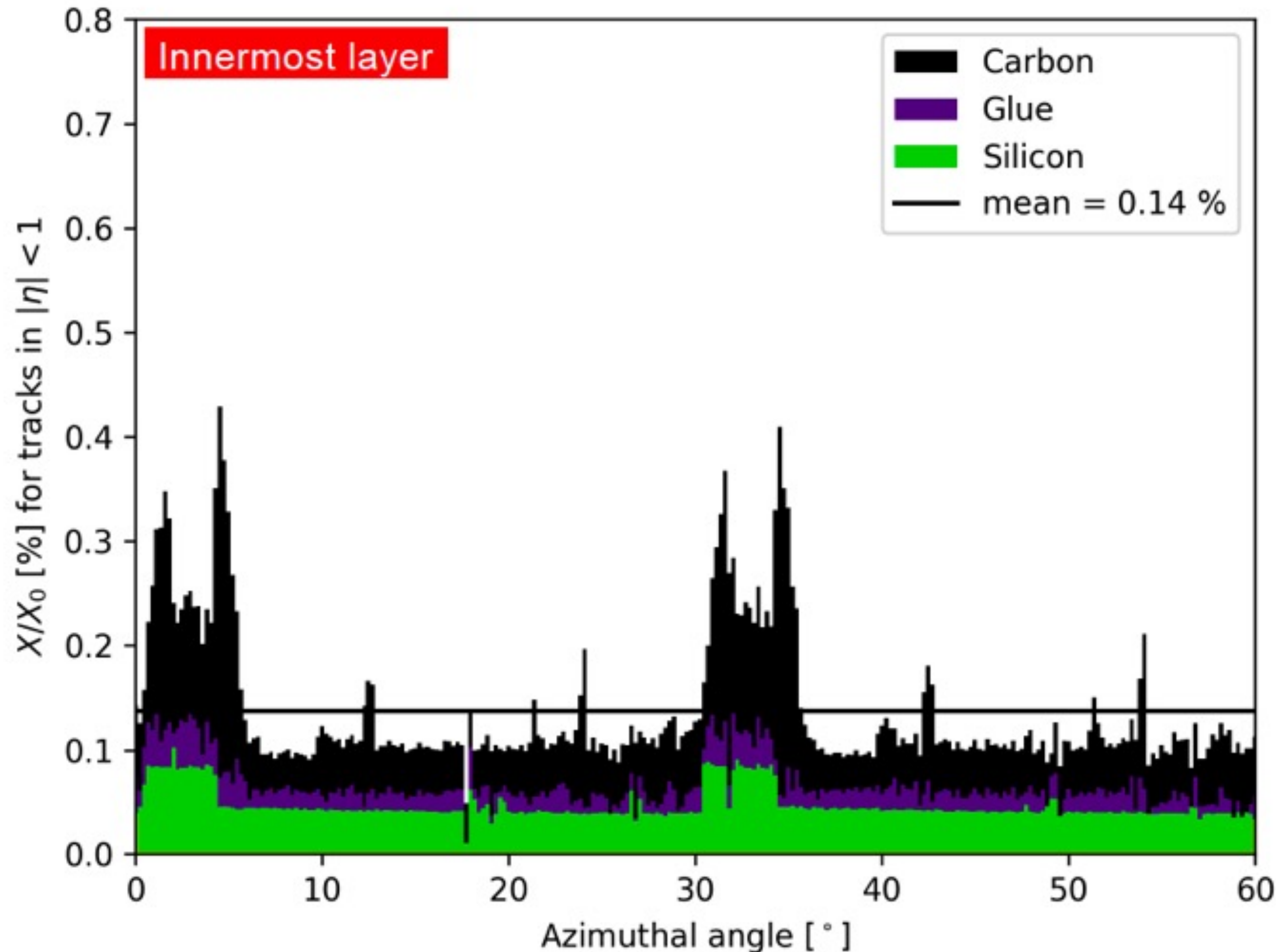

- Observations:
  - Silicon makes up ~15% of total material
  - Irregularities due to support, cooling, & overlap

# How?→Reduce Material Budget




- Observations:
  - Silicon makes up ~15% of total material
  - Irregularities due to support, cooling, & overlap
- Remove water cooling
  - If power consumption < 20 mW/cm$^2$

# How?→Reduce Material Budget




- Observations:
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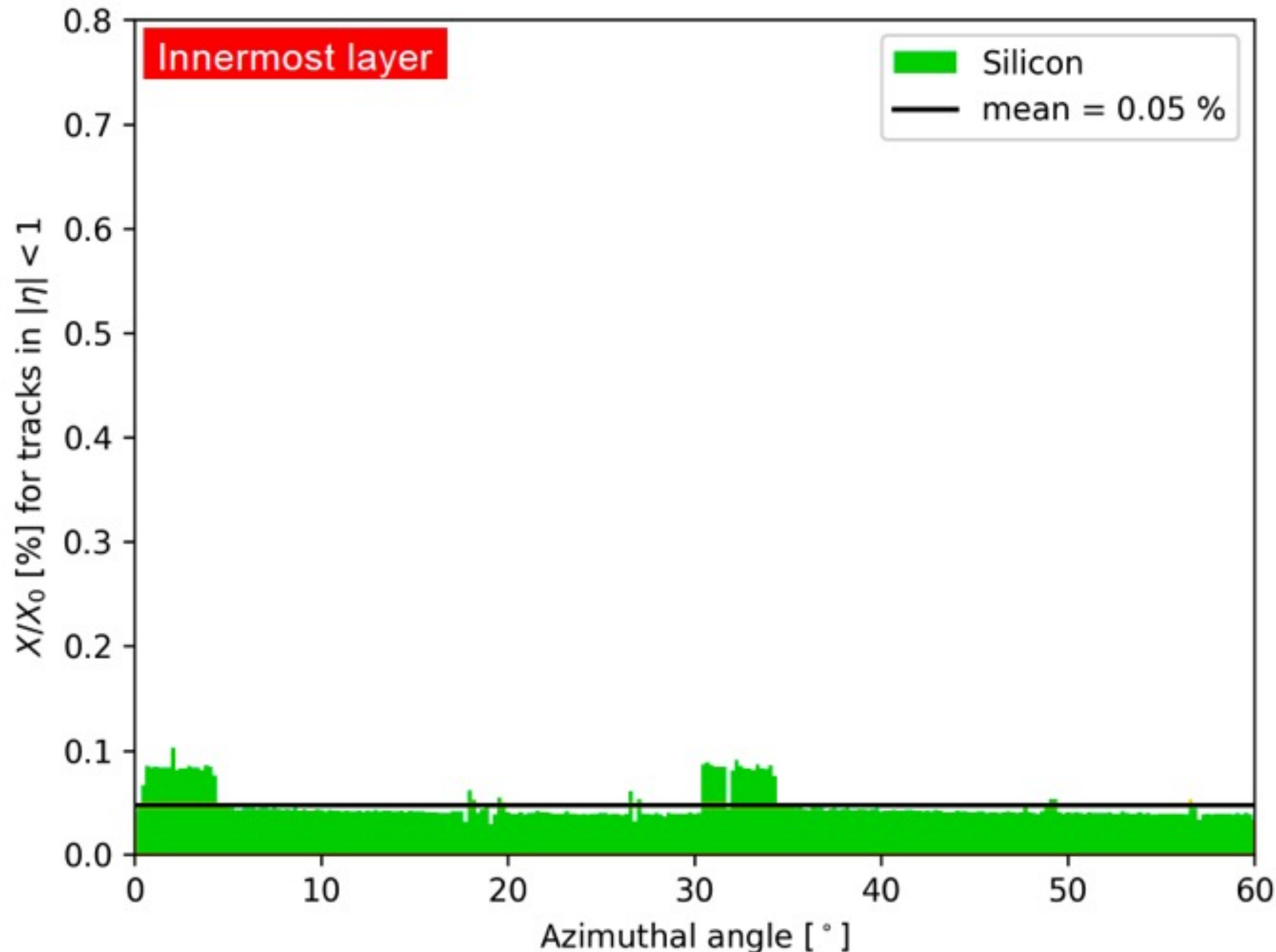
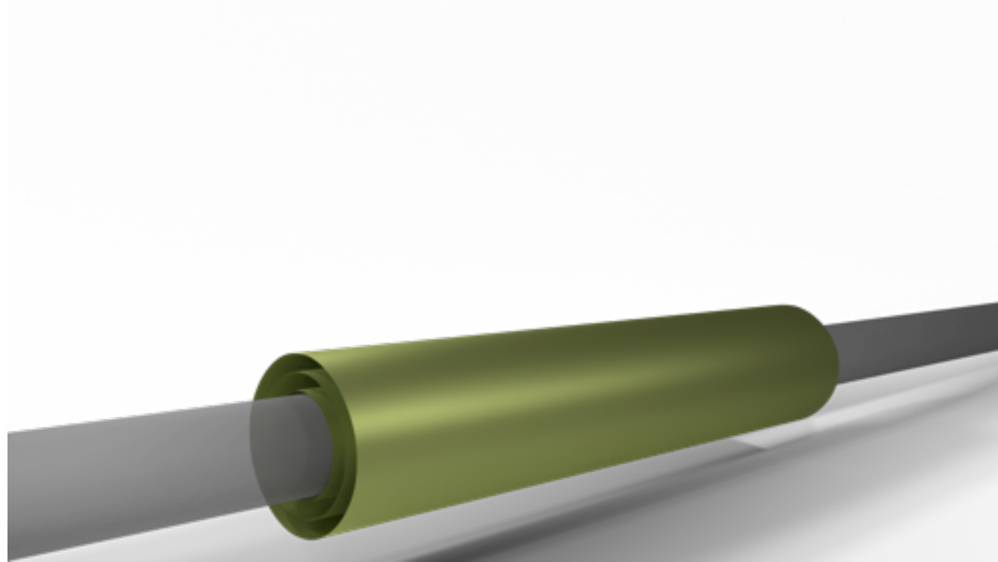
- Remove water cooling
  - If power consumption < 20 mW/cm²
- Remove circuit board for power & data
  - If integrated on chip

# How?→Reduce Material Budget




- Observations:
  - Silicon makes up ~15% of total material
  - Irregularities due to support, cooling, & overlap
- Remove water cooling
  - If power consumption < 20 mW/cm²
- Remove circuit board for power & data
  - If integrated on chip
- Remove mechanical support
  - Self-supporting arched structure from rolling Si wafers

# Thinning & Bending Silicon



- Below 50 μm, Si wafers become flexible, “paper-like”
- Bending Si wafers + circuits is possible & has been tried
  - Radii much smaller than needed have been achieved
- Use 65 nm process for thinner metal stack
- Smaller pixels would allow for thinner epi-layer

| Die type | Front/back side | Ground/polished/plasma | Bumps | Die thickness (μm) | CDS (MPa) | Weibull modulus | MDS (MPa) | $r_{min}$ (mm) |
|---|---|---|---|---|---|---|---|---|
| Blank | Front | Ground | No | 15–20 | 1263 | 7.42 | 691 | 2.46 |
| Blank | Back | Ground | No | 15–20 | 575 | 5.48 | 221 | 7.72 |
| IZM28 | Front | Ground | Yes | 15–20 | 1032 | 9.44 | 636 | 2.70 |
| IZM28 | Back | Ground | Yes | 15–20 | 494 | 2.04 | 52 | 32.7 |
| Blank | Back | Polished | No | 25–35 | 1044 | 4.17 | 334 | 7.72 |
| IZM28 | Back | Polished | Yes | 25–35 | 482 | 2.98 | 107 | 24.3 |
| Blank | Back | Plasma | Yes | 18–22 | 2340 | 12.6 | 679 | 2.50 |
| IZM28 | Front | Plasma | Yes | 18–22 | 1207 | 2.64 | 833 | 2.05 |
| IZM28 | Back | Plasma | Yes | 18–22 | 2139 | 3.74 | 362 | 4.72 |

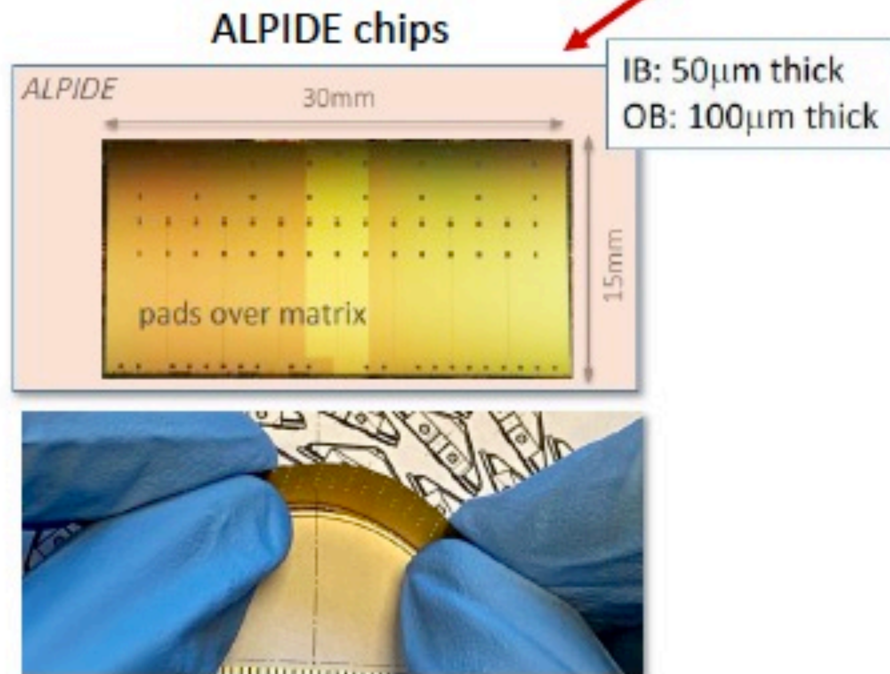
D.A. van den Ende et al., Microelectronics Reliability, vol. 54, pp. 2860-2870, 2014
http://dx.doi.org/10.1016/j.microrel.2014.07.125

# Testing Bent Silicon

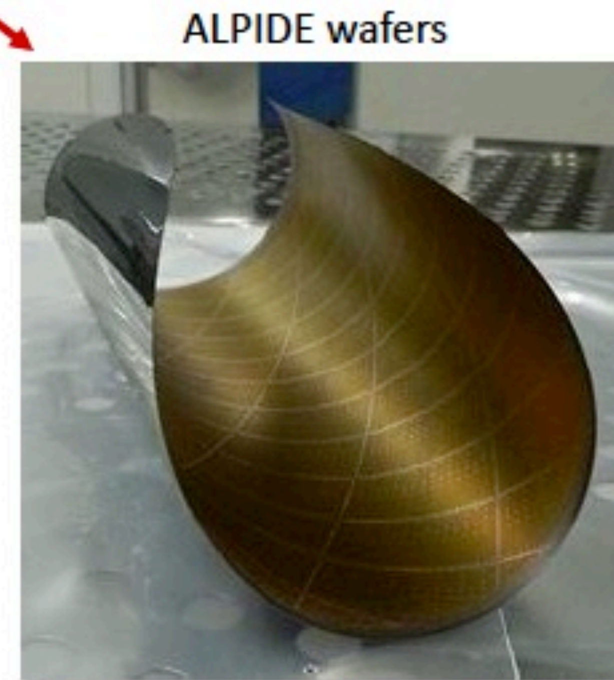
Starting from what is available

ALPIDE chips

IB: 50μm thick
OB: 100μm thick

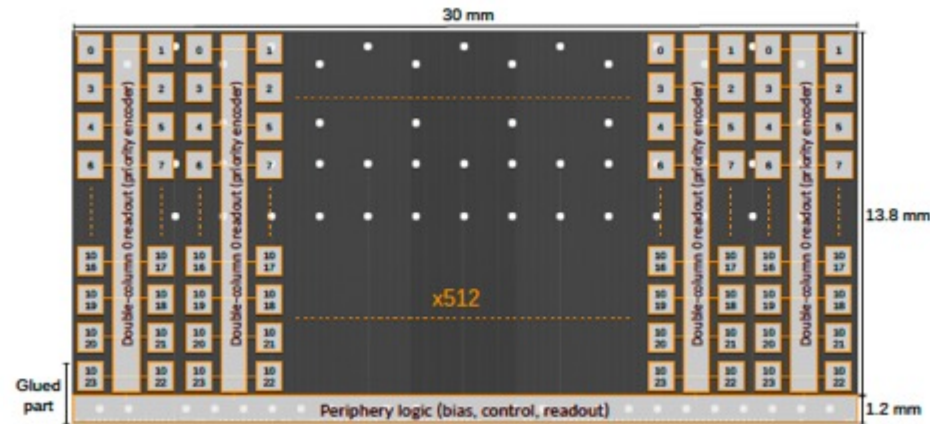


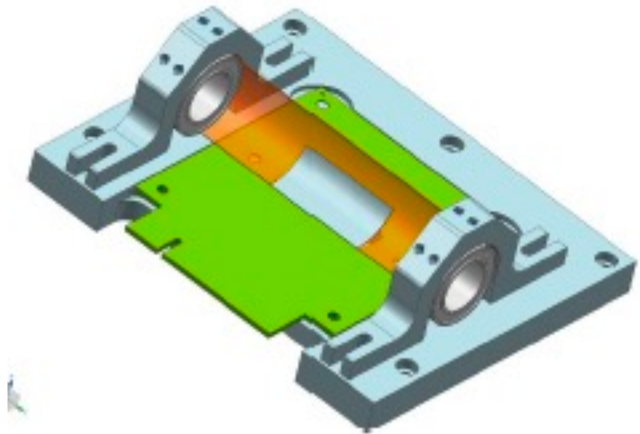

ALPIDE wafers

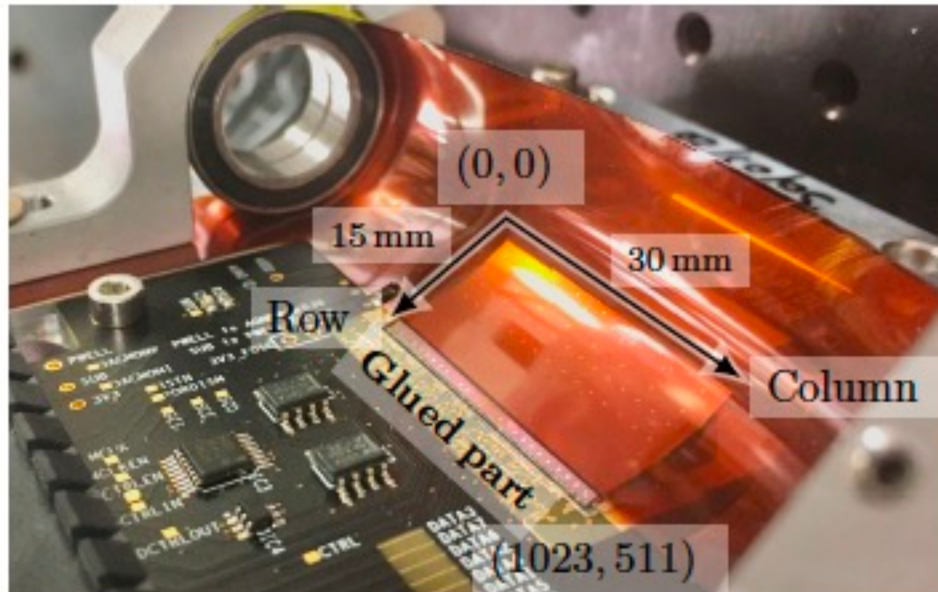


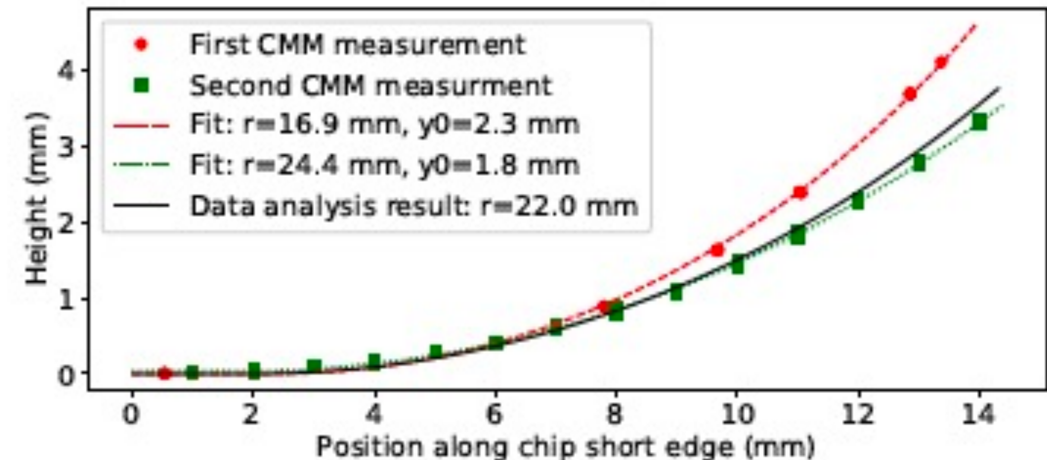
# Testing bent silicon with ALPIDE

- Bent along short side
  - Affects pixel matrix only
  - Bonding area is glued
    - Flat & secured



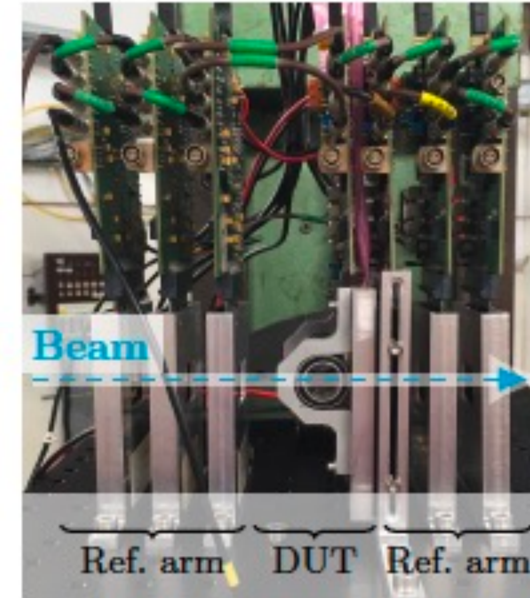





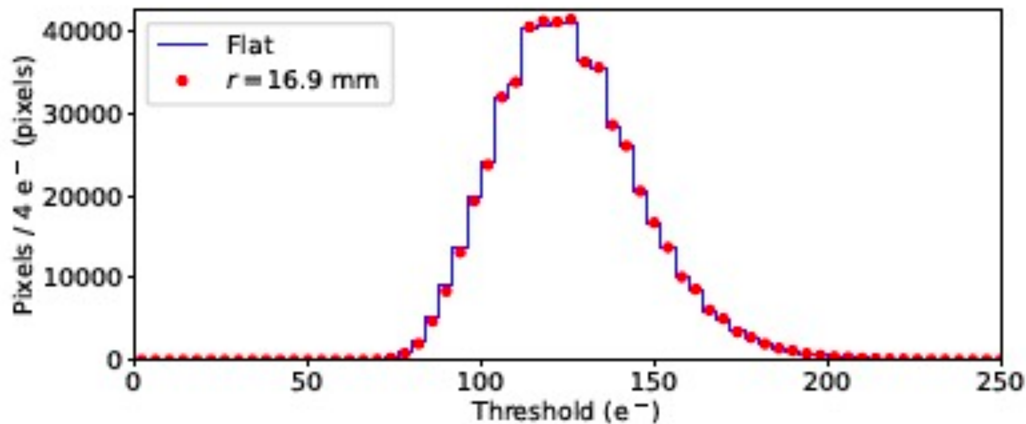



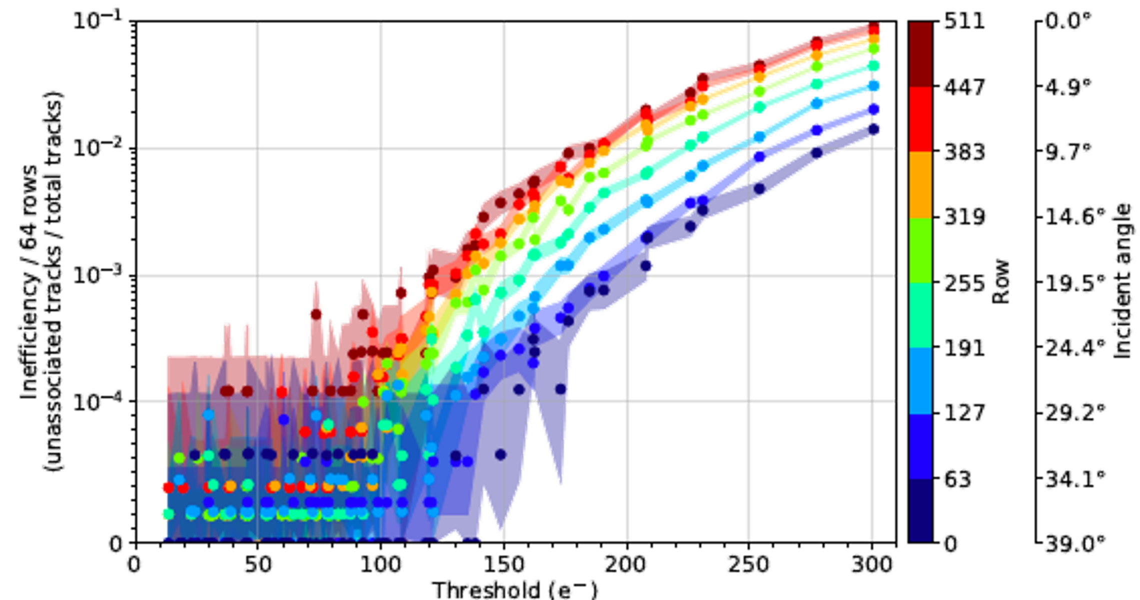
# Bent ALPIDE in beam test

- Curvature effect not noticeable on:
  - Pixel thresholds, FHR, pixel responsiveness
- Difference between pixel threshold negligible before and after bending
- Below threshold of 100 $e^-$ (~operating point) inefficiency < $10^{-4}$




DESY
5.4 GeV $e^-$



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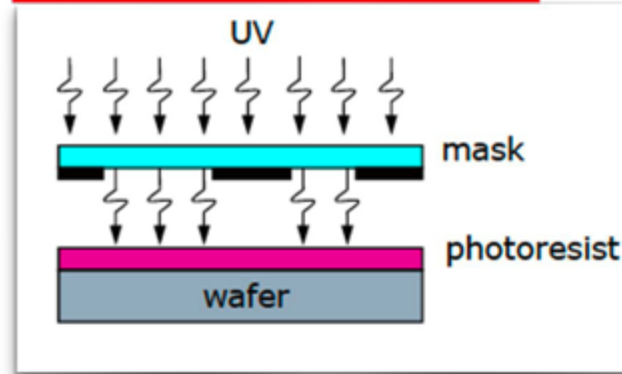
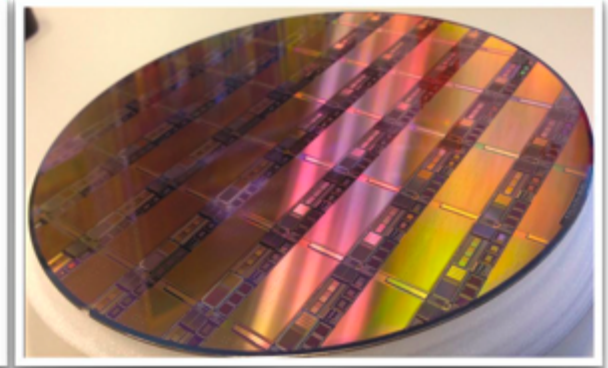
# Wafer-scale Chip

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - ~ few $cm^2$
  - Modules → chips tiled & connected to flexible printed circuit board

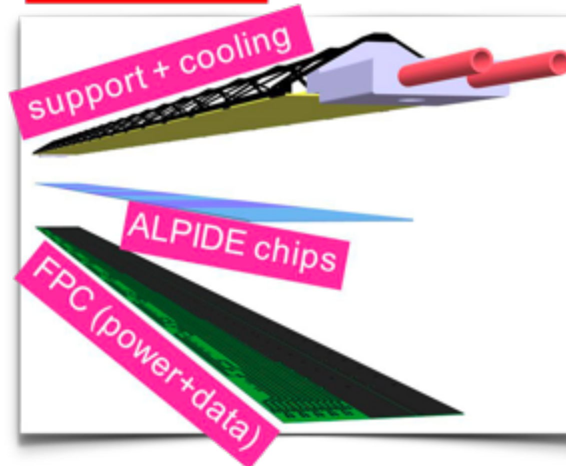
Principle of photolithography



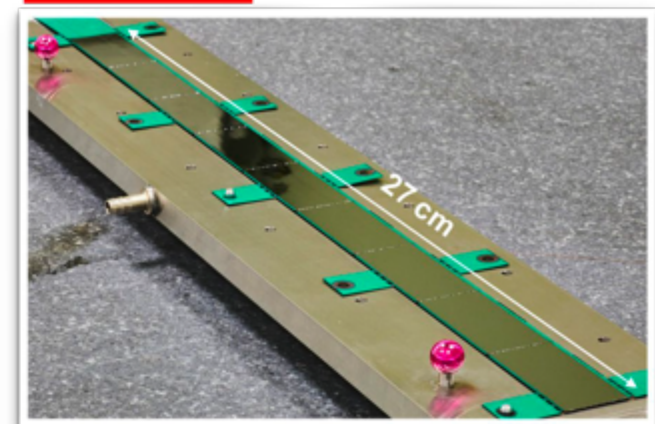

200 mm ALPIDE prototype wafer



Stave design



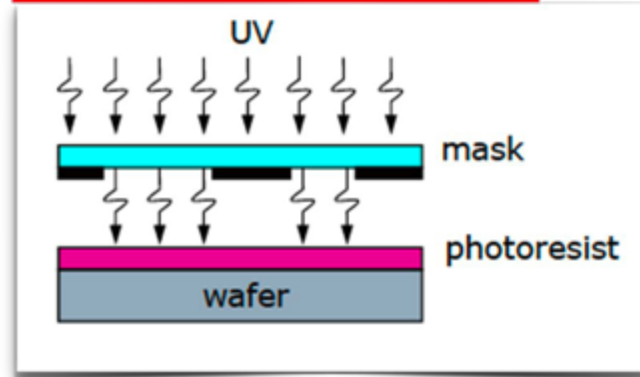

FPC + chips



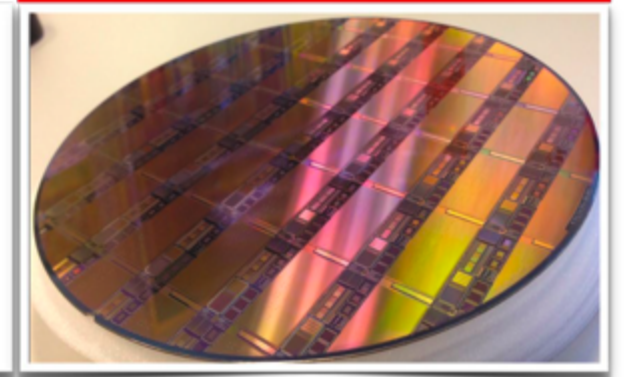
# Wafer-scale Chip

- Chip size is traditionally limited by CMOS manufacturing ("reticle size")
  - ~ few $cm^2$
  - Modules → chips tiled & connected to flexible printed circuit board
- New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
  - Actively used in industry
  - Requires dedicated chip design
- Switch to 65 nm CMOS process
  - 200 mm wafer (ALPIDE, 180 nm CMOS) → 300 mm wafer

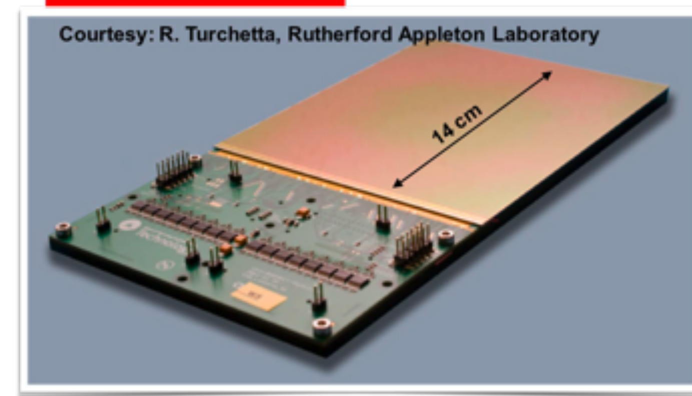
Principle of photolithography



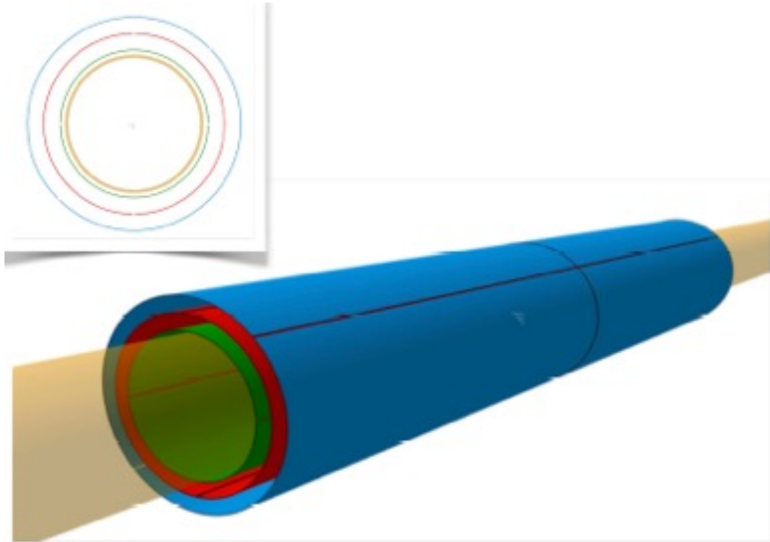

200 mm ALPIDE prototype wafer

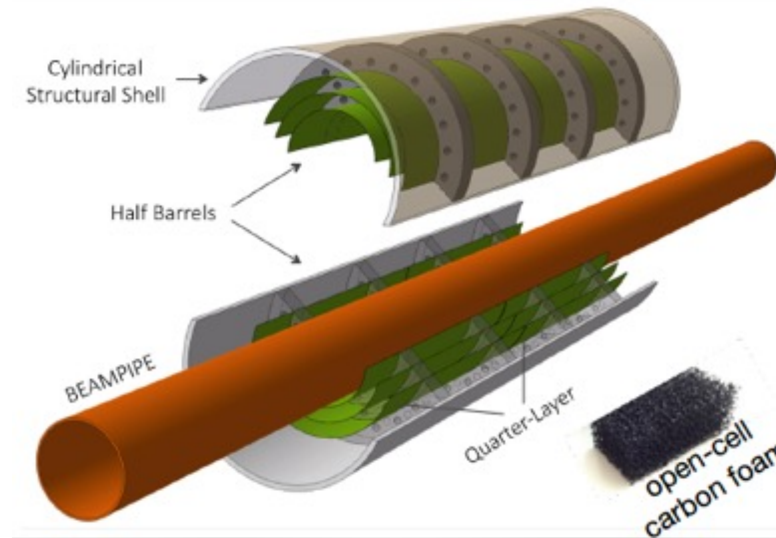


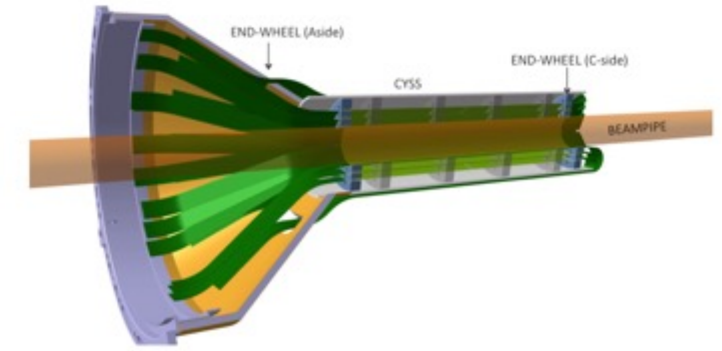
Wafer-scale sensor



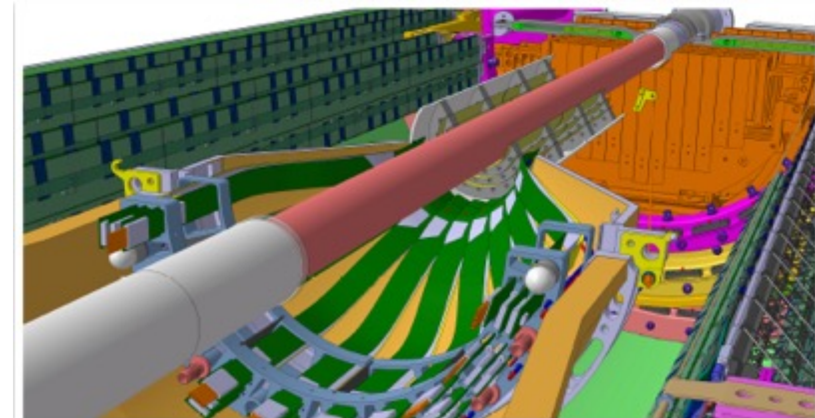
# ITS3 Layout & Mechanics






- Smaller beam pipe diameter & wall thickness (0.14% $X_0$)
- Sensor thickness 20 – 40 μm (0.02 – 0.04% $X_0$)
- Total material (up to r ~ 4 cm) reduced by factor of 3
- Material distributed homogeneously
- Low-density carbon foam used to hold sensors in place
- Cooling at extremities
- Meant as plug-in replacement of ITS2 inner barrel



# Summary

- The MAPS based ITS2 will dramatically improve ALICE tracking capabilities, especially at low $p_T$
- ITS2 installed in April & May 2021
  - ALICE global commissioning ongoing
- ITS3 planned for Run 4 operation
  - Further improve tracking & pointing resolution
- ITS3 will feature a minimal material budget & smaller radius of innermost layer
  - Thinner silicon (20 – 40 μm) & curved

# Summary

ALICE

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- The MAPS based ITS2 will dramatically improve ALICE tracking capabilities, especially at low $p_T$
- ITS2 installed in
  - ALICE global co
- ITS3 planned for
  - Further improve tracking & pointing resolution
- ITS3 will feature a minimal material budget & smaller radius of innermost layer
  - Thinner silicon (20 – 40 μm) & curved

Thank you!

# Backups

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**Table 8.6:** Summary of the physics reach: minimum accessible $p_T$ and relative statistical uncertainty in Pb–Pb collisions for an integrated luminosity of 10 nb$^{-1}$. For heavy flavour, the statistical uncertainties are given at the maximum between $p_T = 2\,\mathrm{GeV}/c$ and $p_T^{min}$. For elliptic flow measurements, the value of $v_2$ used to calculate the relative statistical uncertainty $\sigma_{v_2}/v_2$ is given in parenthesis. The case of the programme up to Long Shutdown 2, with a luminosity of 0.1 nb$^{-1}$ collected with minimum-bias trigger, is shown for comparison.

| Observable | Current, 0.1 nb$^{-1}$ | | Upgrade, 10 nb$^{-1}$ | |
|---|---|---|---|---|
| | $p_T^{min}$ (GeV/$c$) | statistical uncertainty | $p_T^{min}$ (GeV/$c$) | statistical uncertainty |
| **Heavy Flavour** | | | | |
| D meson $R_{AA}$ | 1 | 10 % | 0 | 0.3 % |
| $D_s$ meson $R_{AA}$ | 4 | 15 % | < 2 | 3 % |
| D meson from B $R_{AA}$ | 3 | 30 % | 2 | 1 % |
| $J/\psi$ from B $R_{AA}$ | 1.5 | 15 % ($p_T$-int.) | 1 | 5 % |
| $B^+$ yield | not accessible | | 2 | 10 % |
| $\Lambda_c$ $R_{AA}$ | not accessible | | 2 | 15 % |
| $\Lambda_c/D^0$ ratio | not accessible | | 2 | 15 % |
| $\Lambda_b$ yield | not accessible | | 7 | 20 % |
| D meson $v_2$ ($v_2 = 0.2$) | 1 | 10 % | 0 | 0.2 % |
| $D_s$ meson $v_2$ ($v_2 = 0.2$) | not accessible | | < 2 | 8 % |
| D from B $v_2$ ($v_2 = 0.05$) | not accessible | | 2 | 8 % |
| $J/\psi$ from B $v_2$ ($v_2 = 0.05$) | not accessible | | 1 | 60 % |
| $\Lambda_c$ $v_2$ ($v_2 = 0.15$) | not accessible | | 3 | 20 % |
| **Dielectrons** | | | | |
| Temperature (intermediate mass) | not accessible | | | 10 % |
| Elliptic flow ($v_2 = 0.1$) [4] | not accessible | | | 10 % |
| Low-mass spectral function [4] | not accessible | | 0.3 | 20 % |
| **Hypernuclei** | | | | |
| $^3_\Lambda$H yield | 2 | 18 % | 2 | 1.7 % |

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**Table 1.2:** Expected maximum hit densities and radiation levels (see text for details).

| Layer | Radius (mm) | Particle fluxes: Prim. & sec. particles[a] ($cm^{-2}$) | Particle fluxes: QED electrons[b] ($cm^{-2}$) | Radiation doses: NIEL[c] (1 MeV $n_{eq}/cm^2$) | Radiation doses: TID[c] (krad) |
|---|---|---|---|---|---|
| 0 | 23 | 30.4 | 6.02 | $9.2 \times 10^{12}$ | 646 |
| 1 | 32 | 20.4 | 3.49 | $6.0 \times 10^{12}$ | 380 |
| 2 | 39 | 14.9 | 2.35 | $3.8 \times 10^{12}$ | 216 |
| 3 | 196 | 1.0 | $2.1 \times 10^{-2}$ | $5.4 \times 10^{11}$ | 15 |
| 4 | 245 | 0.7 | $9.0 \times 10^{-3}$ | $5.0 \times 10^{11}$ | 10 |
| 5 | 344 | 0.3 | $1.3 \times 10^{-3}$ | $4.8 \times 10^{11}$ | 8 |
| 6 | 393 | 0.3 | $4.0 \times 10^{-4}$ | $4.6 \times 10^{11}$ | 6 |

[a] maximum hit densities in central Pb–Pb collisions (including secondaries produced in material)
[b] for an integration time of 10 µs, an interaction rate of 50 kHz, a magnetic field of 0.2 T and $p_T > 0.3$ MeV/$c$; a magnetic field of 0.2 T, which is planned for a run dedicated to the measurement of low-mass di-electrons, corresponds to the worst case scenario in terms of detector occupancy
[c] including a safety factor of ten

Table 2: Expected maximum particle density in the layers of the ITS Inner Barrel.

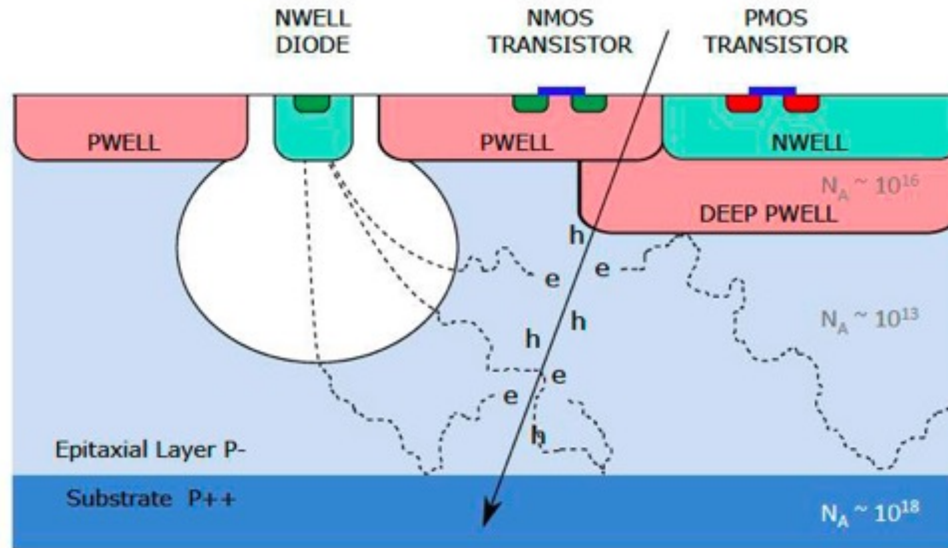
| Layer | Particle density ($cm^{-2}$): LS2 Upgrade Hadronic[a] | LS2 Upgrade QED electrons[b] | LS3 Upgrade Hadronic[a] | LS3 Upgrade QED electrons[b] |
|---|---|---|---|---|
| 0 | 43 | 7 | 73 | 12 |
| 1 | 25 | 3 | 43 | 8 |
| 2 | 17 | 2 | 29 | 6 |

[a] maximum particle density in central Pb–Pb collisions (including secondaries produced in material) for a magnetic field of 0.2 T.
[b] for an integration time of 10 µs, an interaction rate of 50 kHz, a magnetic field of 0.2 T

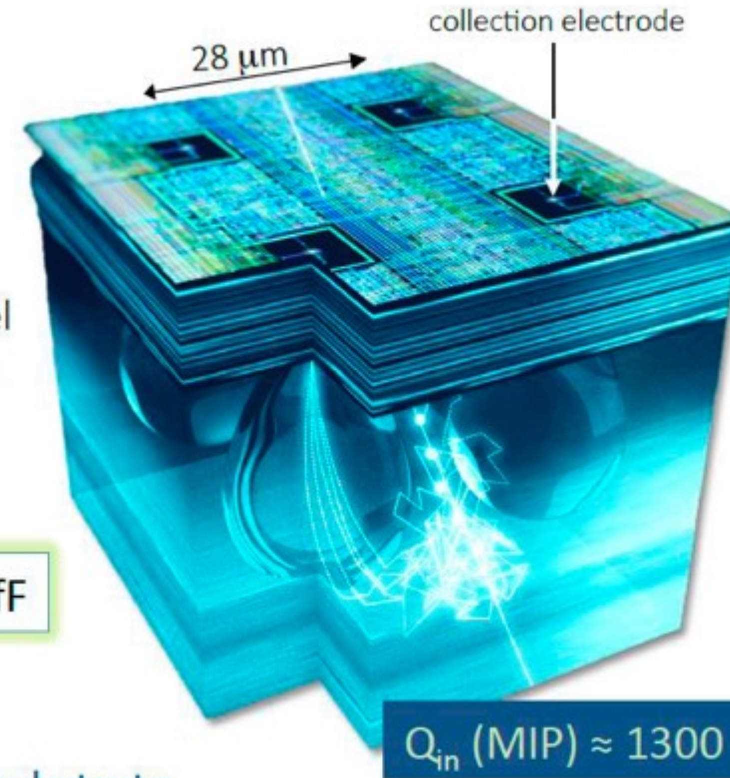
Occupancy ~$10^{-3}$

# ALICE PIxel DEtector (ALPIDE)

## CMOS Pixel Sensor using 0.18μm CMOS Imaging Process




*pixel capacitance ≈5 fF (@ $V_{bb}$ = -3 V)*




- High-resistivity (> 1kΩ cm) p-type epitaxial layer (25μm) on p-type substrate
- Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance (~fF)
- Reverse bias voltage (-6V < $V_{BB}$ < 0V) to substrate (contact from the top) to increase depletion zone around NWELL collection diode
- Deep PWELL shields NWELL of PMOS transistors

➔ full CMOS circuitry within active area

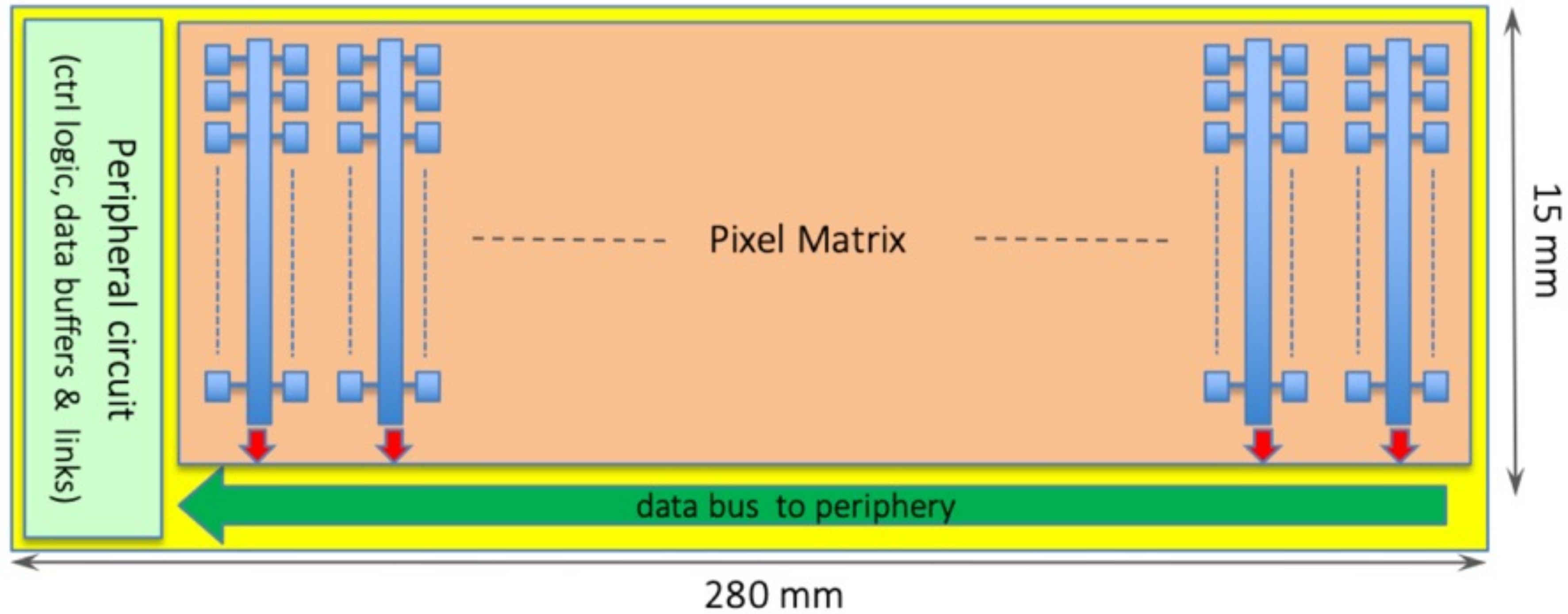



Figure 6: Diagram of stitched sensor in one direction (horizontal and vertical dimensions not to scale). Stitching in the vertical direction is also possible.

The data bus is conservatively estimated to take an area of up to 50 µm × 280 mm (a factor 2.8 larger for the 180 nm process), which amounts to a dead area that corresponds to about 0.3 % of the detector acceptance. As a comparison, the ITS2 has gaps in the $z$-direction between adjacent chips (matrix to matrix) of 150 µm, which result in a total dead area of 0.5 %. The simulations presented in the document take into account a dead area of 5 %.

# ITS Upgrade in LS3 (ITS3)

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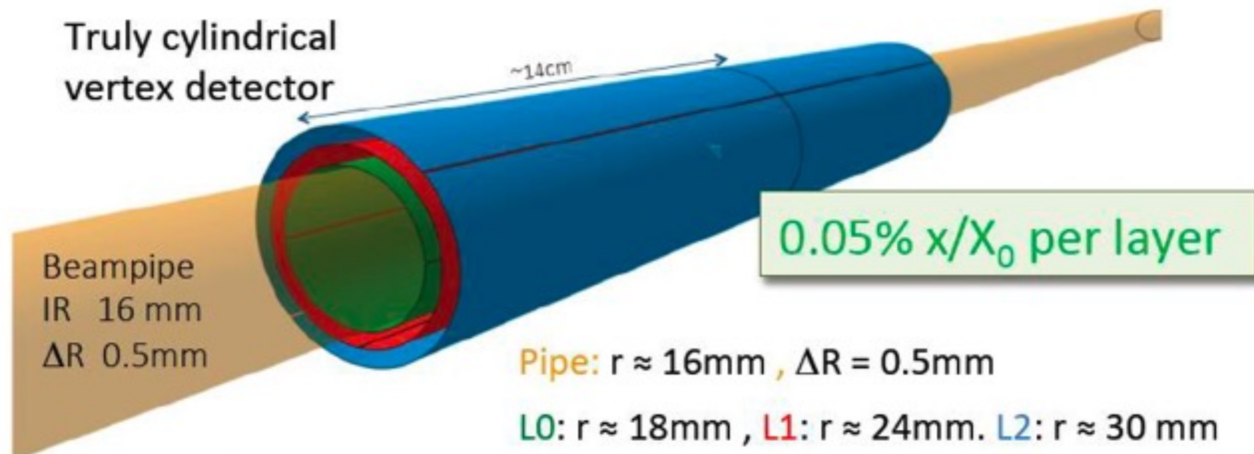
EoI for a nearly 0-mass Inner Barrel in LS3 (http://cds.cern.ch/record/2644611/)

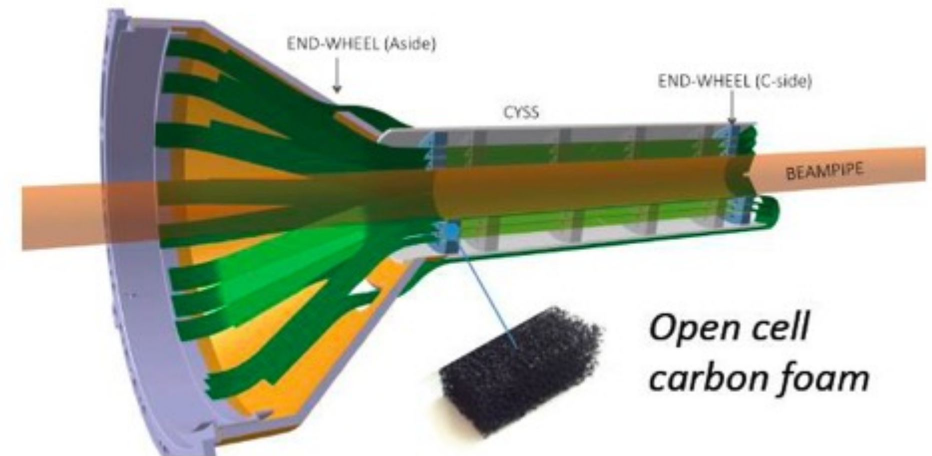
Driving requirements of ITS Upgrade in LS2

- Improved tracking precision (smaller pixels, closer to IP, less material)
- Faster readout

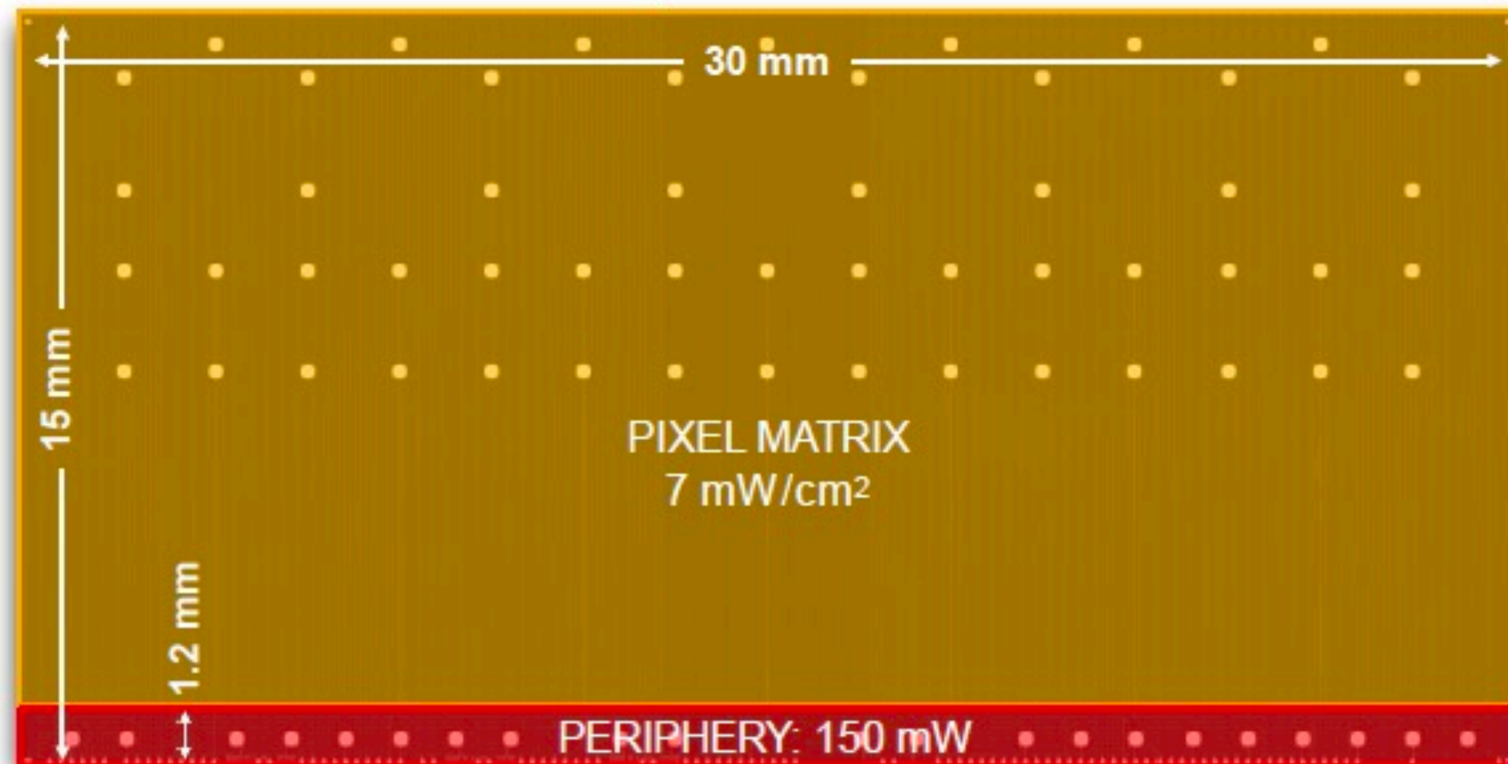
Can be pushed further using technologies that are becoming mature

- Eliminate active cooling ⇨ possible for power < 20mW/cm²
- Eliminate electrical substrate ⇨ Possible if the sensor covers the full stave length
- Sensors arranged with a perfectly cylindrical shape ⇨ sensors thinned to ~30μm can be cruved to a radii 10-20mm



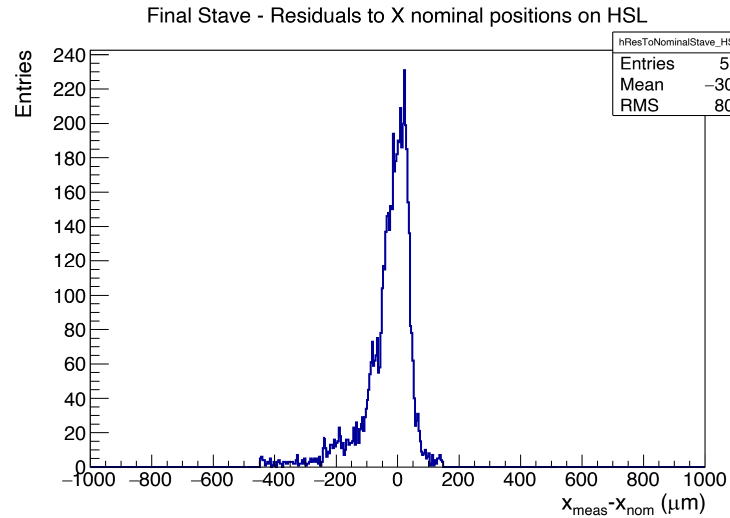



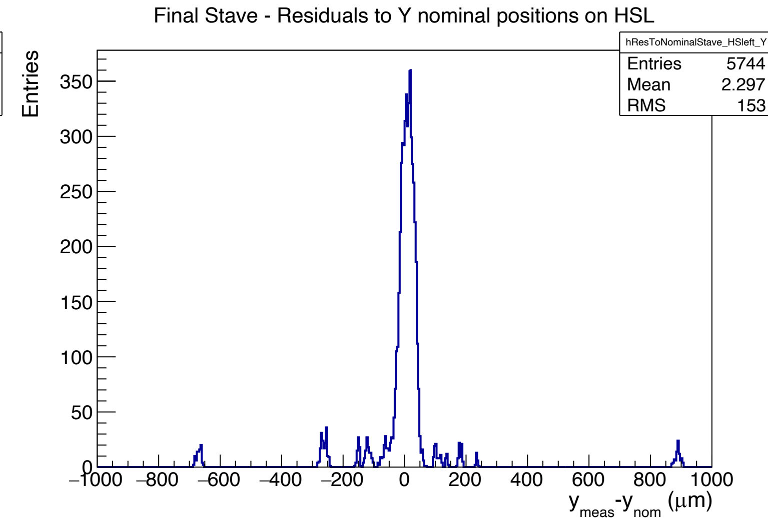
# Cooling

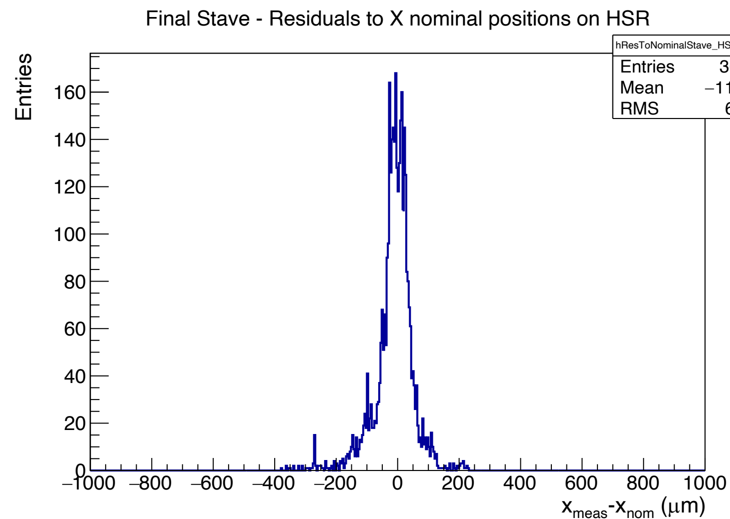


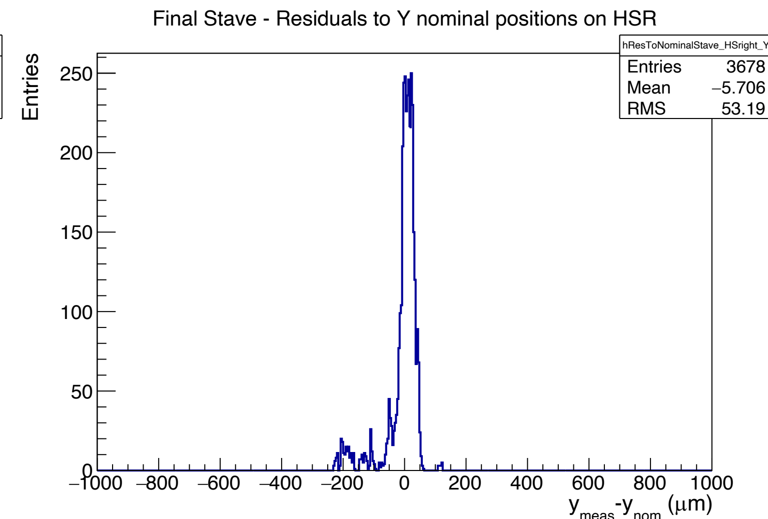

- Air cooling possible from ~20 mW/cm$^2$
- ALPIDE already close: ~40 mW/cm$^2$
- actually largely sufficient if periphery outside fiducial volume

# ML Residuals




- 2 measurements per sensor

# ML Planarity

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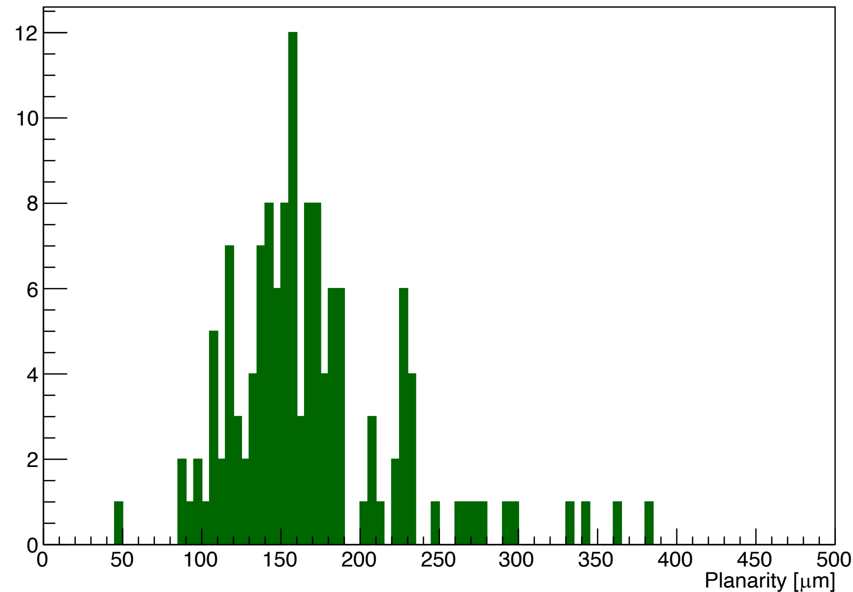
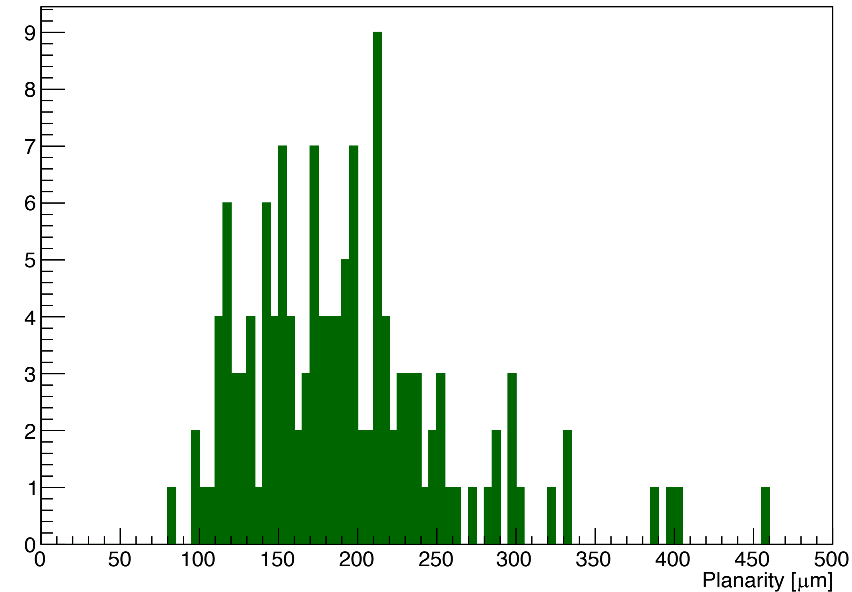
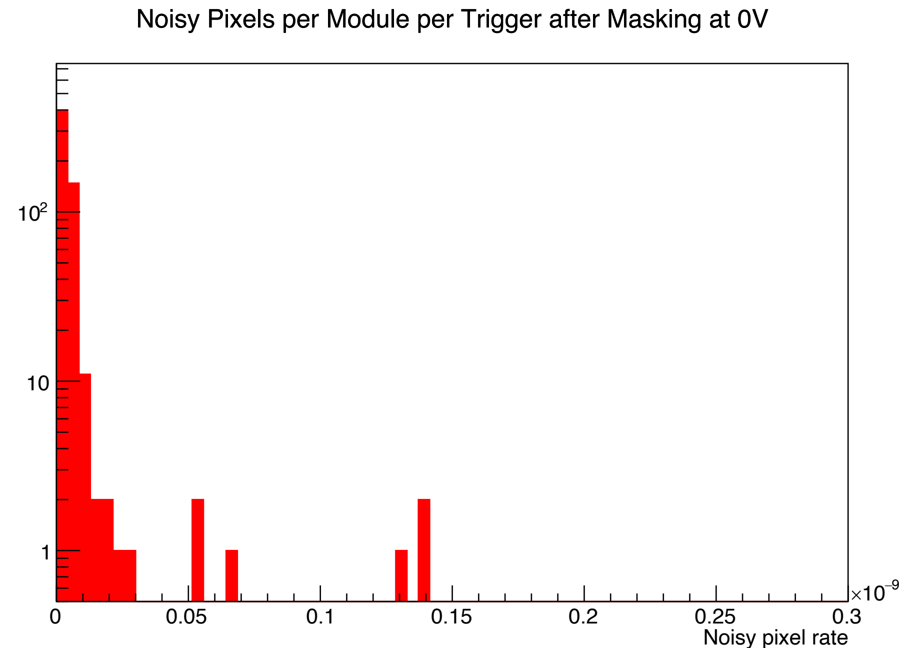
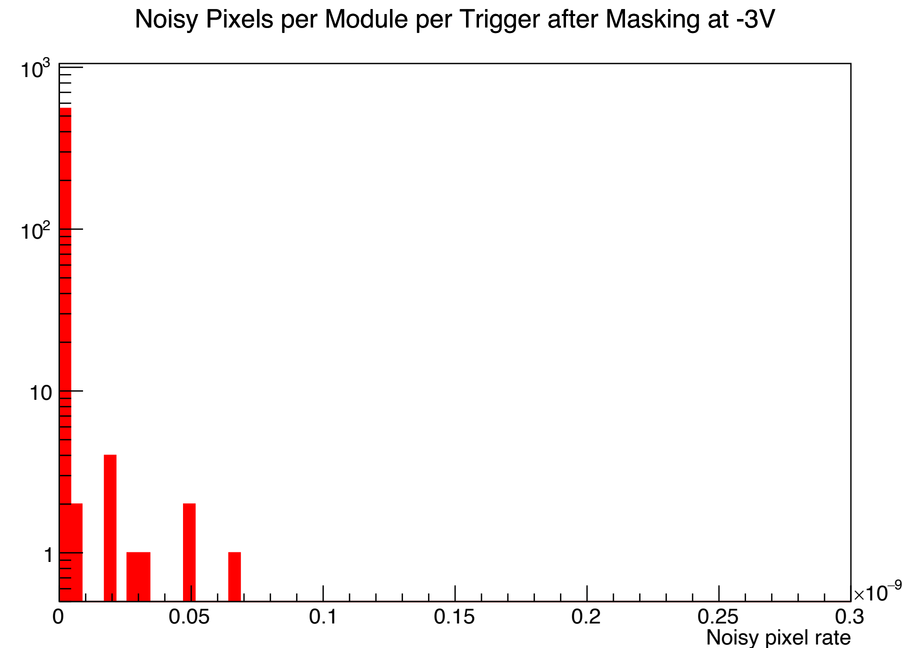



- 2 measurements per sensor
- Tolerance of 1 mm for planarity
- Flatness from reference system x-y plane

# ML Noisy Pixels




- Tune threshold to ~100 $e^-$
- Pixels readout for $10^5$ triggers
- Mask noisy pixels (at least 2 "hits" during previous test)
- Re-run test (Done for 0 V and -3 V)
- Noise rate well below the $10^{-5}$ design goal