TDC development for future detectors

Initial technology evaluation

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Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

Motivation

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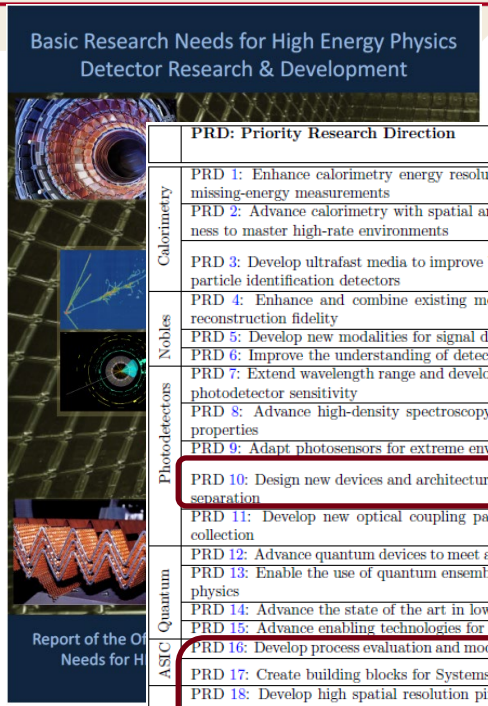
DOE Basic Research Needs Study on High Energy Physics Detector Research and Development

- Future high energy, high luminosity hadron colliders will present much higher levels of pileup and extreme radiation environments
- Future detectors will require higher segmentation (3D position resolution) and additional time resolving capabilities while sustaining higher radiation doses (Instrumentation BRN – Science Driver: Higgs and the energy frontier - PRD10, PRD16, PRD17, PRD18, PRD19, PRD20)
- To satisfy requirements front-end sensors and readout ASICs will need to be compatible with:
  - Larger channel density – Low power, Smaller feature size (Deep sub-micron technologies)
  - Precision timing resolution – fast sensors, in pixel high precision timing circuits
  - Unprecedented radiation levels (dose of up to 30 GRad and 10^{18} neutrons/cm^2)



	PRD: Priority Research Direction	Grand Challenge
Calorimetry	PRD 1: Enhance calorimetry energy resolution for precision electroweak mass and missing-energy measurements	1
	PRD 2: Advance calorimetry with spatial and timing resolution and radiation hardness to master high-rate environments	1,4
	PRD 3: Develop ultrafast media to improve background rejection in calorimeters and particle identification detectors	1,3,4
Photodetectors Noble	PRD 4: Enhance and combine existing modalities to increase signal-to-noise and reconstruction fidelity	1,2
	PRD 5: Develop new modalities for signal detection	1
	PRD 6: Improve the understanding of detector microphysics and characterization	1
	PRD 7: Extend wavelength range and develop new single-photon counters to enhance photodetector sensitivity	1,3
	PRD 8: Advance high-density spectroscopy and polarimetry to extract all photon properties	2,3
	PRD 9: Adapt photosensors for extreme environments	2,4
	PRD 10: Design new devices and architectures to enable picosecond timing and event separation	1,2,4
	PRD 11: Develop new optical coupling paradigms for enhanced or dynamic light collection	1,2,3
Quantum	PRD 12: Advance quantum devices to meet and surpass the Standard Quantum Limit	1,3
	PRD 13: Enable the use of quantum ensembles and sensor networks for fundamental physics	1,2
	PRD 14: Advance the state of the art in low-threshhold quantum calorimeters	1,3
	PRD 15: Advance enabling technologies for quantum sensing	1,2,3
ASIC	PRD 16: Develop process evaluation and modeling for ASICs in extreme environments	3,4
	PRD 17: Create building blocks for Systems-on-Chip for extreme environments	1,4
SolidState	PRD 18: Develop high spatial resolution pixel detectors with precise high per-pixel time resolution to resolve individual interactions in high-collision-density environments	1,4
	PRD 19: Adapt new materials and fabrication/integration techniques for particle tracking	2,3
	PRD 20: Realize scalable, irreducible-mass trackers	2,3
TDAQ	PRD 21: Achieve on-detector, real-time, continuous data processing and transmission to reach the exascale	2,4
	PRD 22: Develop technologies for autonomous detector systems	2
	PRD 23: Develop timing distribution with picosecond synchronization	1
Xcut	PRD 24: Manipulate detector media to enhance physics reach	1,3
	PRD 25: Advance material purification and assay methods to increase sensitivity	1,2,3,4
	PRD 26: Addressing challenges in scaling technologies	2,3

Timing ASICs @ SLAC

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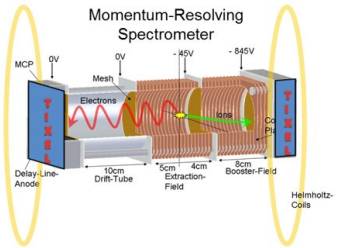
Tixel (SparkPix family)

- Application: **Photon Science**
- Detector Type: Hybrid **PAD**
- Sensor: Thin **Si**
- ASIC Technology: 0.13µm
- Resolution: **100ps**
- Pixel: **100x100µm²**
- TDC area: **85x45µm²**
- TDC DR: **16bits (4 + 4 + 8) - 1µs**
- TDC Power: **16µW**

LCLS



HGTD (Altiroc)

- Application: **HEP**
- Detector Type: Hybrid **PAD**
- Sensor: **LGAD**
- ASIC Technology: 0.13µm
- Resolution: **20ps**
- Pixel: **1.3x1.3mm²**
- TDC area: **210x430µm²**
- TDC DR: **7bits (5 + 2) – 2.56ns**
- TDC Power: **460µW (10% occupancy)**

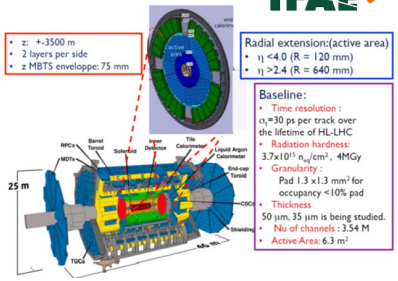
OMEGA Microelectronics

ATLAS EXPERIMENT

LAL Laboratoire de l'Accélérateur Linéaire

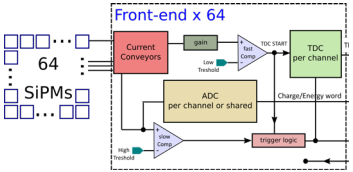
SMU

IFAE



SiPM ToF PET

- Application: **Nuclear Medicine**
- Detector Type: Hybrid
- Sensor: **SiPM**
- ASIC Technology: 0.13µm
- Resolution: **10ps**
- Channel width: **250µm (64 channels)**
- TDC area: **450x430µm²**
- TDC DR: **11bits (5+2+4) – 20ns**
- TDC Power: **650µW (10% occupancy)**

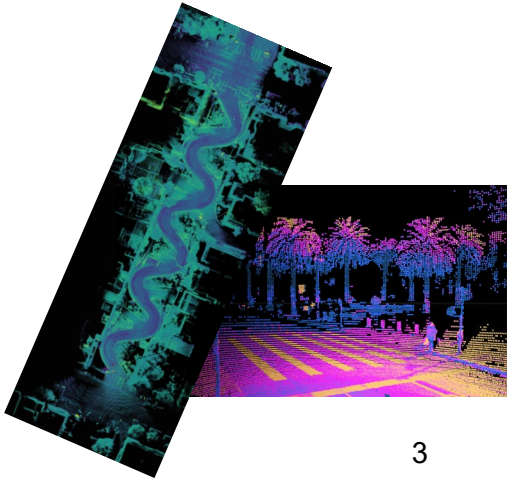


Stanford MEDICINE

DIPARTIMENTO DI INGEGNERIA ELETTRICA E DELL'INFORMAZIONE

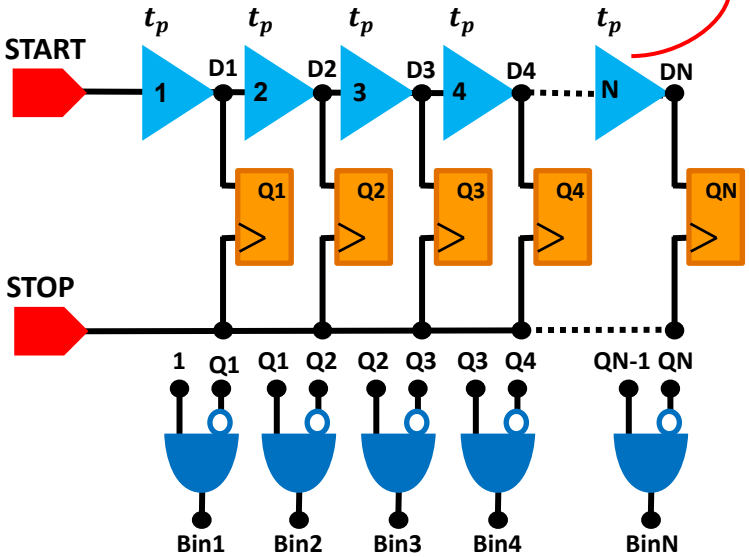
ToF LiDAR (CRADA)

- Application: **Automotive**
- Detector Type: Monolithic
- Sensor: **SPAD**
- ASIC Technology: 0.13µm HV
- Resolution: **1ns**
- Channel width: **400µm (80 channels)**
- TCSPC area: **200x140 µm²**
- TDC DR: **10bits**
- TCSPC Power: **1000µW**



Delay Line TDC

- Majority of modern TDCs is based on some version of a delay-line structure:

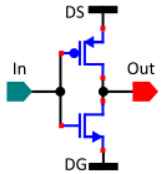


- TDC resolution given by the propagation delay of the elementary cell:

$$LSB_{TDC} = t_p$$

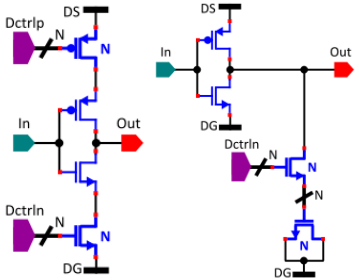
- Basic element: **Delay Cell**

- Simple Logic Gate:

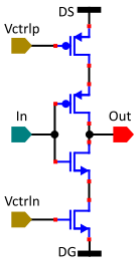


  - Used in FPGA TDCs
  - Requires constant calibration

- Digitally-Controlled Delay Cell:

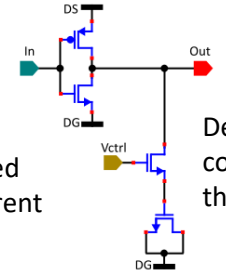


- Voltage-Controlled Delay Cell:
  - Current starved:



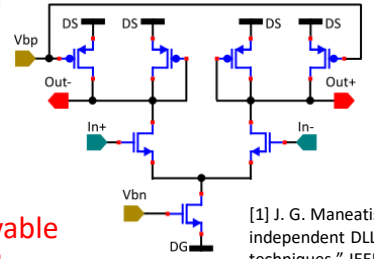
Delay controlled thru current

  - Shunt capacitor:



Delay controlled thru load

- Differential delay cell with symmetric loads (Maneatis cell [1]):



  - Frequently used in PLL VCOs and DLLs
  - Consumes Static Bias Current

Minimum delay limited by fastest achievable logic propagation delay in target technology

[1] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," IEEE J. Solid-State Circuits, vol. 31, no. 11, pp. 1723–1732, Nov. 1996.

Vernier Delay Line TDC

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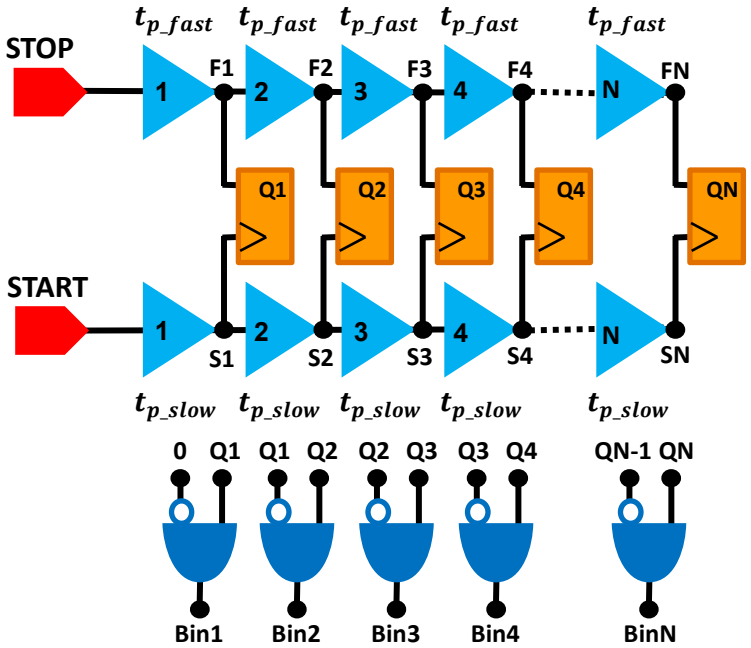
- What if resolutions lower than minimum propagation delay is required? → **Vernier Delay Line**



$$LSB_{TDC} = t_{p\_slow} - t_{p\_fast}$$

- **START** signal propagates in the **Slow Delay Line** ($t_{p\_slow} > t_{p\_fast}$)
- **STOP** signal propagates in the **Fast Delay Line**

  - The **START** pulse comes first and initializes the TDC operation.
  - The **STOP** pulse follows the **START** with a delay that represents the time interval to be digitalized.
  - At each tap of the Delay Line the **STOP** signal catches up to the **START** signal by the deference of the propagation delays of cells in Slow and Fast branches, i.e., $t_{p\_slow} - t_{p\_fast}$ represents the **LSB** of time measurement.
  - The number of cells necessary for **STOP** signal to surpass the **START** signal represents the result of TDC conversion.

Compare to the simple Delay Line, Vernier Delay Line allows for TDC resolutions below the minimum logic propagation delay in the technology but suffer from higher power and area consumption and slower conversion times.

Studying the logic propagation delay in the technology necessary for defining the TDC architecture

Testbench: Minimum Propagation Delay

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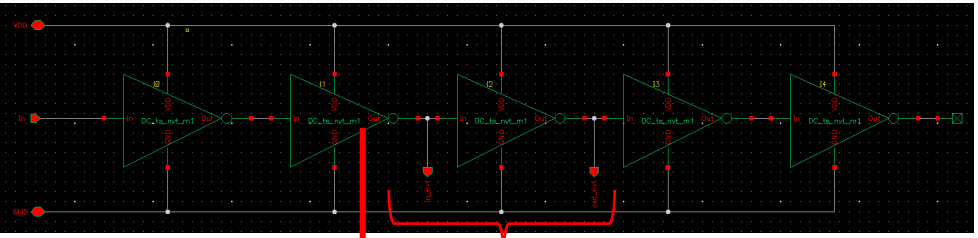
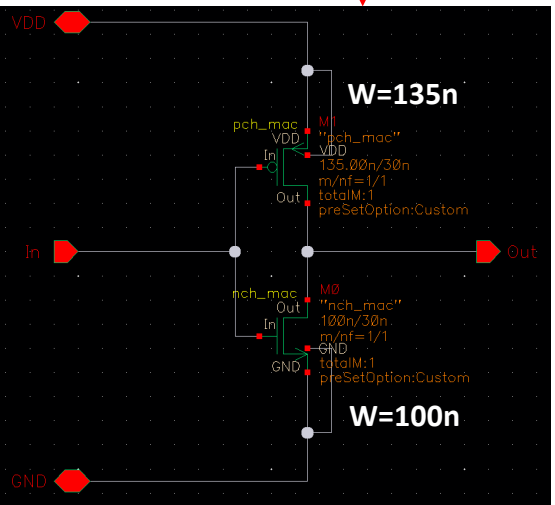
Delay Line Testbench:

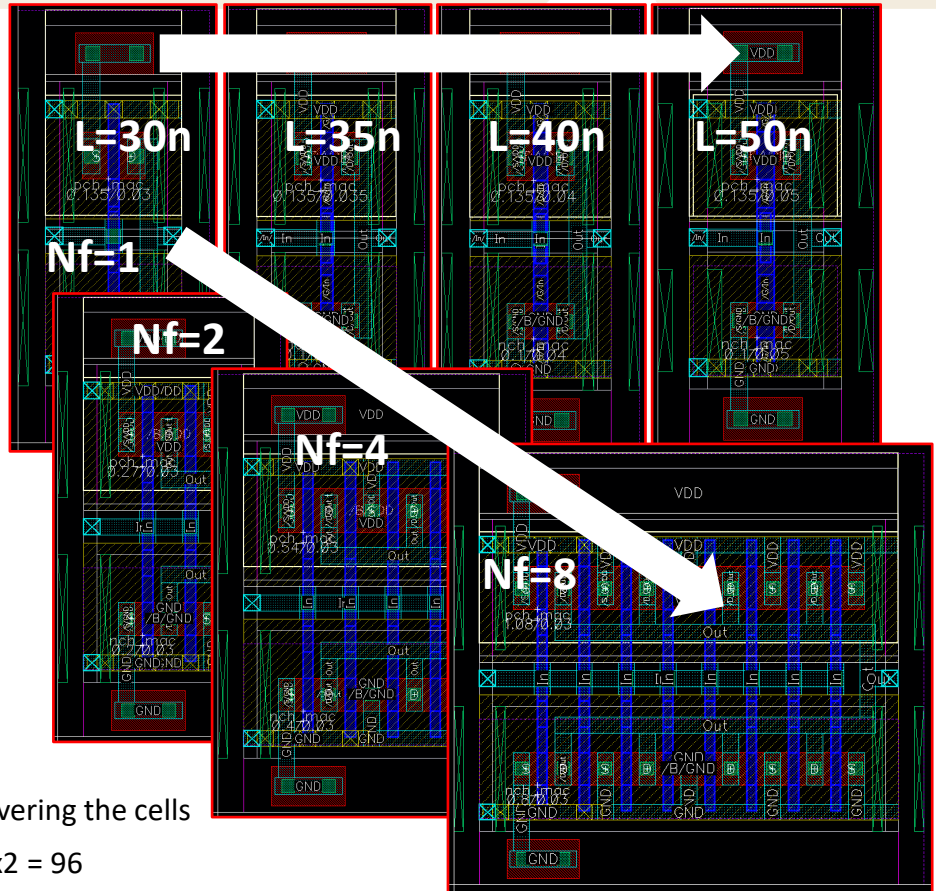


t_p - Cell Propagation Delay

Inverter as a Delay Cell:



SVT, LVT, HVT



Simulations: Spectre

- **SCH** – Schematic
- **RCX** – Parasitic Extracted

Extraction: Calibre PEX

- M1 – Signal Connections
- M2 – VDD & GND planes covering the cells

Total Number of Views: 4x4x3x2 = 96

SVT Propagation Delay: HL / LH VS Corners

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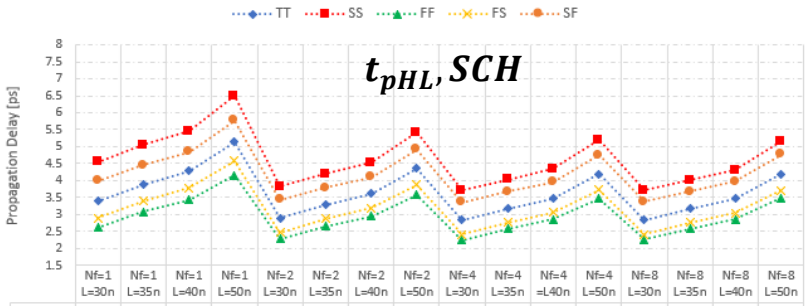
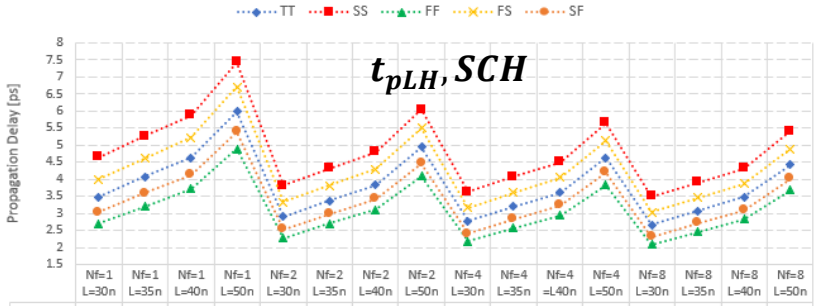
HL Delay VS Nf & L @SVT, VDD=0.9, temp=27 (SCH)

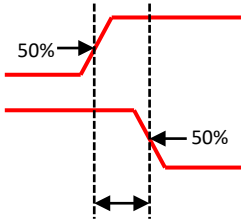


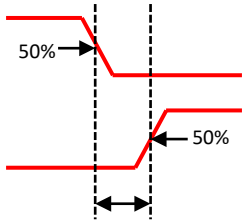
	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	3.391	3.882	4.276	5.13	2.901	3.285	3.61	4.354	2.83	3.173	3.476	4.197	2.846	3.169	3.464	4.185
SS	4.545	5.052	5.461	6.483	3.818	4.197	4.527	5.411	3.703	4.029	4.333	5.187	3.707	4.005	4.298	5.148
FF	2.62	3.073	3.427	4.154	2.286	2.65	2.947	3.587	2.245	2.576	2.855	3.479	2.268	2.586	2.86	3.487
FS	2.889	3.401	3.788	4.58	2.471	2.871	3.188	3.877	2.41	2.768	3.064	3.731	2.422	2.761	3.049	3.714
SF	3.997	4.46	4.841	5.768	3.429	3.787	4.102	4.918	3.352	3.667	3.961	4.757	3.385	3.678	3.964	4.764

LH Delay VS Nf & L @SVT, VDD=0.9, temp=27 (SCH)

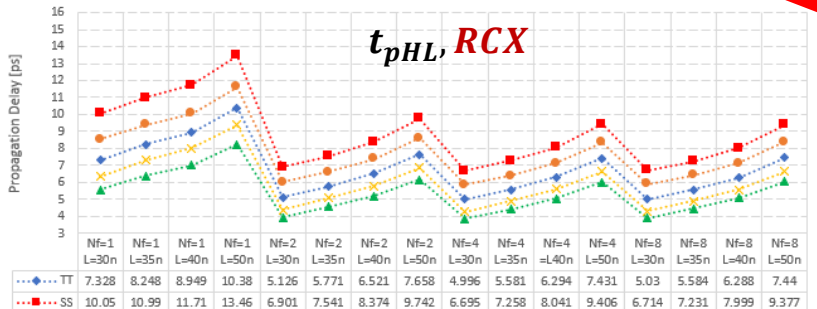


	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	3.48	4.062	4.632	5.98	2.904	3.371	3.831	4.934	2.766	3.195	3.616	4.629	2.663	3.07	3.469	4.426
SS	4.639	5.259	5.866	7.421	3.819	4.305	4.785	6.041	3.631	4.069	4.505	5.652	3.496	3.907	4.317	5.397
FF	2.699	3.208	3.714	4.881	2.28	2.697	3.113	4.08	2.174	2.561	2.944	3.838	2.092	2.462	2.827	3.675
FS	3.997	4.61	5.221	6.697	3.326	3.814	4.301	5.495	3.161	3.606	4.047	5.131	3.033	3.451	3.866	4.88
SF	3.034	3.591	4.128	5.39	2.53	2.982	3.419	4.462	2.405	2.824	3.227	4.195	2.31	2.71	3.097	4.02





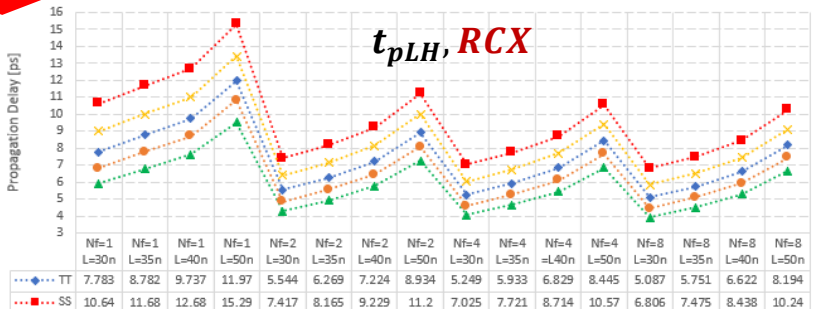
HL Delay VS Nf & L @SVT, VDD=0.9, temp=27 (RCX)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	7.328	8.248	8.949	10.38	5.126	5.771	6.521	7.658	4.996	5.581	6.294	7.431	5.03	5.584	6.288	7.44
SS	10.05	10.99	11.71	13.46	6.901	7.541	8.374	9.742	6.695	7.258	8.041	9.406	6.714	7.231	7.999	9.377
FF	5.556	6.399	7.022	8.219	3.948	4.555	5.204	6.17	3.868	4.429	5.051	6.02	3.91	4.45	5.067	6.052
FS	6.33	7.322	8.03	9.393	4.385	5.073	5.794	6.862	4.284	4.908	5.592	6.658	4.317	4.909	5.583	6.661
SF	8.538	9.386	10.05	11.59	6.005	6.607	7.37	8.607	5.857	6.396	7.122	8.366	5.912	6.415	7.132	8.395

× ~2

LH Delay VS Nf & L @SVT, VDD=0.9, temp=27 (RCX)

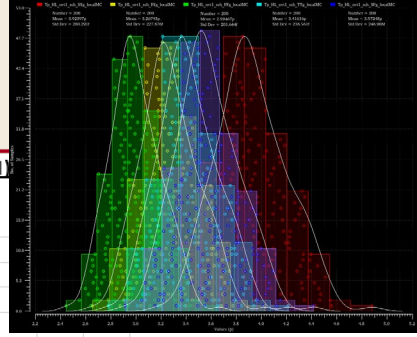


	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	7.783	8.782	9.737	11.97	5.544	6.269	7.224	8.934	5.249	5.933	6.829	8.445	5.087	5.751	6.622	8.194
SS	10.64	11.68	12.68	15.29	7.417	8.165	9.229	11.2	7.025	7.721	8.714	10.57	6.806	7.475	8.438	10.24
FF	5.91	6.78	7.623	9.522	4.289	4.932	5.758	7.237	4.056	4.668	5.446	6.849	3.931	4.526	5.285	6.652
FS	8.983	10	11	13.41	6.397	7.139	8.156	9.994	6.042	6.74	7.69	9.41	5.831	6.507	7.427	9.089
SF	6.81	7.786	8.702	10.82	4.844	5.548	6.444	8.069	4.584	5.252	6.097	7.643	4.442	5.093	5.918	7.432

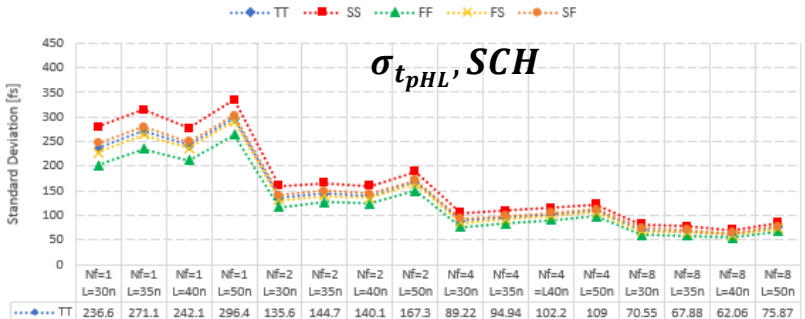
t_{pSCH}~4ps

t_{pRCX}~8ps

SVT Propagation Delay – Monte Carlo: HL / LH



HL Delay Std VS Nf & L @SVT, VDD=0.9, temp=27 (SCH)



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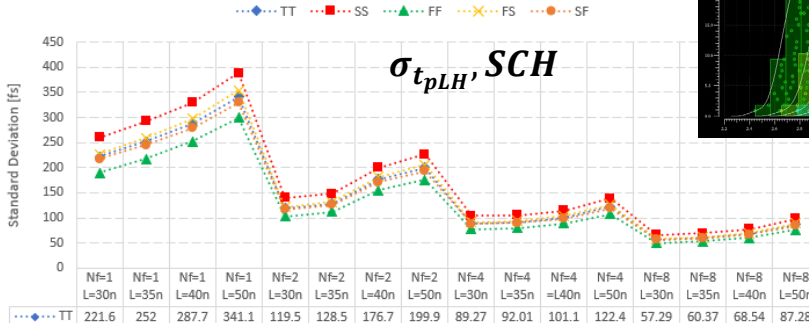
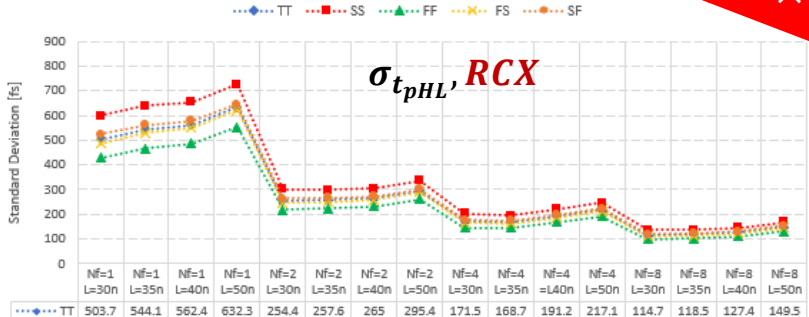
TT	236.6	271.1	242.1	296.4	135.6	144.7	140.1	167.3	89.22	94.94	102.2	109	70.55	67.88	62.06	75.87
SS	280.3	314.5	277.5	335.2	159.4	166.4	159.5	188.4	104.5	109	115.7	122.7	82.71	77.96	70.38	85.27
FF	201.6	235.4	212.4	263.2	116.5	126.8	123.7	149.2	76.92	83.27	90.77	97.19	60.76	59.56	55.05	67.81
FS	227.9	263.3	236.1	291	130.4	140.1	136	163.7	85.58	91.79	99.1	106.4	67.44	65.43	60.01	73.79
SF	246.9	280.1	249	302.6	141.8	150.2	144.7	171.4	93.54	98.63	105.8	111.9	74.28	70.75	64.42	78.24

LH Delay Std VS Nf & L @SVT, VDD=0.9, temp=27 (SCH)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	221.6	252	287.7	341.1	119.5	128.5	176.7	199.9	89.27	92.01	101.1	122.4	57.29	60.37	68.54	87.28
SS	260.1	292.9	329	387.8	139.9	148.2	200.6	226.9	103.8	105.9	114.8	138.4	65.87	69.35	77.74	98.74
FF	190	217.6	251.7	299.4	103	111.9	155.5	176	77.44	80.27	89.13	108.2	50.15	52.97	60.46	77.18
FS	226.4	258.6	297.3	353.3	122.2	131.6	182	206.5	91.12	94.1	104	126	58.24	61.57	70.02	89.44
SF	217.4	245.7	278.5	329.2	117.3	125.7	171.5	193.6	87.72	90.01	98.37	118.9	56.53	59.4	67.07	85.14

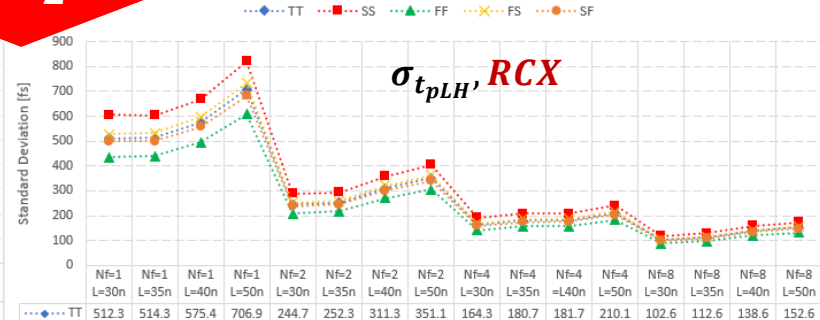
HL Delay Std VS Nf & L @SVT, VDD=0.9, temp=27 (RCX)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	503.7	544.1	562.4	632.3	254.4	257.6	265	295.4	171.5	168.7	191.2	217.1	114.7	118.5	127.4	149.5
SS	599.4	638.7	653.4	726.8	300.9	298.1	303.3	335.8	202.9	195.4	219.1	246.7	135.5	137.7	146.1	169.8
FF	427.7	467.2	487.1	553	217.1	224.5	233	261.1	146.2	146.7	167.8	192	98.13	102.8	111.9	132.3
FS	486.5	530.1	548.8	621.4	246.3	250.2	258.7	289.8	165.6	163.8	186.1	212.5	110.4	114.9	123.8	146
SF	524.9	560.8	578.1	645.4	264.2	266.4	272.3	301.9	178.4	174.5	197	222.4	119.9	122.5	131.6	153.6

× ~2

LH Delay Std VS Nf & L @SVT, VDD=0.9, temp=27 (RCX)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	512.3	514.3	575.4	706.9	244.7	252.3	311.3	351.1	164.3	180.7	181.7	210.1	102.6	112.6	138.6	152.6
SS	606.2	603.5	669.1	821.1	289.3	294.5	357.8	404.3	193.1	207.8	209	241.3	119.6	130.9	159.7	174.5
FF	436.1	440.4	495.8	608.1	208.5	217.3	271.2	304.9	140.8	157.8	158.2	183.1	88.63	97.39	120.2	133.4
FS	528.2	531.6	595.8	732.7	251.7	259.4	322.9	363.6	168.9	186.9	187.9	217.1	105.3	115.4	142.3	157.6
SF	498.6	498.5	556.2	682.1	238.5	245.9	300.4	339.2	160.4	175.1	175.9	203.5	100.3	110.1	134.9	147.8

Settings:

- Global Corner + Local MC
- 5 corners:
  - ❑ TT, 0.9V, 27°C
  - ❑ SS, 0.9V, 27°C
  - ❑ FF, 0.9V, 27°C
  - ❑ FS, 0.9V, 27°C
  - ❑ SF, 0.9V, 27°C
- N° of runs per corner: 200

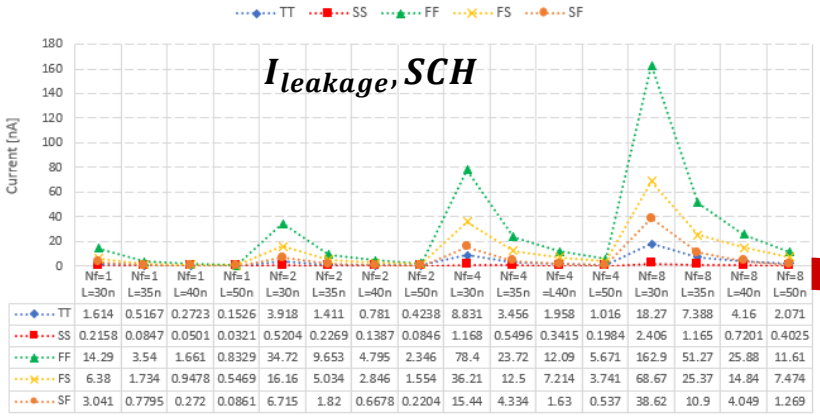
$\sigma_{t_{pSCH}} \sim 200fs$

$\sigma_{t_{pRCX}} \sim 400fs$

SVT Current Consumption: Leakage / Dynamic@1MHz

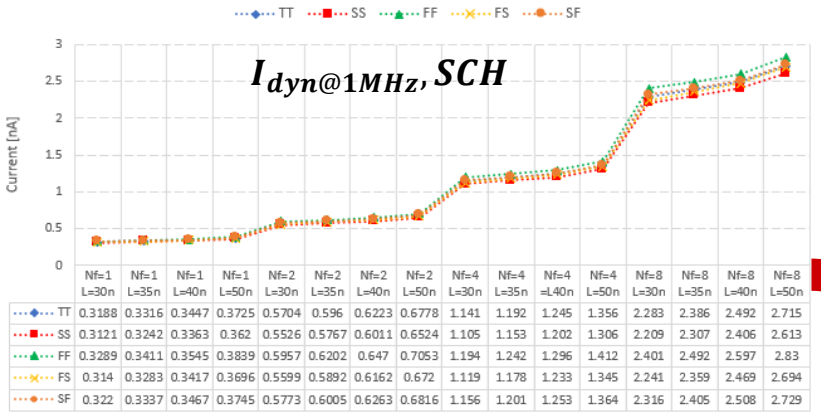
TID-ID

Leakage I VS Nf & L @SVT, VDD=0.9, temp=27 (SCH)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	1.614	0.5167	0.2723	0.1526	3.918	1.411	0.781	0.4238	8.831	3.456	1.958	1.016	18.27	7.388	4.16	2.071
SS	0.2158	0.0847	0.0501	0.0321	0.5204	0.2269	0.1387	0.0846	1.168	0.5496	0.3415	0.1984	2.406	1.165	0.7201	0.4025
FF	14.29	3.54	1.661	0.8329	34.72	9.653	4.795	2.346	78.4	23.72	12.09	5.671	162.9	51.27	25.88	11.61
FS	6.38	1.734	0.9478	0.5469	16.16	5.034	2.846	1.554	36.21	12.5	7.214	3.741	68.67	25.37	14.84	7.474
SF	3.041	0.7795	0.272	0.0861	6.715	1.82	0.6678	0.2204	15.44	4.334	1.63	0.537	38.62	10.9	4.049	1.269

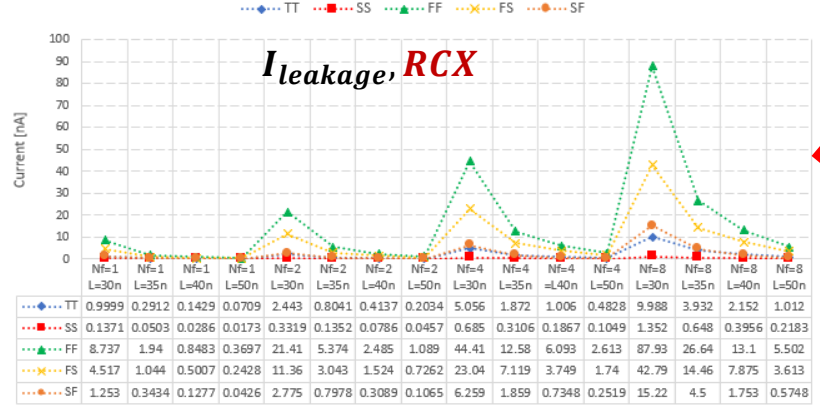
Dynamic I @ 1MHz VS Nf & L @SVT, VDD=0.9, temp=27 (SCH)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	0.3188	0.3316	0.3447	0.3725	0.5704	0.596	0.6223	0.6778	1.141	1.192	1.245	1.356	2.283	2.386	2.492	2.715
SS	0.3121	0.3242	0.3363	0.362	0.5526	0.5767	0.6011	0.6524	1.105	1.153	1.202	1.306	2.209	2.307	2.406	2.613
FF	0.3289	0.3411	0.3545	0.3839	0.5957	0.6202	0.647	0.7053	1.194	1.242	1.296	1.412	2.401	2.492	2.597	2.83
FS	0.314	0.3283	0.3417	0.3696	0.5599	0.5892	0.6162	0.672	1.119	1.178	1.233	1.345	2.241	2.359	2.469	2.694
SF	0.322	0.3337	0.3467	0.3745	0.5773	0.6005	0.6263	0.6816	1.156	1.201	1.253	1.364	2.316	2.405	2.508	2.729

× ~0.5

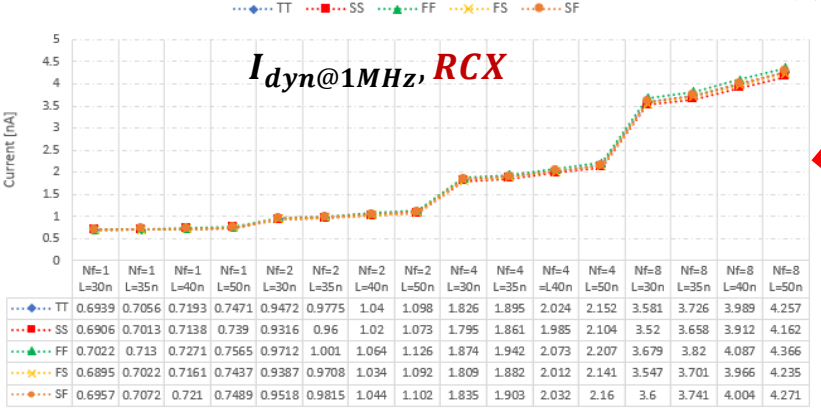
Leakage I VS Nf & L @SVT, VDD=0.9, temp=27 (RCX)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	0.9999	0.2912	0.1429	0.0709	2.443	0.8041	0.4137	0.2034	5.056	1.872	1.006	0.4828	9.988	3.932	2.152	1.012
SS	0.1371	0.0503	0.0286	0.0173	0.3319	0.1352	0.0786	0.0457	0.685	0.3106	0.1867	0.1049	1.352	0.648	0.3956	0.2183
FF	8.737	1.94	0.8483	0.3697	21.41	5.374	2.485	1.089	44.41	12.58	6.093	2.613	87.93	26.64	13.1	5.502
FS	4.517	1.044	0.5007	0.2428	11.36	3.043	1.524	0.7262	23.04	7.119	3.749	1.74	42.79	14.46	7.875	3.613
SF	1.253	0.3434	0.1277	0.0426	2.775	0.7978	0.3089	0.1065	6.259	1.859	0.7348	0.2519	15.22	4.5	1.753	0.5748

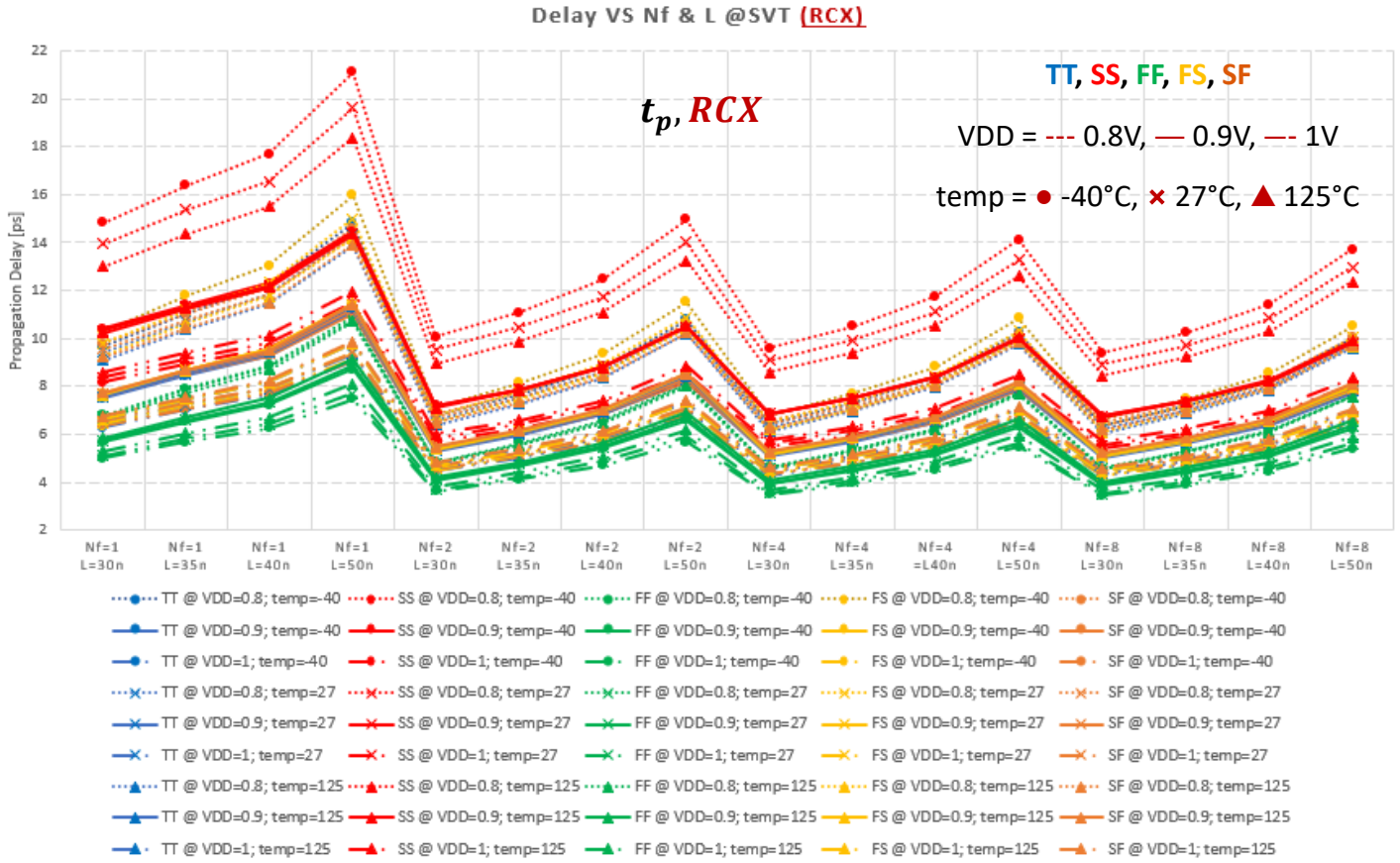
× ~1.8

Dynamic I @ 1MHz VS Nf & L @SVT, VDD=0.9, temp=27 (RCX)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	0.6939	0.7056	0.7193	0.7471	0.9472	0.9775	1.04	1.098	1.826	1.895	2.024	2.152	3.581	3.726	3.989	4.257
SS	0.6906	0.7013	0.7138	0.739	0.9316	0.96	1.02	1.073	1.795	1.861	1.985	2.104	3.52	3.658	3.912	4.162
FF	0.7022	0.713	0.7271	0.7565	0.9712	1.001	1.064	1.126	1.874	1.942	2.073	2.207	3.679	3.82	4.087	4.366
FS	0.6895	0.7022	0.7161	0.7437	0.9387	0.9708	1.034	1.092	1.809	1.882	2.012	2.141	3.547	3.701	3.966	4.235
SF	0.6957	0.7072	0.721	0.7489	0.9518	0.9815	1.044	1.102	1.835	1.903	2.032	2.16	3.6	3.741	4.004	4.271

SVT Propagation Delay VS corners, VDD, temp



$$t_p = \frac{t_{pHL} + t_{pLH}}{2}$$

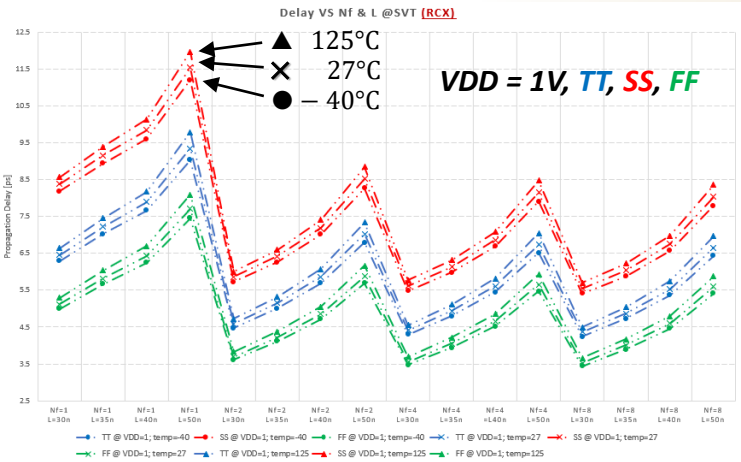
- Best Case (Fastest):
  FF @ VDD=1V & -40°C
- Worst Case (Slowest):
  SS @ VDD=0.8V & -40°C
  [expected: SS @ VDD=0.8V & 125°C]

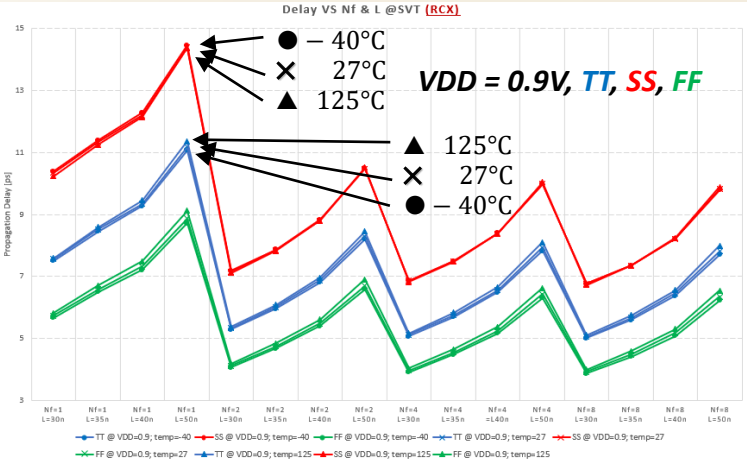
$$\frac{WorstCase}{Typical} \sim 1.9$$

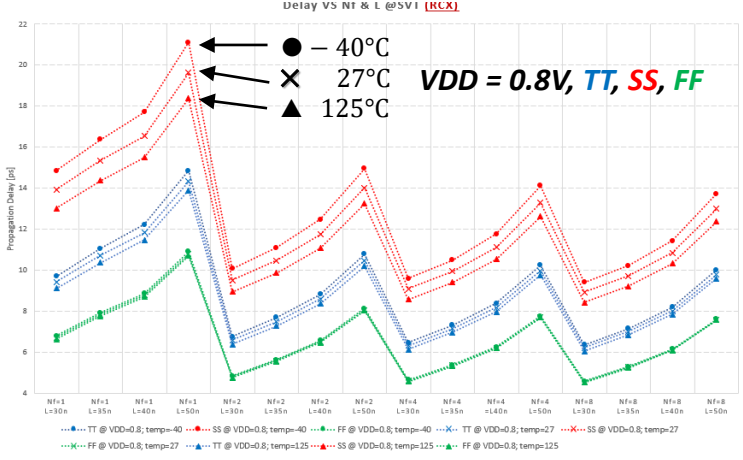
$$\frac{BestCase}{Typical} \sim 0.68$$

- Typical:
  TT @ VDD=0.9V & 27°C

SVT Propagation Delay VS corners, VDD, temp



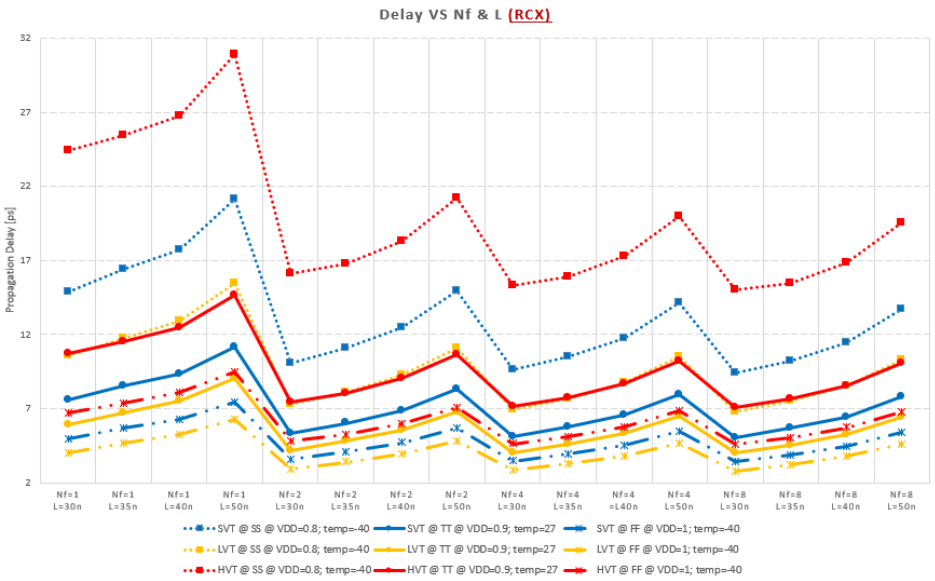




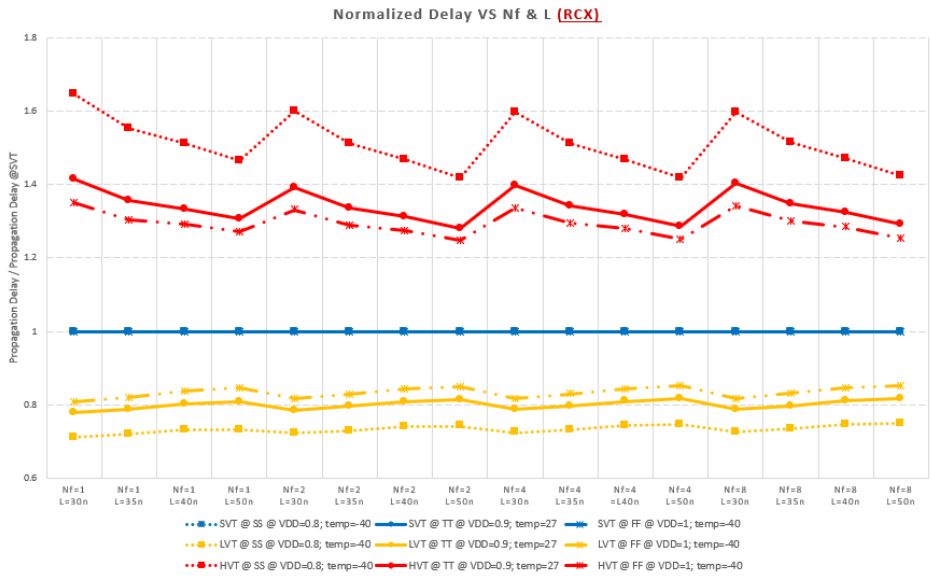
- Very small variation with temperature [especially at VDD=0.9V)] **(?)**
- At VDD = 0.8V, the delay is higher for lower temperatures [weak inversion effect **(?)**; $I_{diffusion} > I_{drift}$ **(?)**]

Propagation Delay: SVT, LVT, HVT

t_p, RCX

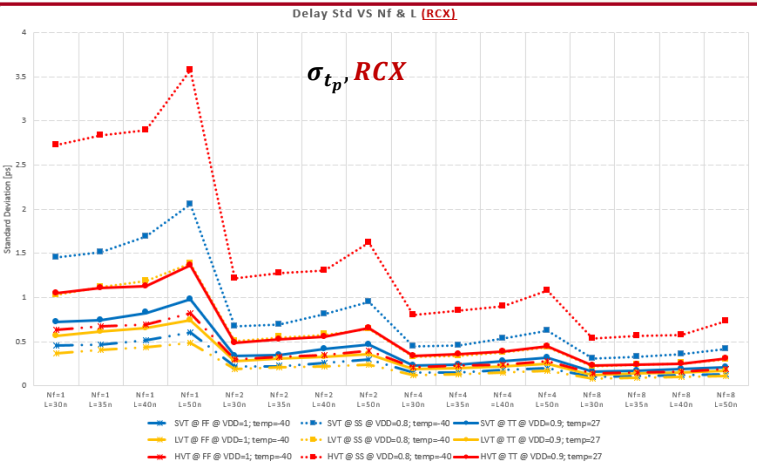


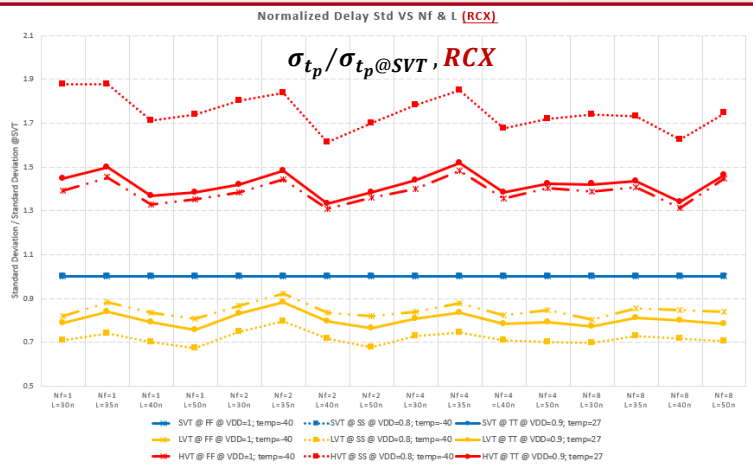
$\frac{t_p}{t_{p@SVT}}, RCX$

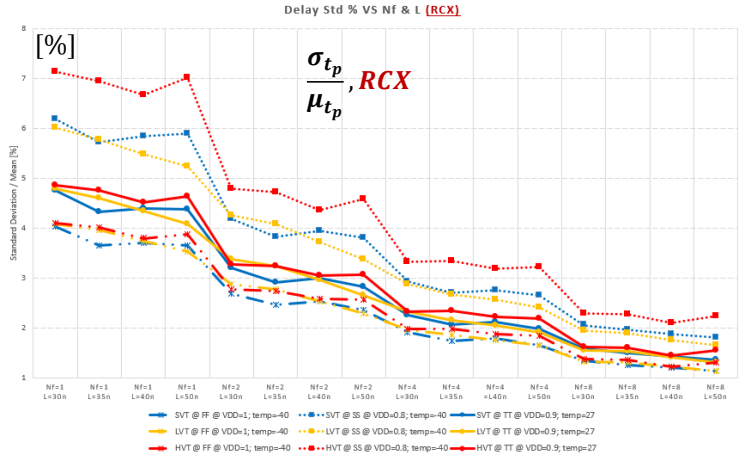


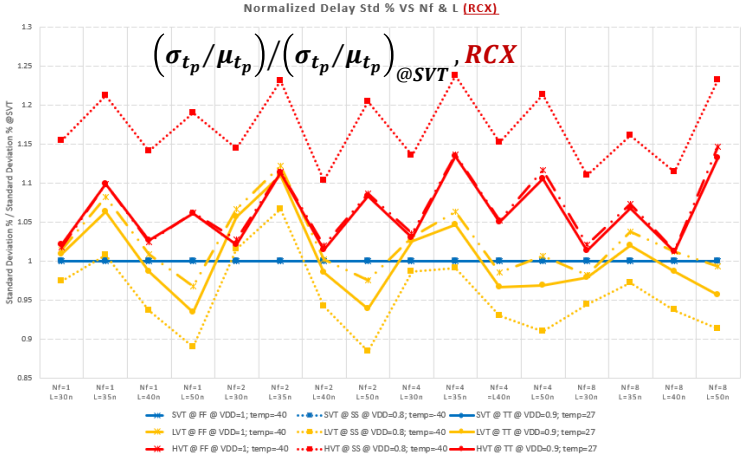
SVT	$SS;\ VDD = 0.8V;\ temp = -40°C$
LVT	$TT;\ VDD = 0.9V;\ temp = 27°C$
HVT	$FF;\ VDD = 1V;\ \ temp = -40°C$

Propagation Delay – Monte Carlo: SVT, LVT, HVT









Settings:

- Global Corner + Local MC
- 5 corners:
  - ❑ TT, 0.9V, 27°C
  - ❑ SS, 0.8V, -40°C
  - ❑ FF, 1V, -40°C
- N° of runs per corner: 1000

$$\sigma_{t_p} = \sqrt{\sigma_{t_{pHL}}{}^2 + \sigma_{t_{pLH}}{}^2}$$

- $\frac{\sigma_{t_p}}{\mu_{t_p}}$ similar (+24%, -11%) for SVT, LVT and HVT structures

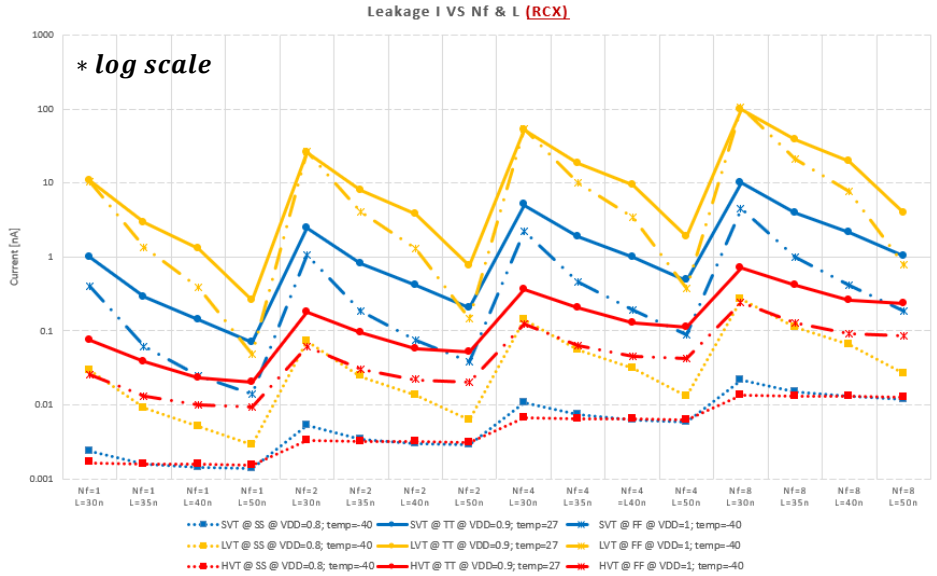
SVT
LVT
HVT

---■ $SS;\ VDD = 0.8V; T = -40°C$
—● $TT;\ VDD = 0.9V; T = 27°C$
---× $FF;\ VDD = 1V;\quad T = -40°C$

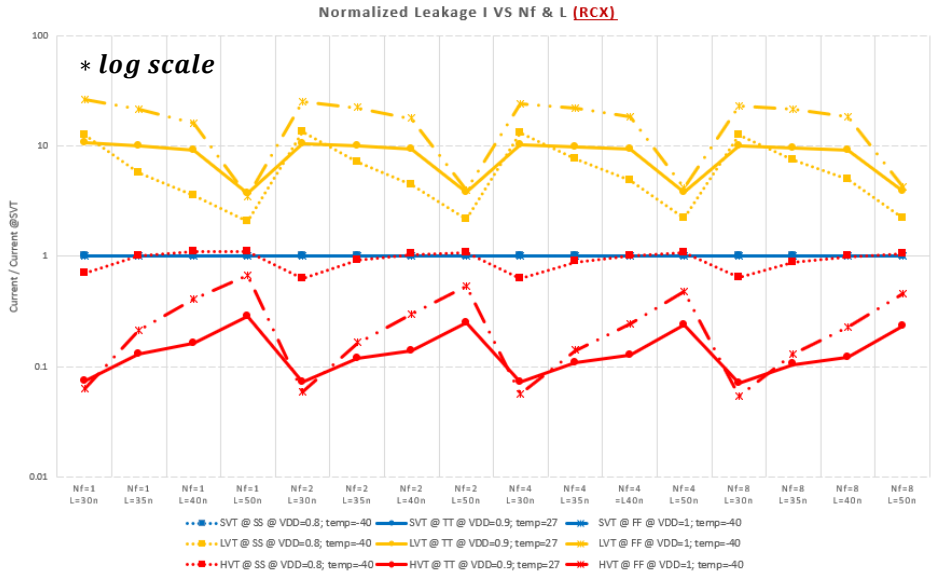
Leakage Current: SVT, LVT, HVT

TID-ID SLAC

$I_{leakage}$, RCX



$\frac{I_{leakage}}{I_{leakage@SVT}}$, RCX

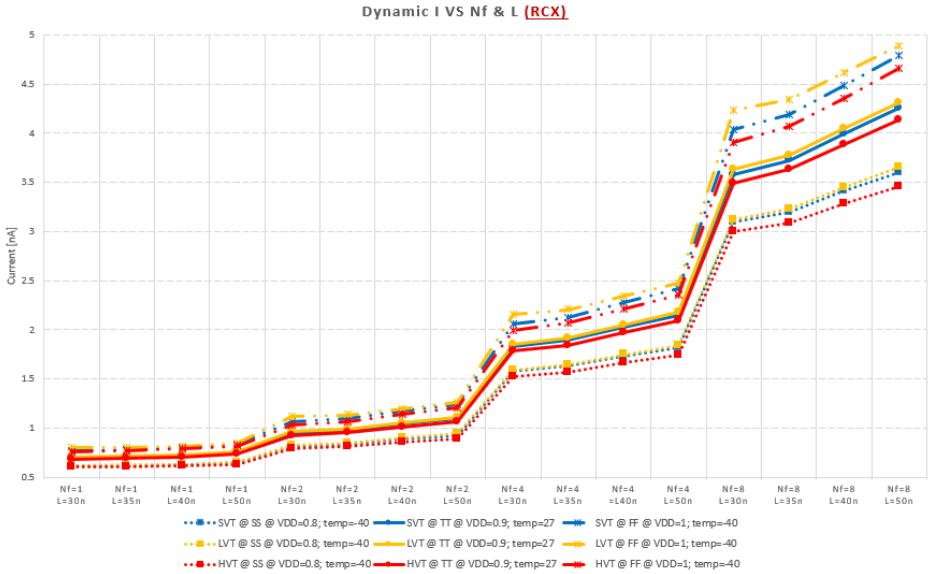


SVT	---■ $SS;\ VDD = 0.8V;\ temp = -40°C$
LVT	—● $TT;\ VDD = 0.9V;\ temp = 27°C$
HVT	—--× $FF;\ VDD = 1V;\quad temp = -40°C$

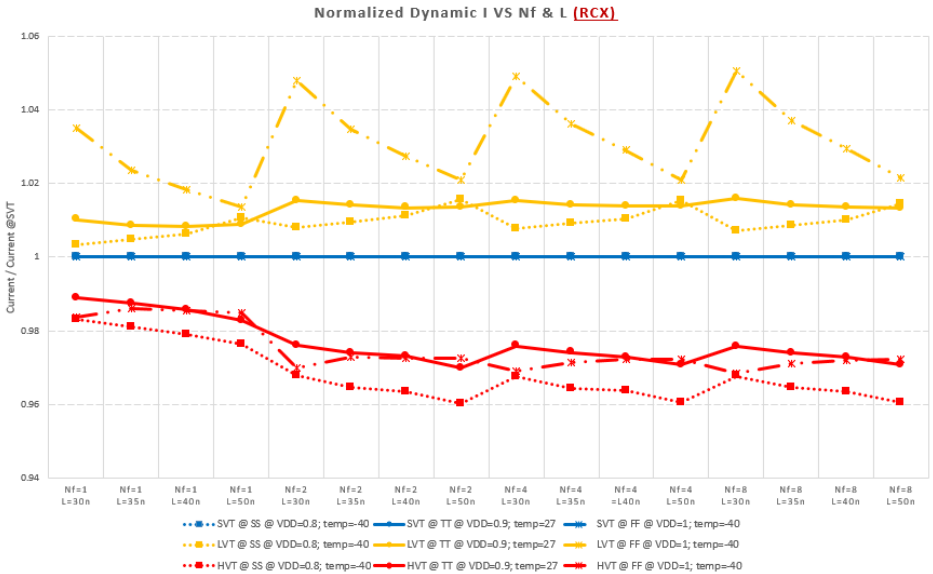
Dynamic Current @1MHz: SVT, LVT, HVT

TID-ID SLAC

$I_{dyn@1MHz}$, RCX



$\frac{I_{dyn@1MHz}}{I_{dyn@1MHz@SVT}}$, RCX



SVT ---■ $SS;\ VDD = 0.8V;\ temp = -40°C$

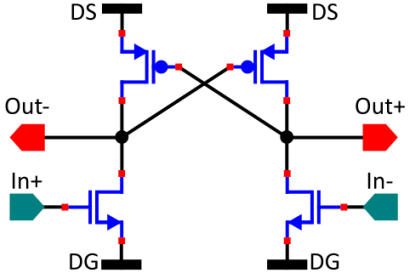
LVT —● $TT;\ VDD = 0.9V;\ temp = 27°C$

HVT —-×- $FF;\ VDD = 1V;\quad temp = -40°C$

- Dynamic consumption very similar (+5%, -4%) for SVT, LVT and HVT structures

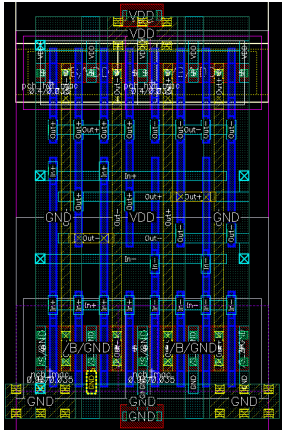
More complex Delay Cells

- Differential Cascode Voltage Switch Logic (DCVSL) implementation:



Cell variants:

- **Cell A**: nmos: **SVT**; pmos: **HVT**
- **Cell B**: nmos: **LVT**; pmos: **HVT**
- **Cell C**: nmos: **LVT**; pmos: **SVT**
- **Cell D**: nmos: **LVT**; pmos: **LVT**

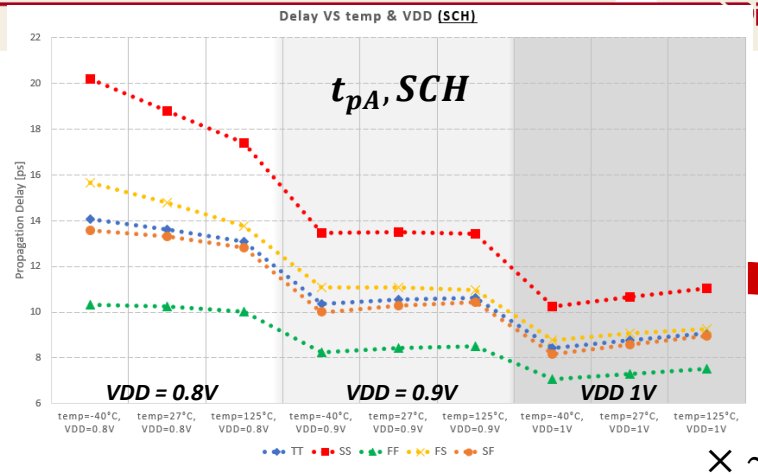


MOS dimensions:

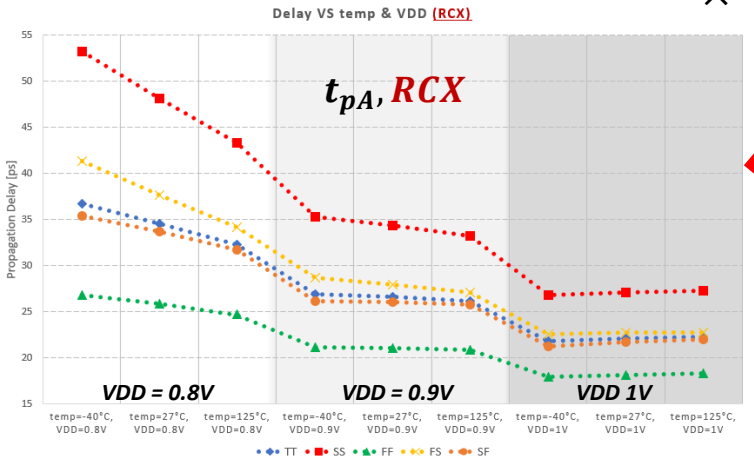
- Wp=100n
- Wn=240n
- L=35n
- Nf=4

Layout:

- M1&M2 – Signal Connections
- M3 – VDD & GND planes covering the cells

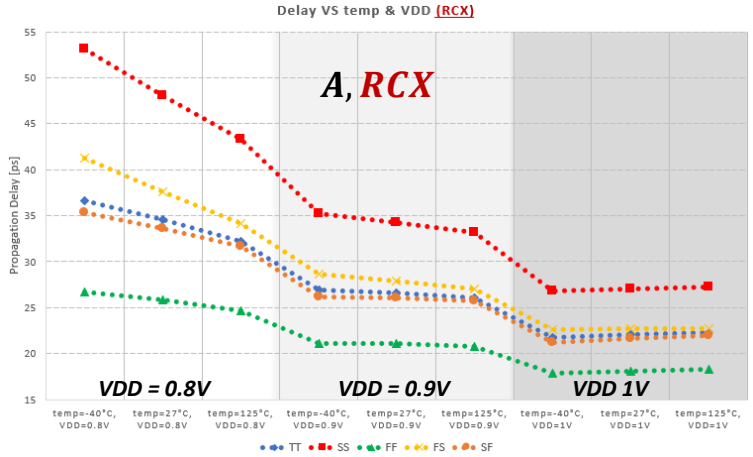


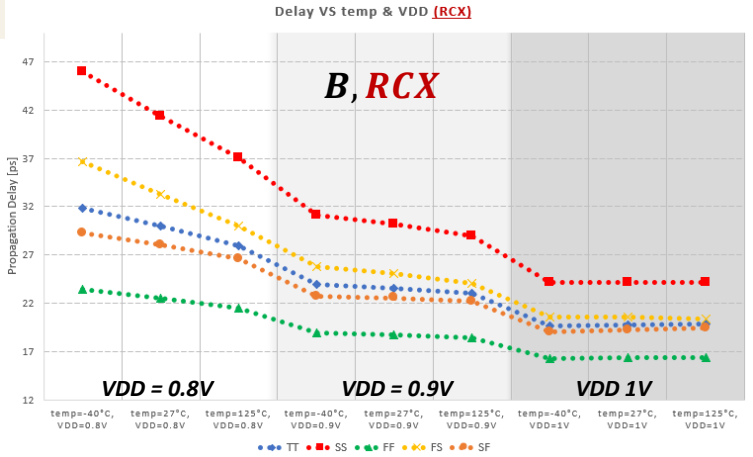
$\times \sim 2.5^{*}$

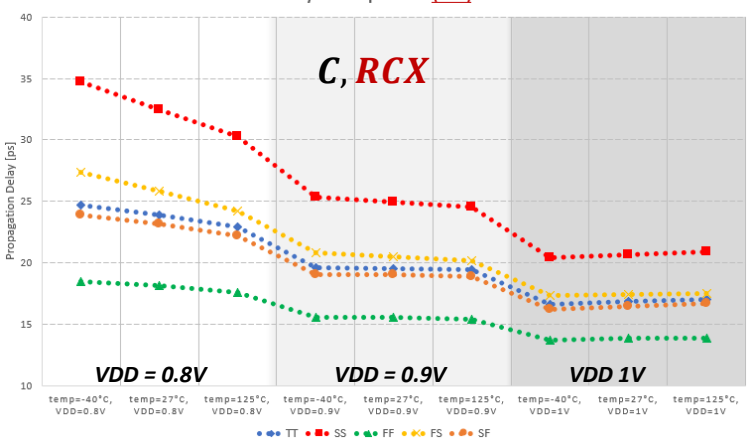


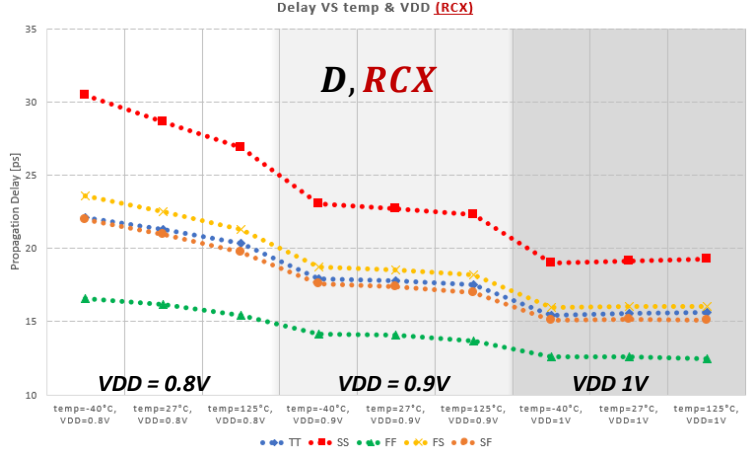
*First layout iteration had propagation delay 3.5x times bigger than in the schematic; parasitics play a big role

More complex Delay Cells: Propagation Delay









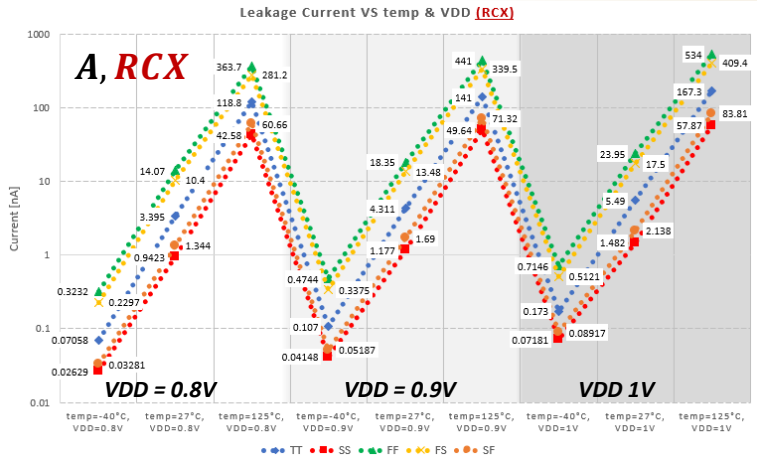
Cell variants:

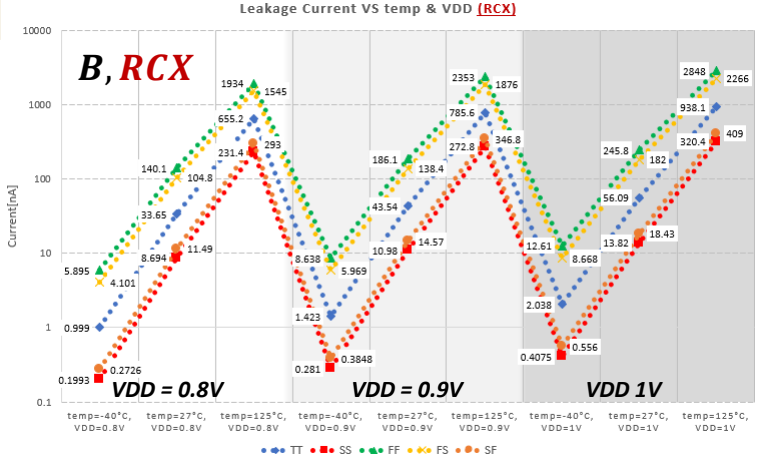
- **Cell A**: nmos: **SVT**; pmos: **HVT**
- **Cell B**: nmos: **LVT**; pmos: **HVT**
- **Cell C**: nmos: **LVT**; pmos: **SVT**
- **Cell D**: nmos: **LVT**; pmos: **LVT**

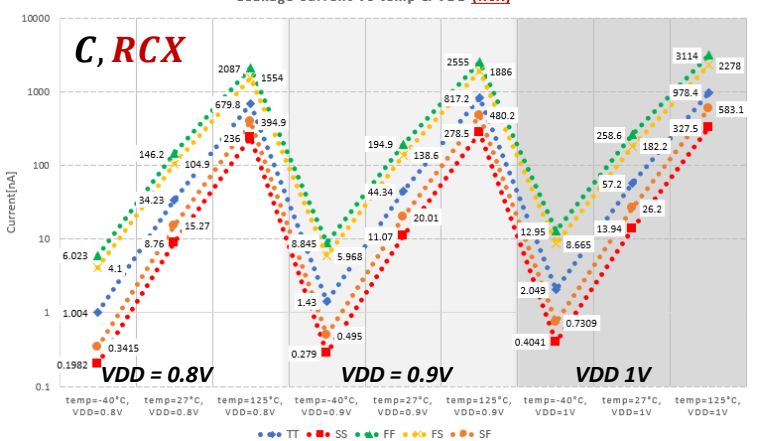
Very low propagation delay dependance on temperature

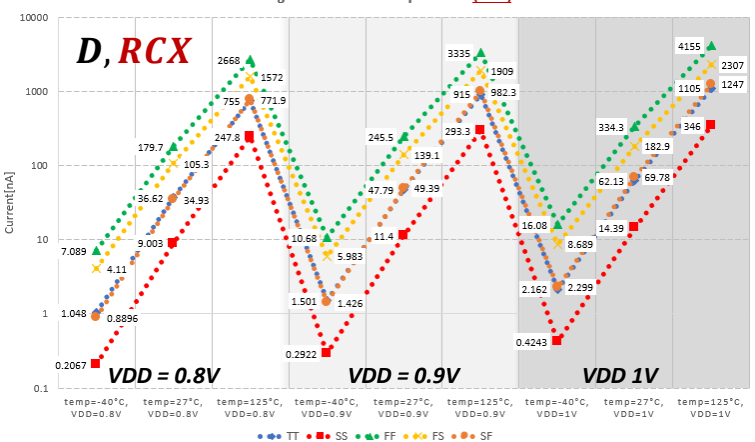
More complex Delay Cells: Leakage Current

TID-ID SLAC









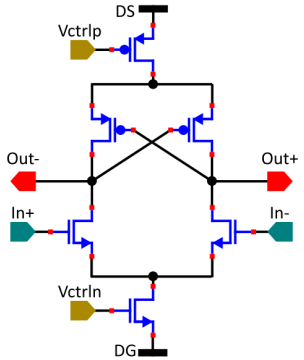
Cell variants:

- **Cell A**: nmos: **SVT**; pmos: **HVT**
- **Cell B**: nmos: **LVT**; pmos: **HVT**
- **Cell C**: nmos: **LVT**; pmos: **SVT**
- **Cell D**: nmos: **LVT**; pmos: **LVT**

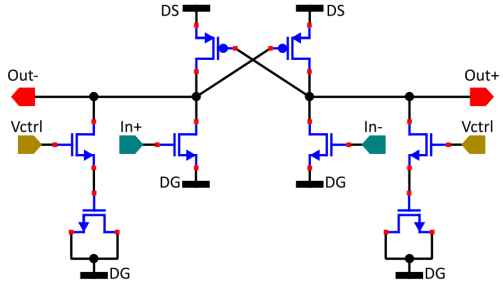
Very high leakage current dependance on temperature

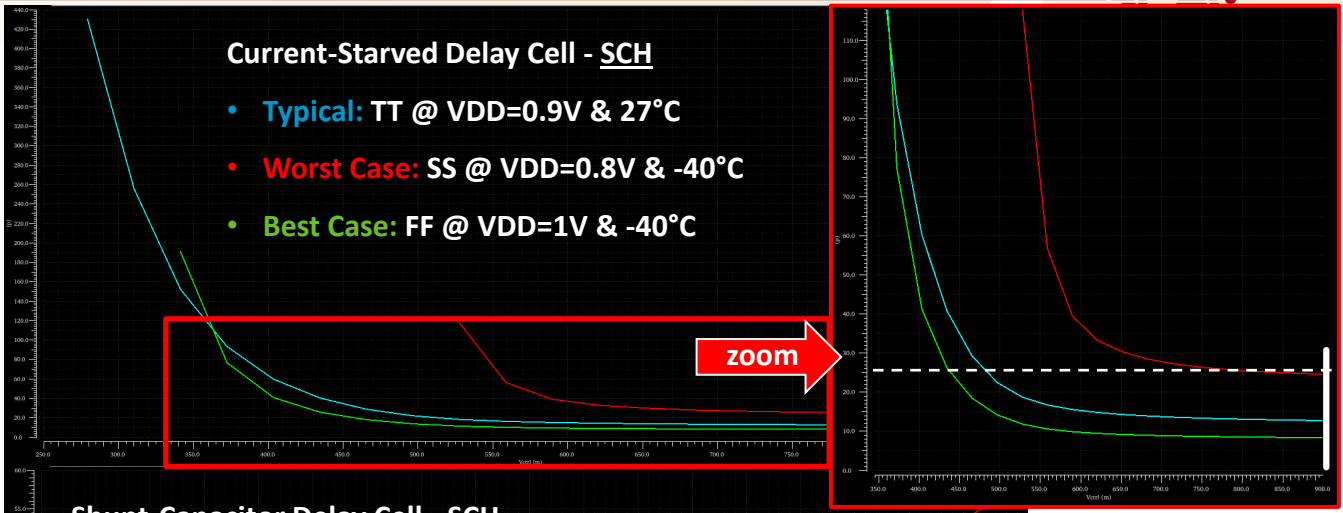
Voltage-Controlled Delay Cells – Quick Comparison

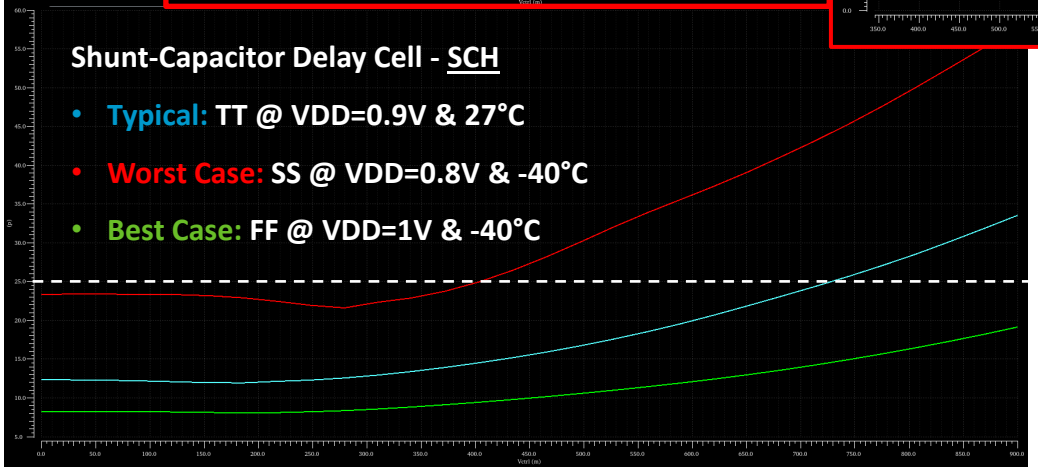
- Current-Starved Delay Cell:



- Shunt-Capacitor Delay Cell:







Next Steps

- ❑ Design and layout of Current-Starved and Shunt-Capacitor delay cells (different variants)
- ❑ Performance comparison between CS and SC approaches
- ❑ Schematic and layout optimization of the chosen Voltage-Controlled Delay Cell
- ❑ TDC architecture definition & design