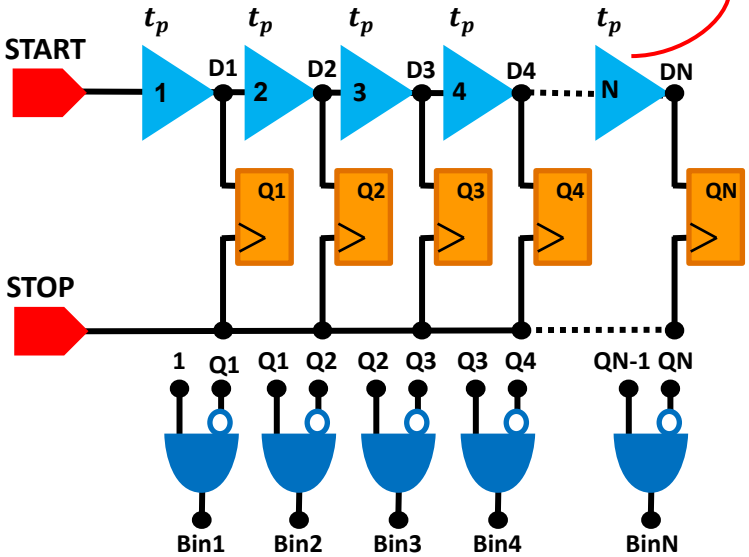
Delay Line TDC

- Majority of modern TDCs is based on some version of a delay-line structure:

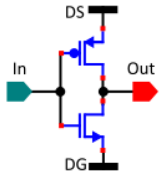


- TDC resolution given by the propagation delay of the elementary cell:

$$LSB_{TDC} = t_p$$

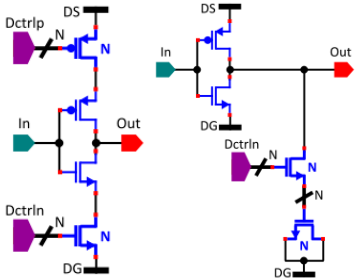
- Basic element: **Delay Cell**

- Simple Logic Cell:



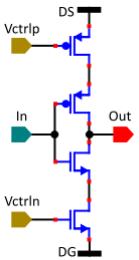
  - Used in FPGA TDCs
  - Requires constant calibration

- Digitally-Controlled Delay Cell:



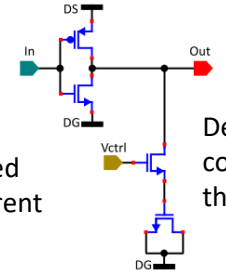
- Voltage-Controlled Delay Cell:

  - Current starved:



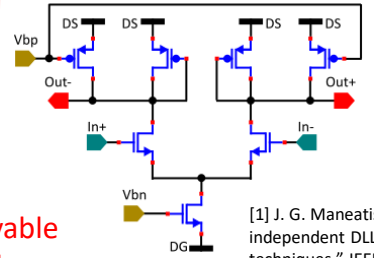
Delay controlled thru current

  - Shunt capacitor:



Delay controlled thru load

- Differential delay cell with symmetric loads (Maneatis cell [1]):



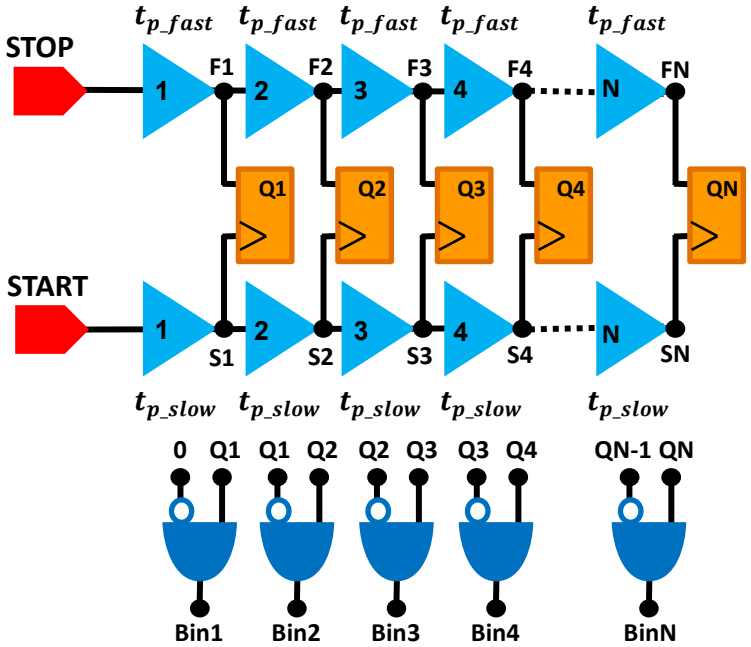
  - Frequently used in PLL VCOs and some DLLs
  - Consumes Static Bias Current

Minimum delay limited by fastest achievable logic propagation delay in target technology

[1] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," IEEE J. Solid-State Circuits, vol. 31, no. 11, pp. 1723–1732, Nov. 1996.

Vernier Delay Line TDC

- What if resolutions lower than minimum propagation delay is required? → **Vernier Delay Line**



$$LSB_{TDC} = t_{p\_slow} - t_{p\_fast}$$

- **START** signal propagates in the **Slow Delay Line** ($t_{p\_slow} > t_{p\_fast}$)
- **STOP** signal propagates in the **Fast Delay Line**

  - The **START** pulse comes first and initializes the TDC operation.
  - The **STOP** pulse follows the **START** with a delay that represents the time interval to be digitalized.
  - At each tap of the Delay Line the **STOP** signal catches up to the **START** signal by the deference of the propagation delays of cells in Slow and Fast branches, i.e., $t_{p\_slow} - t_{p\_fast}$ represents the **LSB** of time measurement.
  - The number of cells necessary for **STOP** signal to surpass the **START** signal represents the result of TDC conversion.

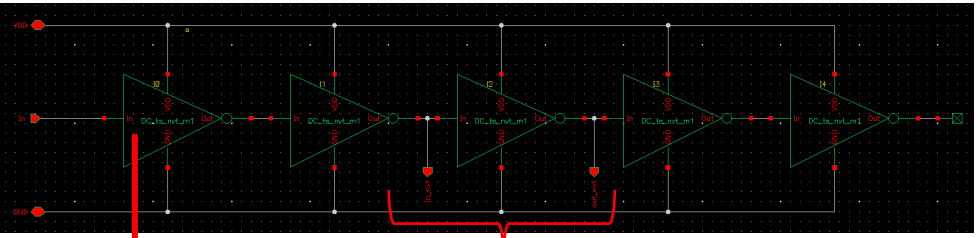
Compare to the simple Delay Line, Vernier Delay Line allows for TDC resolutions below the minimum logic propagation delay in the technology but suffer from higher power and area consumption and slower conversion times.

Characterizing the propagation delay in the technology necessary for defining the TDC architecture

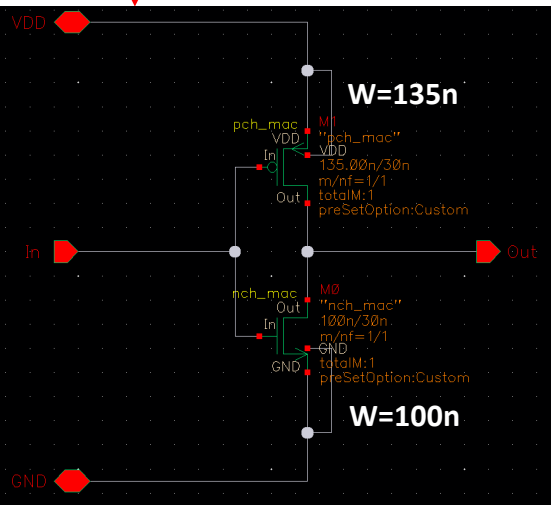
Testbench

TID-ID SLAC

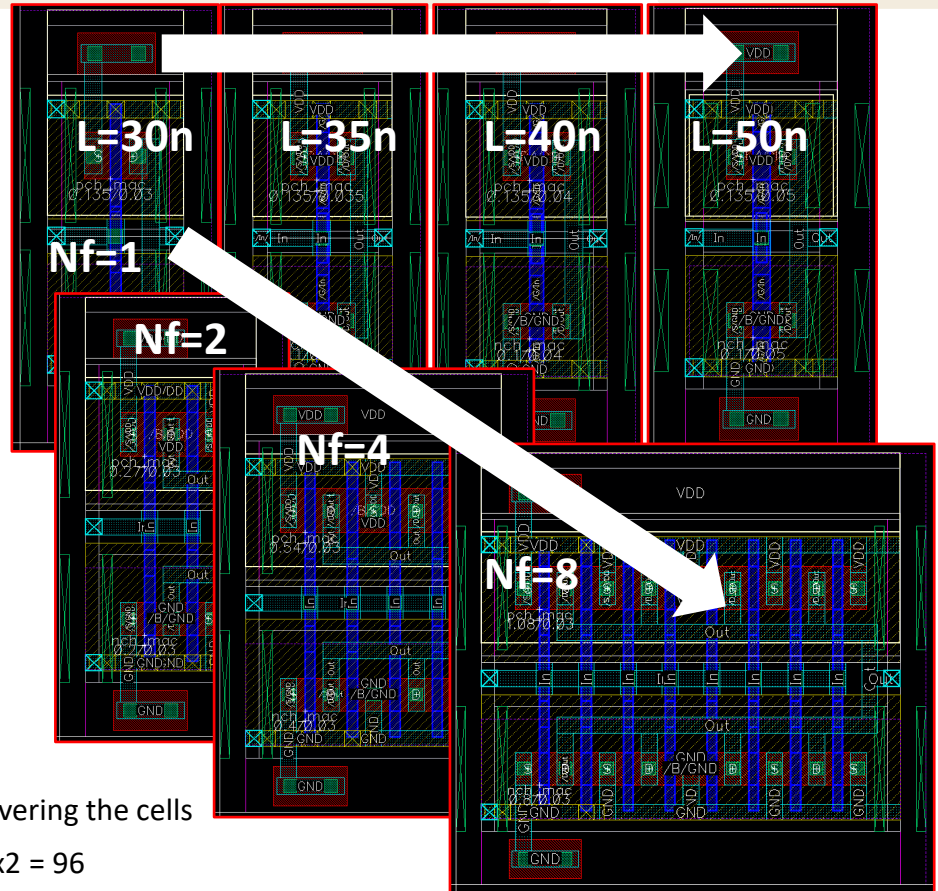
Delay Line Test Structure:



t_p - Cell Propagation Delay



SVT, LVT, HVT



Simulations: Spectre

- **SCH** – Schematic
- **RCX** – Parasitic Extracted

Extraction: Calibre PEX

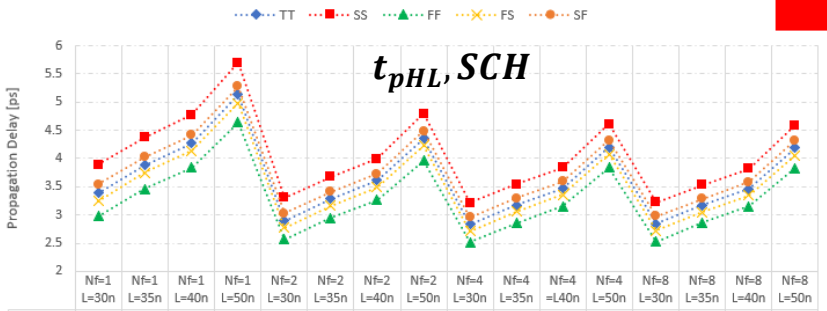
- M1 – Signal Connections
- M2 – VDD & GND planes covering the cells

Total Number of Views: 4x4x3x2 = 96

SVT Propagation Delay: HL / LH VS Corners

TID-ID SLAC

HL Delay VS Nf & L @SVT, VDD=0.9, temp=27 (SCH)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	3.39	3.882	4.276	5.13	2.901	3.285	3.61	4.354	2.83	3.173	3.476	4.197	2.846	3.169	3.464	4.185
SS	3.892	4.377	4.773	5.697	3.302	3.674	3.997	4.798	3.213	3.539	3.838	4.614	3.225	3.528	3.818	4.59
FF	2.974	3.458	3.841	4.638	2.568	2.952	3.269	3.968	2.512	2.86	3.157	3.836	2.532	2.862	3.154	3.834
FS	3.244	3.744	4.141	4.984	2.776	3.167	3.493	4.227	2.707	3.058	3.362	4.072	2.721	3.052	3.349	4.057
SF	3.544	4.023	4.411	5.279	3.034	3.406	3.727	4.485	2.961	3.292	3.591	4.327	2.979	3.291	3.582	4.319

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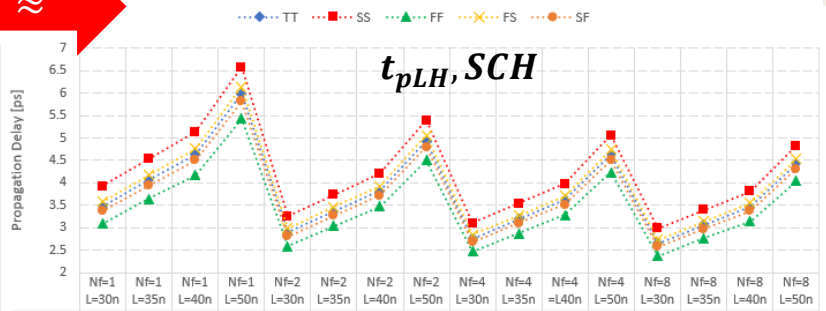
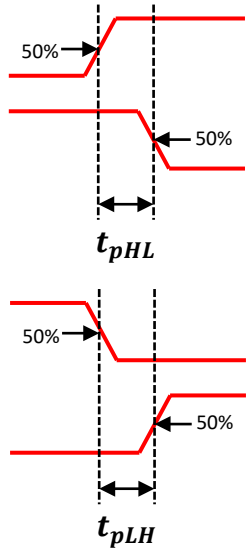
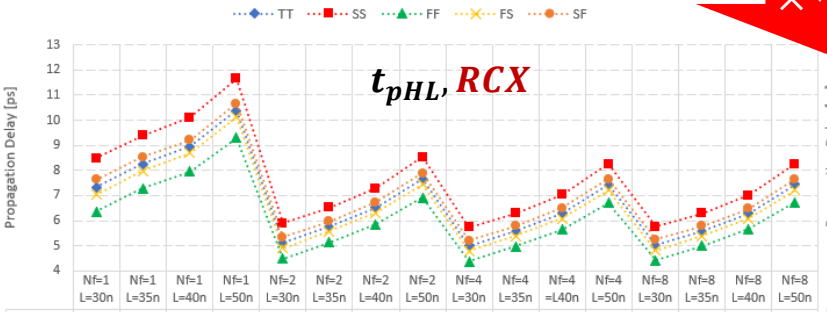
LH Delay VS Nf & L @SVT, VDD=0.9, temp=27 (SCH)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	3.48	4.064	4.634	5.98	2.904	3.37	3.832	4.935	2.766	3.193	3.615	4.63	2.663	3.069	3.469	4.428
SS	3.931	4.536	5.13	6.578	3.26	3.74	4.216	5.396	3.103	3.54	3.974	5.056	2.989	3.402	3.81	4.832
FF	3.091	3.641	4.179	5.425	2.595	3.038	3.476	4.505	2.474	2.881	3.284	4.232	2.381	2.77	3.151	4.05
FS	3.582	4.175	4.757	6.137	2.989	3.462	3.931	5.059	2.846	3.279	3.707	4.742	2.738	3.149	3.554	4.53
SF	3.374	3.945	4.502	5.814	2.816	3.273	3.724	4.804	2.683	3.102	3.516	4.511	2.582	2.981	3.374	4.318



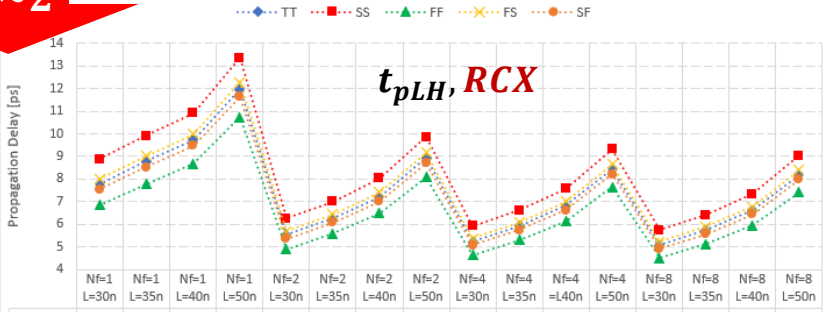
HL Delay VS Nf & L @SVT, VDD=0.9, temp=27 (RCX)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	7.328	8.249	8.95	10.38	5.127	5.771	6.52	7.659	4.997	5.582	6.294	7.432	5.031	5.585	6.288	7.44
SS	8.49	9.394	10.1	11.66	5.895	6.519	7.295	8.528	5.733	6.292	7.026	8.256	5.762	6.283	7.006	8.25
FF	6.372	7.281	7.96	9.286	4.49	5.135	5.845	6.907	4.387	4.978	5.656	6.72	4.425	4.991	5.661	6.74
FS	7.032	7.979	8.69	10.12	4.911	5.572	6.317	7.445	4.788	5.389	6.097	7.223	4.82	5.39	6.09	7.228
SF	7.639	8.526	9.211	10.66	5.353	5.976	6.723	7.879	5.217	5.781	6.491	7.648	5.254	5.787	6.488	7.66

× ~2

LH Delay VS Nf & L @SVT, VDD=0.9, temp=27 (RCX)

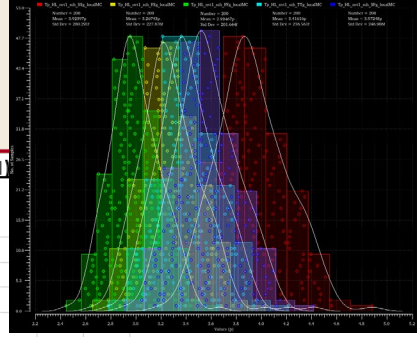


	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	7.784	8.784	9.738	11.97	5.544	6.268	7.224	8.936	5.249	5.933	6.829	8.447	5.089	5.75	6.62	8.195
SS	8.889	9.921	10.91	13.34	6.271	7.014	8.028	9.871	5.94	6.638	7.584	9.325	5.758	6.432	7.35	9.042
FF	6.846	7.786	8.683	10.73	4.919	5.606	6.497	8.078	4.657	5.306	6.143	7.641	4.513	5.145	5.958	7.417
FS	8.013	9.025	9.997	12.28	5.71	6.443	7.419	9.168	5.405	6.096	7.01	8.659	5.234	5.905	6.791	8.393
SF	7.549	8.531	9.464	11.64	5.372	6.084	7.018	8.692	5.089	5.759	6.636	8.222	4.935	5.586	6.437	7.984

$t_{pSCH} \sim 3.5ps$

$t_{pRCX} \sim 7ps$

SVT Propagation Delay – Monte Carlo: HL / LH



HL Delay Std VS Nf & L @SVT, VDD=0.9, temp=27 (SCH)

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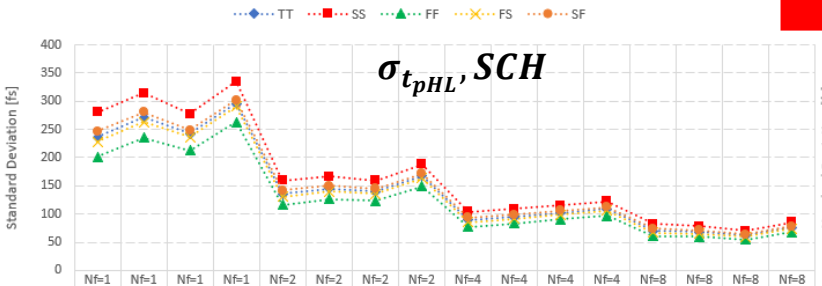
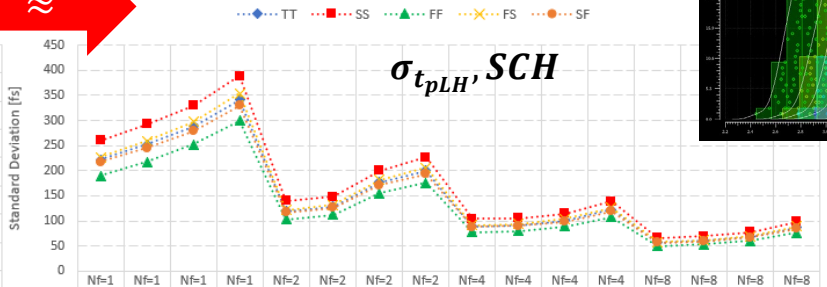
LH Delay Std VS Nf & L @SVT, VDD=0.9, temp=27 (SCH)





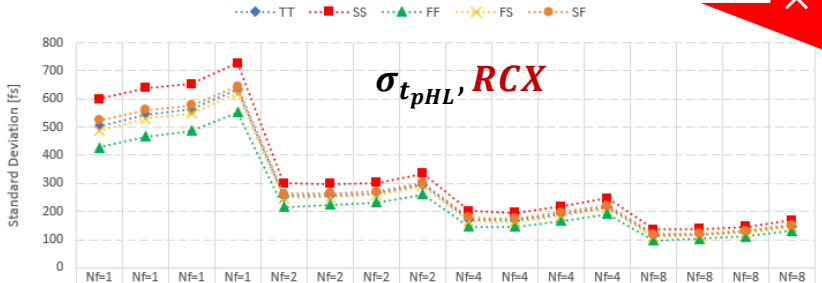
	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	236.6	271.1	242.1	296.4	135.6	144.7	140.1	167.3	89.22	94.94	102.2	109	70.55	67.88	62.06	75.87
SS	280.3	314.5	277.5	335.2	159.4	166.4	159.5	188.4	104.5	109	115.7	122.7	82.71	77.96	70.38	85.27
FF	201.6	235.4	212.4	263.2	116.5	126.8	123.7	149.2	76.92	83.27	90.77	97.19	60.76	59.56	55.05	67.81
FS	227.9	263.3	236.1	291	130.4	140.1	136	163.7	85.58	91.79	99.1	106.4	67.44	65.43	60.01	73.79
SF	246.9	280.1	249	302.6	141.8	150.2	144.7	171.4	93.54	98.63	105.8	111.9	74.28	70.75	64.42	78.24

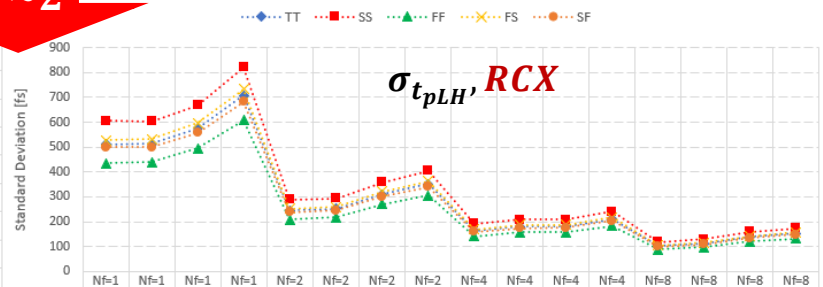
	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	221.6	252	287.7	341.1	119.5	128.5	176.7	199.9	89.27	92.01	101.1	122.4	57.29	60.37	68.54	87.28
SS	260.1	292.9	329	387.8	139.9	148.2	200.6	226.9	103.8	105.9	114.8	138.4	65.87	69.35	77.74	98.74
FF	190	217.6	251.7	299.4	103	111.9	155.5	176	77.44	80.27	89.13	108.2	50.15	52.97	60.46	77.18
FS	226.4	258.6	297.3	353.3	122.2	131.6	182	206.5	91.12	94.1	104	126	58.24	61.57	70.02	89.44
SF	217.4	245.7	278.5	329.2	117.3	125.7	171.5	193.6	87.72	90.01	98.37	118.9	56.53	59.4	67.07	85.14

HL Delay Std VS Nf & L @SVT, VDD=0.9, temp=27 (RCX)

× ~2

LH Delay Std VS Nf & L @SVT, VDD=0.9, temp=27 (RCX)





	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	503.7	544.1	562.4	632.3	254.4	257.6	265	295.4	171.5	168.7	191.2	217.1	114.7	118.5	127.4	149.5
SS	599.4	638.7	653.4	726.8	300.9	298.1	303.3	335.8	202.9	195.4	219.1	246.7	135.5	137.7	146.1	169.8
FF	427.7	467.2	487.1	553	217.1	224.5	233	261.1	146.2	146.7	167.8	192	98.13	102.8	111.9	132.3
FS	486.5	530.1	548.8	621.4	246.3	250.2	258.7	289.8	165.6	163.8	186.1	212.5	110.4	114.9	123.8	146
SF	524.9	560.8	578.1	645.4	264.2	266.4	272.3	301.9	178.4	174.5	197	222.4	119.9	122.6	131.6	153.6

	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	512.3	514.3	575.4	706.9	244.7	252.3	311.3	351.1	164.3	180.7	181.7	210.1	102.6	112.6	138.6	152.6
SS	606.2	603.5	669.1	821.1	289.3	294.5	357.8	404.3	193.1	207.8	209	241.3	119.6	130.9	159.7	174.5
FF	436.1	440.4	495.8	608.1	208.5	217.3	271.2	304.9	140.8	157.8	158.2	183.1	88.63	97.39	120.2	133.4
FS	528.2	531.6	595.8	732.7	251.7	259.4	322.9	363.6	168.9	186.9	187.9	217.1	105.3	115.4	142.3	157.6
SF	498.6	498.5	556.2	682.1	238.5	245.9	300.4	339.2	160.4	175.1	175.9	203.5	100.3	110.1	134.9	147.8

Settings:

- Global Corner + Local MC
- 5 corners:
  - ❑ TT, 0.9V, 27°C
  - ❑ SS, 0.9V, 27°C
  - ❑ FF, 0.9V, 27°C
  - ❑ FS, 0.9V, 27°C
  - ❑ SF, 0.9V, 27°C
- N° of runs per corner: 200

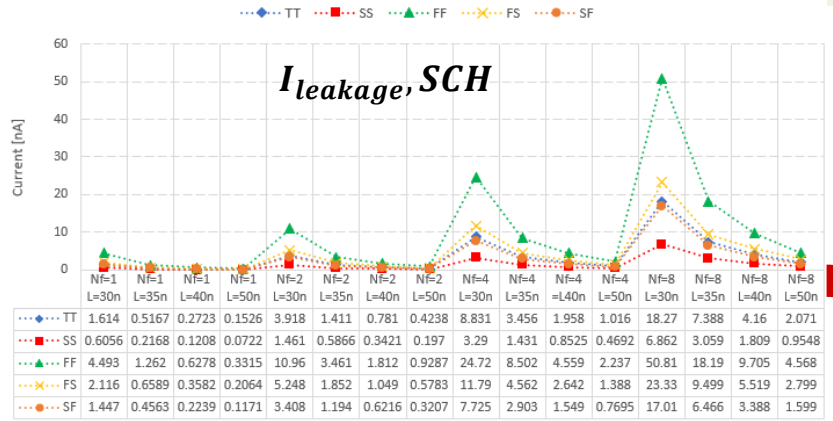
$\sigma_{t_{pSCH}} \sim 150fs$

$\sigma_{t_{pRCX}} \sim 300fs$

SVT Current Consumption: Leakage / Dynamic@1MHz

TID-ID

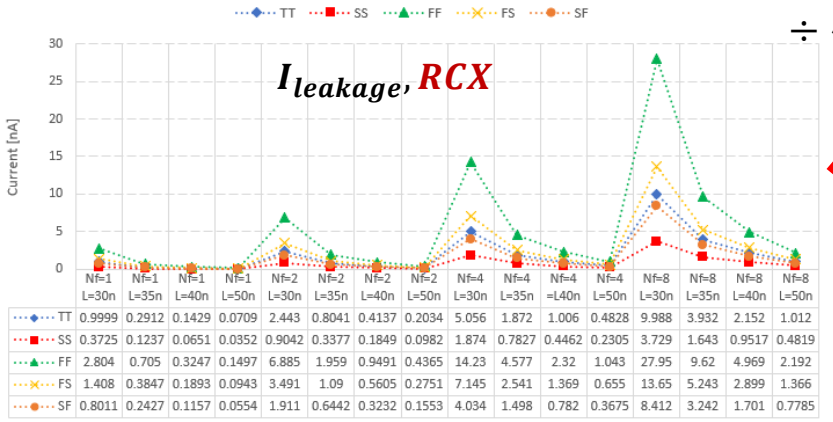
Leakage I VS Nf & L @SVT, VDD=0.9, temp=27 (SCH)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	1.614	0.5167	0.2723	0.1526	3.918	1.411	0.781	0.4238	8.831	3.456	1.958	1.016	18.27	7.388	4.16	2.071
SS	0.6056	0.2168	0.1208	0.0722	1.461	0.5866	0.3421	0.197	3.29	1.431	0.8525	0.4692	6.862	3.059	1.809	0.9548
FF	4.493	1.262	0.6278	0.3315	10.96	3.461	1.812	0.9287	24.72	8.502	4.559	2.237	50.81	18.19	9.705	4.568
FS	2.116	0.6589	0.3582	0.2064	5.248	1.852	1.049	0.5783	11.79	4.562	2.642	1.388	23.33	9.499	5.519	2.799
SF	1.447	0.4563	0.2239	0.1171	3.408	1.194	0.6216	0.3207	7.725	2.903	1.549	0.7695	17.01	6.466	3.388	1.599

÷ ~1.6

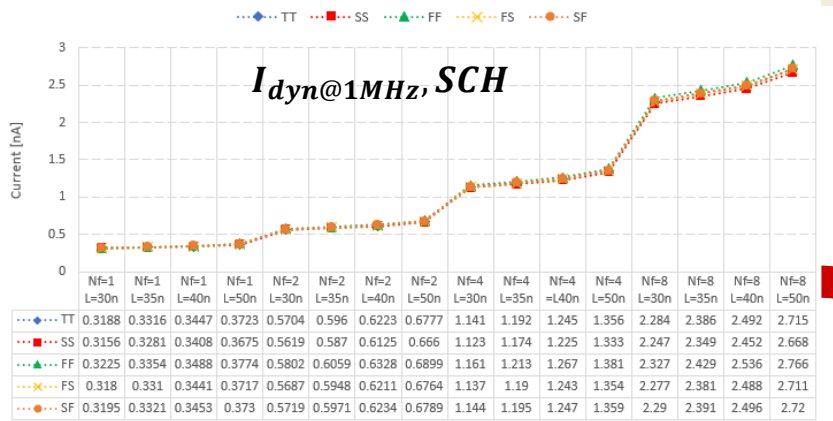
Leakage I VS Nf & L @SVT, VDD=0.9, temp=27 (RCX)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	0.9999	0.2912	0.1429	0.0709	2.443	0.8041	0.4137	0.2034	5.056	1.872	1.006	0.4828	9.988	3.932	2.152	1.012
SS	0.3725	0.1237	0.0651	0.0352	0.9042	0.3377	0.1849	0.0982	1.874	0.7827	0.4462	0.2305	3.729	1.643	0.9517	0.4819
FF	2.804	0.705	0.3247	0.1497	6.885	1.959	0.9491	0.4365	14.23	4.577	2.32	1.043	27.95	9.62	4.969	2.192
FS	1.408	0.3847	0.1893	0.0943	3.491	1.09	0.5605	0.2751	7.145	2.541	1.369	0.655	13.65	5.243	2.899	1.366
SF	0.8011	0.2427	0.1157	0.0554	1.911	0.6442	0.3232	0.1553	4.034	1.498	0.782	0.3675	8.412	3.242	1.701	0.7785

÷ ~2.1

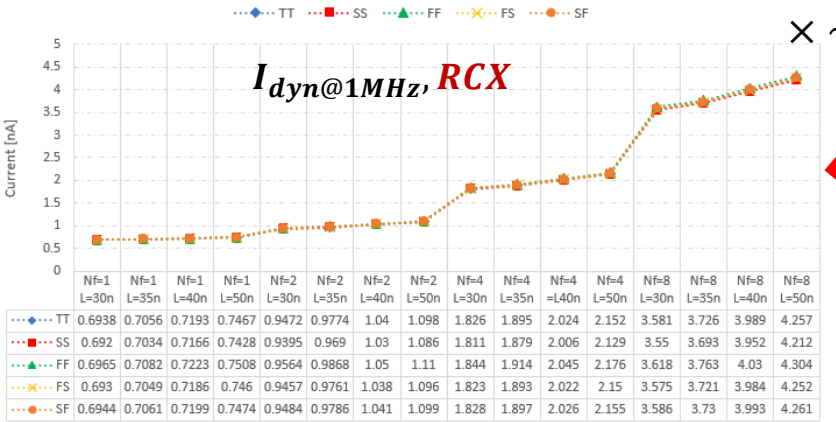
Dynamic I @ 1MHz VS Nf & L @SVT, VDD=0.9, temp=27 (SCH)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	0.3188	0.3316	0.3447	0.3723	0.5704	0.596	0.6223	0.6777	1.141	1.192	1.245	1.356	2.284	2.386	2.492	2.715
SS	0.3156	0.3281	0.3408	0.3675	0.5619	0.587	0.6125	0.666	1.123	1.174	1.225	1.333	2.247	2.349	2.452	2.668
FF	0.3225	0.3354	0.3488	0.3774	0.5802	0.6059	0.6328	0.6899	1.161	1.213	1.267	1.381	2.327	2.429	2.536	2.766
FS	0.318	0.331	0.3441	0.3717	0.5687	0.5948	0.6211	0.6764	1.137	1.19	1.243	1.354	2.277	2.381	2.488	2.711
SF	0.3195	0.3321	0.3453	0.373	0.5719	0.5971	0.6234	0.6789	1.144	1.195	1.247	1.359	2.29	2.391	2.496	2.72

× ~2.1

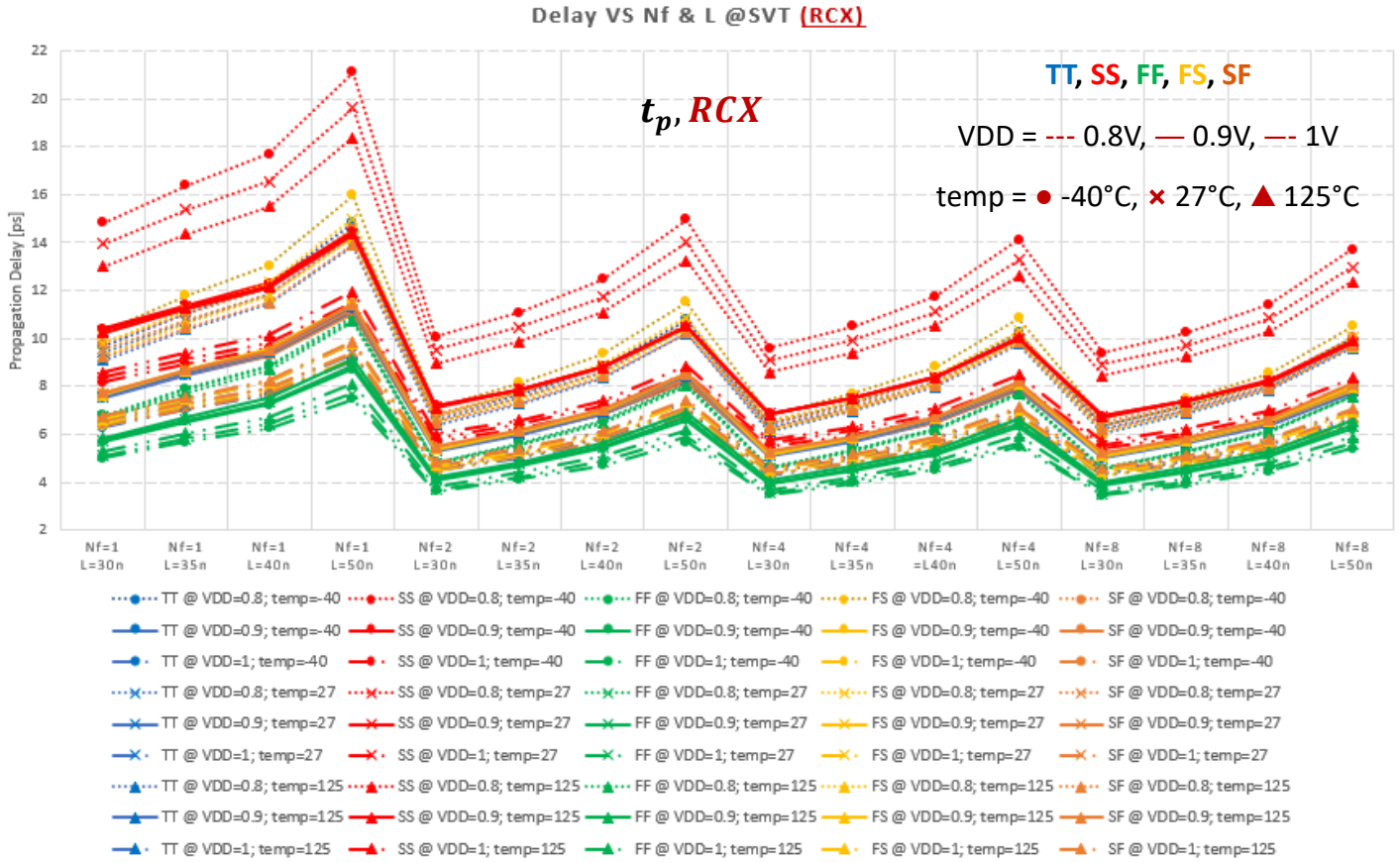
Dynamic I @ 1MHz VS Nf & L @SVT, VDD=0.9, temp=27 (RCX)



	Nf=1 L=30n	Nf=1 L=35n	Nf=1 L=40n	Nf=1 L=50n	Nf=2 L=30n	Nf=2 L=35n	Nf=2 L=40n	Nf=2 L=50n	Nf=4 L=30n	Nf=4 L=35n	Nf=4 =L40n	Nf=4 L=50n	Nf=8 L=30n	Nf=8 L=35n	Nf=8 L=40n	Nf=8 L=50n
TT	0.6938	0.7056	0.7193	0.7467	0.9472	0.9774	1.04	1.098	1.826	1.895	2.024	2.152	3.581	3.726	3.989	4.257
SS	0.692	0.7034	0.7166	0.7428	0.9395	0.969	1.03	1.086	1.811	1.879	2.006	2.129	3.55	3.693	3.952	4.212
FF	0.6965	0.7082	0.7223	0.7508	0.9564	0.9868	1.05	1.11	1.844	1.914	2.045	2.176	3.618	3.763	4.03	4.304
FS	0.693	0.7049	0.7186	0.746	0.9457	0.9761	1.038	1.096	1.823	1.893	2.022	2.15	3.575	3.721	3.984	4.252
SF	0.6944	0.7061	0.7199	0.7474	0.9484	0.9786	1.041	1.099	1.828	1.897	2.026	2.155	3.586	3.73	3.993	4.261

× ~1.6

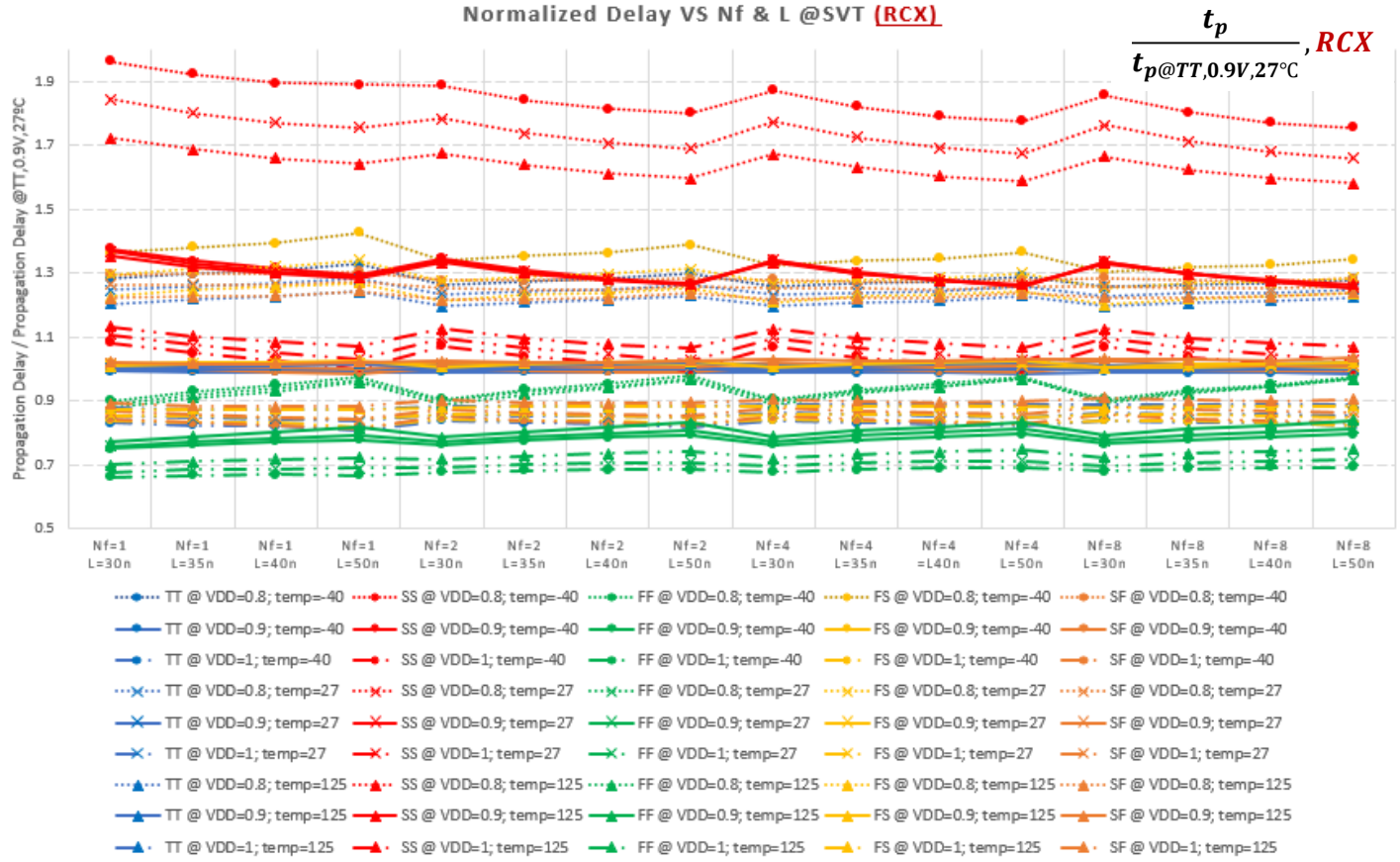
SVT Propagation Delay VS corners, VDD, temp



$$t_p = \frac{t_{pHL} + t_{pLH}}{2}$$

- Best Case (Fastest):
  FF @ VDD=1V & -40°C
- Worst Case (Slowest):
  SS @ VDD=0.8V & -40°C

SVT Propagation Delay VS corners, VDD, temp



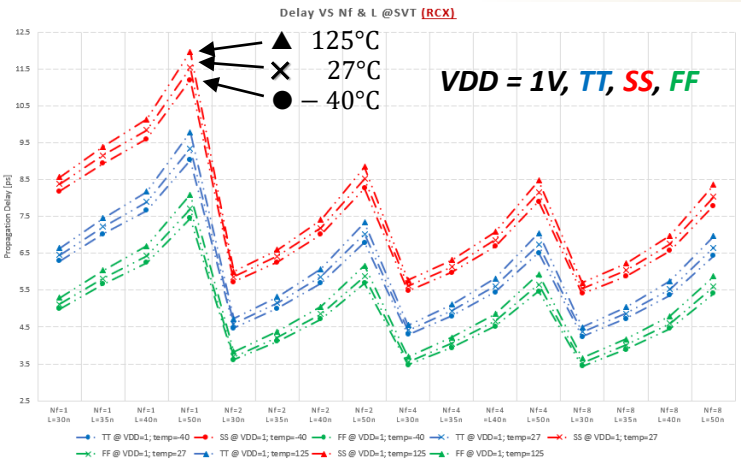
$$t_p = \frac{t_{pHL} + t_{pLH}}{2}$$

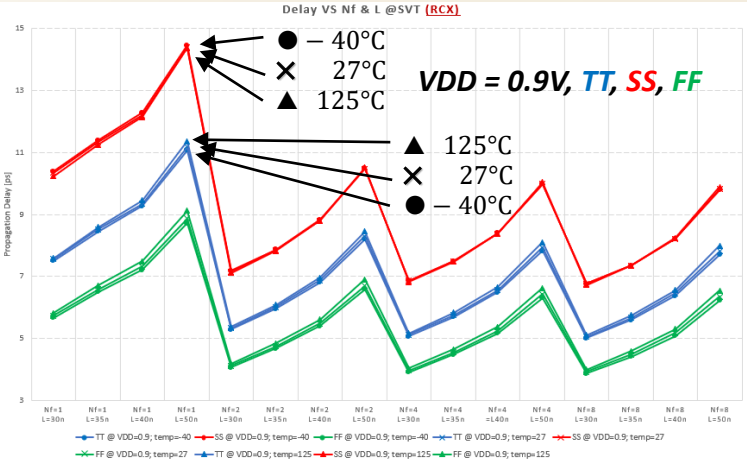
- Best Case (Fastest):
  FF @ VDD=1V & -40°C
- Worst Case (Slowest):
  SS @ VDD=0.8V & -40°C

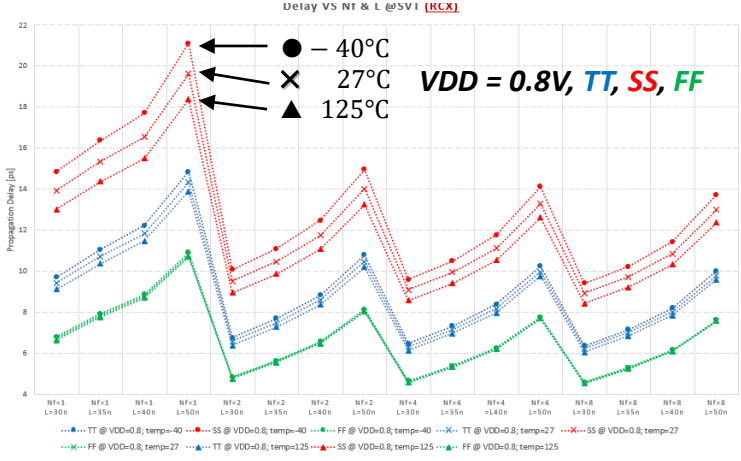
$$\frac{WorstCase}{Typical} \sim 1.9$$

$$\frac{BestCase}{Typical} \sim 0.68$$

SVT Propagation Delay VS corners, VDD, temp



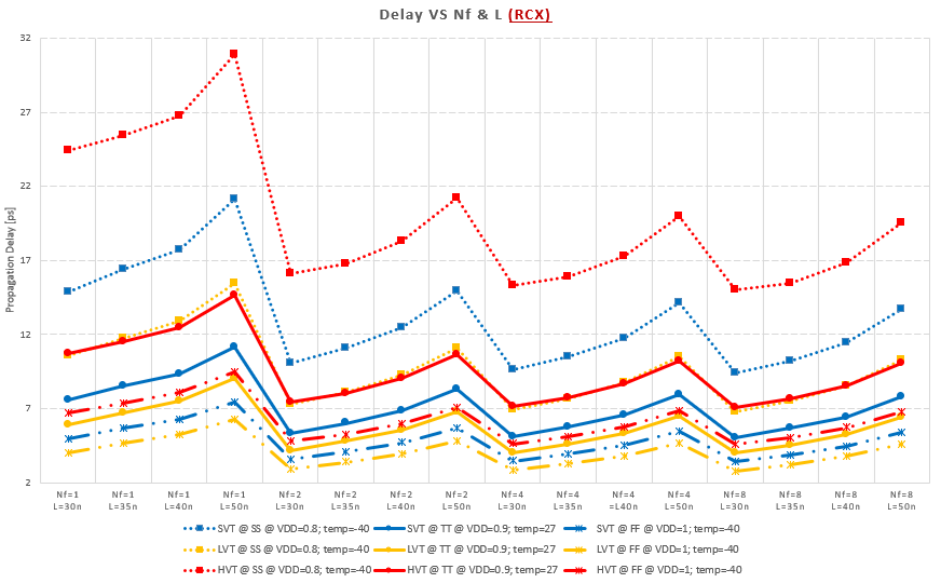




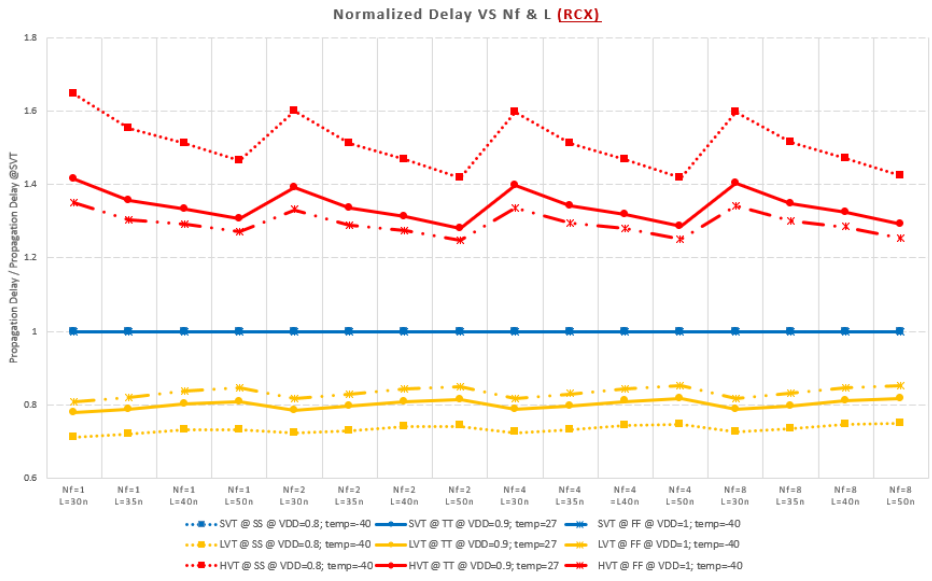
- Very small variation with temperature (especially at VDD=0.9V)
- At VDD = 0.8V, the delay is higher for lower temperatures (?)

Propagation Delay: SVT, LVT, HVT

t_p, RCX

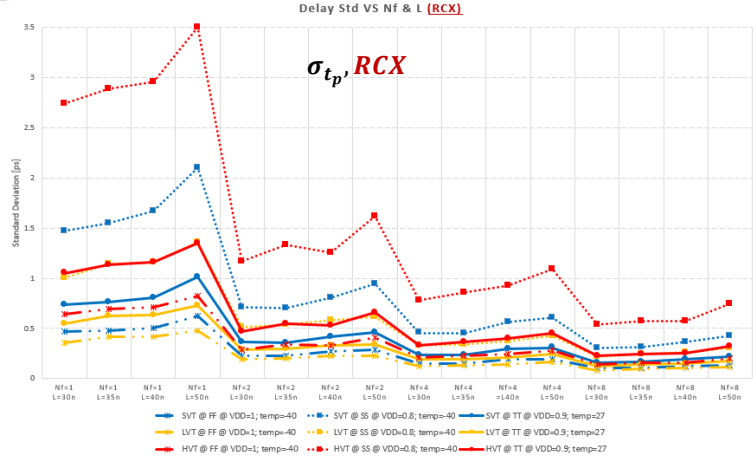


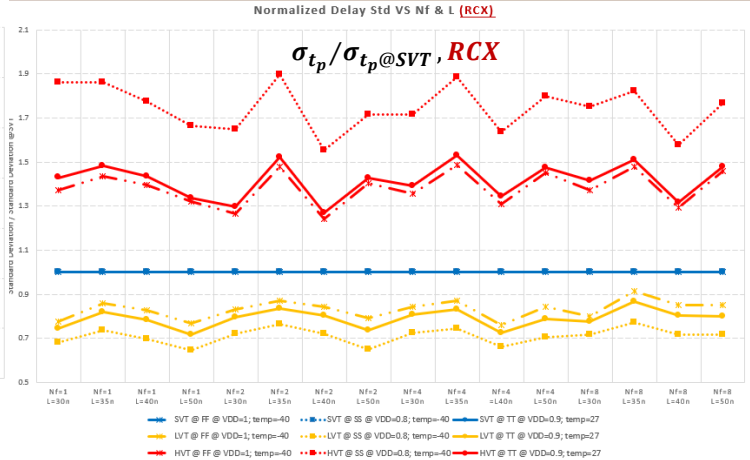
$\frac{t_p}{t_{p@SVT}}, RCX$

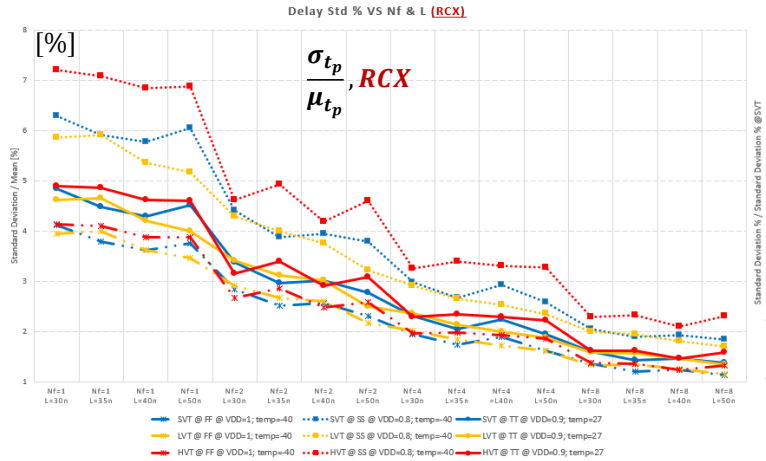


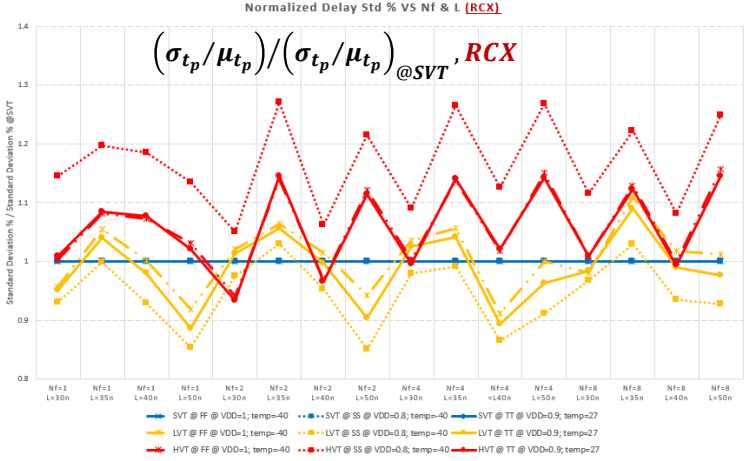
SVT	$SS;\ VDD = 0.8V;\ temp = -40°C$
LVT	$TT;\ VDD = 0.9V;\ temp = 27°C$
HVT	$FF;\ VDD = 1V;\ \ temp = -40°C$

Propagation Delay – Monte Carlo: SVT, LVT, HVT









Settings:

- Global Corner + Local MC
- 5 corners:
  - ❑ TT, 0.9V, 27°C
  - ❑ SS, 0.8V, -40°C
  - ❑ FF, 1V, -40°C
- N° of runs per corner: 500

$$\sigma_{t_p} = \sqrt{\sigma_{t_{pHL}}{}^2 + \sigma_{t_{pLH}}{}^2}$$

- $\frac{\sigma_{t_p}}{\mu_{t_p}}$ similar (+27%, -15%) for SVT, LVT and HVT structures

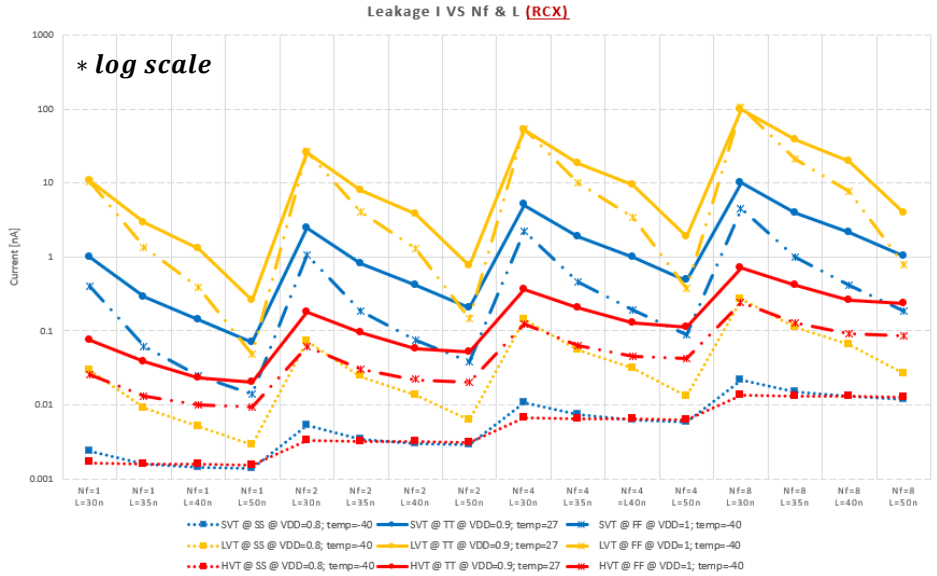
SVT
LVT
HVT

---■ $SS;\ VDD = 0.8V; T = -40°C$
—● $TT;\ VDD = 0.9V; T = 27°C$
---× $FF;\ VDD = 1V;\quad T = -40°C$

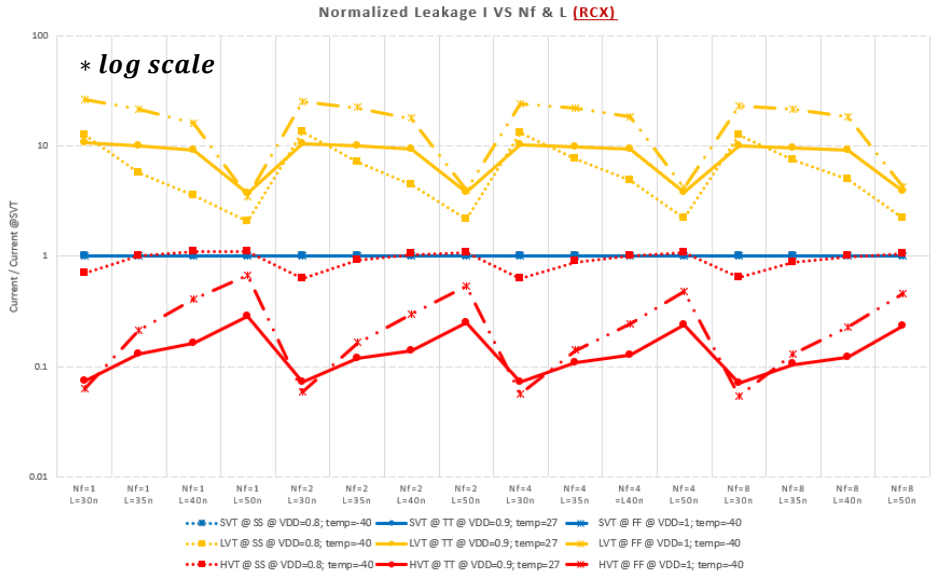
Leakage Current: SVT, LVT, HVT

TID-ID SLAC

$I_{leakage}$, RCX



$\frac{I_{leakage}}{I_{leakage@SVT}}$, RCX

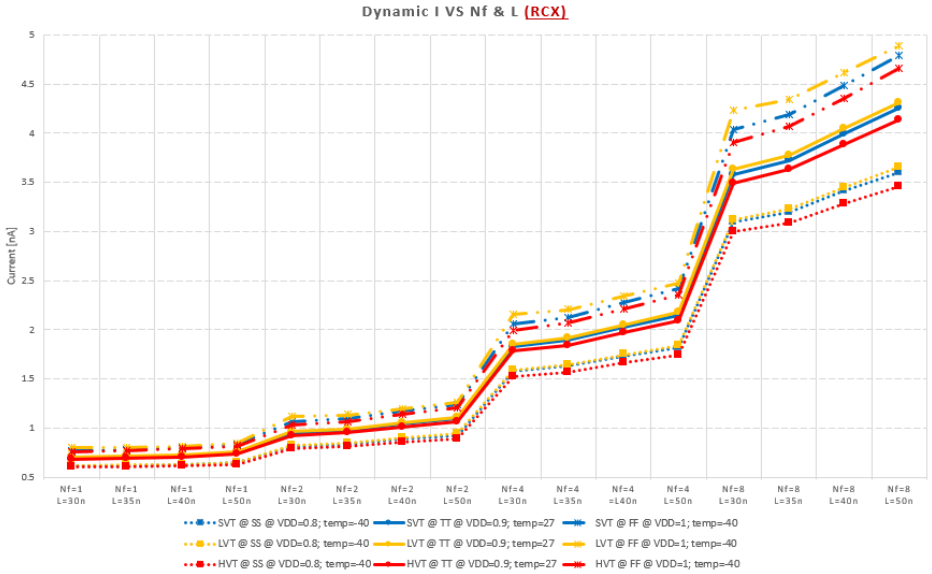


SVT	---■ $SS;\ VDD = 0.8V;\ temp = -40°C$
LVT	—● $TT;\ VDD = 0.9V;\ temp = 27°C$
HVT	—--× $FF;\ VDD = 1V;\quad temp = -40°C$

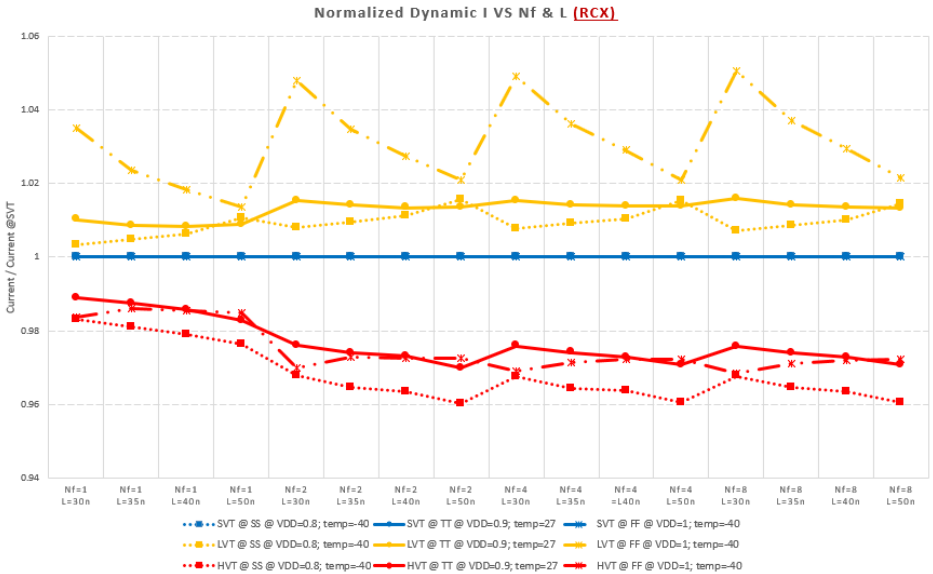
Dynamic Current @1MHz: SVT, LVT, HVT

TID-ID SLAC

$I_{dyn@1MHz}$, RCX



$\frac{I_{dyn@1MHz}}{I_{dyn@1MHz@SVT}}$, RCX



SVT ---■ $SS;\ VDD = 0.8V;\ temp = -40°C$

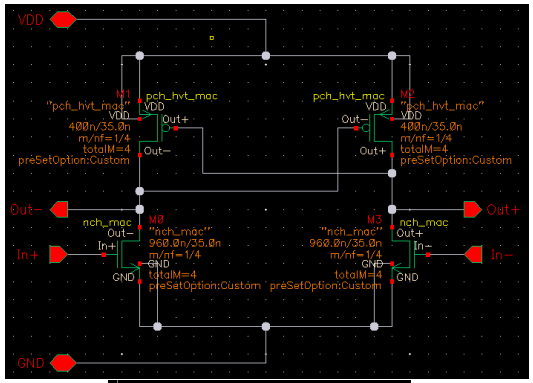
LVT —● $TT;\ VDD = 0.9V;\ temp = 27°C$

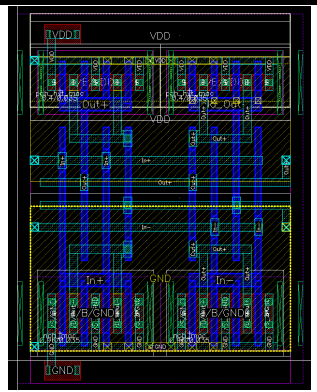
HVT —-×- $FF;\ VDD = 1V;\quad temp = -40°C$

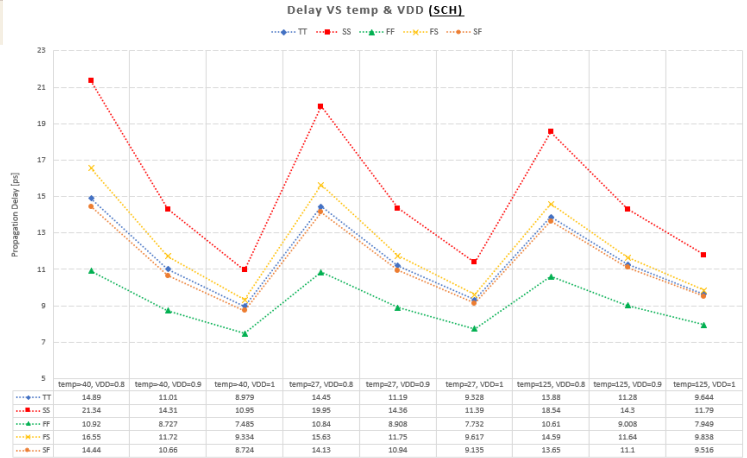
- Dynamic consumption very similar (+5%, -4%) for SVT, LVT and HVT structures

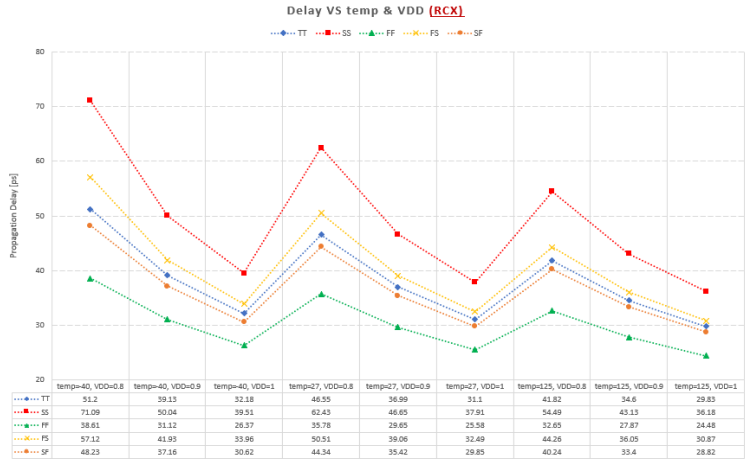
DCVSL Delay Cell

- Differential Cascode Voltage Switch Logic (DCVSL) Implementation:









× ~3.5