HPS DAQ updates

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HPS DAQ & Trigger Requirements

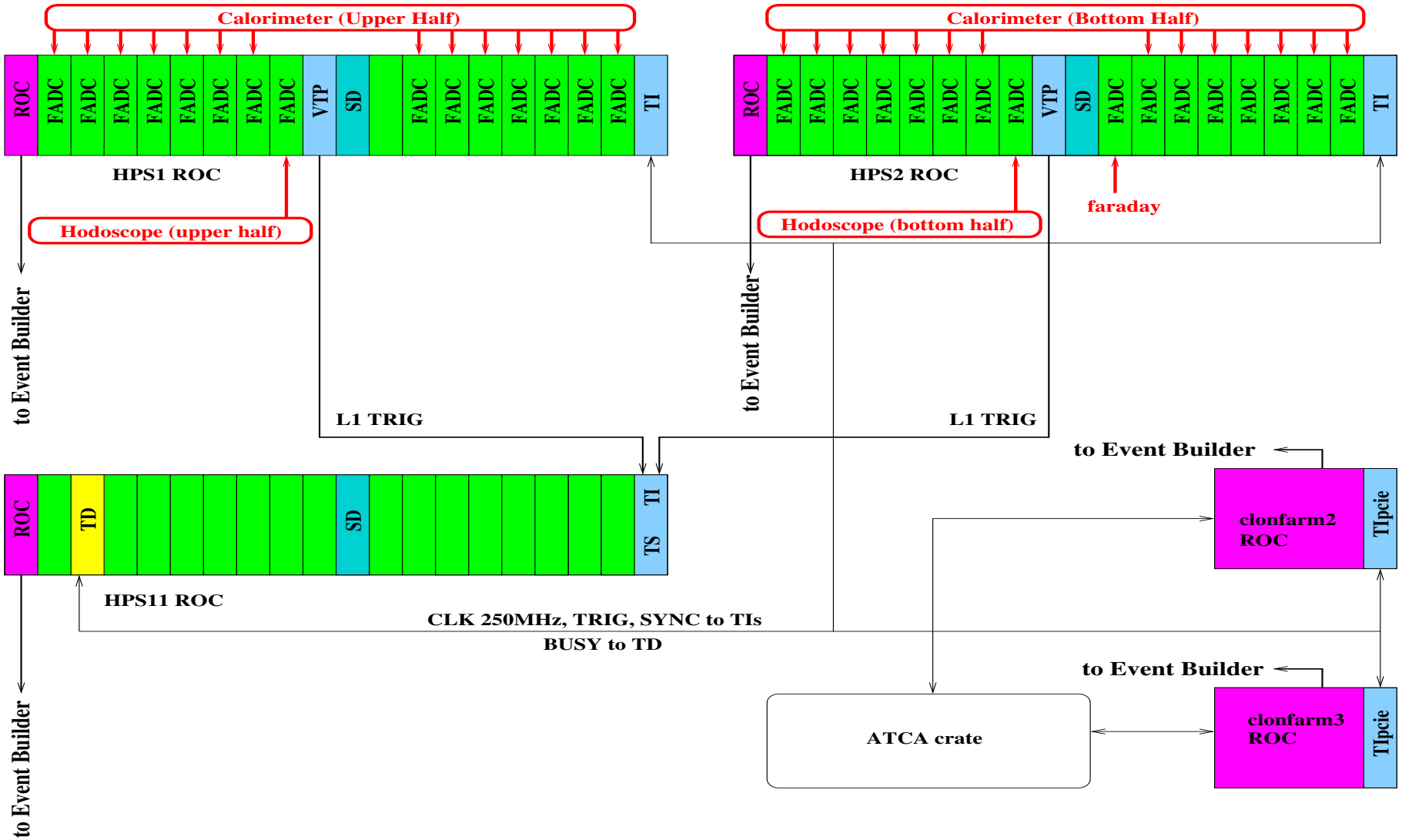
20kHz event rate

100MB/s data rate

>95% livetime

Achieved event rate 27kHz

HPS DAQ/Trigger Front-End Electronics



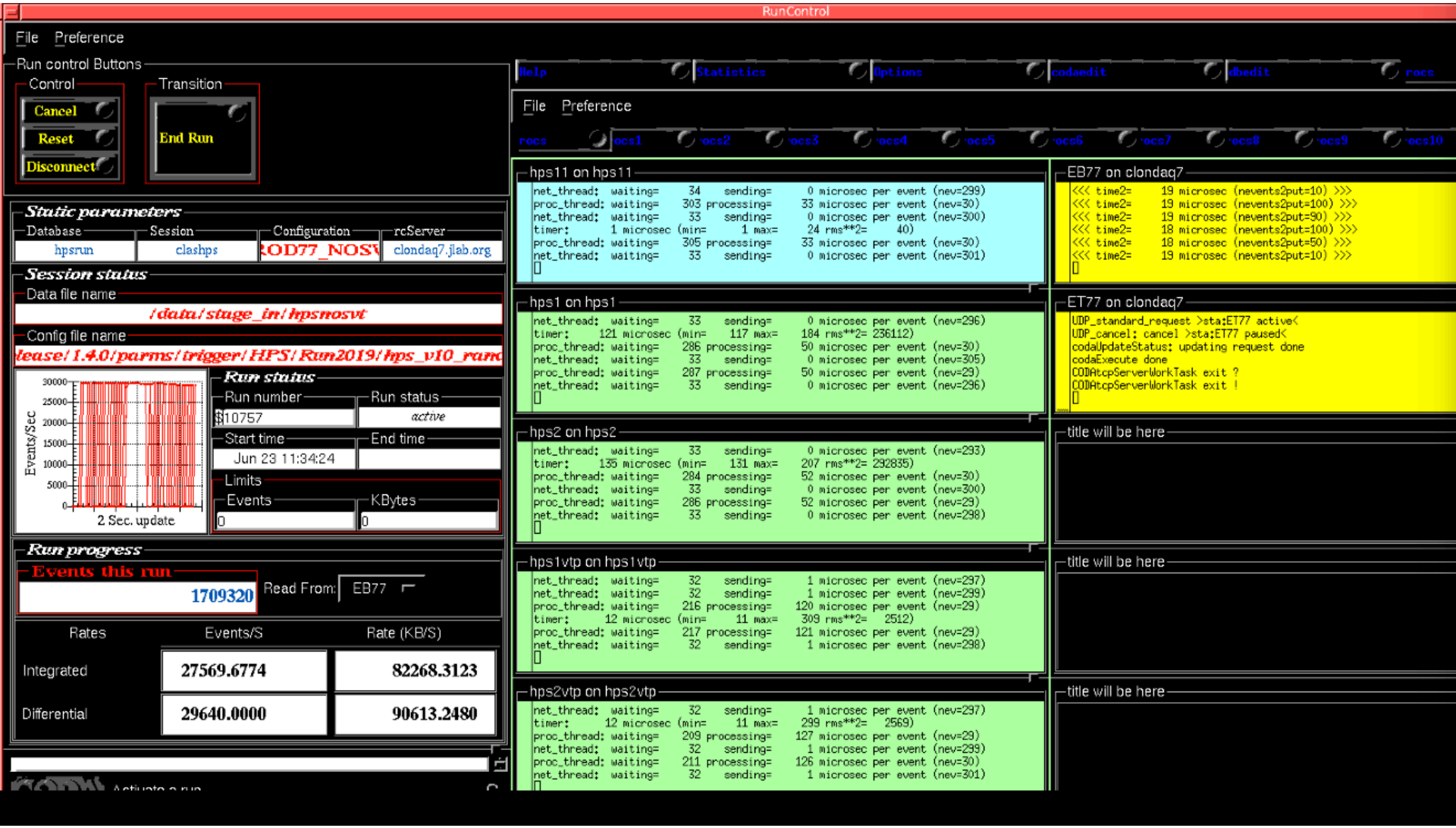
3 VXS crates, 2 servers, 1 ATCA crate, 7 Readout Controllers

HPS DAQ Status

- Calorimeter Readout: 442 channels of 12bit 250MHz Flash ADCs
- Hodoscope Readout: 32 channels of 12bit 250MHz Flash ADCs
- CPU/VTP/TS/SD/TD trigger and signal distribution boards
- 3 VXS crates
- 2 servers (clonfarm2/3) with TIpcie cards for SVT readout
- SVT readout (front-end and ATCA blades)

Back-end computing and software is CLAS12 facility: network, computing (clondaq7), DAQ software, data monitoring, messaging system, realtime database

HPS DAQ Status



Development for upcoming run – SLAC setup

Two TIpcie boards and one TIpcie-new board were shipped to SLAC, along with VME TI board; VME crate with CPU was already at SLAC

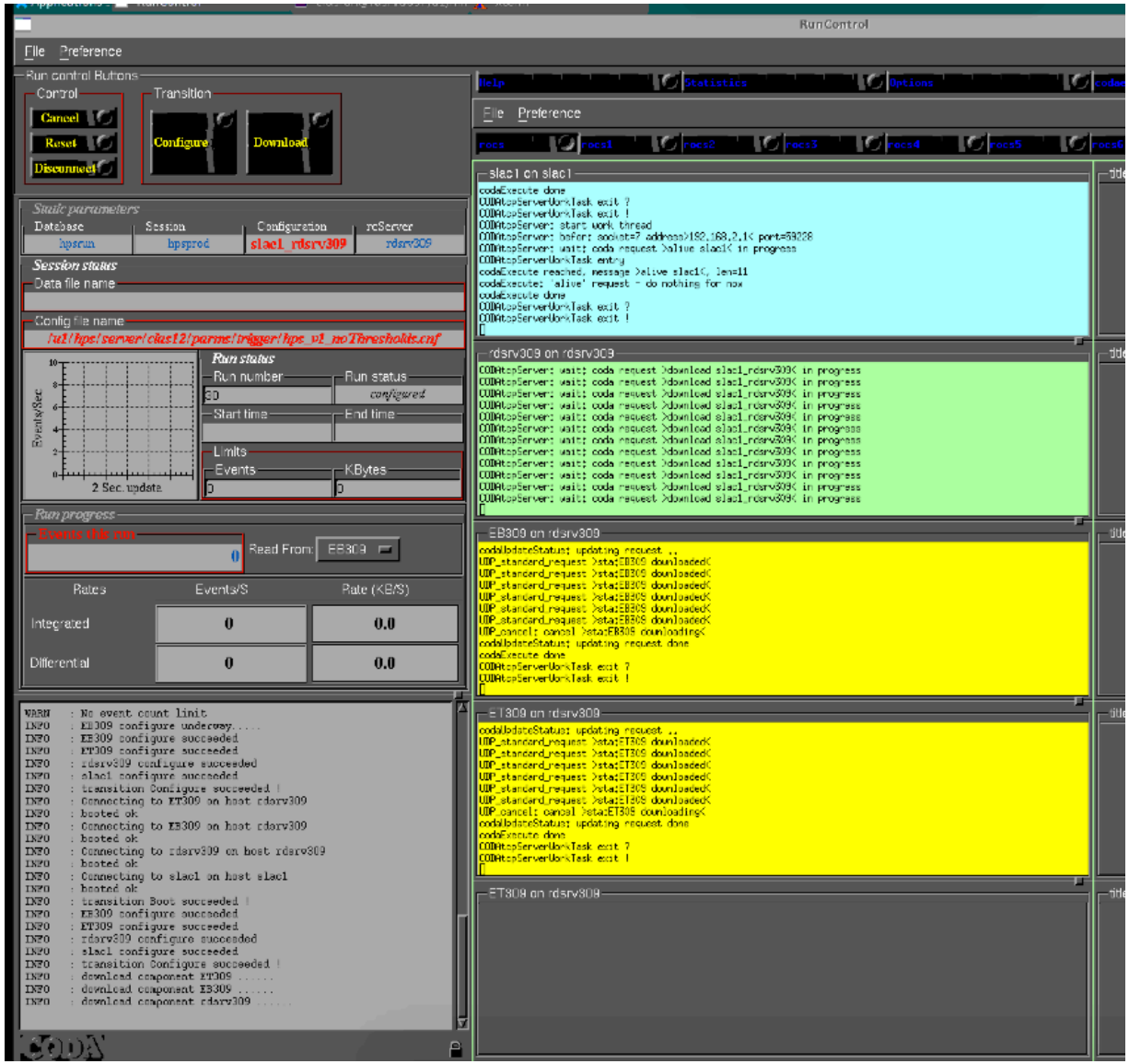
Setup built at SLAC includes VME crate as master and two Linux servers with TIpcie cards as slaves

CODA software was installed at SLAC with appropriate libraries, some modifications were made for Ubuntu (JLAB runs RHEL/CentOS, not Ubuntu) and for newer gcc

DAQ without SVT runs at 60kHz random pulser and 95% live, it indicates that all 3 TI cards communicates correctly

SVT integration has been started

Development for upcoming run – SLAC setup



Development for upcoming run – Tipcie-new

Two TIpcie-new boards were produced so far

TIpcie-new was tested in servers at JLAB where old version failed, and it works, servers recognize it as standard PCI device

Library being developed, takes longer then expected, hope to get it ready soon

More boards are in production, it was delayed because of chips shortage problem, but recently all components arrived so production was resumed

SVT readout have to be (probably) adjusted using TIpcie-new boards

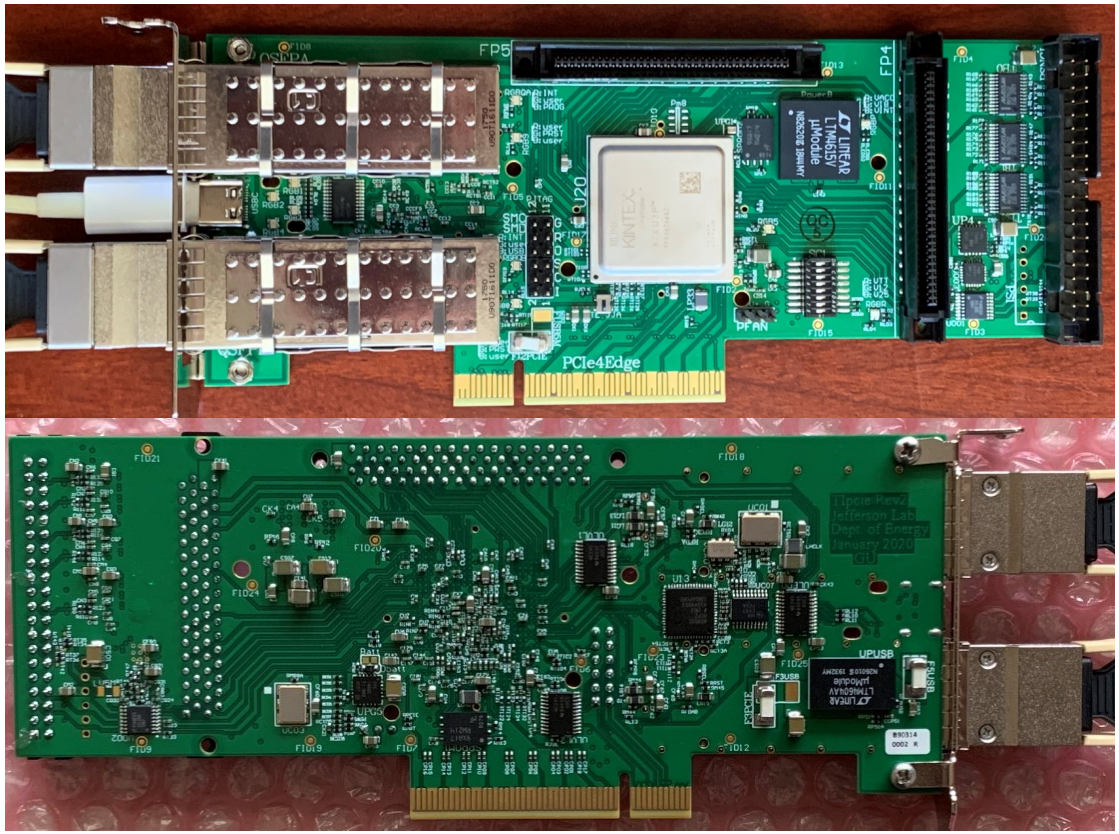
Tipcie-new module

Better PCIe compatibility:
- Xilinx UltraScale+ FPGA: xcku3p
- PCIexpress from gen1x1 (low power) to gen3x8 (high bandwidth)

More like a VME TI:
- TI fiber#1, fiber#5
- 40-pin IO to the second front panel
  8 outputs + 1 clock output; (LVDS, 3 optional ECL)
  10 inputs + 1 clock input; (any diff. level)

More potentials:
- Another 64 LVDS connection to the FPGA:
  64-channel FPGA based TDC
- USBC connector on the front panel
  +5V in for standalone operation

Two boards available, one in JLAB and another in SLAC, library being developed, more boards are in production



DAQ Status

All hardware and software on JLAB side is ready to run any time

Integration with SVT DAQ has underway in test setup at SLAC using old Tlpcie modules

Tlpcie-new modules to be commissioned, it will provide enough spares for upcoming run