Altiroc1 ASIC Design:

Experience, Challenges and Lessons Learned

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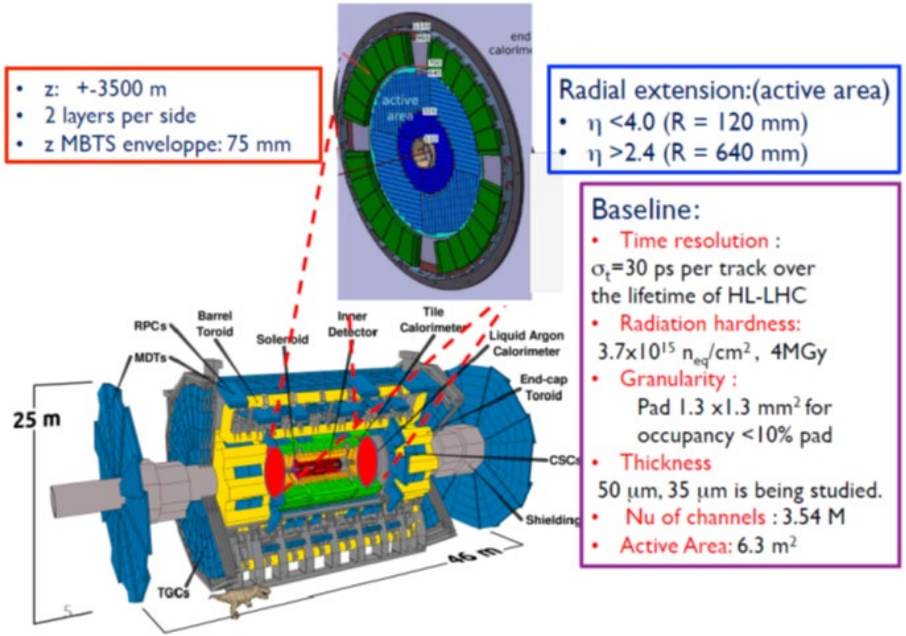
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

High-Granularity Timing Detector (HGTD) for ATLAS Phase II

- **High-Luminosity Large Hadron Collider (HL-LHC)** beginning in 2026
- on average **200 interaction** per **bunch crossing** → **Pile-up** challenge
- **High-Granularity Timing Detector (HGTD)** for pile-up mitigation



- Placed in the **forward region**, between the **Inner Tracker** and the **endcap of EM Calorimeter**
- **2 disks**, **2 layers/disk** containing **modules** with **sensors** and on-detector **electronics**
- Time resolution: **30 ps**
- Granularity (<10% Occupancy): **1.3 x 1.3 mm²**
- **50 µm** thick **Low Gain Avalanche Diodes (LGAD)** n-on-p Si detectors

HGTD electronics: General Architecture

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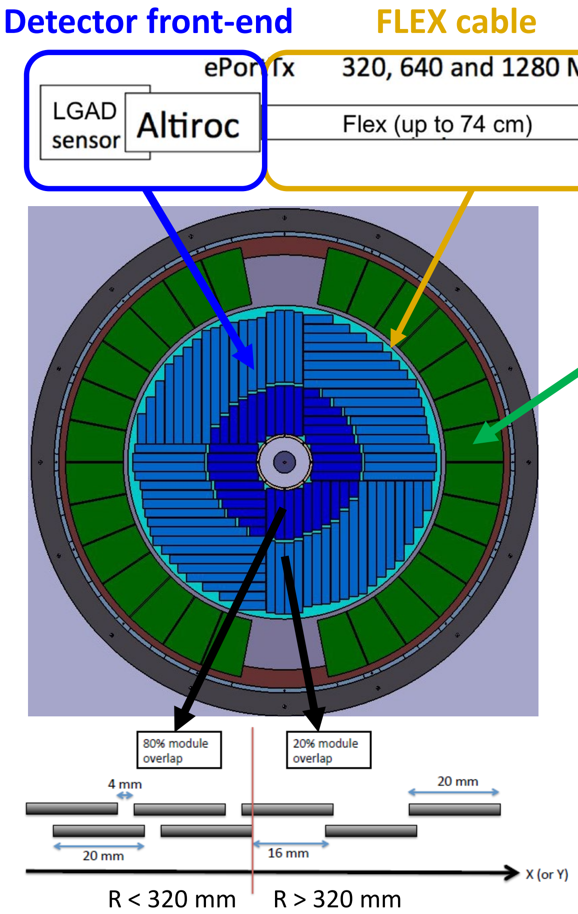
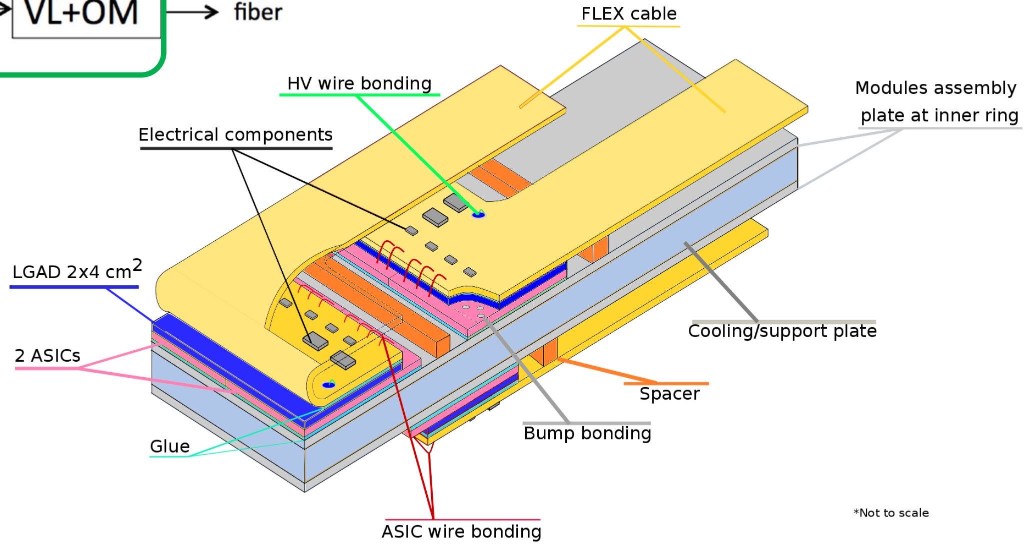




- Final ASIC: **2 x 2 cm²**, 1.3 x 1.3 mm² **225 pixels** (15 x 15 matrix)
- Module: **2 x 4 cm²** LGAD sensor + **2 ASICs**
- Disk: **double-sided**, modules mounted on both sides (**3 952** modules per disk)
- 2 disks ➡ total: **7 904** modules; **15 808** ASICs

ASIC Requirements

- **ALTIROC** (ATLAS LGAD Timing Read-Out Circuit) – **Front-End ASIC** for LGAD sensor **readout** and **time-measurement** of each hit of events selected by L0/L1 trigger with a resolution smaller than **30 ps/MIP**

LGAD pixel size (thickness ~ 45 µm)	1.3 x 1.3 mm^2	
Detector capacitance	3.4 pF	
Collected charge (1 MIP) at gain = 20	9.2 fC	
Dynamic range	20 MIPs	
Preamplifier + discriminator jitter at gain = 20	< 20 ps	=> Electronics total contribution < 30 ps
Time walk contribution	< 10 ps	
TDC binning	20 ps (TOA, TZ TOT) , 40 ps (VPA TOT)	
TDC range	2.5 ns (TOA), 20 ns (VPA TOT) / 5 ns (TZ TOT)	
Number of bits / hit	7 bits (TOA), 9 bits (VPA TOT) / 8 bits (TZ TOT)	
FIFO latency	10 µs / 35 µs latency for L0/L1 trigger	
Luminosity counters per ASIC	7 bits (sum) + 5 bits (outside window)	
Number of channels/ASIC	225 (15 x 15 pixel matrix)	
elink driver bandwidth	320 Mb/s, 640 Mb/s and 1.28 Gb/s	
Total power per area (ASIC)	< 300 mW/cm^2 (< 1.2 W) => 5 mW/pixel (4 mA/pixel)	
TID and neutron fluence	Inner region: 4.5 MGy, 4.5 x 10^{15} n/cm^2 Outer region: 2.1 MGy, 4.0 x 10^{15} n/cm^2	=> CMOS 130 nm

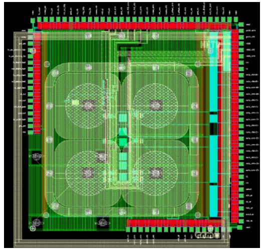
ALTIROC Prototypes

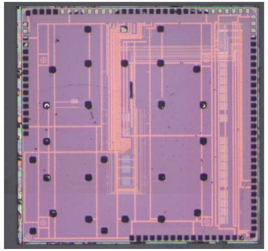
SLAC

ALTIROC0_V1

ΩMEGA Microelectronics

- Submitted mid **December 2016**, received **March 2017**
- **8 channels:** 4 for 1x1 mm² sensors (2 pF)
  4 for 3x3 mm² sensors (20 pF) – NOT USED
- **Analog front-end** only:
  - Voltage Preamplifier (**VPA**)
  - Discriminator
- **Testbench** and **testbeam** characterization **done**





3.4 mm

3.4 mm

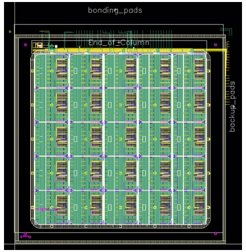
ALTIROC0_V2

ΩMEGA Microelectronics

- Submitted **December 2017**
- Same as ALTIROC0_V1 but with **faster VPA** and
  with four 20 pF channels replaced by **4 Transimpedance (TZ) Preamplifiers**
- **Testbench** and **testbeam** characterization **done**

ALTIROC1 (3 versions)

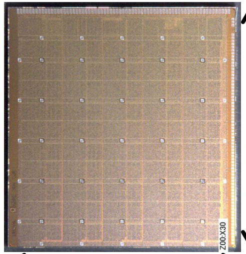
- V1 Submitted mid **June 2018**, received mid **September 2018**
- **25 channels** for readout of **5 x 5** sensor cells (**1.3x1.3 mm²**)
- **Complete front-end channels:**
  - **15 VPA** and **10 TZ** channels; Discriminator with Hysteresis
  - 2 Time-to-Digital Converter (**TDC**) / channel:
    - Time-of-Arrival (**TOA**) **TDC**
    - Time-over-Threshold (**TOT**) **TDC**
  - **Local FIFO** memory (**1 µs latency**)
- Standalone **97.7 ps** step **Phase-Shifter**
- V2 Submitted **March 2019**, received **June 2019**
  - **Analog Part** optimization; **TOA** & **TOT TDC** range issue fix; **DLLs** fix; Phase-Shifter fix; (1.2V MOS leakage current considered in design)
- V3 Submitted mid **April 2020**, received **June 2020**
  - **Analog Part** optimization; **TZ** channels replaced with **VPA**; **TOT TDC** bin 32, 64, 96 issue fix; **DLLs** mod; **Vctrl** buffers; and more…



ΩMEGA Microelectronics

SLAC

SMU

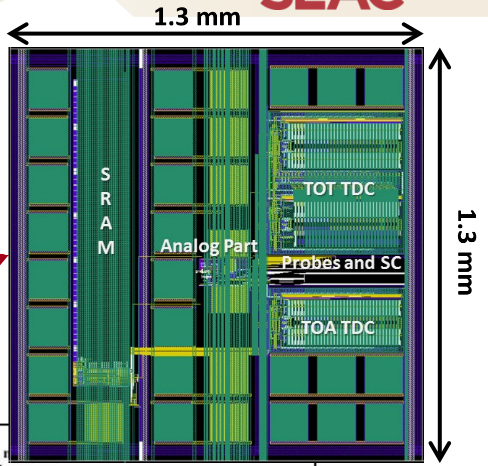


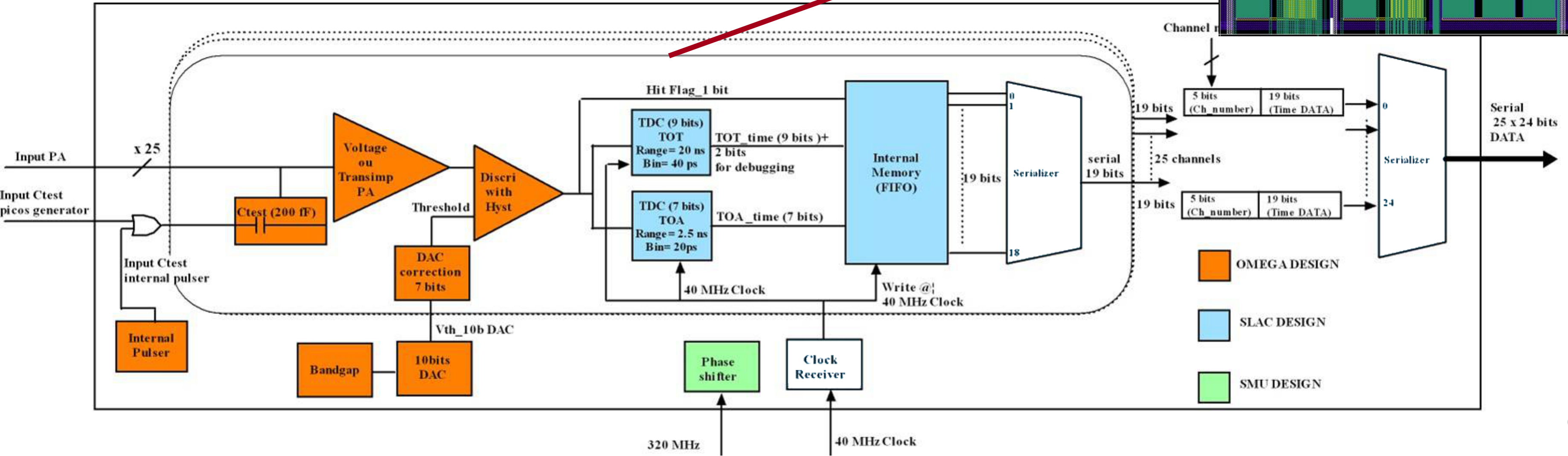
7.5 mm

7 mm

ALTIRO C1 Architecture

- **ALTIROC1** = Second ALTIROC ASIC prototype with **25 complete FE channels** to readout **5 x 5** sensor cells of **1.3 mm x 1.3 mm** (6.5 mm x 6.5 mm) + **Phase shifter**
- 3 Labs involved: OMEGA (analog Part & Full-chip Integration), SLAC (Digital part: TDCs, DLLs & FIFO), SMU (Phase shifter)
- ASIC size: **7 x 7.5 mm²**, fabricated in **TSMC 0.13 µm CMOS** technology



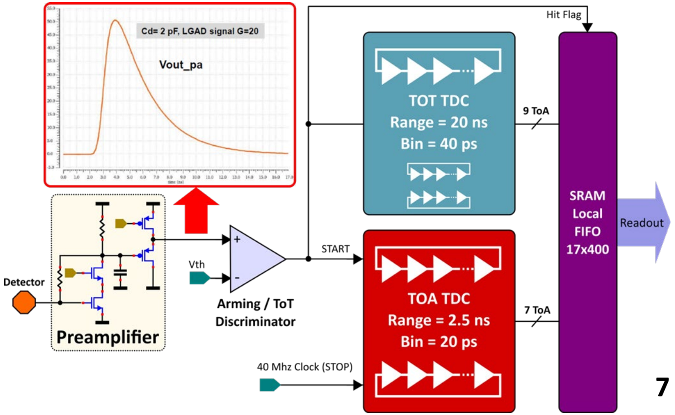


ASIC Design Timeline (SLAC perspective)

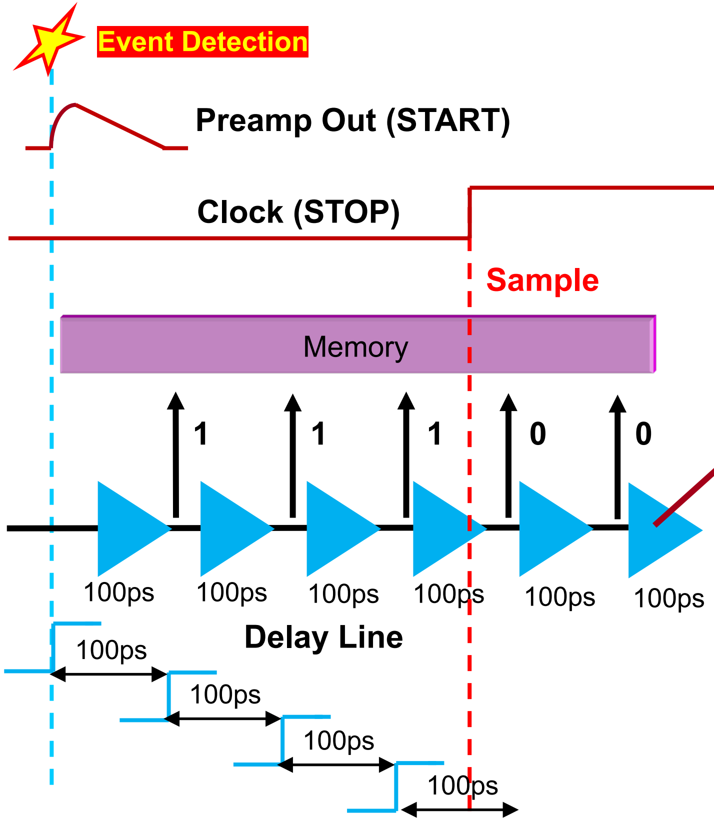
- Project Origins: **Jetfinder** detector initial studies - **Second half of 2016**
  - SLAC ASIC Design Personnel: **Konin M. Koua** (visiting from Université de Sherbrooke; 6 months); **Bojan Markovic** (supervision)
  - Initial studies and design of a **Constant-Fraction Discriminator (CFD)** for **Time-Walk** compensation
  - Initial studies of a **Time-of-Arrival (TOA) TDC**
- Altiroc1 Design: **2017 – June 2018** (originally planned submission date **February 2018**)
  - SLAC ASIC Design Personnel: **Bojan Markovic** (~1/3 of fulltime)
  - Design of: **Time-of-Arrival (TOA) TDC**; **Time-over-Threshold (TOT) TDC** (2 versions suitable for 2 different preamplifier versions: **VPA** and **TZ**); 3 **Delay-Locked-Loops (DLLs)** necessary for biasing the TDCs; 1 µs latency **local FIFO** memory **(SRAM)**

Challenge: project requirements, design specs, project timeline, etc. are somewhat fluid and change along the way (typical for R&D environments)

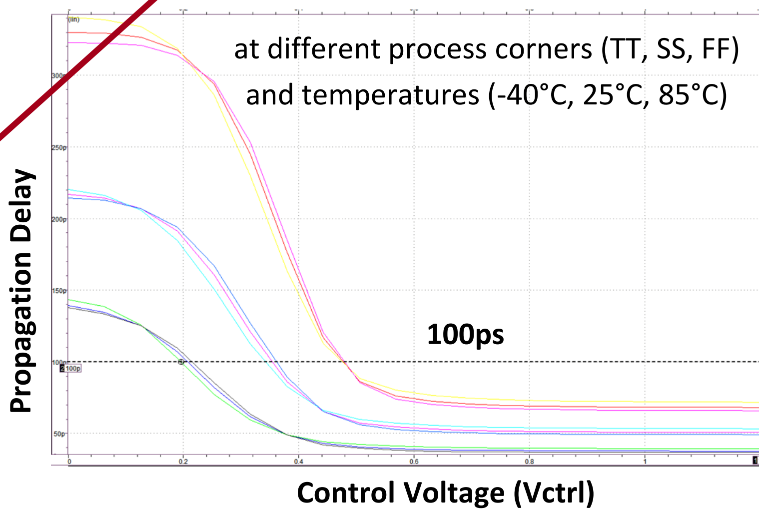
Challenge: limited personnel; multiple projects and designs going in parallel



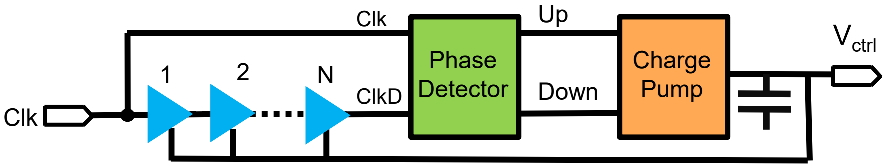
TDC Basics: Delay Line



Voltage-Controlled Delay Cell:



Delay-Locked Loop (DLL):



Cell Delay = Tck / N

Vernier Delay Line (1/2)

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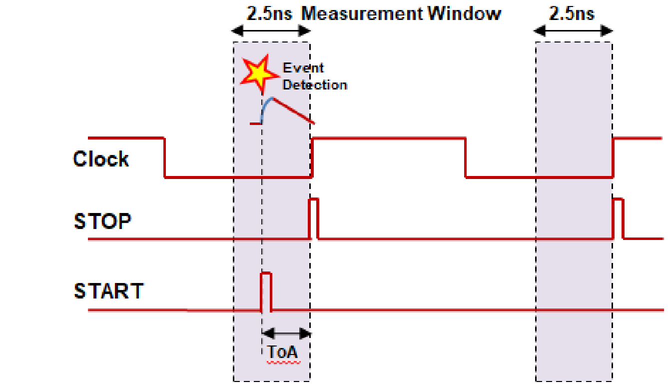
Required TDC resolution is below / at the limit of smallest logic propagation delay in the target technology (0.13µm)

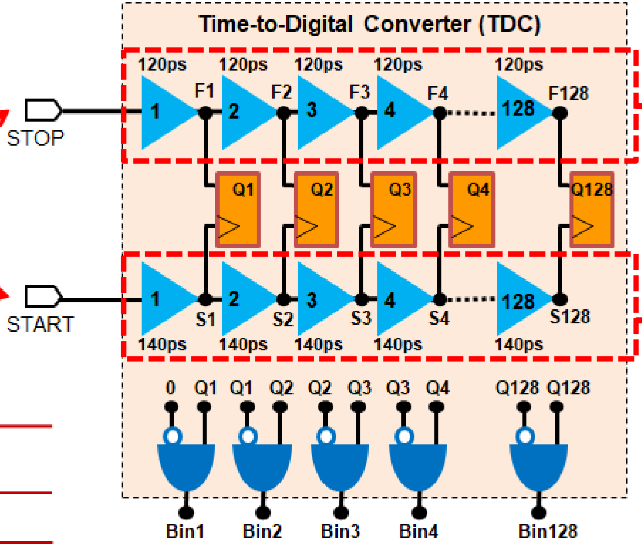
Vernier Delay Line:

The **resolution** (**LSB**) of time measurement is not given by the propagation delay of a single delay cell, but by the **difference of propagation delays** of two delay cells

TDC **resolution** (**LSB**) can be smaller than the smallest logic propagation time of the technology

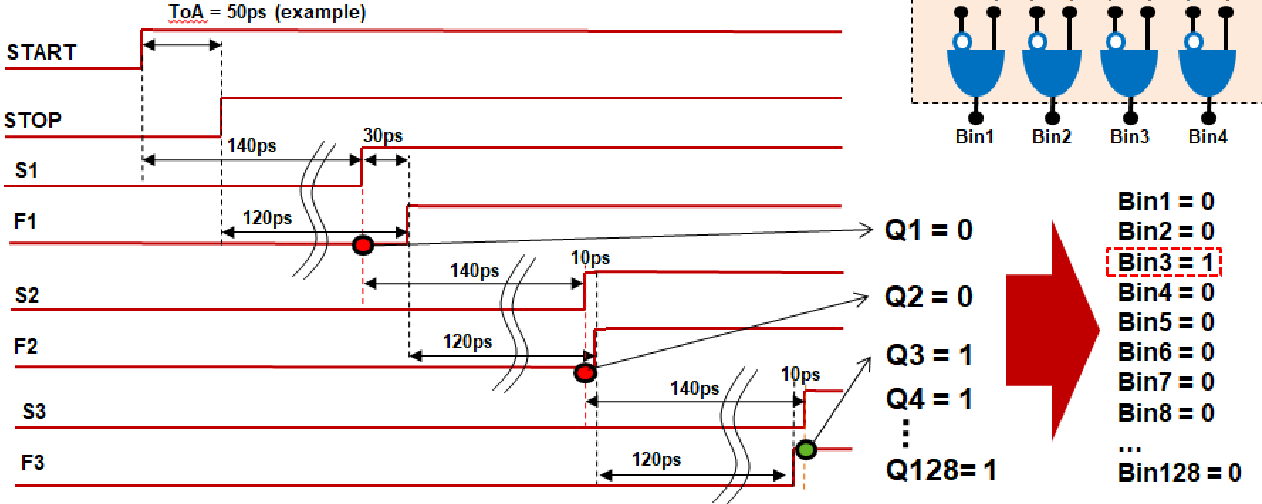
Vernier Delay Line (2/2)





STOP signal propagates in the **Fast Delay Line** (Delay of one cell = **120 ps**)

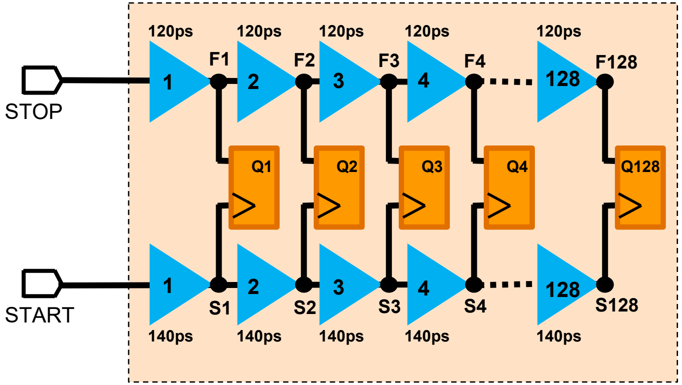
START signal propagates in the **Slow Delay Line** (Delay of one cell = **140 ps**)



- At each tap of the Delay Line the **STOP** signal catches up to the **START** signal by the deference of the propagation delays of cells in Slow and Fast delay lines: i.e. **140ps – 120ps = 20ps** (**LSB** of time measurement).
- The number of cells necessary for **STOP** signal to surpass the **START** signal represents the result of TDC conversion.

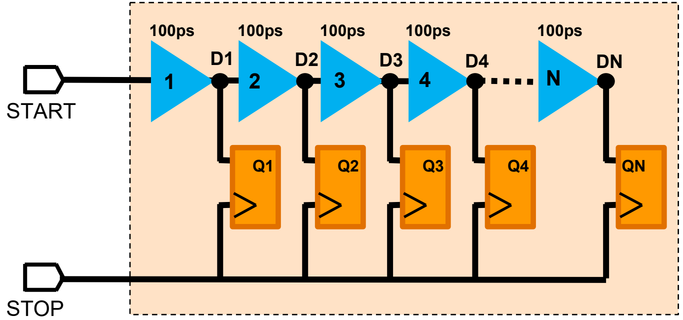
Vernier VS Tapped Delay Line (1/3)

Vernier Delay Line:



VS

Regular (Tapped) Delay Line:



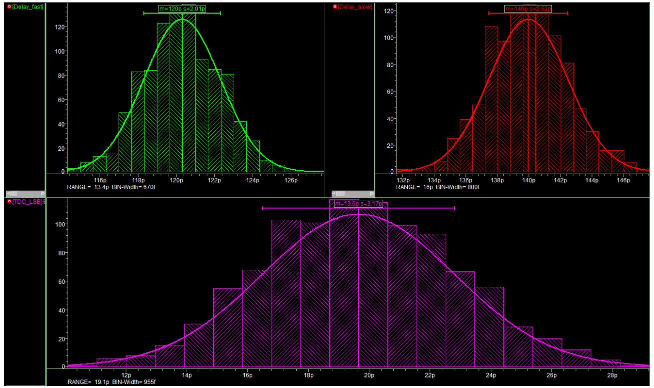
- More complex
- Resolution (LSB) not limited by technology
- Bigger Area:
  - 2 delay lines instead of one
  - Bigger delay cells due to more stringent mismatch requirements
- Longer Conversion Time (dependent on time interval being measured)
- Higher Power Consumption

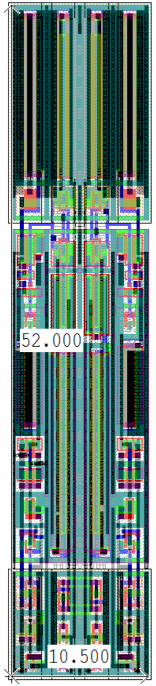
- Simpler
- Resolution (LSB) limited by technology
- Smaller Area
- Shorter Conversion Time (independent on time interval being measured)
- Lower Power Consumption

Vernier VS Tapped Delay Line (2/3)

Vernier Delay Line:

Altiroc Delay Cells:





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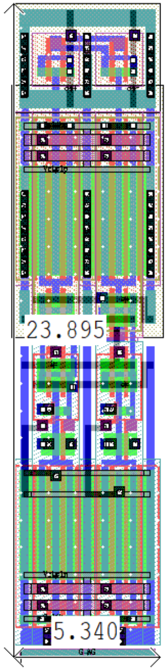
VS

Regular (Tapped) Delay Line:

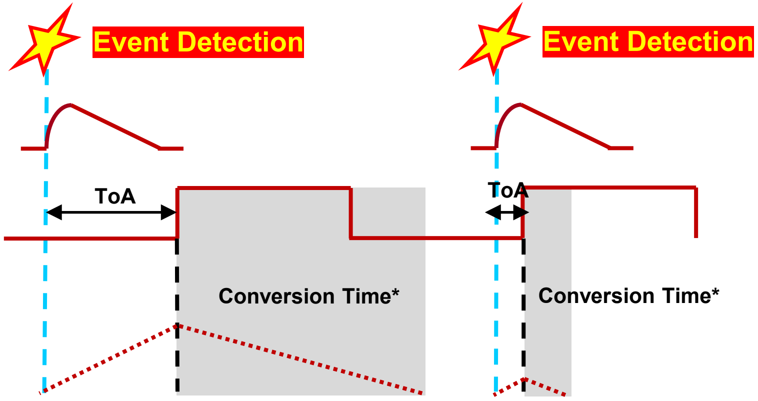
Tixel Delay Cells:



- Simpler
- Resolution (LSB) limited by technology
- Smaller Area
- Shorter Conversion Time (independent on time interval being measured)
- Lower Power Consumption

Vernier VS Tapped Delay Line (3/3)

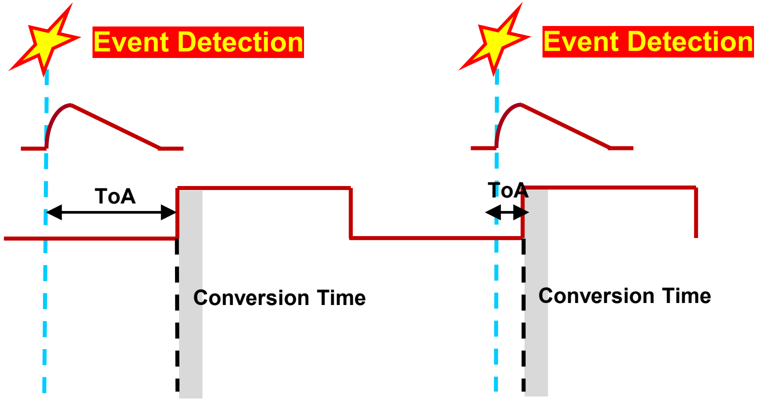
Vernier Delay Line:



*Similar to Dual-Slope ADC

VS

Regular (Tapped) Delay Line:



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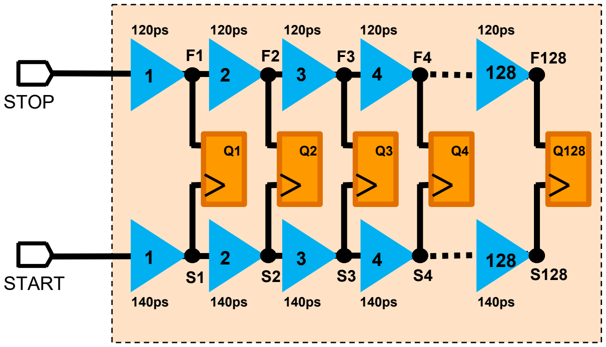
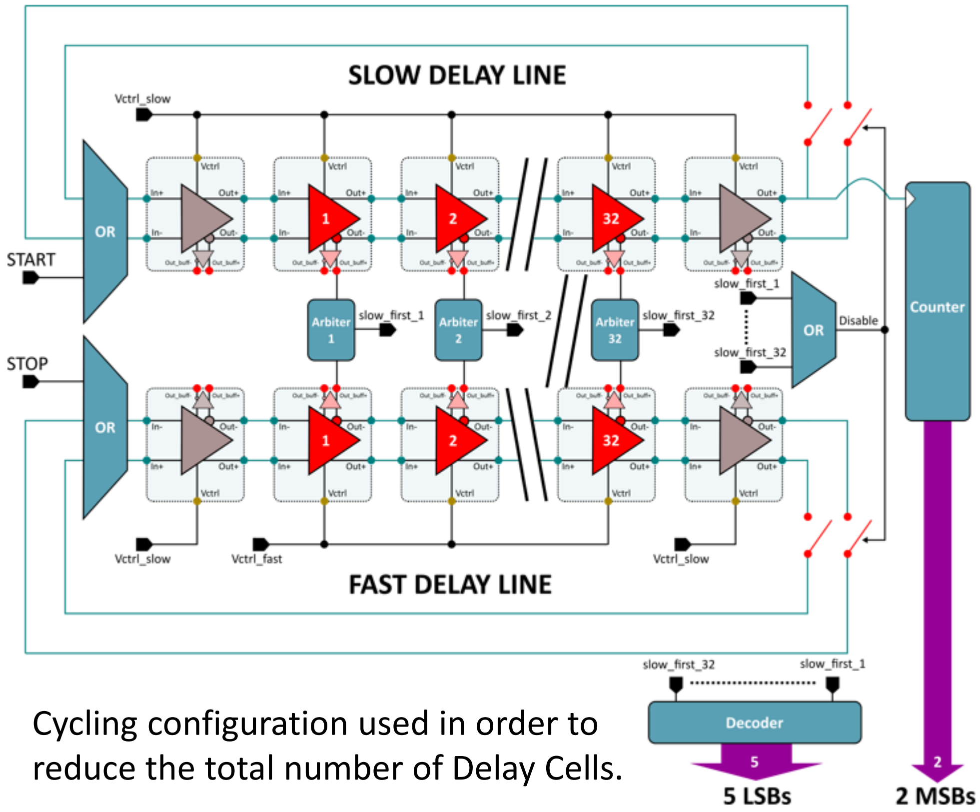
ALTIROC TOA TDC: Cycling Vernier Delay Line

Vernier Delay Line:



- Resolution: 20ps
- Range: 2.5ns
- 7 bits

ALTIROC TOA TDC Schematics:



- Cycling configuration used in order to reduce the total number of Delay Cells.

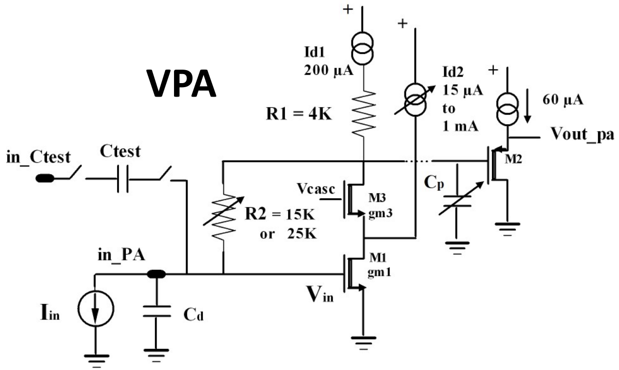
ALTIROC Analog Front-End: Preamplifiers

Voltage Preamp (VPA): Common source configuration

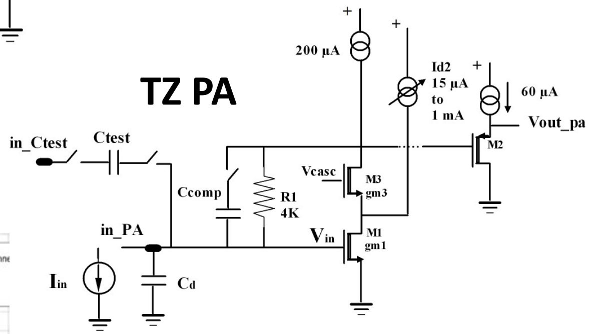
- Power: 350 µW – 1.3 mW; Id (M1) = 200 µA – 1 mA, I (M2)= 60 µA
- Bandwidth tunable with Cp: 400 MHz – 1.2 GHz
  (Rise time: 1 ns – 300 ps)
- R2=25K: for DC bias, Rin ~ 1.6 KΩ, Fall time= 2.2*RinCd
- I leakage sensor: absorbed by R2

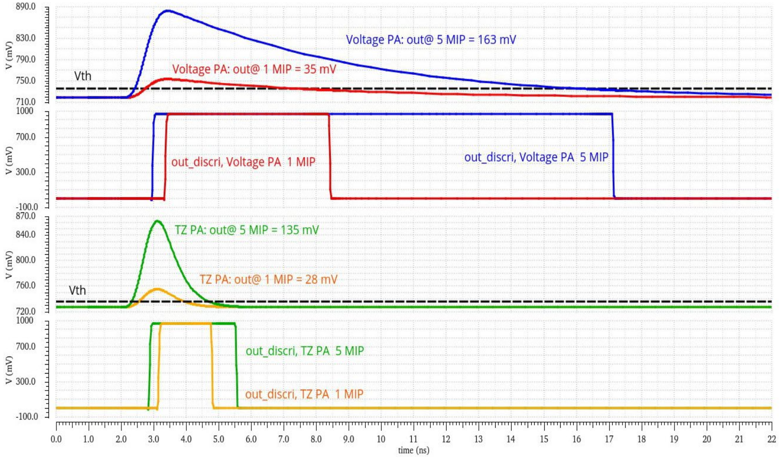
Transimpedance Preamp (TZ PA):

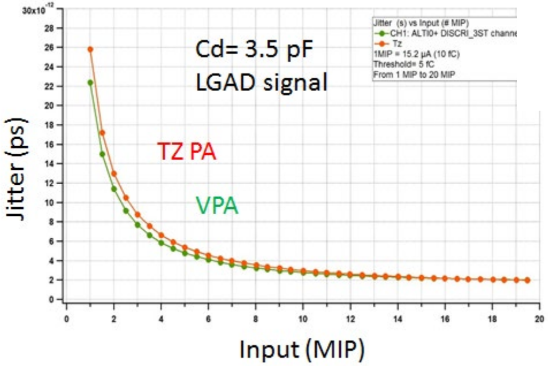
- Power: 350 µW – 1.3 mW; Id (M1) = 200 µA – 1 mA, I (M2)= 60 µA
- Bandwidth (not tunable): 1.4 GHz (with Ccomp)
- Rin ~ 150 Ω, Fall time= 2.2*RinCd



@ N. Seguin-Moreau

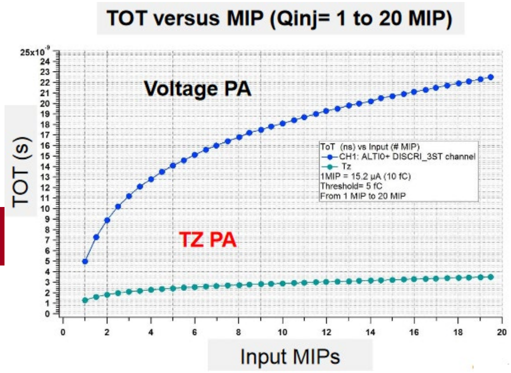






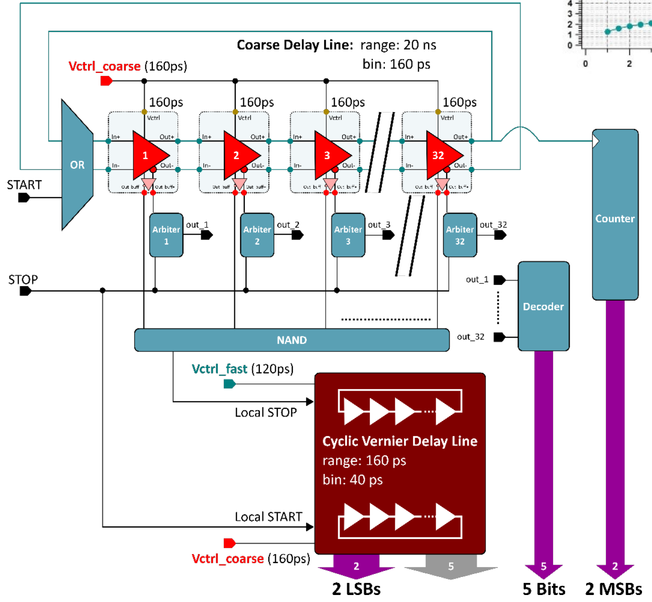
ALTIROC TOT TDC: Coarse Delay Line + TOA TDC (1/2)

- **VPA** and **TZ PA** have very different **TOT duration** due to different input resistance (**1.6 KΩ** vs **150 Ω**)

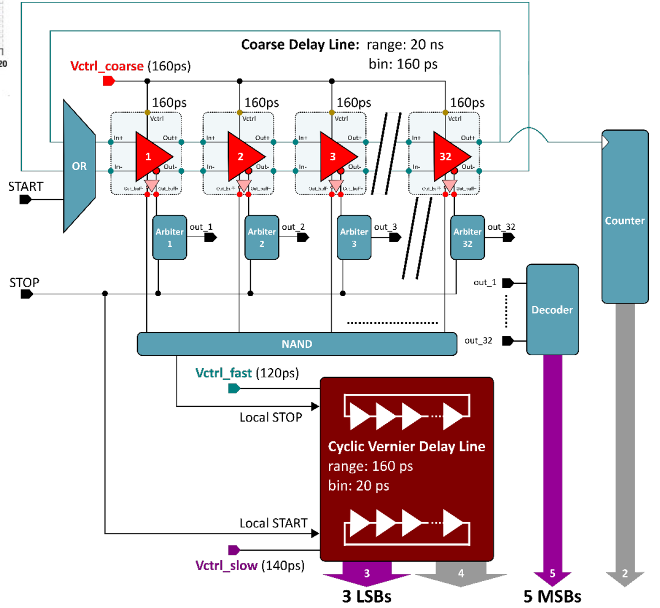


- Common architecture which exploits the **TOA TDC** combined with a range-extending **"coarse" delay line** can be adapted for both preamplifier architectures
- high complexity

TOT VPA: Resolution: 40 ps; Range: 20 ns; 9 bits

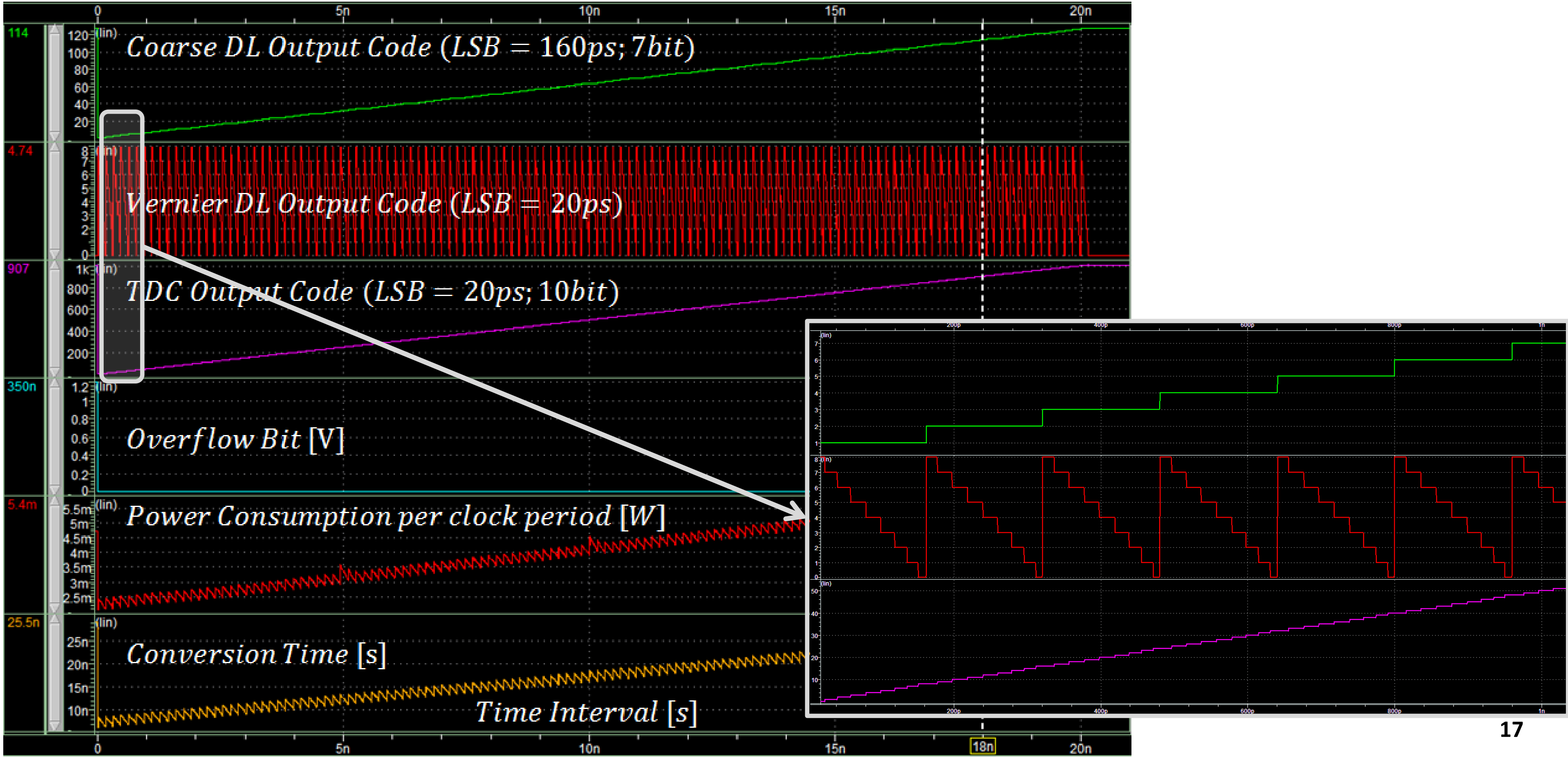


TOT TZ: Resolution: 20 ps; Range: 5 ns; 8 bits

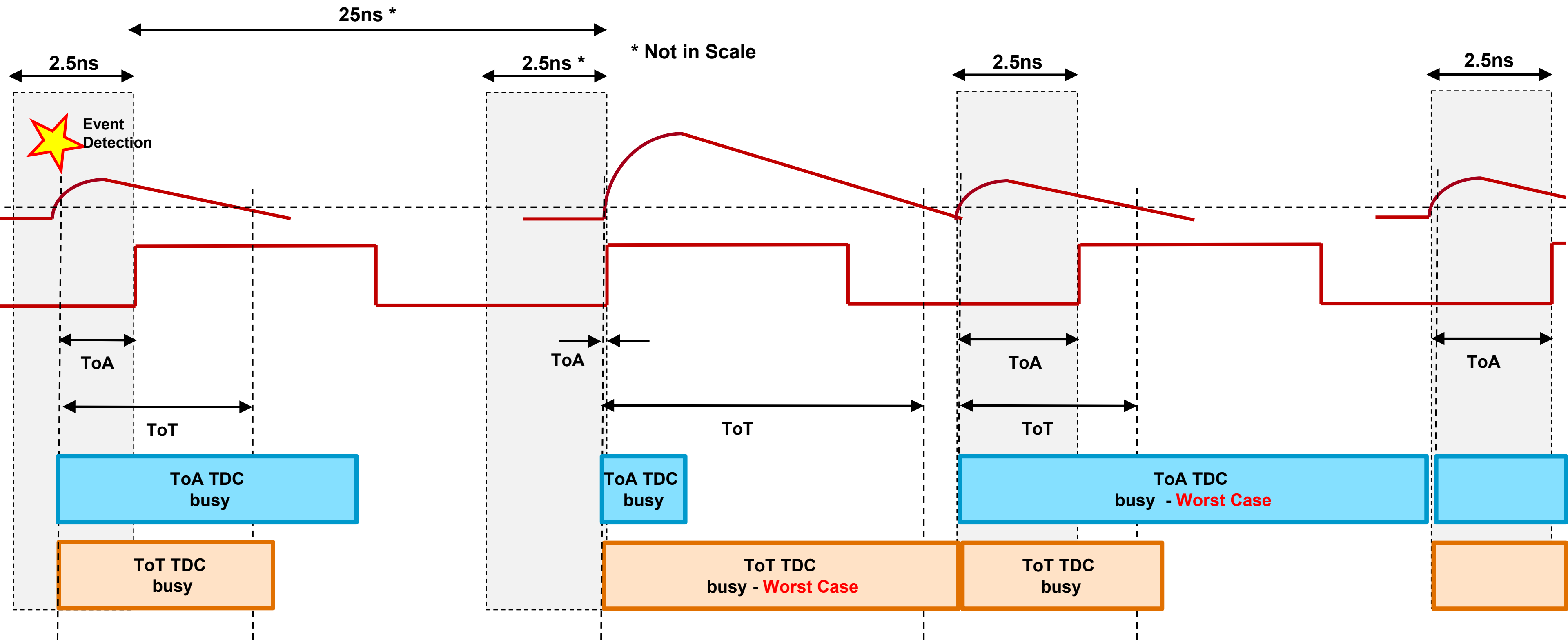


Challenge: designing TOT TDC architecture able to cover 2 different specs on a tight schedule

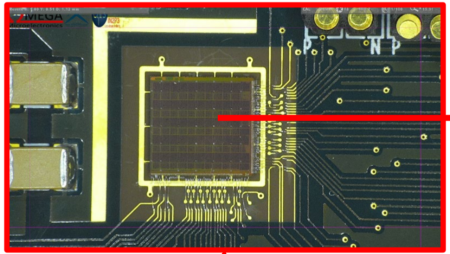
ALTIROC TOT TDC: Coarse Delay Line + TOA TDC (2/2)

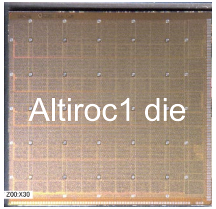


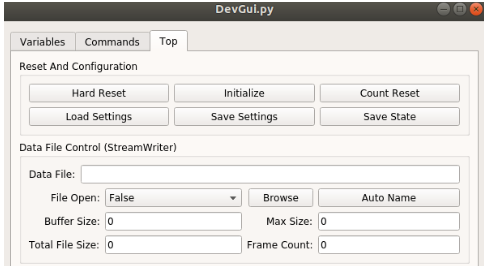
ALTIROC TDC Timing



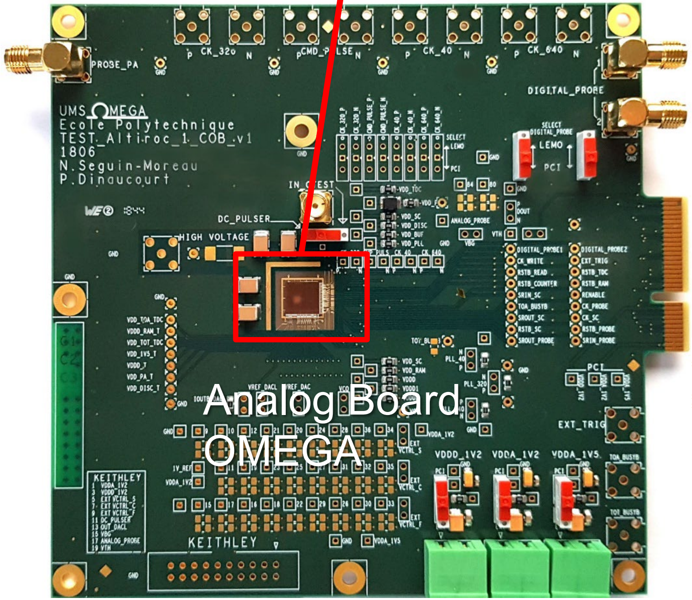
ALTIROC1 Test Setup (1/3)

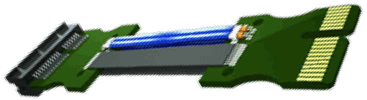


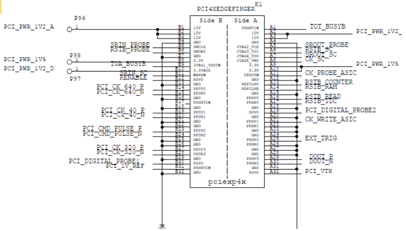




Development GUI*
SLAC
@ Larry Ruckman





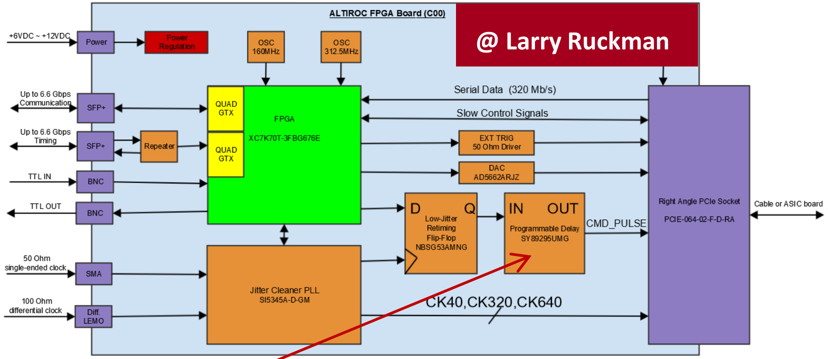


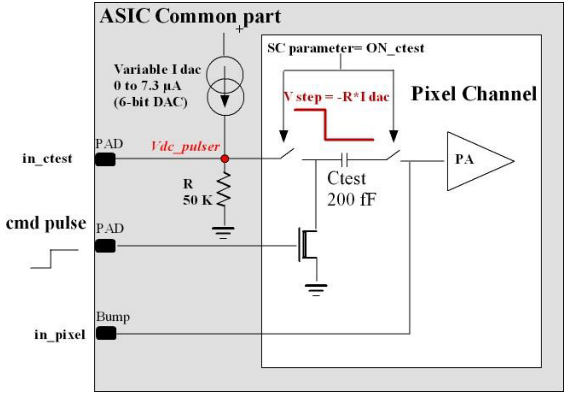
*More Details in Larry's talk

ALTIROC1 Test Setup (2/3)

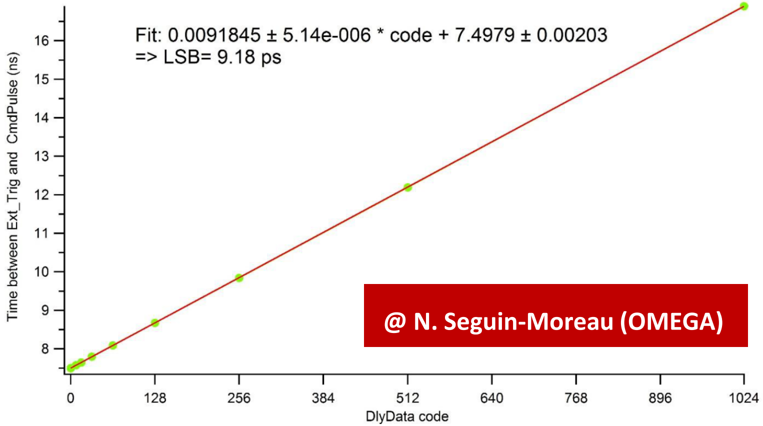
- Injection of charge (3.5 fC up to 70 fC) using the ASIC internal pulser controlled by **cmd_pulse** input
- **cmd_pulse** signal generated by the FPGA, synchronous to 40 MHz clock

ALTIROC FPGA Board:

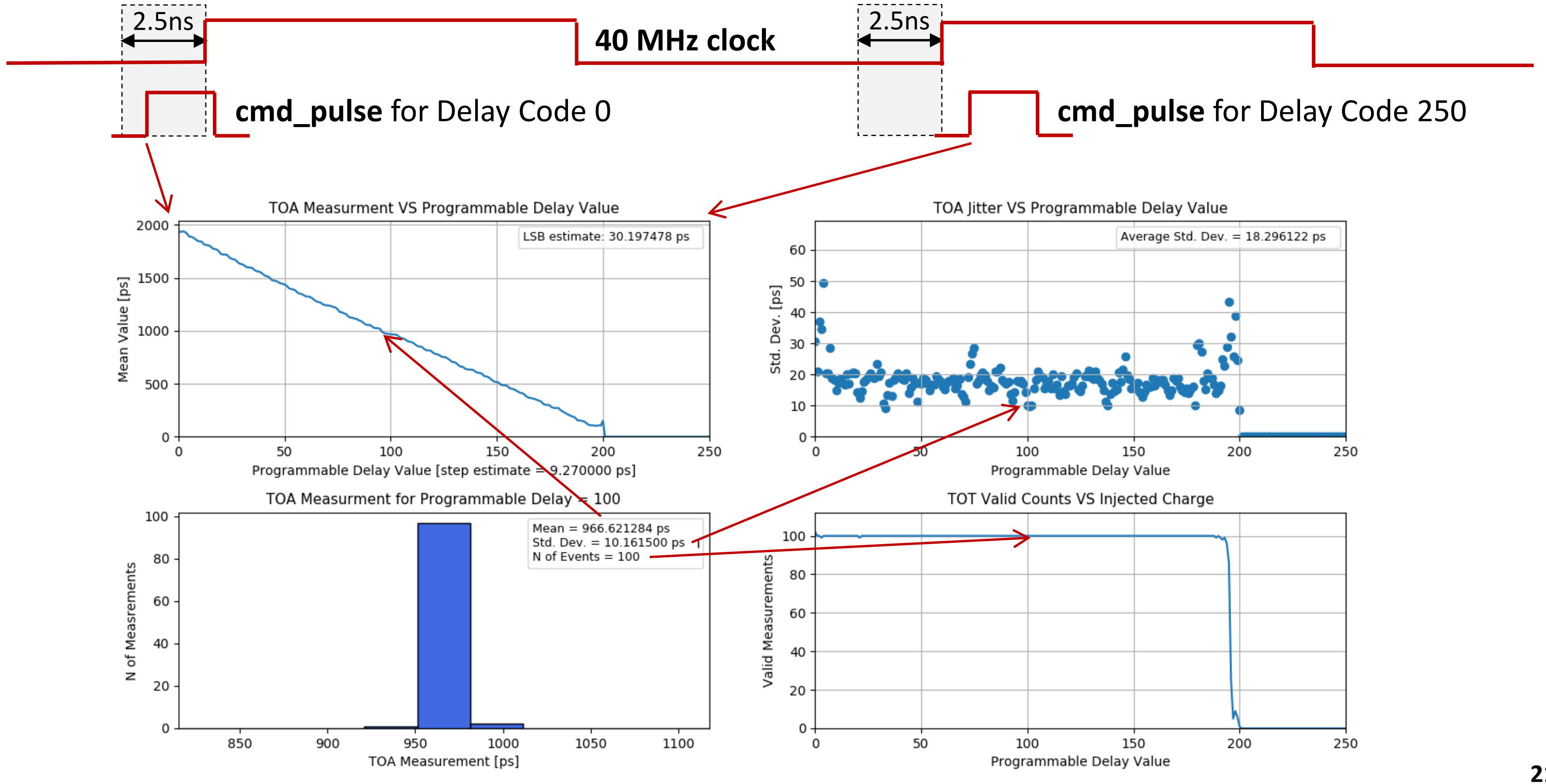




- Using **SY89295UMG** as a programmable delay, the **cmd_pulse** can be delayed by software with steps ~10 ps in ~10 ns range
- Delay to be calibrated:
  - 9.18 ps / Delay Code with FPGA board @ OMEGA
  - 9.27 ps / Delay Code with FPGA board @ SLAC



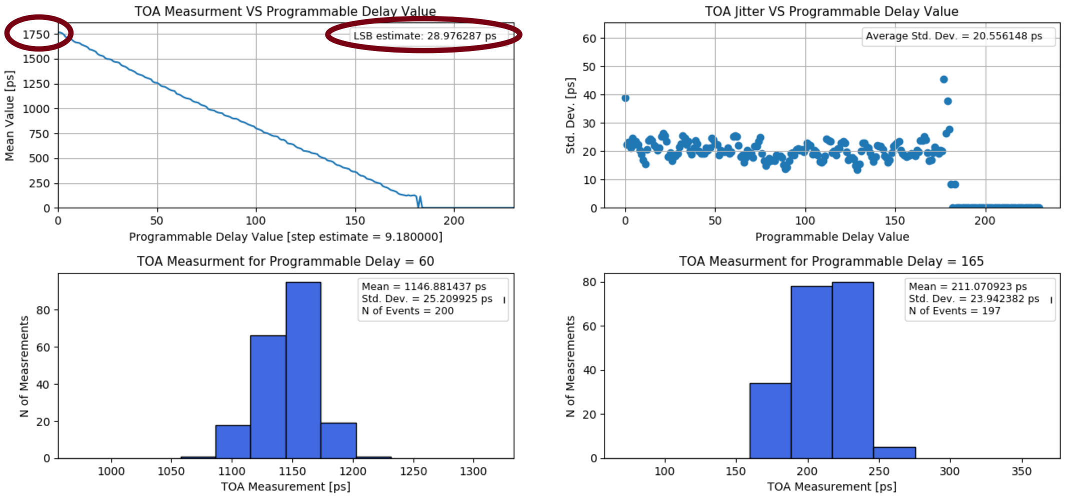
ALTIROC1 Test Setup (3/3)



ALTIROC1_v1 Test Results - Issues (1/2)

SLAC

TOA: VPA; Cd=3pF; Id=1mA; Qinj=10fC; Vth=5fC



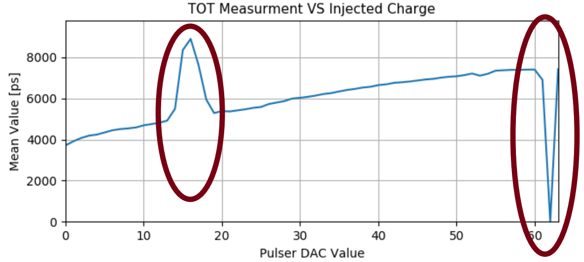
TOA generally ok, with some issues:

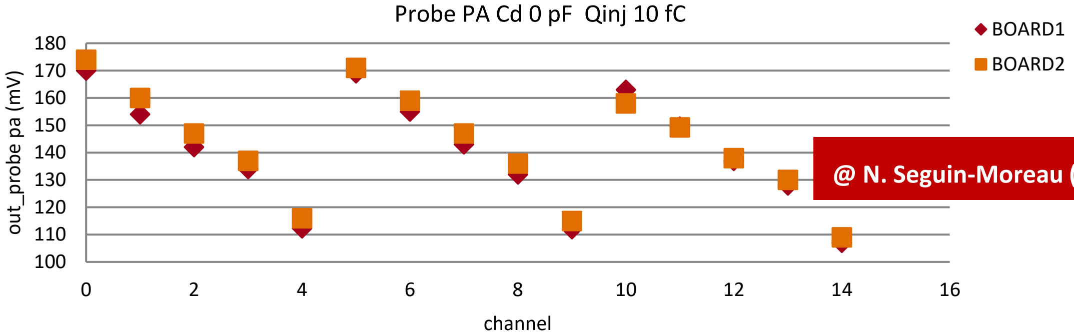
- LSB on the order of 28-30ps; Range on the order of 1.75-2.1ns

TOT had more issues:

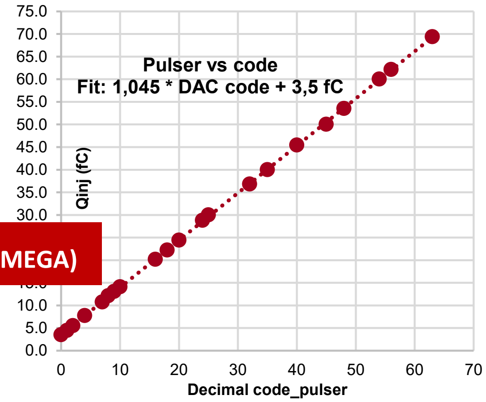
- Range limited to around 7-8ns; presence of artifacts; fine part issue

DLLs had issue with locking values





@ N. Seguin-Moreau (OMEGA)

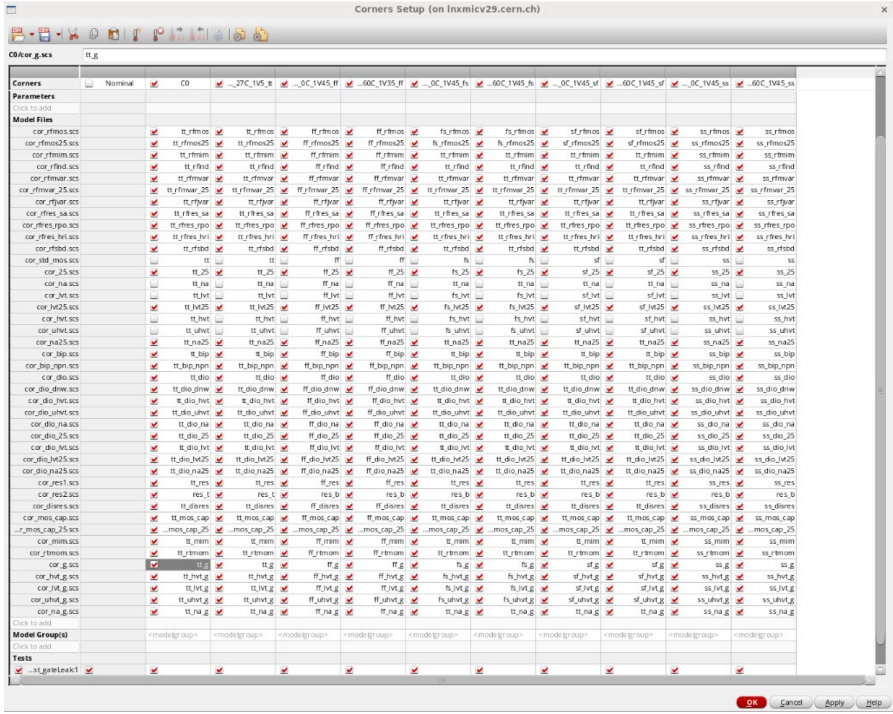


- Analog part had some issues with uniformity and crosstalk;
- Pulser had some issues with injection value
- Phase shifter had issues
- Etc.

ALTIROC1_v1 Test Results - Issues (2/2)

- Most (not all) of the issues that affected every part of ALTIROC1_v1 where traced to leakage current of 1.2V MOSFET transistors
- The standard technology model library does not include the leakage current; special model library has to be used
- ALTIROC1 design re-evaluated with new models and ALTIROC1_v2 submitted in March 2019

Challenge: using new technologies (most of SLAC ASIC designs prior to ALTIROC where in 0.25µm technology) always presents additional challenges and a learning curve necessary in mastering the technology should be taken into account (very important especially for transition in very scaled technologies like 28 or 22nm)



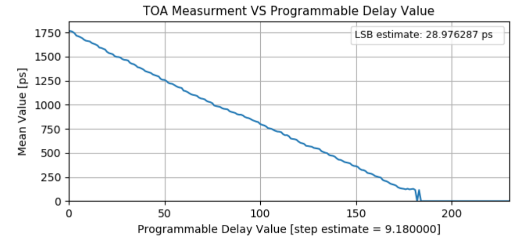
Challenge: initial issues with project integration due to different design softwares used by SLAC (Tanner EDA and HSpice) and OMEGA (CADENCE and Spectre); had to redo the design in CADENCE between ALTIROC1_v1 and ALTIROC1_v2

ALTIROC1: v1 VS v2 VS v3 (SLAC part)

SLAC

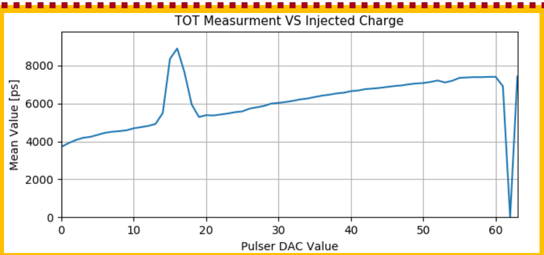
V1

TOA TDC



- Limited range, bigger LSB

TOT TDC



- Limited range, artefacts, etc.

DLLs

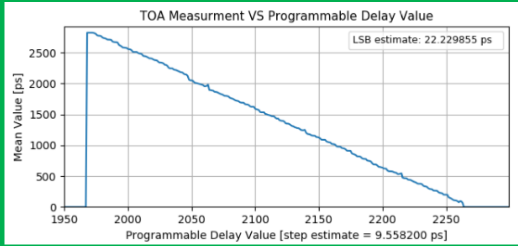
- Leakage Current Issue

SRAM

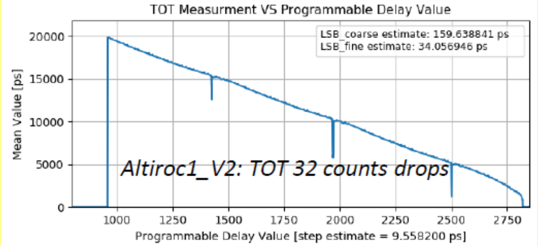
- No Issues

V2

TOA TDC



TOT TDC



DLLs

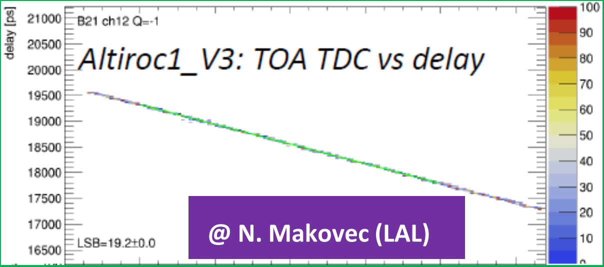
- Some DLLs have difficulty locking; need external R

SRAM

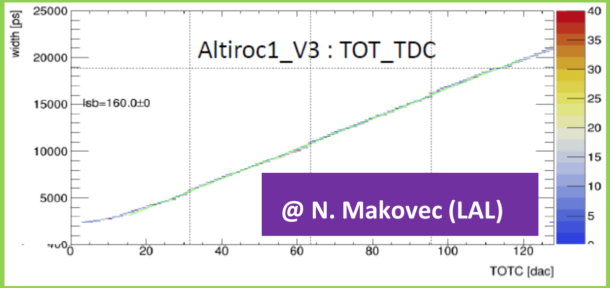
- No Issues

V3

TOA TDC



TOT TDC



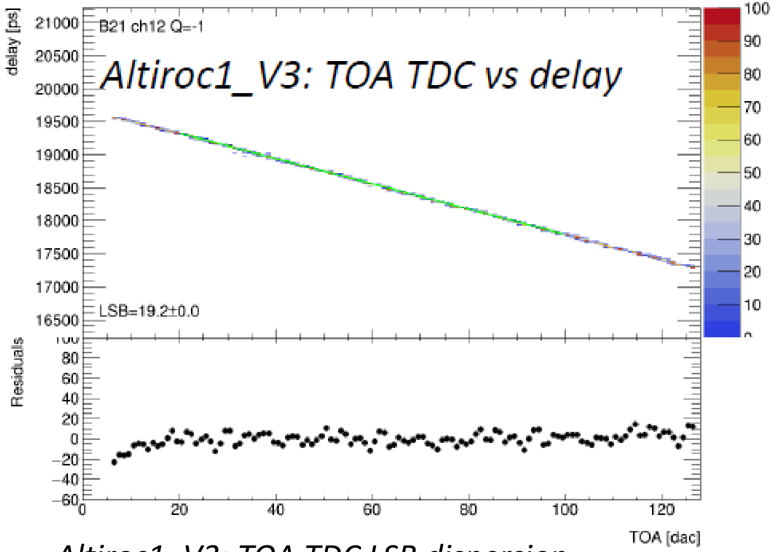
DLLs

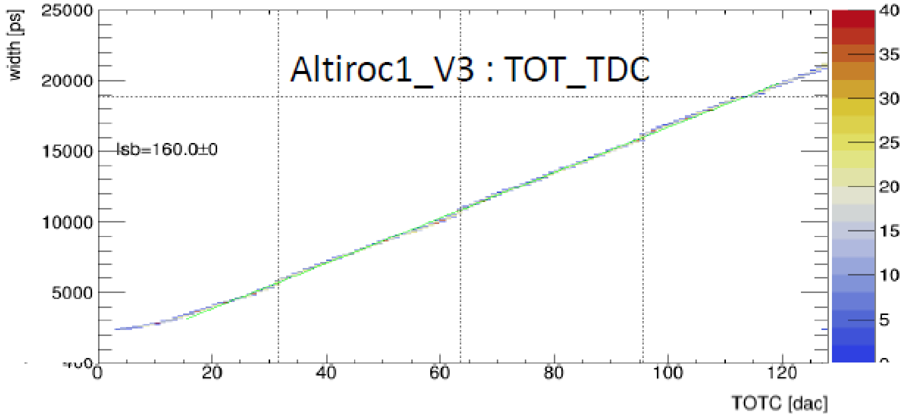
- Locking Issues appear mostly solved (more verification required)

SRAM

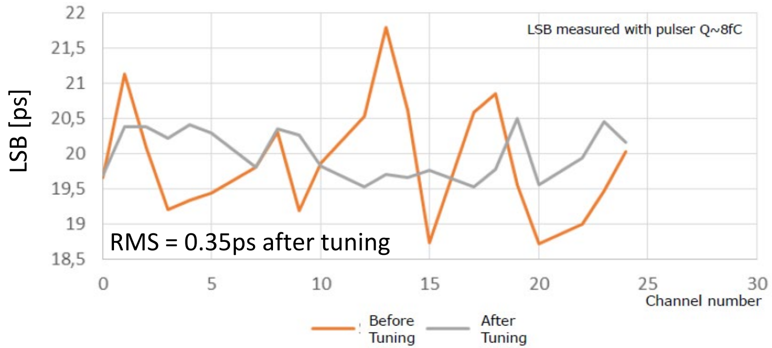
- No Issues

ALTIROC1 Characterization Summary (1/3)

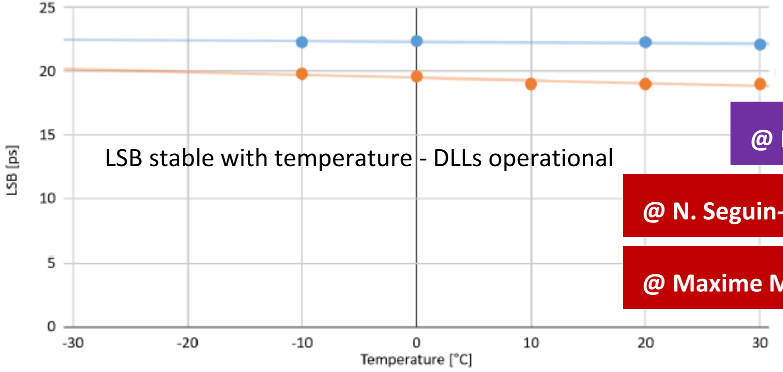




Altiroc1_V3: TOA TDC LSB dispersion



Altiroc1_V3: LSB vs Temperature

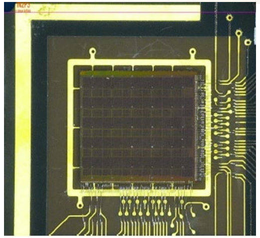


@ N. Makovec (LAL)

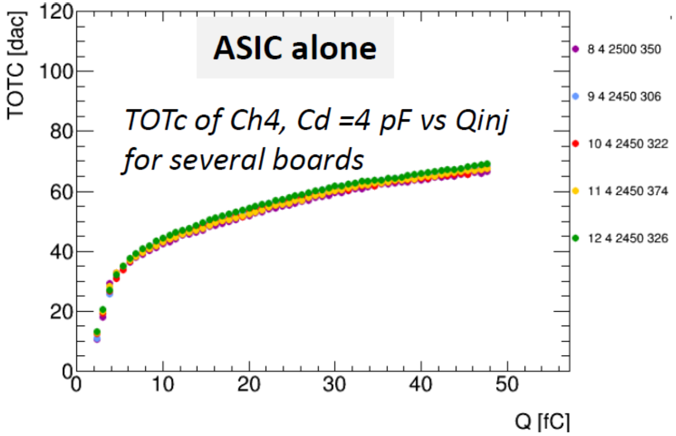
@ N. Seguin-Moreau (OMEGA)

@ Maxime Morenas (OMEGA)

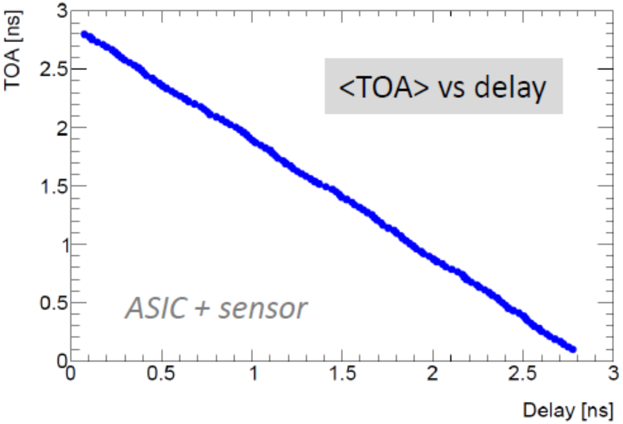
ALTIROC1 Characterization Summary (2/3)

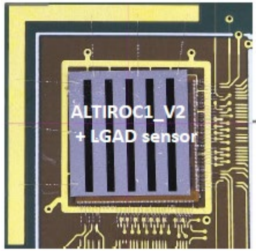


Altiroc1_V2: TOT vs Qinj

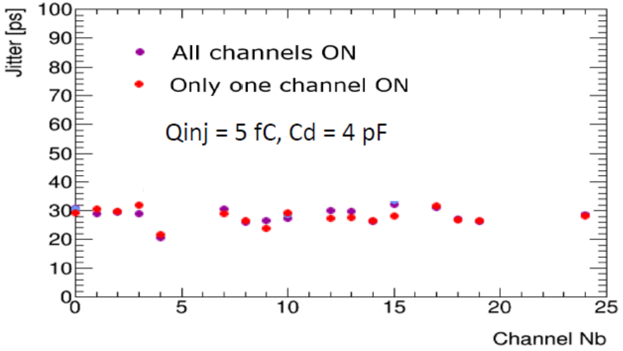


Altiroc1_V2: TOA vs delay

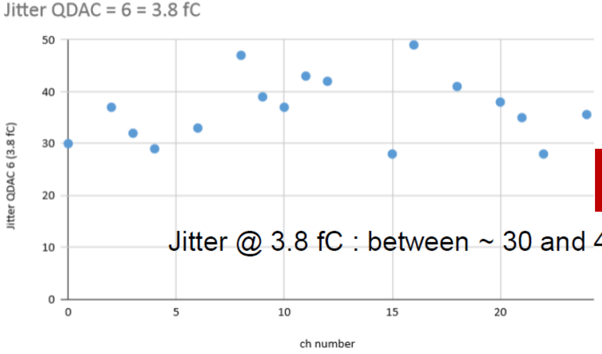




Altiroc1_V3: Jitter vs channel (ASIC alone)



Altiroc1_V3: Jitter vs channel (ASIC + sensor)



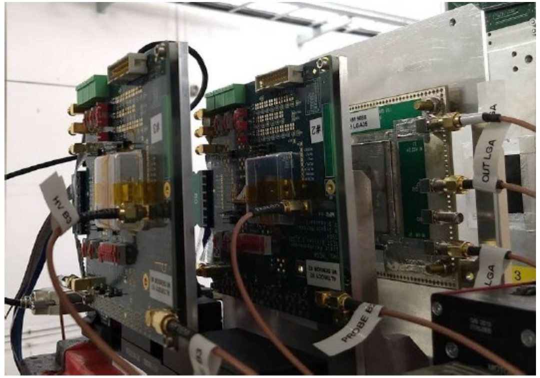
Jitter @ 3.8 fC : between ~ 30 and 42 ps for most of the channels

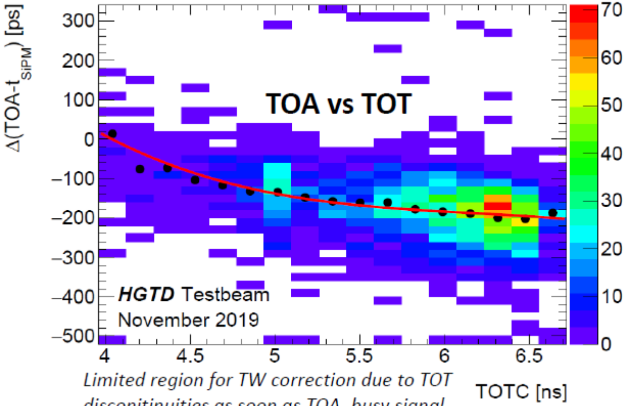
@ N. Makovec (LAL)

@ N. Seguin-Moreau (OMEGA)

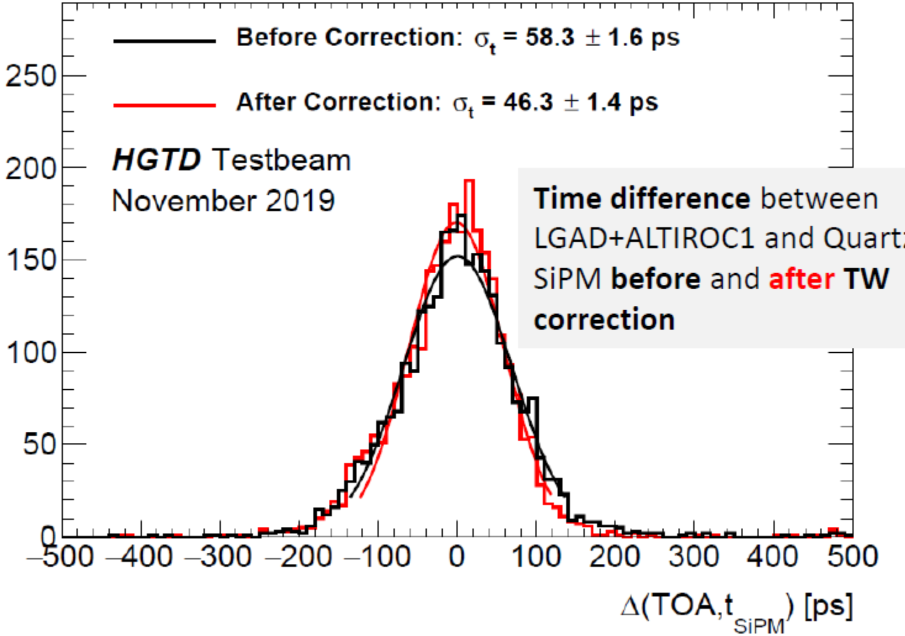
ALTIROC1 Characterization Summary (3/3)

Altiroc1_V2: TEST BEAM measurement





Limited region for TW correction due to TOT disconitinuities as soon as TOA_busy signal is output. Solved in Altiroc1_V3



Time difference between LGAD+ALTIROC1 and Quartz + SiPM **before** and **after TW correction**

Time resolution= 46 ps => electronics jitter 39 ps after substracting Landau fluctuations (25 ps) $\sigma_{hit}^2 = \sigma_{Landau}^2 + \sigma_{clock}^2 + \sigma_{elec}^2$

New interface boards designed after this TB => jitter should be reduced by 35 % and so electronic jitter contribution should be 26 ps in testbeam (36 ps for time resolution)

@ L. Serin (LAL)

@ N. Makovec (LAL)

@ C. Agapopoulou (LAL)

@ S. Sacerdoti (OMEGA)

@ L. Ruckman (SLAC)

@ C. Milke (SLAC)

Lessons Learned (Personal Takeaway)

- A good experience in big international collaborations
- Gained familiarity with ATLAS / LHC operation (my first CERN project)
- Importance of taking time to master a new technology
- Using the same software helps in a collaboration
- Having well defined specs sooner rather than later helps with the design
  - What is the required resolution? TOA and TOT*?
  - What is the measurement range? TOA and TOT*? (*TOT specs depend on the preamplifier thus are more difficult to define early on)
  - What is the necessary conversion time? (does the pixel needs to be able to covert in 2 successive bunch crossings; can there be more then one event per pixel in the same bunch crossing? What is the bunch crossing frequency?)
  - Power consumption?
  - What is the pixel size?
  - What is the technology?
- Having more design personnel would be helpful
- Additional experience with some weak points of various TDC architectures that require particular attention