Timing Extraction for 4D detectors:
SLAC experience and some initial considerations

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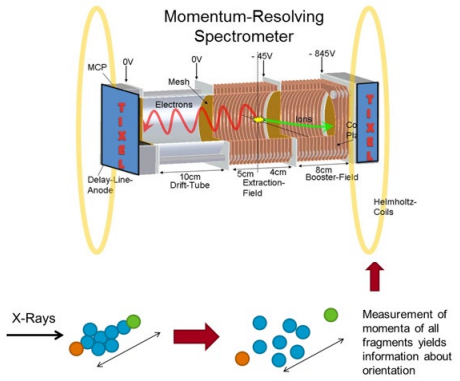
SLAC NATIONAL ACCELERATOR LABORATORY

Timing Detectors @ SLAC

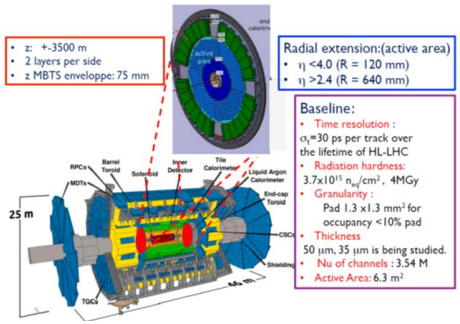
Tixel

- Application: **Photon Science**
- Detector Type: Hybrid
- Sensor: **Si PAD**
- ASIC Technology: 0.13µm
- Resolution: **100ps**
- Granularity: 48x48 prototype, 176x192 full, **100x100µm²** pixels
- Status: prototype done; prototype with sparse readout in progress



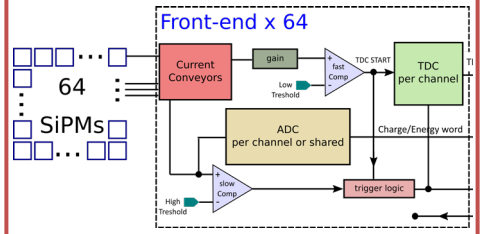
HGTD

- Application: **HEP**
- Detector Type: Hybrid
- Sensor: **LGAD**
- ASIC Technology: 0.13µm
- Resolution: **20ps**
- Granularity: 5x5 prototype, 15x15 full, **1.3x1.3mm²** pixels
- Status: Altiroc1 done; Altiroc2 in progress



SiPM ToF PET

- Application: **Medicine**
- Detector Type: Hybrid
- Sensor: **SiPM**
- ASIC Technology: 0.13µm
- Resolution: **10ps**
- Granularity: 12 channel prototype, 64 channel full, **250µm** channel width
- Status: prototype in progress



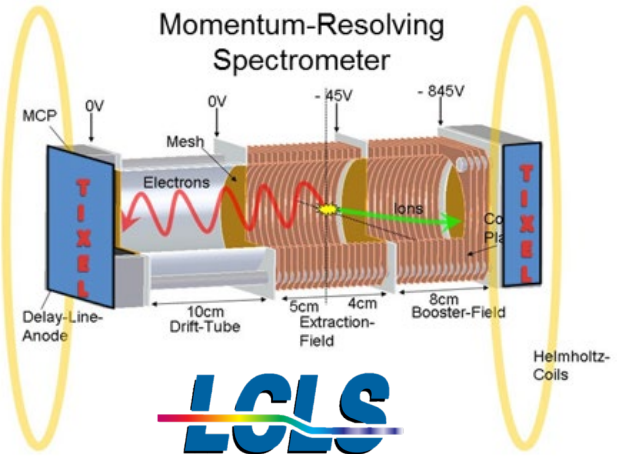
ToF LiDAR (CRADA)

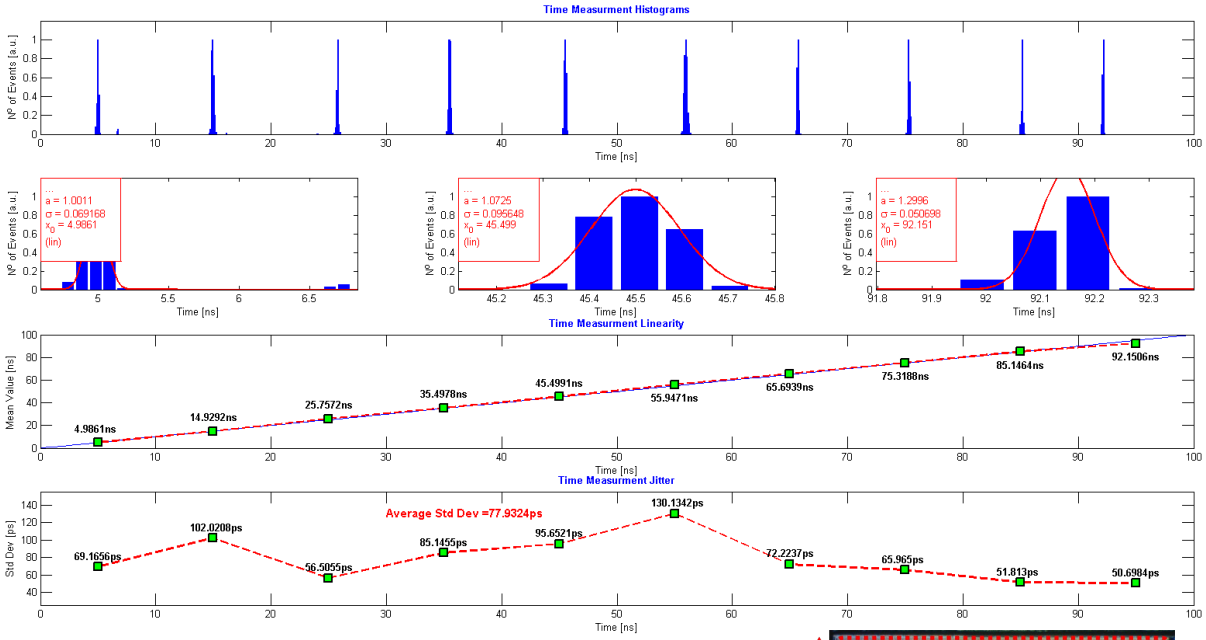
- Application: **Automotive**
- Detector Type: Monolithic
- Sensor: **SPAD**
- ASIC Technology: 0.13µm HV
- Resolution: **1ns**
- Granularity: 80 channel, **400µm** channel width
- Status: project done; product commercially available

Timing Detectors @ SLAC - Tixel

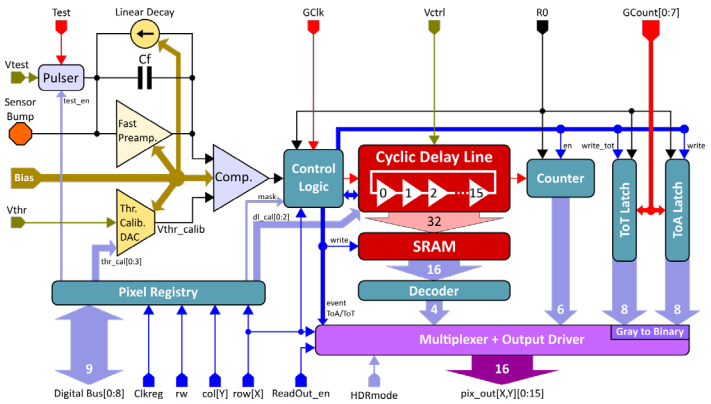
Detector R&D SLAC

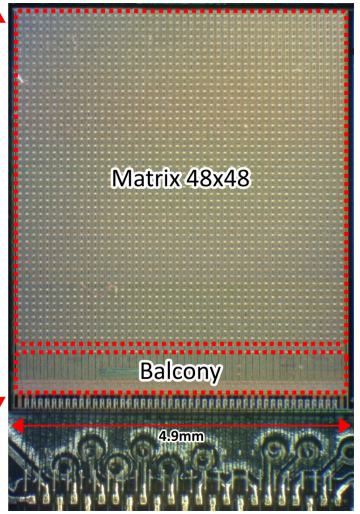
	tPix Specifications
Mode of Operation	Time of Arrival (+ ToT)
Timing resolution	100ps / 1ns
Time depth	1µs / 10µs
Technology	0.13µm
Pixel size	100x100 µm²
Array	176x192 **(48x48 prot.)**
Full Size	Full reticule
Frame rate	120Hz (1kHz)
Range	5keV-50keV 0.22fC-2.2fC
Effective ENC	< 270e⁻ (5 sig. from 5keV)
Max leakage	10pA
Pixel capacitance	150fF
TDC depth	14bit / 18bit
Supply	1.2V
Power cons.	< 30uW/pix
Power pulsing	yes





Pixel Architecture:





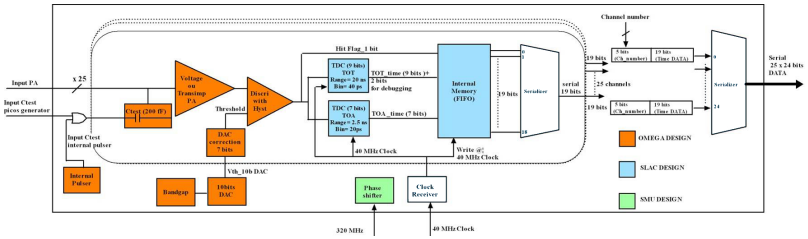
Timing Detectors @ SLAC – HGTD (Altiroc ASIC)

Detector R&D SLAC

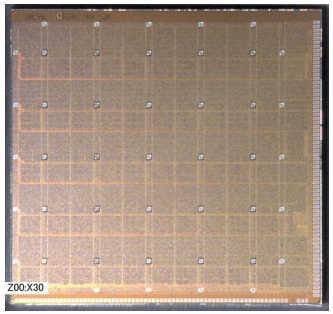
LGAD pixel size (thickness ~ 45 µm)	1.3 x 1.3 mm^2	
Detector capacitance	3.4 pF	
Collected charge (1 MIP) at gain = 20	9.2 fC	
Dynamic range	20 MIPs	
Preamplifier + discriminator jitter at gain = 20	< 20 ps	=> Electronics total contribution < 30 ps
Time walk contribution	< 10 ps	
TDC binning	20 ps (TOA, TZ TOT) , 40 ps (VPA TOT)	
TDC range	2.5 ns (TOA), 20 ns (VPA TOT) / 5 ns (TZ TOT)	
Number of bits / hit	7 bits (TOA), 9 bits (VPA TOT) / 8 bits (TZ TOT)	
FIFO latency	10 µs / 35 µs latency for L0/L1 trigger	
Luminosity counters per ASIC	7 bits (sum) + 5 bits (outside window)	
Number of channels/ASIC	225 (15 x 15 pixel matrix)	
elink driver bandwidth	320 Mb/s, 640 Mb/s and 1.28 Gb/s	
Total power per area (ASIC)	< 300 mW/cm^2 (< 1.2 W) => 5 mW/pixel (4 mA/pixel)	
TID and neutron fluence	Inner region: 4.5 MGy, 4.5 x 10 ^{15} n/cm^2 Outer region: 2.1 MGy, 4.0 x 10 ^{15} n/cm^2	=> CMOS 130 nm

ATLAS EXPERIMENT

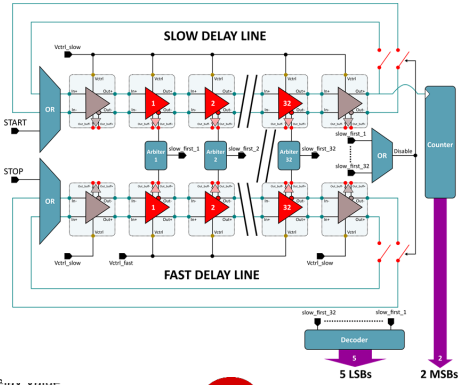
Pixel Architecture:

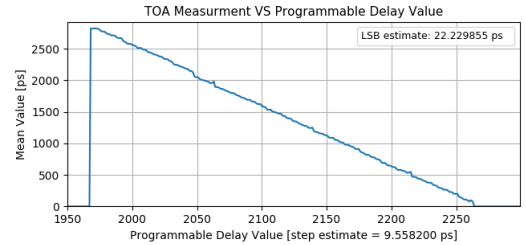


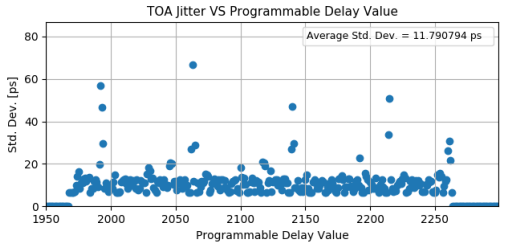
ALTIROC1:

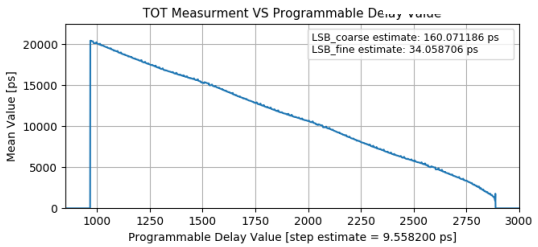


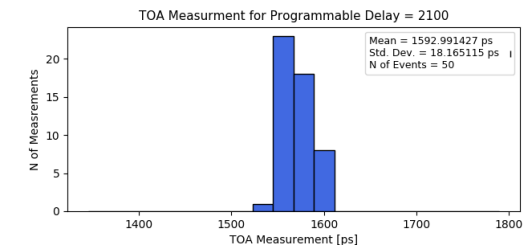
TDC Architecture:

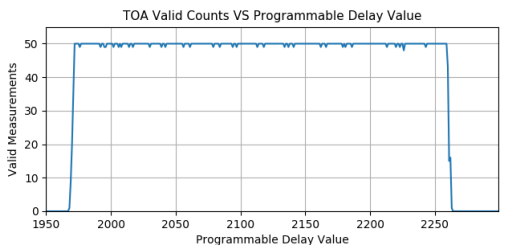


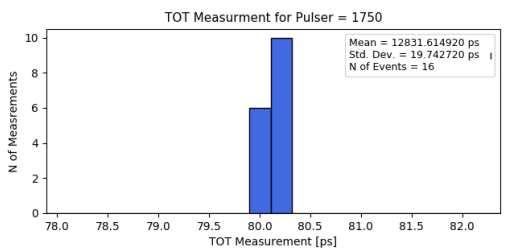












OMEGA Microelectronics

LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

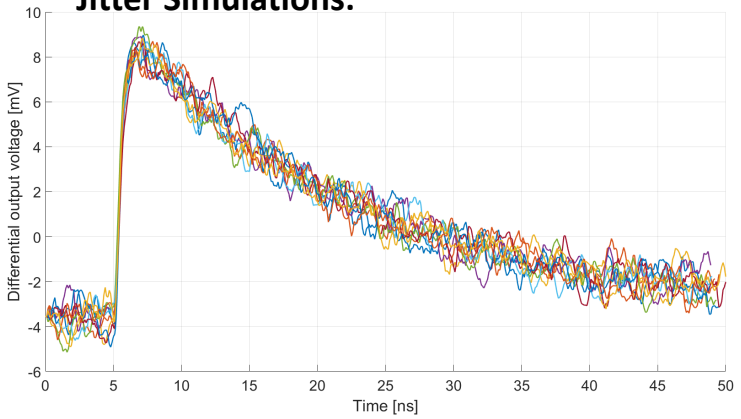
SMU

IFAE

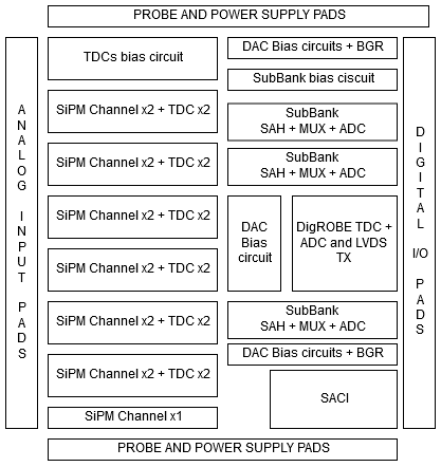
Timing Detectors @ SLAC – SiPM ToF PET

- Electronics Time Resolution — 10 – 20 ps (FWHM)
- TDC Time Window — ~ 20ns
- Max Charge — 1300 pC
- Max Hit Rate — 25K cps
- Charge Resolution — Single photon
- Output Data Rate/CH — 100 KHz
- SiPM/Scintillator — 1:1 coupling
- Resolve Event Across — 4 pixels
- AFE Interface — AC & Differential
- # of Channels — 64

Jitter Simulations:



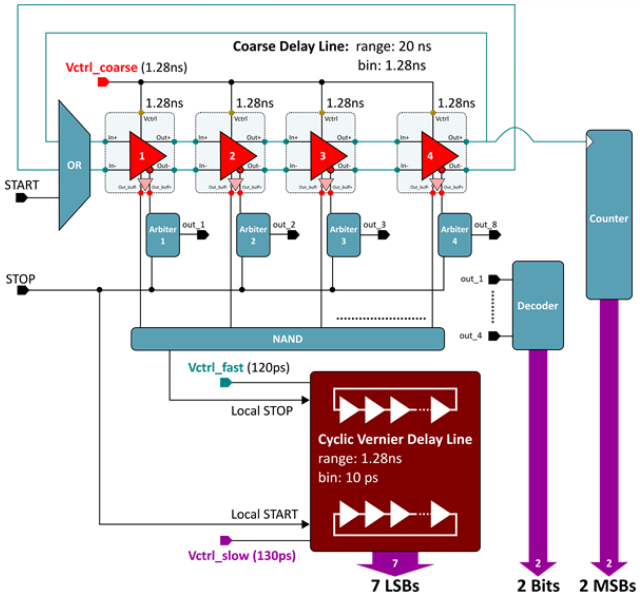
Prototype ASIC Architecture:



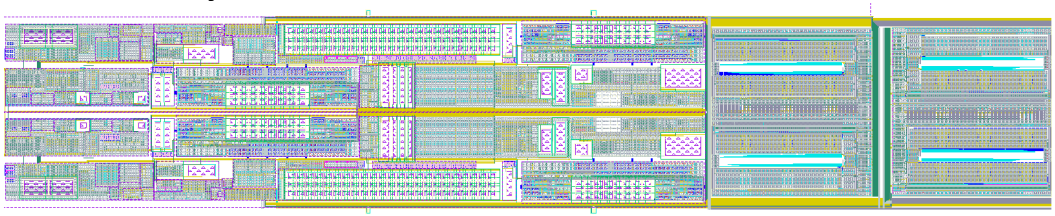
DIPARTIMENTO DI INGEGNERIA ELETTRICA E DELL'INFORMAZIONE

Stanford MEDICINE

TDC Architecture:

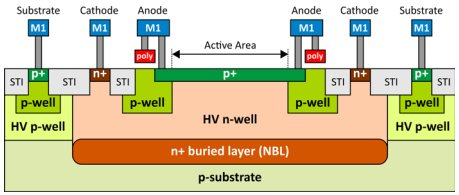


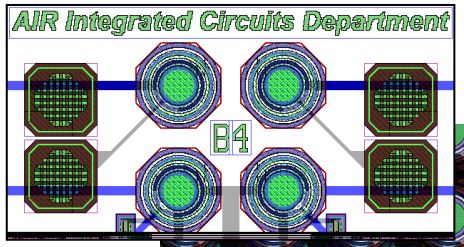
2 Channel Layout:

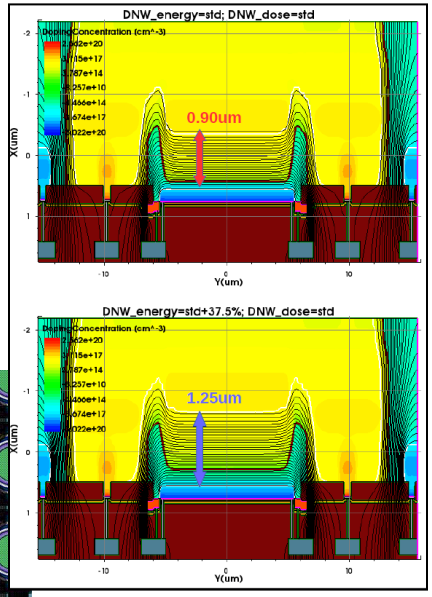


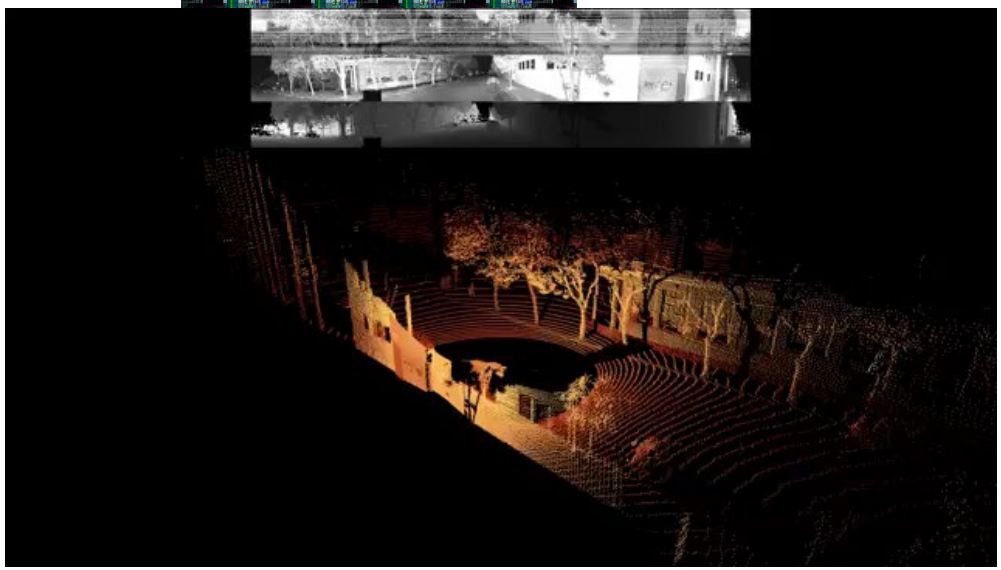
Timing Detectors @ SLAC –ToF LiDAR (CRADA)

SPAD Array Design @ SLAC:



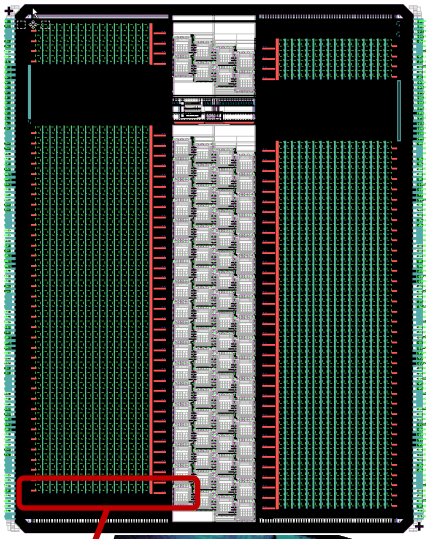


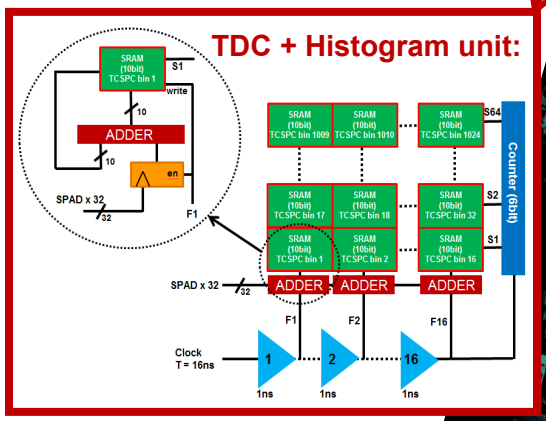


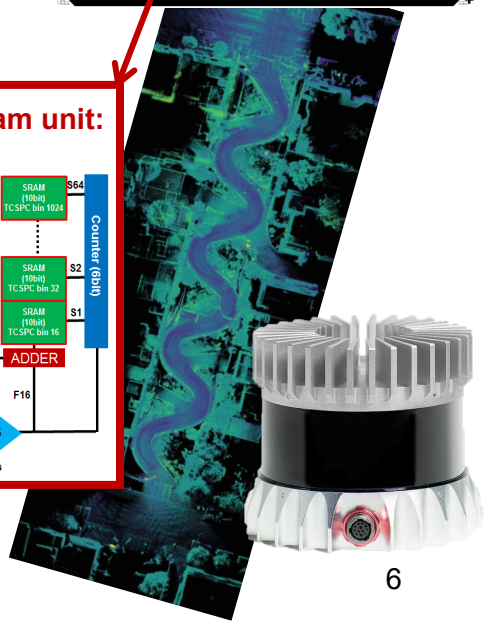


ToF real-time histogramming ASIC with monolithic SPAD array

- 80 macro-pixels with 32 SPADs each
- Photon Counting: 20bit counter for each SPAD
- Photon Timing: 10bit, 1ns resolution TDC and in-chip 1024 bin, 10bit depth Histogram unit per macro-pixel





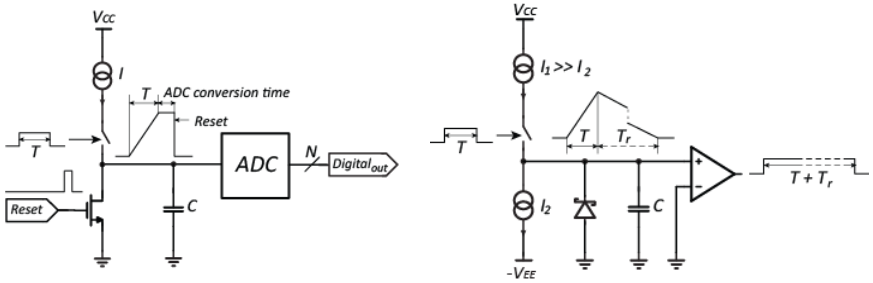


Time-to-Digital Converter (TDC)

- One of the fundamental components of any timing detector is an electronic circuit that converts the time into a digital code, i.e. **Time-to-Digital Converter** (**TDC**)
- In all projects mentioned previously, the TDC was designed exclusively at SLAC
- TDC architectures can roughly be divided in 2 categories: **Analog** and **Digital**:

Analog:

Intermediate step of converting time to analog voltage

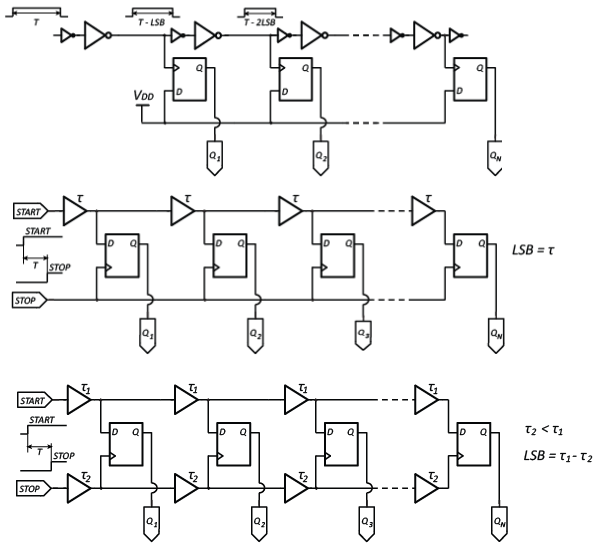


- Time-to-Amplitude Converter (TAC) + ADC
- Time-Stretching + Counter
- Etc…

- **Pros:** up until recently they had undoubtedly better performances in a few channel implementations
- **Cons:** not suitable for massive multi-cannel IC implantations and technology scaling
- **Used in most commercial high-precision timing instruments (few conversion channels)**

Digital:

Direct conversion of time to digital code



- Pulse-Shrinking Delay Line
- Tapped Delay Line
- Vernier Delay Line
- Ring Oscillator
- Time Amplifier
- Etc…

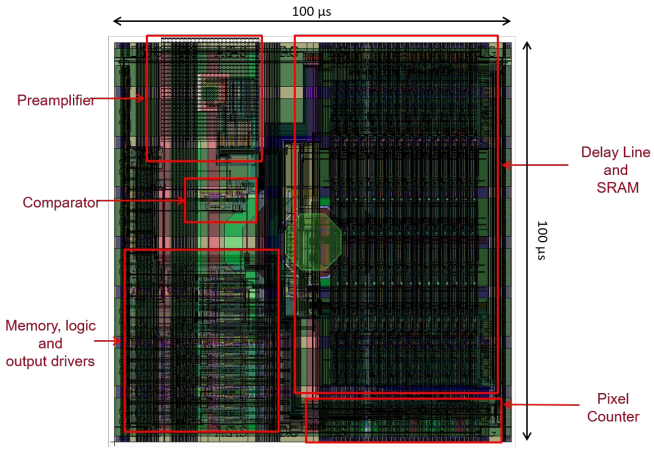
- **Cons:** performances generally not as good as analog counterparts (lately less true)
- **Used in most high-precision timing ASICs (lot of conversion channels)**

- **Pros:** suitable for massive multi-channel IC implementation; performances generally improve with technology scaling

TDC – Trade-offs (simplified)

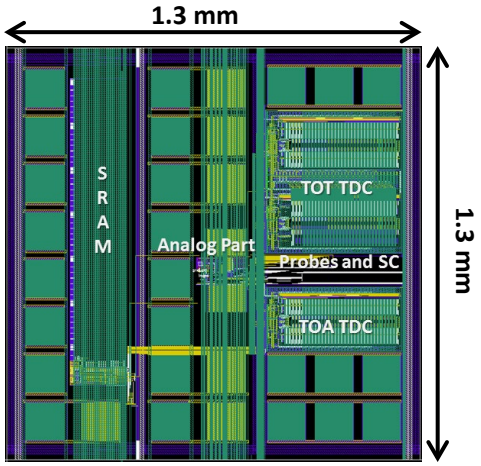
Tixel

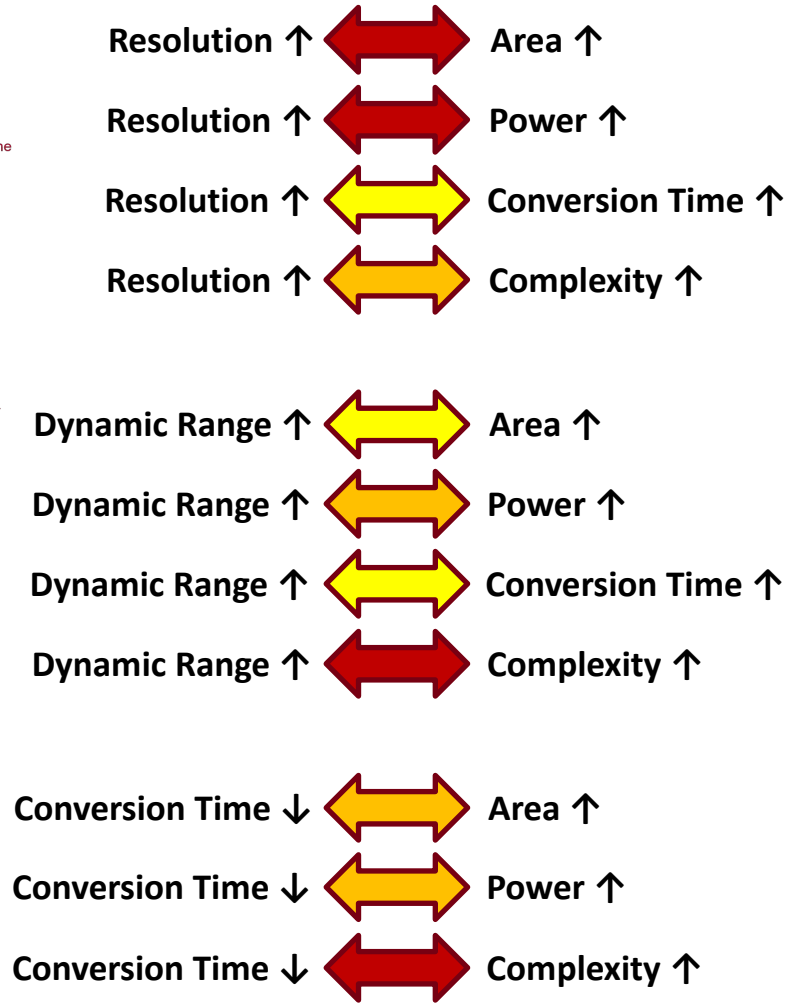
- ASIC Technology: 0.13µm
- Resolution: **100ps**
- Granularity: 48x48 prototype, 176x192 full, **100x100µm²** pixels
- TDC Area: **85x45µm²**
- TDC Range: **1.6µs**



HGTD

- ASIC Technology: 0.13µm
- Resolution: **20ps**
- Granularity: 5x5 prototype, 15x15 full, **1.3x1.3mm²** pixels
- TOA TDC Area: **210x430µm²**
- TOT TDC Area: **450x430µm²**
- TOA TDC Range: **2.5ns**
- TOT TDC Range: **20ns**





5ps, 50x50µm² pixel – Challenges / Discussion

- Detector critical components: **Sensor**; **Analog Front-End**; **TDC**
- What is the best sensor candidate for 5ps timing: **LGAD?** – (needs to detect events with <5ps precision)
- Analog Front-End – designed based on the sensor; needs to convert the sensor signal (typically charge) into digital pulse while not degrading the sensor's timing precision **– typically suffers form technology scaling**
- TDC with 5ps resolution within 50x50µm² pixel area in 0.13µm technology node is very unlikely; TDCs (digital) benefit from technology scaling ➡ **65nm or 28-22nm technology**
- Analog Front-End suffers from technology scaling, TDCs benefit ➡ **65nm technology a compromise?**
- What are the detector's **Dynamic Range** and **Conversion Time** (Dead Time)?
- What about radiation-hardness?