HPS DAQ updates

Sergey Boyarinov
JLAB
May 15, 2020

HPS DAQ & Trigger Requirements

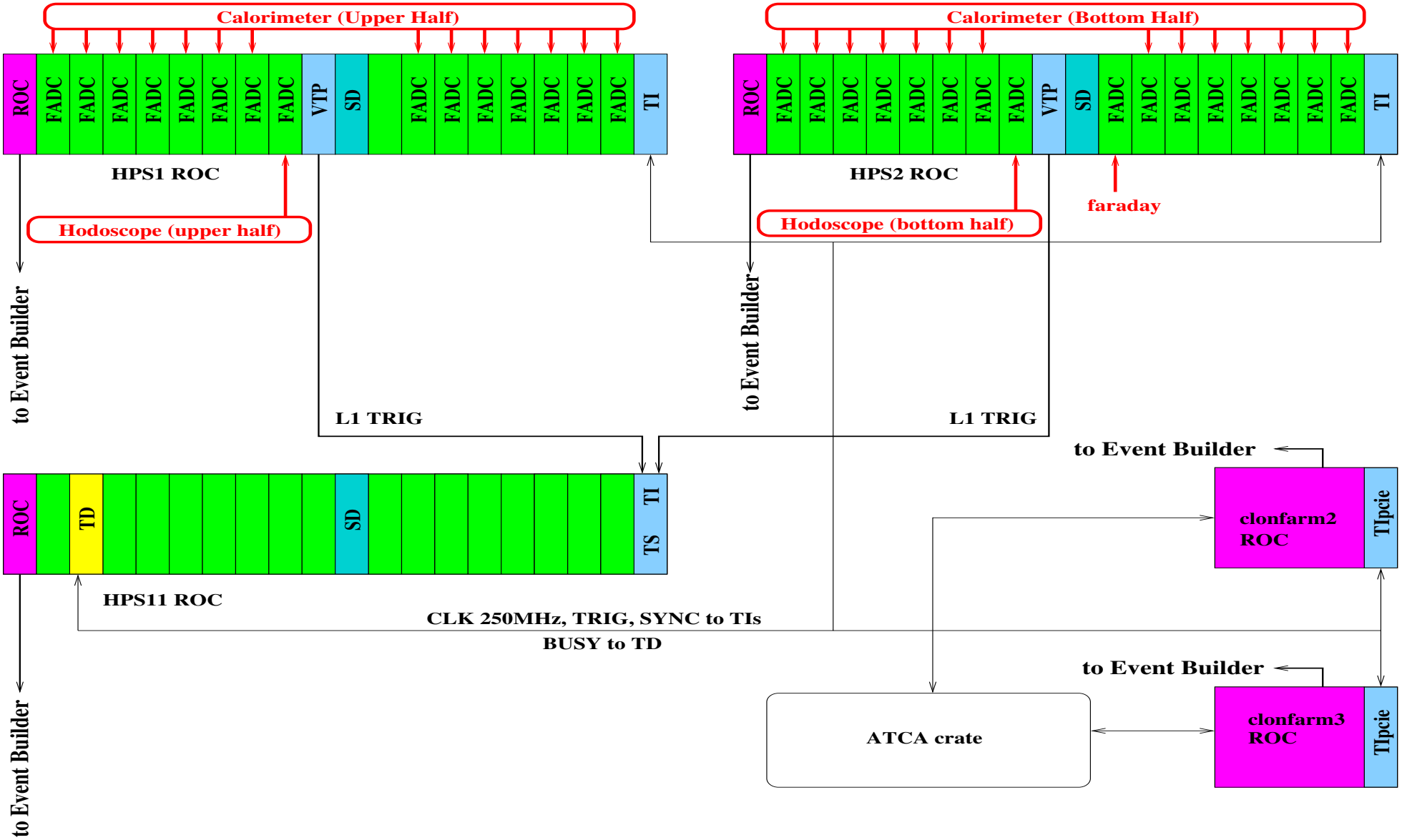
20kHz event rate

100MB/s data rate

>95% livetime

Achieved event rate 27kHz

HPS DAQ/Trigger Front-End Electronics



3 VXS crates, 2 servers, 1 ATCA crate, 7 Readout Controllers

HPS DAQ Status

- Calorimeter Readout: 442 channels of 12bit 250MHz Flash ADCs
- Hodoscope Readout: 32 channels of 12bit 250MHz Flash ADCs
- CPU/VTP/TS/SD/TD trigger and signal distribution boards
- 3 VXS crates
- 2 servers with TIpcie cards for SVT readout
- SVT readout (front-end and ATCA blades)

Back-end computing and software is CLAS12 facility: network, computing, DAQ software, data monitoring, messaging system, realtime database

HPS trigger

Run# 9882 | HPS Triggers | 07/20/2019 15:35:27

Beam Currents (nA) 2C21: 51.28 FCup: 52.56 | Livetime (%): 98.80

#	Description	Raw Rate (Hz)	Prescaled Rate (Hz)	%	Prescale
00	Single-0 Top	331965.0	0.0	0.0	0
01	Single-1 Top	7695.0	0.0	0.0	0
02	Single-2 Top	1725.0	1733.0	45.7	1
03	Single-3 Top	1053.0	0.0	0.0	0
04	Single-0 Bottom	3591944.0	0.0	0.0	0
05	Single-1 Bottom	11395.0	0.0	0.0	0
06	Single-2 Bottom	1896.0	1958.0	51.6	1
07	Single-3 Bottom	1154.0	0.0	0.0	0
08	Pair-0	2425.0	0.0	0.0	0
09	Pair-1	12920.0	0.0	0.0	0
10	Pair-2	10115.0	0.0	0.0	0
11	Pair-3	2170.0	0.0	0.0	0
12	LED	0.0	0.0	0.0	0
13	Cosmic	0.0	0.0	0.0	0
14	Hodoscope	792123.0	0.0	0.0	0
15	Pulser	100.0	101.0	2.7	1
16	Cluster Multiplicity-0	21641.0	0.0	0.0	0
17	Cluster Multiplicity-1	697.0	0.0	0.0	0
18	FEE Top	8297.0	0.0	0.0	0
19	FEE Bottom	9159.0	0.0	0.0	0
		Sum:	3792.00		

Front Panel (Hz): Faraday Cup 0.0 N/A 0.0

FADC Data Rate (MB/s): hps1 3.19 hps2 4.98

Main development for 2019 run

New trigger (Ben Raydo)

FADC firmware was upgraded to implement correct BUSY propagation, allowing to run above 30kHz

TIpcie boards and Linux servers as ROCs: serious development was conducted, including some fixes during the run (clock rewiring, fiber contact losses); new board revision under development

SVT readout was redesigned to be used with TIpci boards; in a future more work will be needed to make it more stable, currently all ATCA electronics back to SLAC

Software: new libraries for SVT and some CODA fixes; runtime database

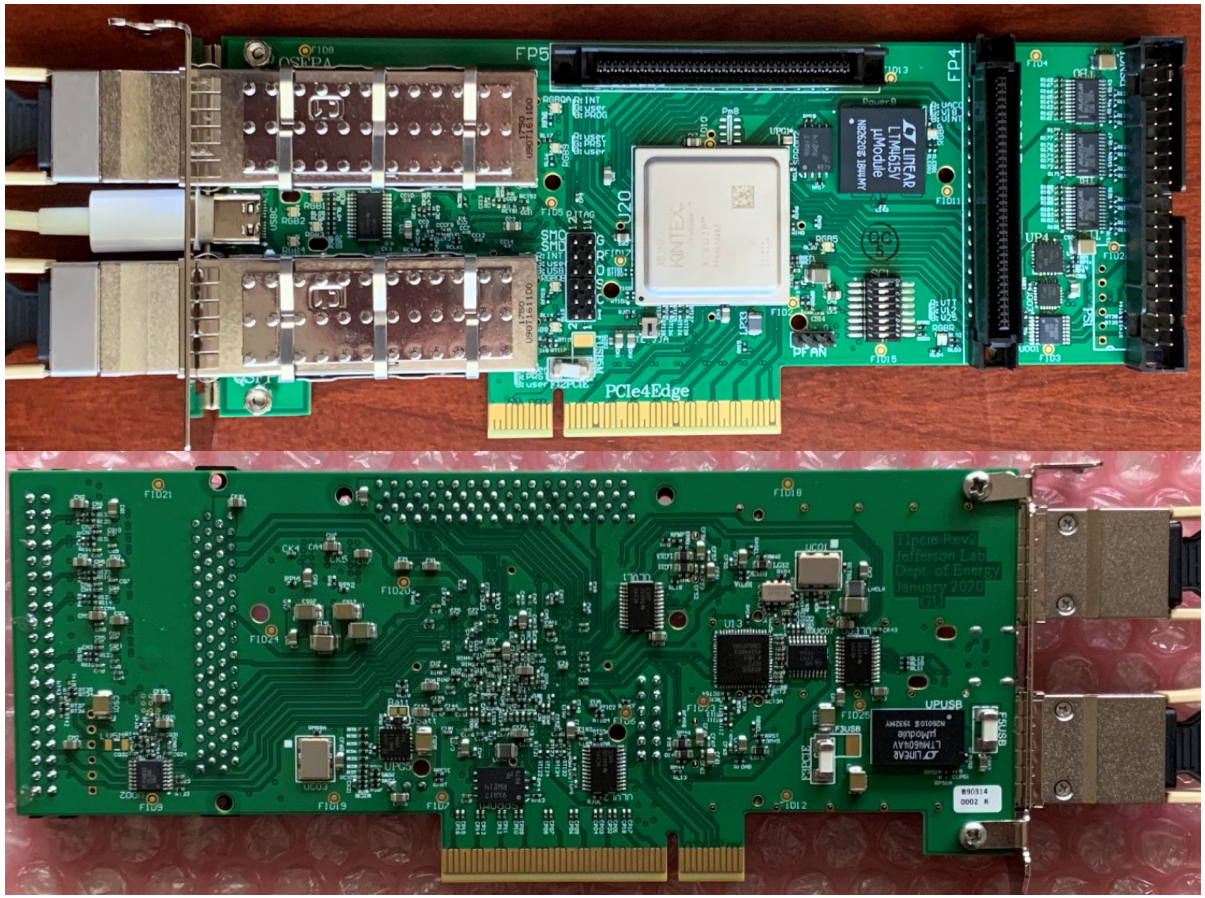
New TIpcie module

Better PCIe compatibility:
- Xilinx UltraScale+ FPGA: xcku3p
- PCIexpress from gen1x1 (low power) to gen3x8 (high bandwidth)

More like a VME TI:
- TI fiber#1, fiber#5
- 40-pin IO to the second front panel
  - 8 outputs + 1 clock output; (LVDS, 3 optional ECL)
  - 10 inputs + 1 clock input; (any diff. level)

More potentials:
- Another 64 LVDS connection to the FPGA:
  - 64-channel FPGA based TDC
- USBC connector on the front panel
  - +5V in for standalone operation

Two prototypes received on May 8, 2020



DAQ Status

All hardware and software on JLAB side is ready to run any time

SVT part is removed

Integration with SVT DAQ has to be repeated again because of new TIpcie module, it has to be discussed and planned (test setup at SLAC)

If SVT readout performance improved we can increase overall DAQ performance (without SVT, DAQ can run >30kHz)