

Dual Readout Calorimetry at SLAC: Status & Planning

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with input from Su Dong, Qibin Liu, Lorenzo Rota, Larry Ruckman, Ariel Schwartzman

16 July 2026

[FPD Higgs Factory WG](#)

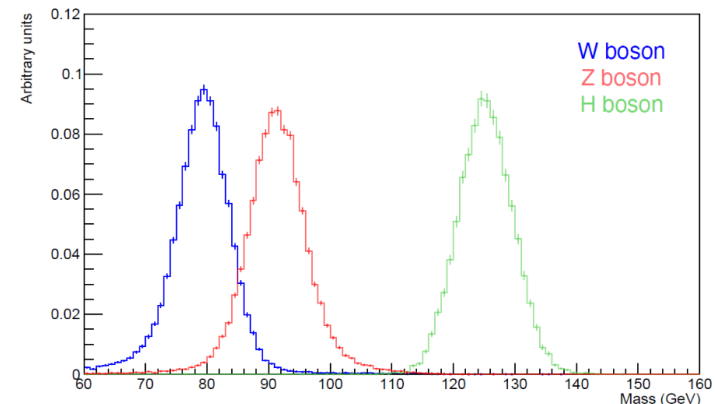
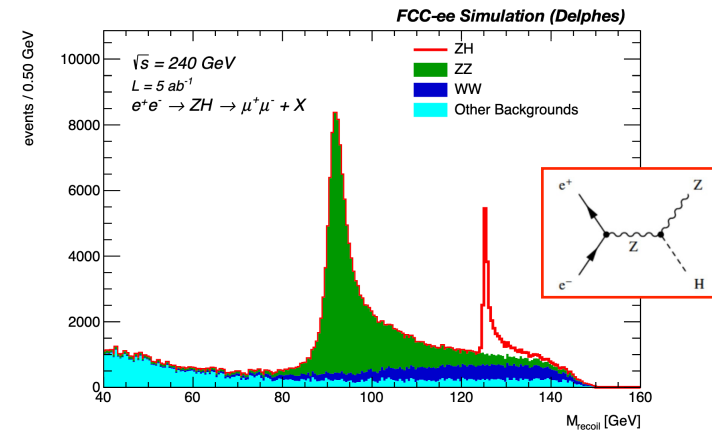


Reminder: Key Physics Drivers

- **Calorimetry is essential to FCC physics goals:**
enables key precision measurements & rare event searches
 - 2-3x better energy resolution than ATLAS
- An **electromagnetic energy resolution of $3\%/\sqrt{E} \oplus 1\%$** provides:
 - Improving the resolution of the $Z \rightarrow ee$ recoil Higgs mass (& also recover bremsstrahlung photons in tracker)
 - e/γ ID & improved ParticleFlow
- A **hadronic energy resolution at $30\%/\sqrt{E} \oplus 1\%$** can be used for:
 - W/Z/H separation (mitigate background in Higgs analyses, precision EWK measurements)
 - PFlow: reduce confusion term

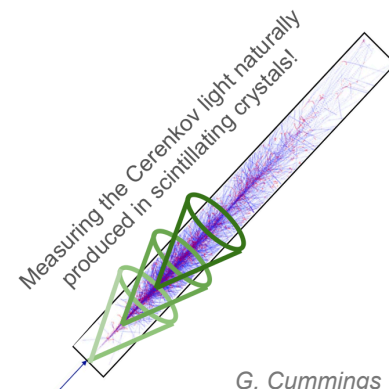
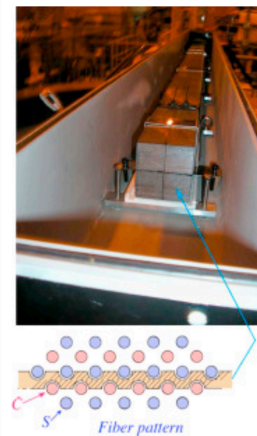
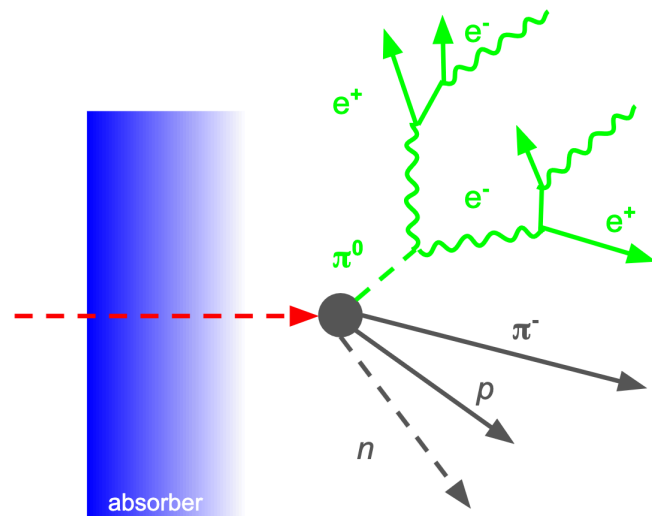
$$m_{recoil}^2 = (\sqrt{s} - E_{ff})^2 - p_{ff}^2$$

$$= s + m_Z^2 - 2E_{ff}\sqrt{s} \approx m_H^2$$



What is Dual Readout?

- Jets have two components which fluctuate event-to-event:
 - “electromagnetic” (EM) fraction, i.e. charged, relativistic (mostly π^0)
 - “hadronic” (had) fraction, i.e. slower stuff (protons and neutrons)
- **Dual readout:** EM/had ratio can be inferred from ratio of Cherenkov C to scintillation S light
- Two approaches:
 - Dedicated Cherenkov radiators + scintillators (DREAM/RD52)
 - Homogeneous (IDEA ECAL): measure Cherenkov light produced inside scintillating crystals (SiPMs)



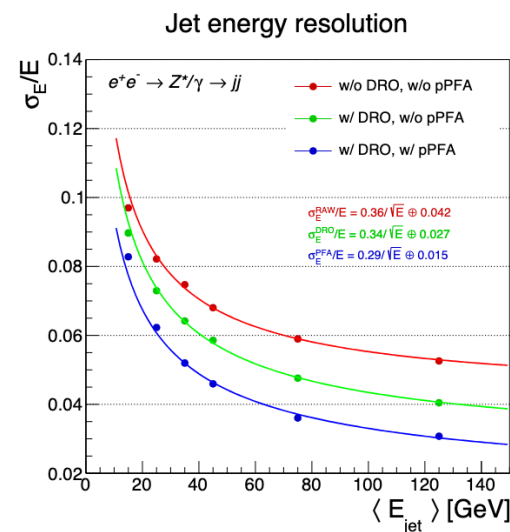
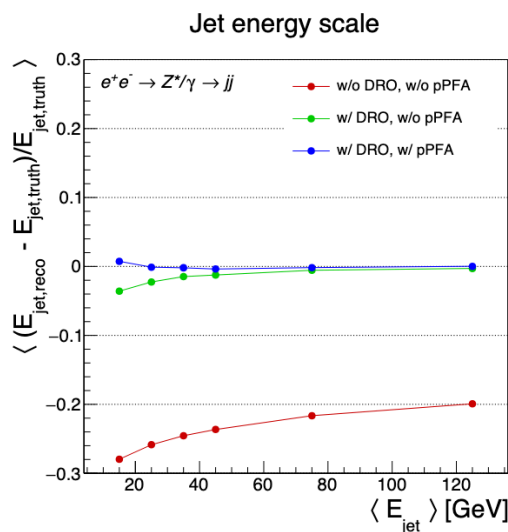
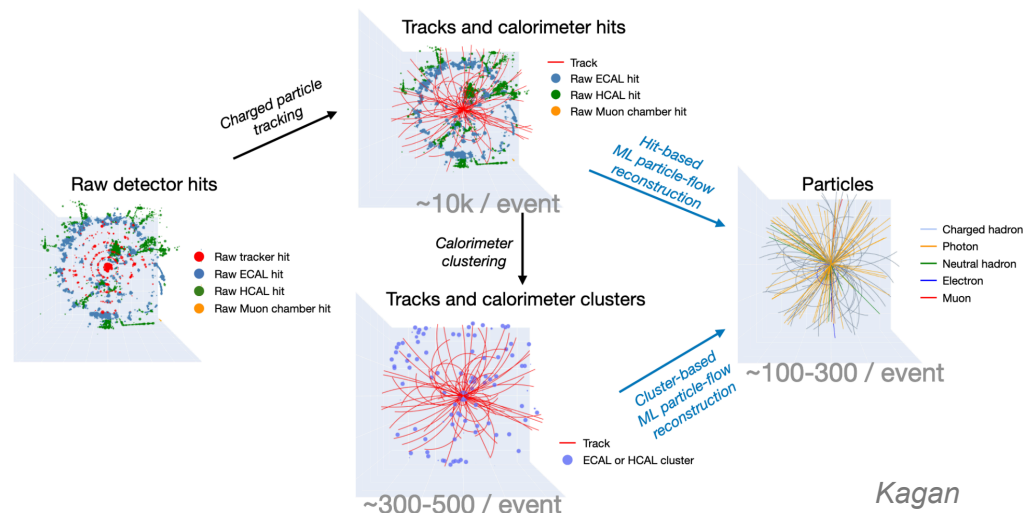
What is Particle Flow?

- Reconstruct individual particles in showers, using tracking info for charged particles + clusters, providing better global event info

- Motivates high granularity (“tracking” capability of calorimeters)
- Limited by confusion term (overlapping showers)

Why we're interested:

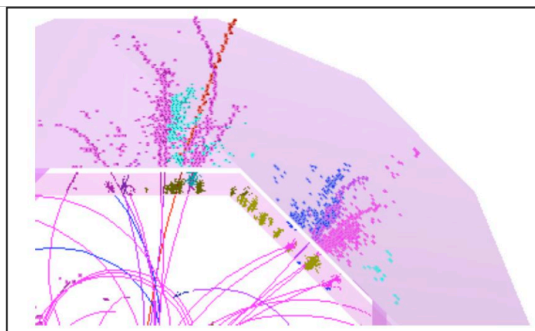
- Combines well with **DRO** to further improve jet reconstruction
- Excellent opportunity for **AI/ML**-based enhancement (eg. GNNs [Krzmanec], FM/fine-tuning [Kagan])
- Precision timing** highly useful



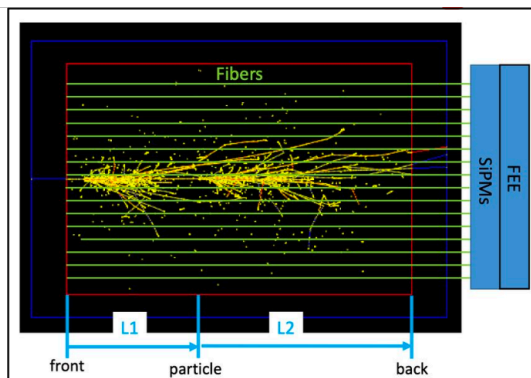
What is 5D Calorimetry?

- Measure (x, y, z, E, t)
 - Requires precision timing: $\sim O(20)$ ps

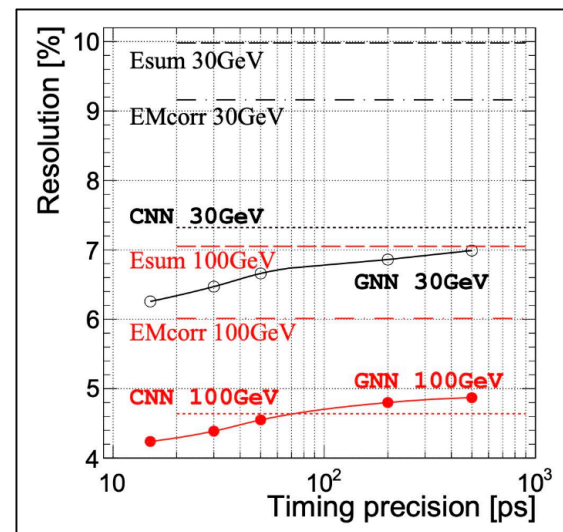
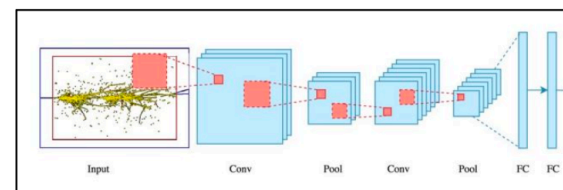
A. Schwartzman



[Akchurin, et. al.](#)

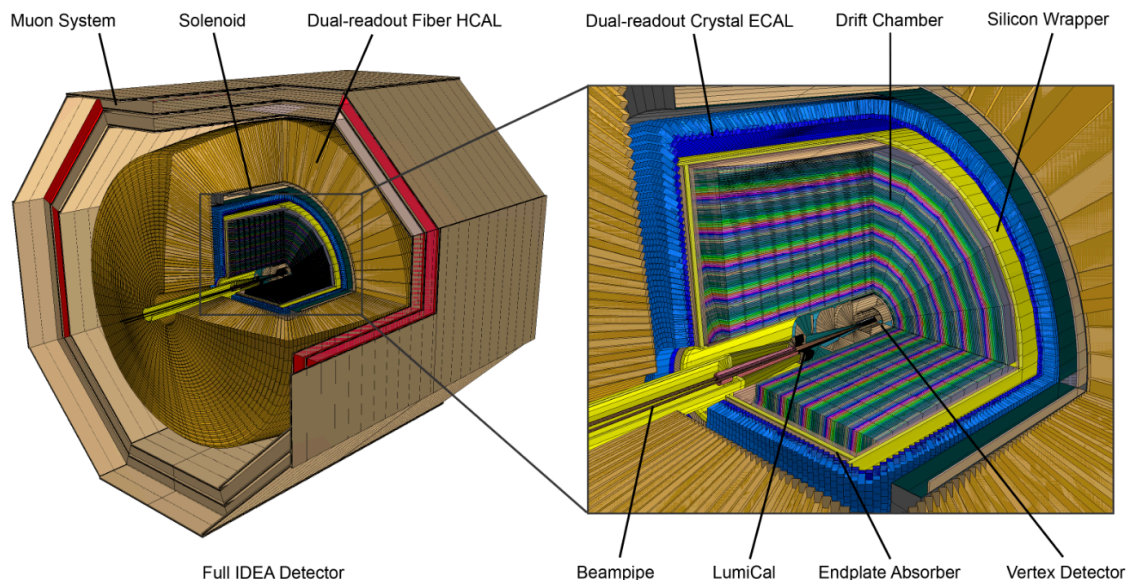


- **Performance of particle flow limited by the ability to accurately *associate tracks to calorimeter clusters***
 - Challenging when showers overlap in space
- **Exploit the full space-time structure of showers to improve the jet energy resolution (*5D PFA*)**
- **Example: IDEA fiber dual-readout hadronic calorimeter**
 - 50ps time resolution for ~ 2 cm depth segmentation
 - $t = L_1/c + L_2/(c/n)$, with $n=1.46$
- **Fast timing can also provide ToF for LLP and PID, and BIB suppression at muon colliders**



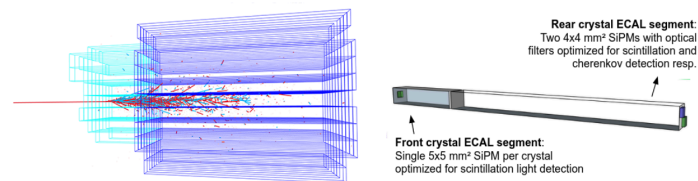
Dual Readout in the IDEA Detector

- IDEA design: crystal ECAL + sampling fiber HCAL
- Timing: 30 ps (20 ps with CMS MTD-style LYSO layers)
- High granularity up to **1.6M readout channels**
- Waveform readout, sampling rate up to **GSa/s**
- **Nominal DRO readout strategy:** 2 SiPMs to both collect high S photon count while filtering for C measurement



ECAL

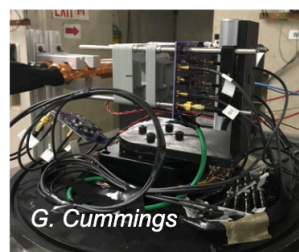
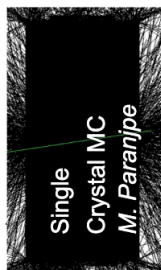
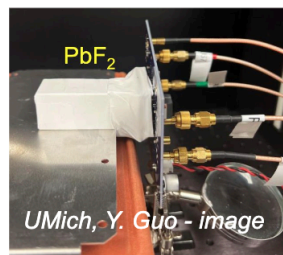
	PWO	BGO	BSO
Density [g/cm^3]	8.3	7.1	6.8
R_M [cm]	2.00	2.23	2.33
X_0 [cm]	0.89	1.12	1.15
λ_I [cm]	20.7	22.7	23.4
Refractive index at 420 nm	2.20	2.15	2.68
Light yield [ph/MeV]	130	7500	1500
Scintillation decay time [ns]	10	300	100
Emission peak [nm]	420	480	470



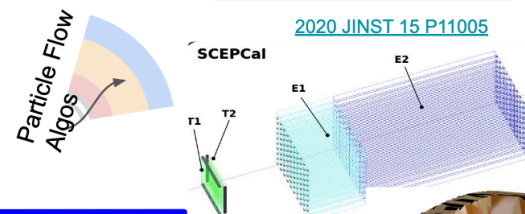
CalVision

CalVision - DR for e⁺e⁻ colliders

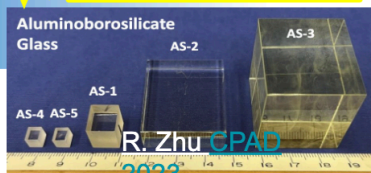
Single crystal +
matrix studies



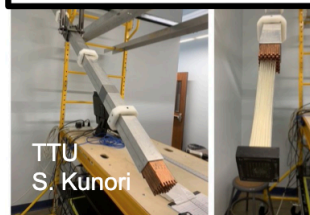
Full detector sim



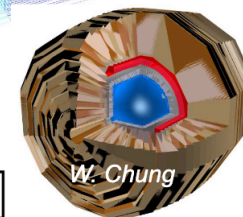
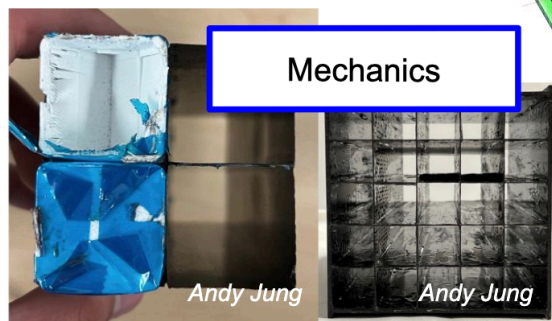
Heavy Glasses
for Homogenous
HCAL



DR Fiber HCAL



Mechanics



Brandeis



UNIVERSITY OF
MARYLAND



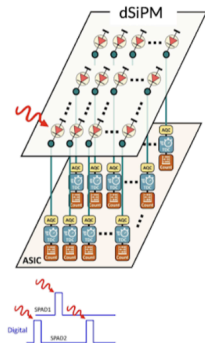
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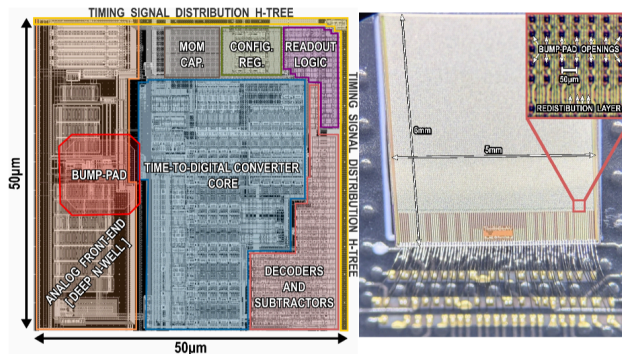
SLAC Technology R&D

TID Technologies in Support of Calorimetry

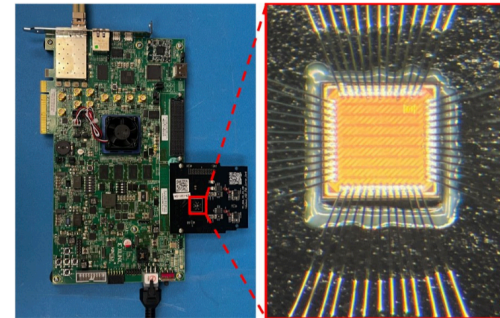
- Sensors:
 - Digital SiPM: for dual readout (crystal or fiber)
 - MAPS: EM calorimeter
- Readout electronics:
 - Fast waveform digitizers: coupled to analog SiPM for dual readout processing
 - Sub-10ps TDC (4D tracking): for timing measurements
- On-chip information extraction (w/ AI/ML)
 - High-level Synthesis: semi-reconfigurable logic with dynamic weights
 - Rad-hard eFPGA: fully **reconfigurable** logic



Digital SiPM:
Fast Timing and
Low Power

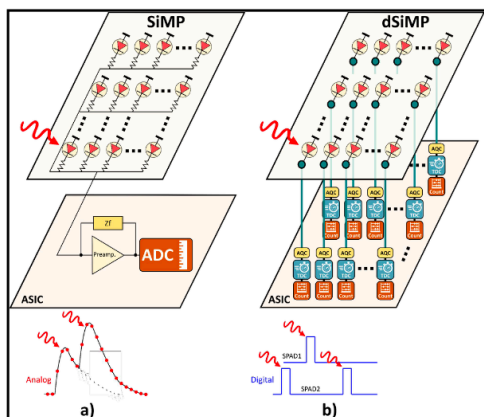


Low Jitter TDC Circuit:
Sub-10 ps TDCs for Particle
4-D (or 5-D) Tracking



Embedded FPGA:
Reconfigurable logic for
dynamically changing
sensors and algorithms

A New Approach: Next-gen dSiPM with 3D-stacked semiconductor imaging technology

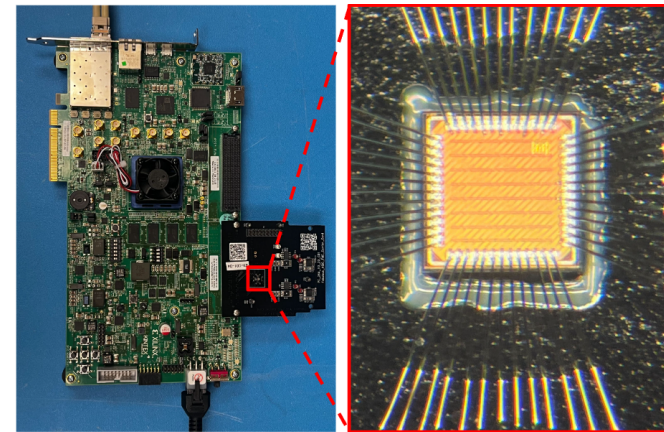
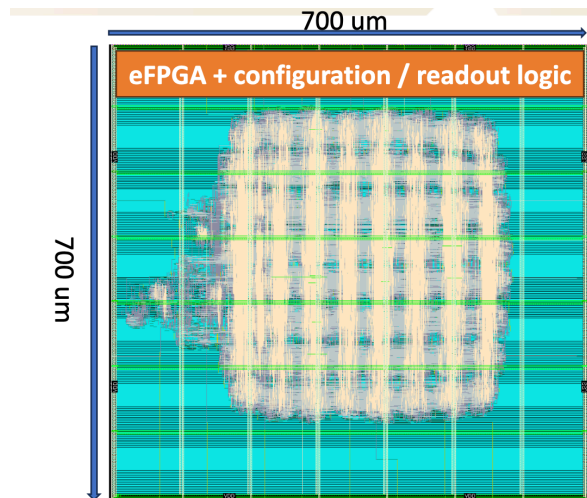


- Develop a fully-digital approach based on digital SiPM 3D stacked to a dedicated front-end ASIC incorporating high-precision TDCs for $\sim 10\text{ps}$ time-tagging and counters for energy measurements
- Unlike conventional SiPMs, in the dSiPM every SPAD microcell provides a separate output that can be treated by digital circuits: the signal amplitude is recovered by counting the number of triggered cells while the timing information is extracted from digital pulses employing high-precision TDCs.
- **Operating every SiPM microcell digitally and in-parallel offers many advantages:**

- **lower power consumption** as power hungry analog front-end and high-speed ADCs are avoided
- **lower data rates** as amplitude and time information are directly extracted in presence of the signal
- separate access to every microcell allows the use of the **fine spatial (tens of μm) information** as well as disabling of “hot” cells that exhibit elevated dark count rates, **improving noise performance**
- the all-digital system is robust and requires **minimal calibration**, making it **easily scale from a prototype to large systems**, a step often not trivial for high-precision analog systems

eFPGAs

- “Embedded” FPGAs: reconfigurable logic in ASIC design for configurability ease of FPGA with low power/footprint/rad-hardenability of chip
- Open-source frameworks (eg. FABulous, openFPGA) lower barrier to entry for ASIC design
- SLAC designed prototype eFPGAs with FABulous and taped out in 130nm & 28nm CMOS on TSMC MPW: proof-of-concept for open-source design tools for eFPGAs
 - Very small logical capacity i.e. “tiny ML”: < 500 look-up tables (LUTs), 0 digital signal processors (DSPs)

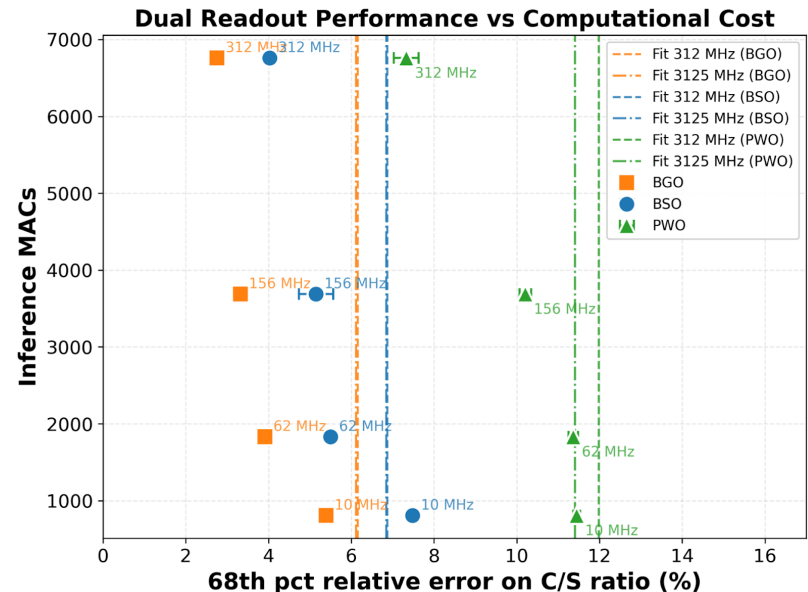
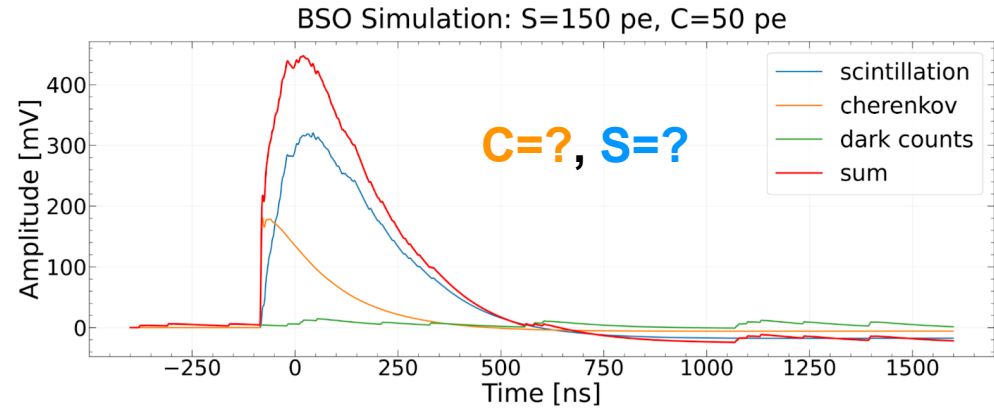


ML-Enhanced DRO Readout

[2604.26090]



- Reading out full waveform allows for leveraging emission time distribution differences in C/S, but generates very high data rate
 - Existing C/S decomposition done with template fitting: too slow for online use
 - ML for real-time/front-end waveform analysis to extract and transmit C/S values only?
- ML solution: one-pass regression with 3-layer NN network
 - Resolution greatly improved across 1-30 GeV incident energy, outperforming template fit approach at 10x lower sampling rate
 - 6% error at 30K LUTs and no DSPs



ML-Enhanced DRO Readout

[2604.26090]

SLAC

- Reading out full waveform allows for leveraging emiss differences in C/S data rate

FCC Week Early Career Award Winner!

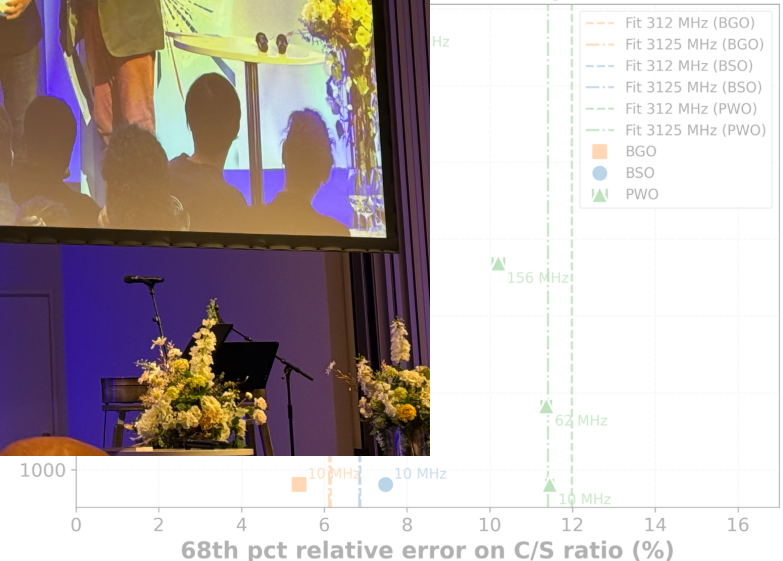
- Existing C/S de template fitting
- ML for real-time analysis to ext values only?
- ML solution: one-p layer NN network
 - Resolution great
 - GeV incident en template fit app
 - sampling rate
 - 6% error at 30K LUTs and no DSPs



BSO Simulation: S=150 pe, C=50 pe



Fit vs Computational Cost

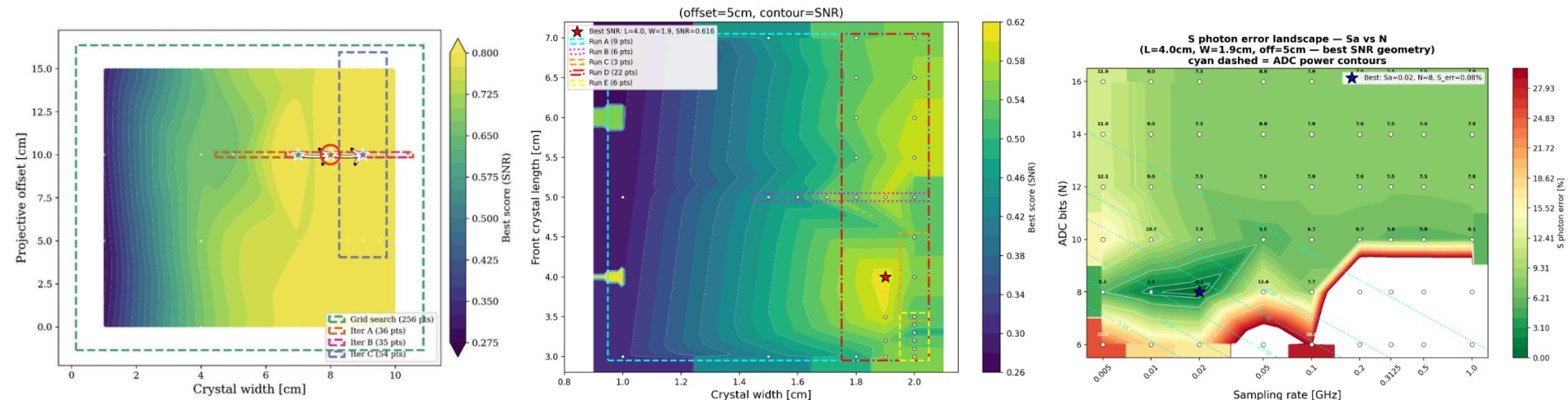
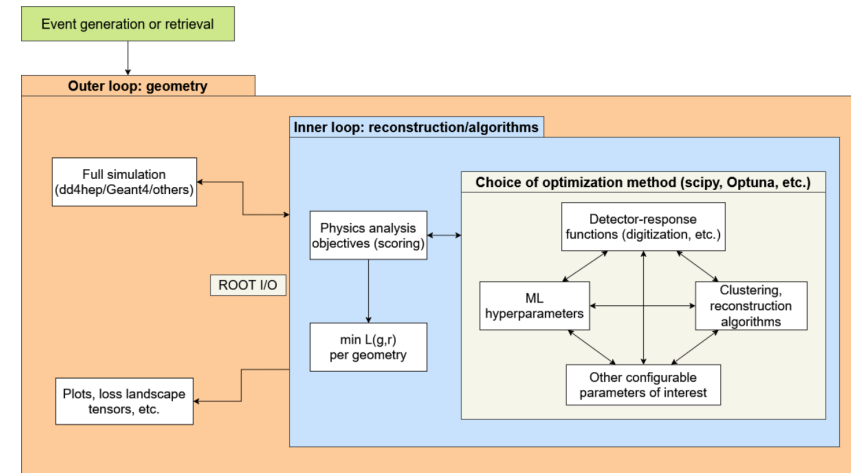


ML-Based Detector Optimization

[2604.21804]

SLAC

- Vertically Integrated Bilevel geometry, Reconstruction, And TDAQ Optimizer (**VIBRATO**): first agentic-assisted framework for ultra-high dimensional vertically integrated optimizations end-to-end (e.g. data to analysis metric)
 - Two loops: outer (geometry) and inner (reconstruction)
- Huge boost for time-to-result:
 - Evaluation of many detector aspects against competing optimization criteria
 - Easy spin-off of detector concepts



16 July 2026

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Looking Ahead

Phase Ia: Tool Development

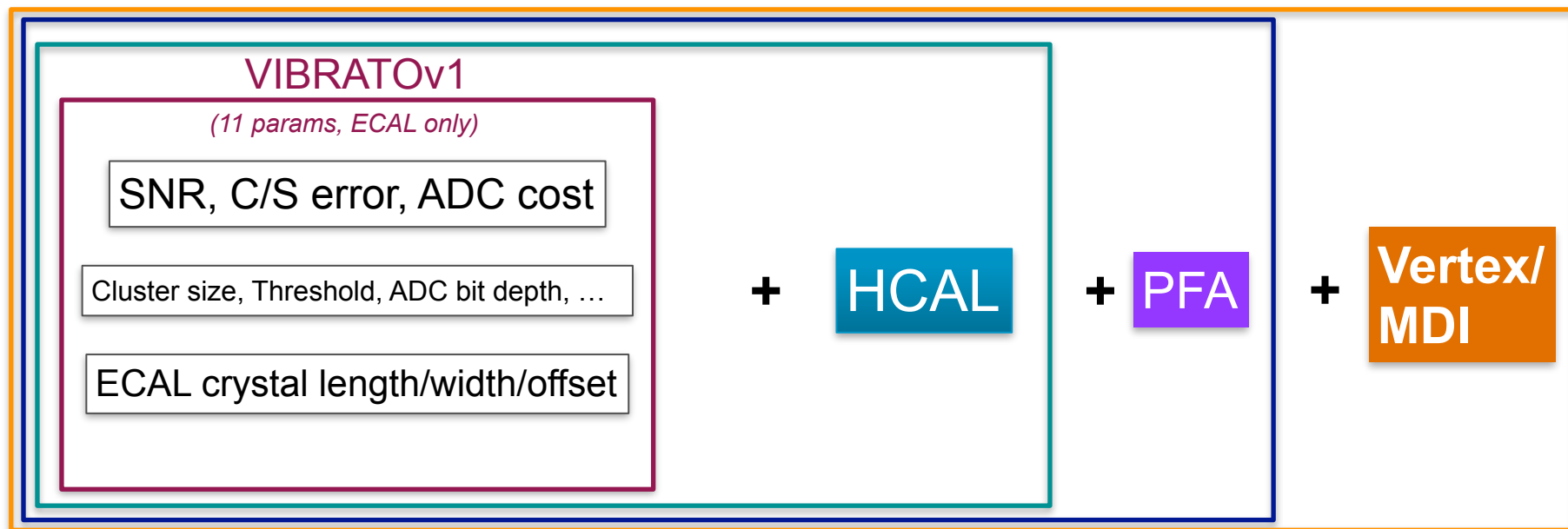
⇒ **First determine: what is possible technologically?**

- Strong efforts across SLAC with synergistic use of funding/resources
- Readout: dSiPM **or** front-end waveform analysis/timing extraction (eFPGA, FPGA, ...)

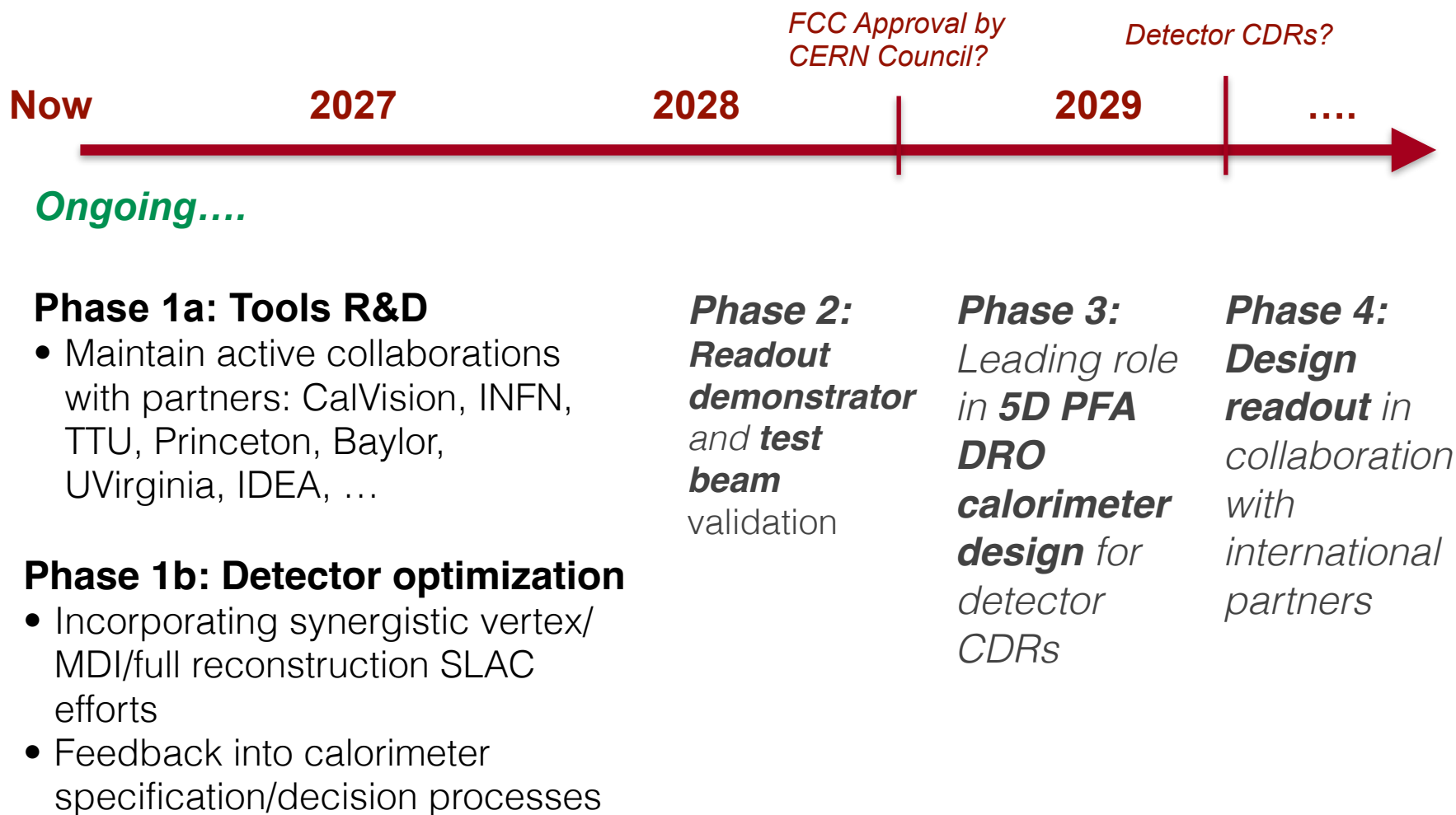
Electronics	dSiPM LDRD pending	Precision timing	eFPGA ECA, LDRD [2404.17701]	Analog KA29
AI/ML	Front-End ML ECA, LDRD	ML Detector Optimization ECA, US HFCC	PFA	
Simulation		Key4HEP		

Phase 1b: End-to-End Design

- Many key detector aspects still outstanding
 - Will the readout be trigger-less?
 - What is the bunch crossing rate? 20 ns, or as low as 1.25 ns (!)
 - Calorimeter: power budget? sampling rate? crystal type? TDC or waveform-based readout?
- Continue developing & employing **VIBRATO** to rapidly incorporate advances in simulation, readout tech, reconstruction algorithms, other subsystems towards **full detector design input**



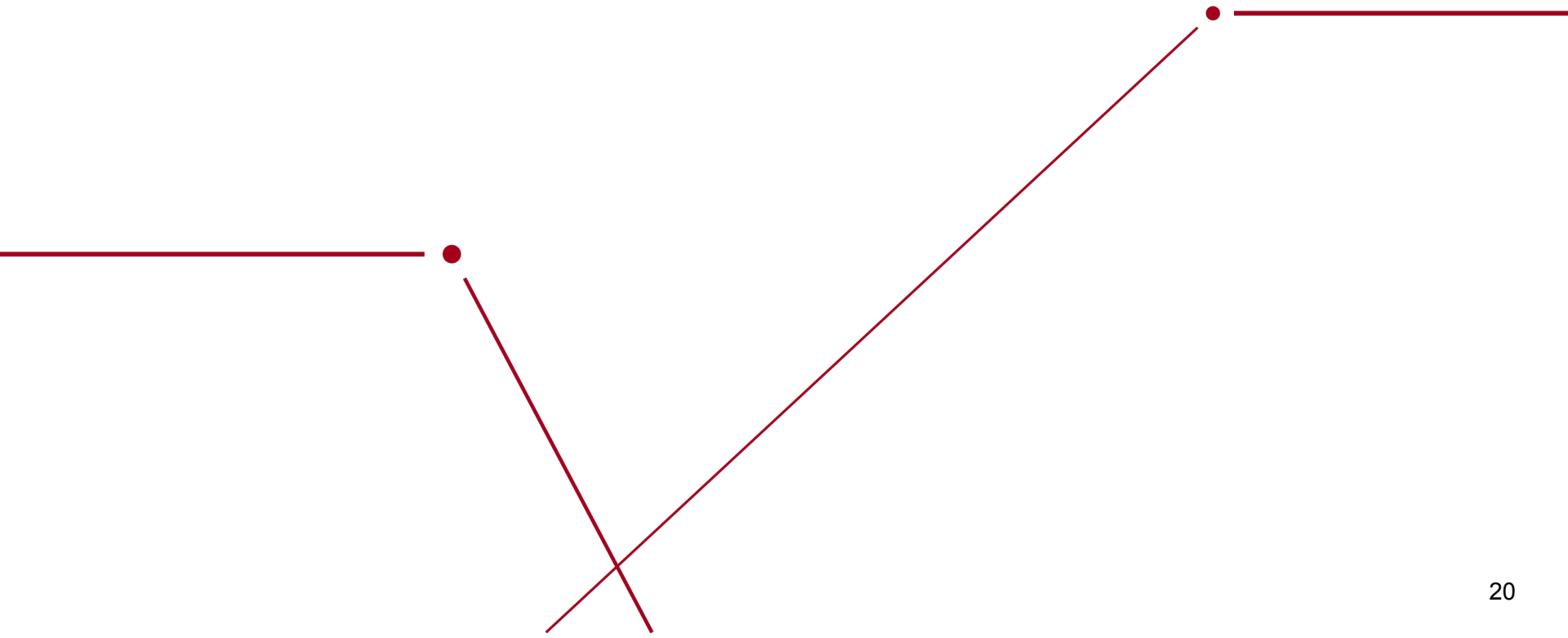
Timeline



Conclusions

- SLAC playing leading role in a variety of components needed to deliver high performance calorimetry with novel technology for FCC
 - Proposed objectives:
 - Design the DR calorimeter readout with international partners optimizing for extraction of high quality physics information
 - dSiPM || front-end AI/ML (eFPGA, FPGA, ...)
 - Optimize in context of full detector, connecting to related SLAC expertise in vertex/MDI and reconstruction
 - Leading role in 5D/PFA DRO calorimeter design for FCC detector CDRs
- SLAC key factors:
- Vast physics experience in calorimeter readout, jet reco, etc. from ATLAS & more
 - TID expertise and co-design
 - Several years of strategic thinking on calorimetry involvement

Backup



IDEA Crystal ECAL Readout Options

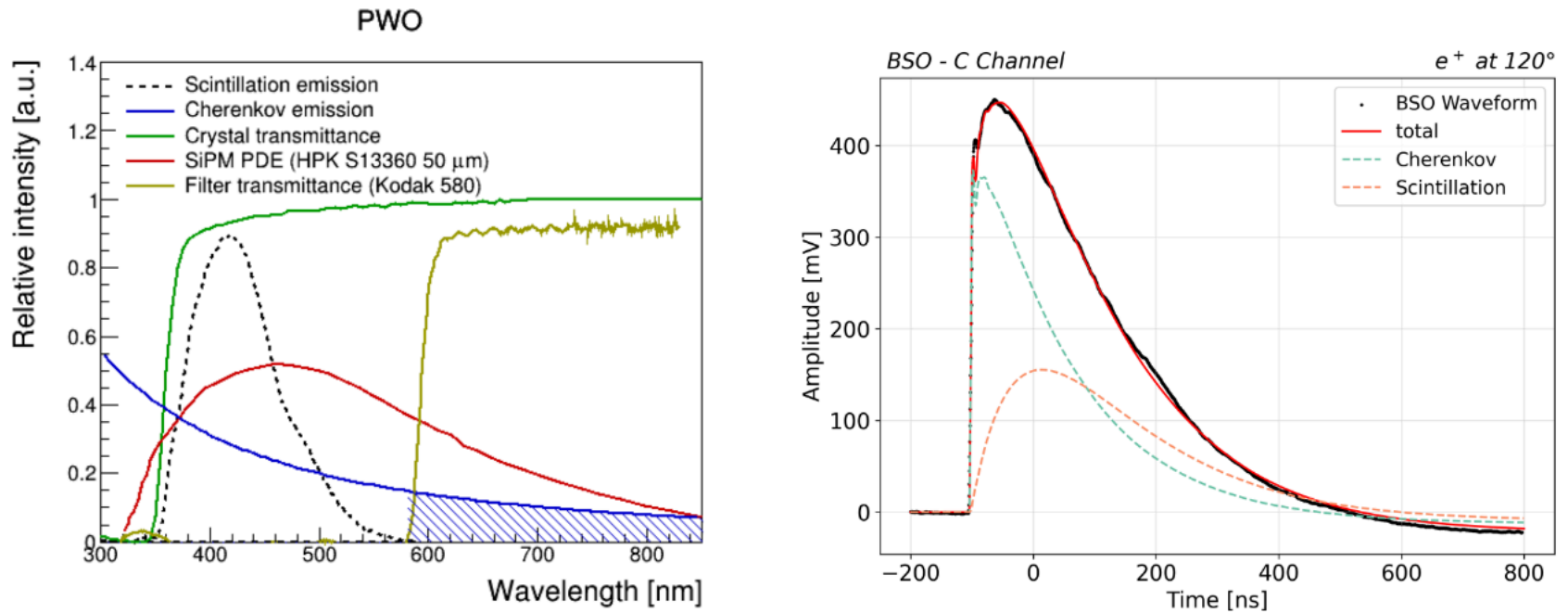
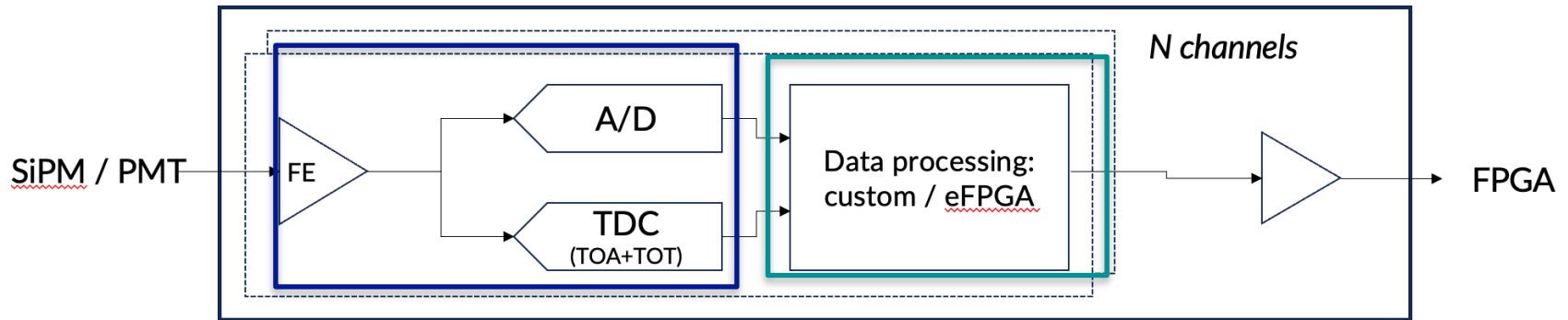


Figure 23: Strategy for implementation of dual readout in PWO crystals (left), which consists in filtering out scintillation photons based on wavelength discrimination, and in BSO crystals (right) which consists in isolating Cherenkov light based on the time distribution of optical photons (prompt for Cherenkov and with a long decay for scintillation) [32]

Calorimeter Readout Demonstrator

Block diagram of readout ASIC for Calorimetry



- Option to leverage **AUREIUS** (part of SLAC Microelectronics Center MEERCAT) to design fast A2D with DRO specs

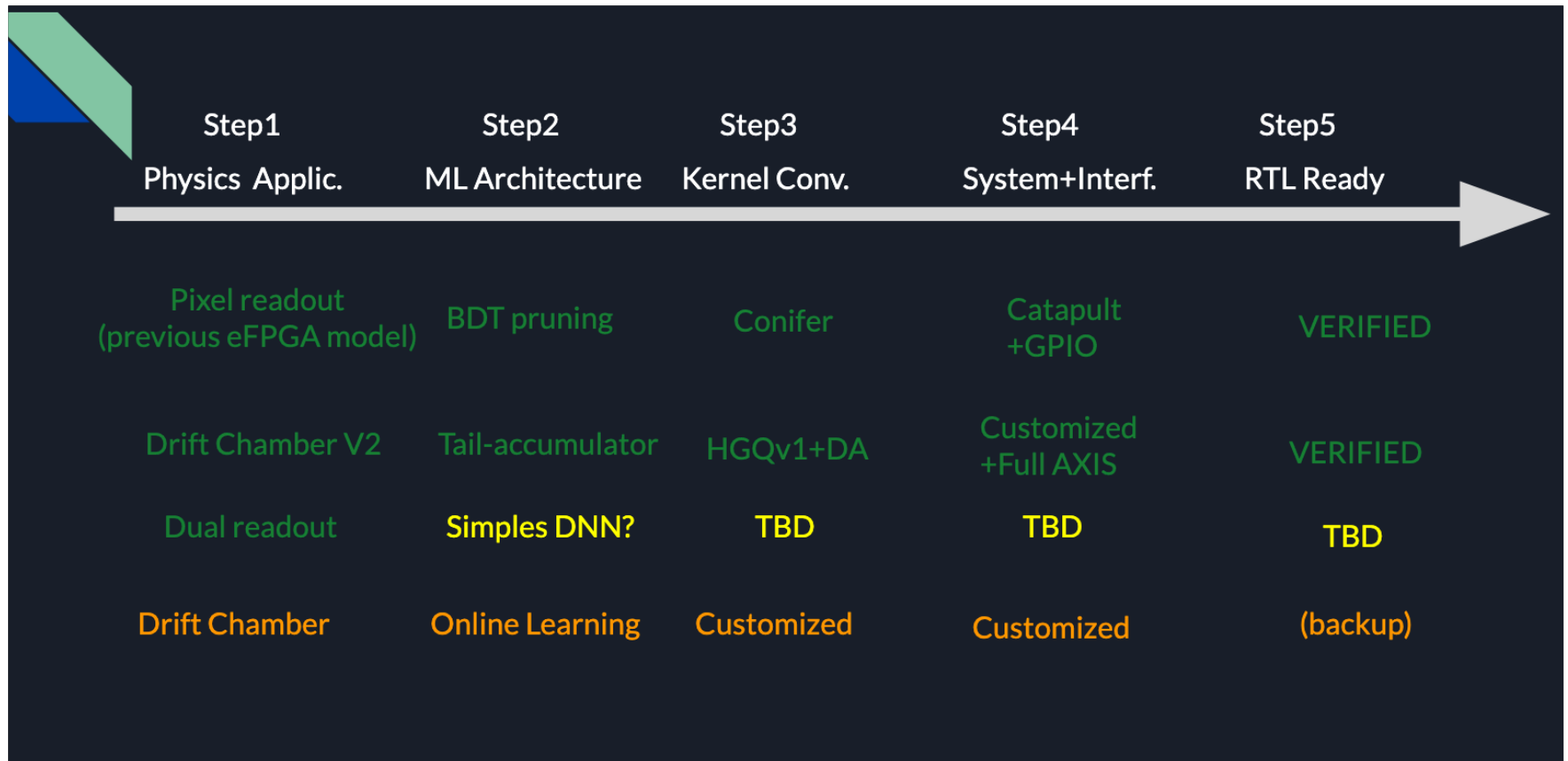
FCC Detector Case

- *Ongoing*: compress for LDRD eFPGA
- ➔ Key checkpoint: is physics performance good enough to test demonstrator with LDRD

- Currently understanding constraints/TMR-G/openFPGA interface
- ASIC design starts FY27
- ➔ Key checkpoint: how much more logic can we handle in an ASIC die with reasonable power? (Funding for v2 eFPGA?)

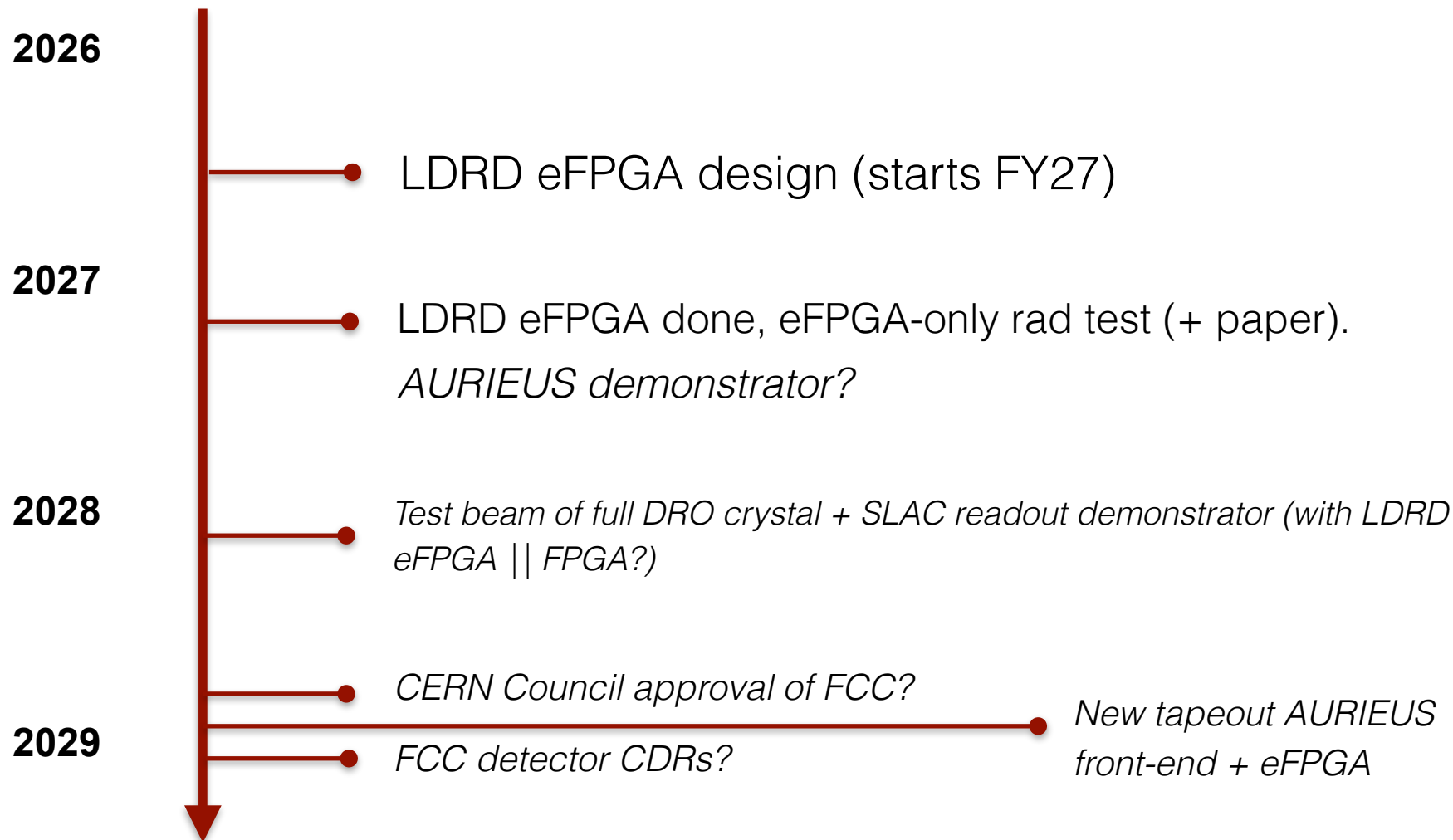
LDRD eFPGA

eFPGA/FCC Codesign



Q. Liu

Timeline

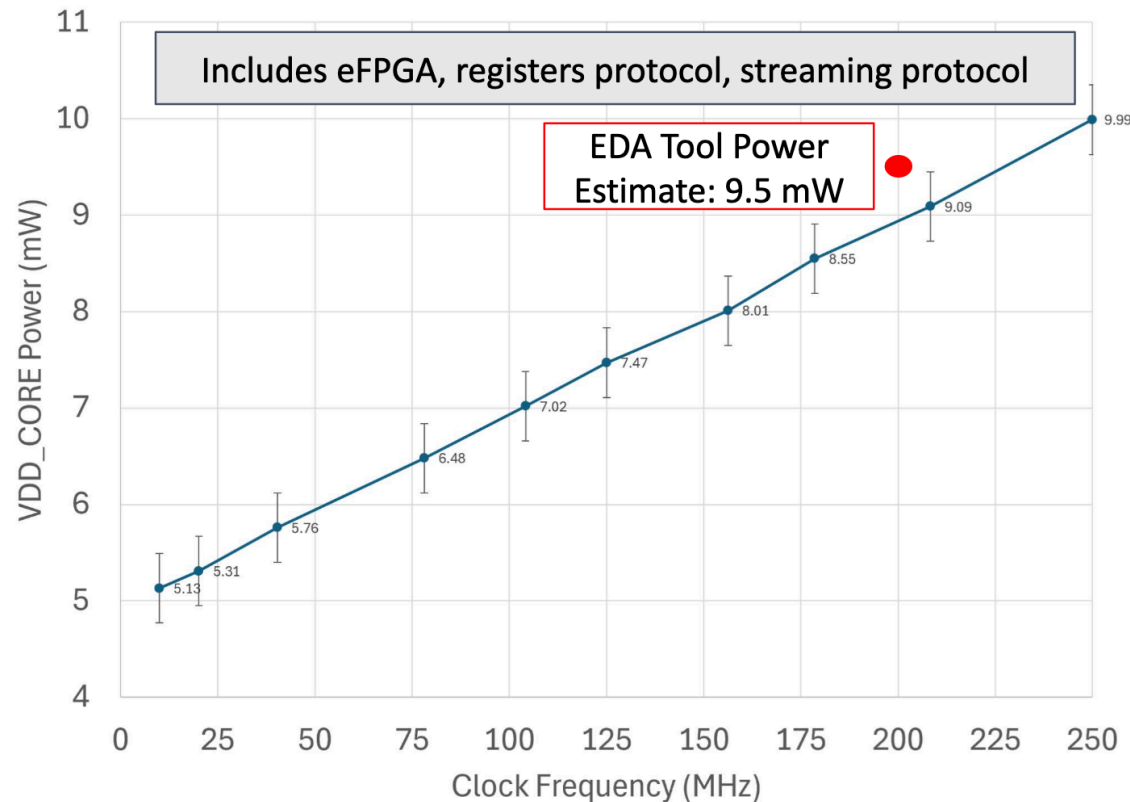


Power Consumption

- E.g. FCC-ee electronics will need extremely low power density
 - [Vertex - O\(20 mW/cm²\)](#)
 - [Tracker - O\(200 mW/cm²\)](#)

Assuming 50 MHz eFPGA clock and current design:

- EDA tool Power Estimate of eFPGA only:
 - 3.7 mW
- **1.8W/cm²**
 - = 3.7mW/0.002025cm²
- Need to aggressively explore power optimization strategies in a proper frontend ASIC design
 - Not just drag and drop open source code with EDA tool auto-router



7

L. Ruckman