Cadence Virtuoso Report Group B

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- Cadence Handson Summary
- Additional Material

Introduction to Cadence Hands-on

- Cadence one of “Big Three” Electronics Design Automation (EDA) tools provider globally
- EDA tools interface foundry processes and MAPS designers
- Cadence allows you to discover “unknown unknowns” of a circuit
- …Cadence itself has many “unknown unknowns” to designers, regarding EDA tools
- Hands-on exercise consisted of 6 exercises

Ideal models

Ideal Operational Amplifier

Ideal Charge Sensitive Amplifier

Ideal CSA with feedback resistor

Transistor based

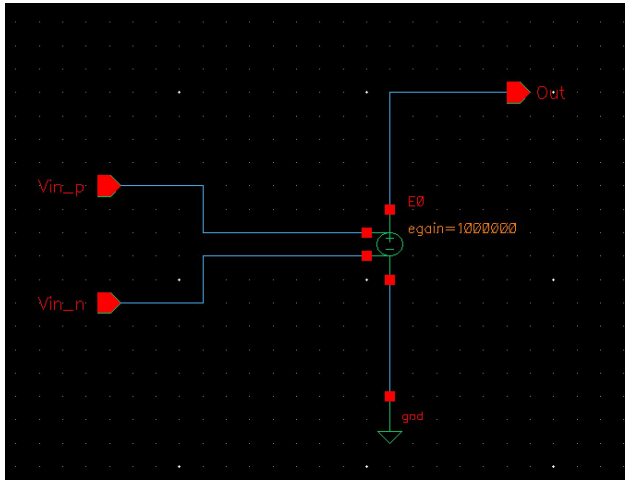
Transistor design of a simple CSA Amplifier

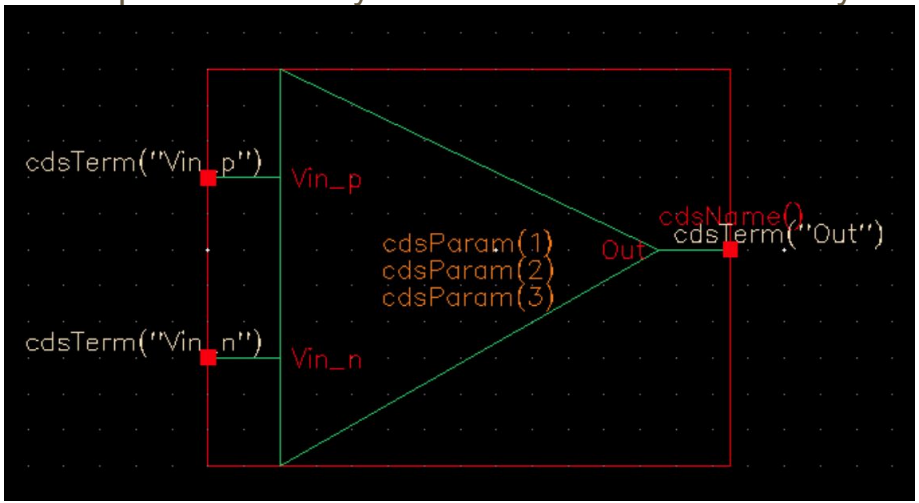
Full CSA simulation

Layout of the CSA Amplifier

Step 1: Ideal Operational Amplifier

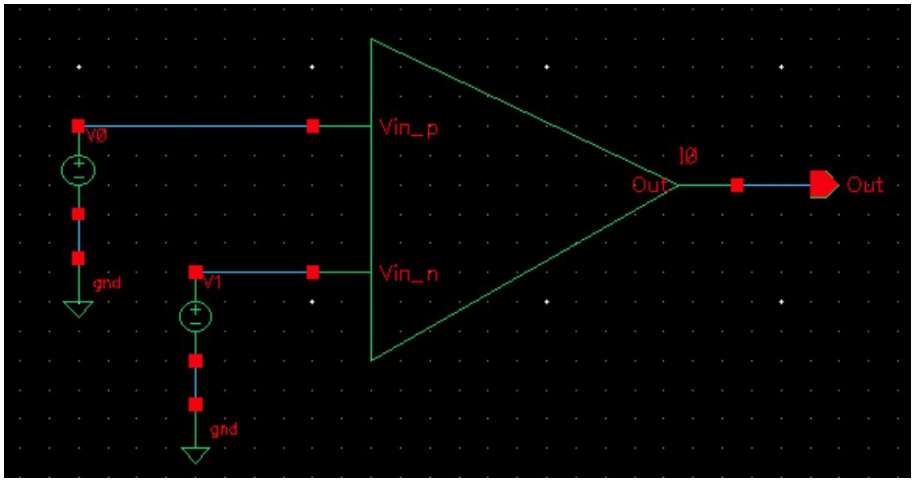
- Ideal Operational Amplifier
  - Theoretical electronics device which amplifies difference between two input voltages
  - Key feature infinite gain, infinite input impedance, and zero output impedance
- Main learning goals: learning how to use Virtuoso
  - step a: create a ideal op-amp
  - step b: define a symbol to reuse it hierarchically



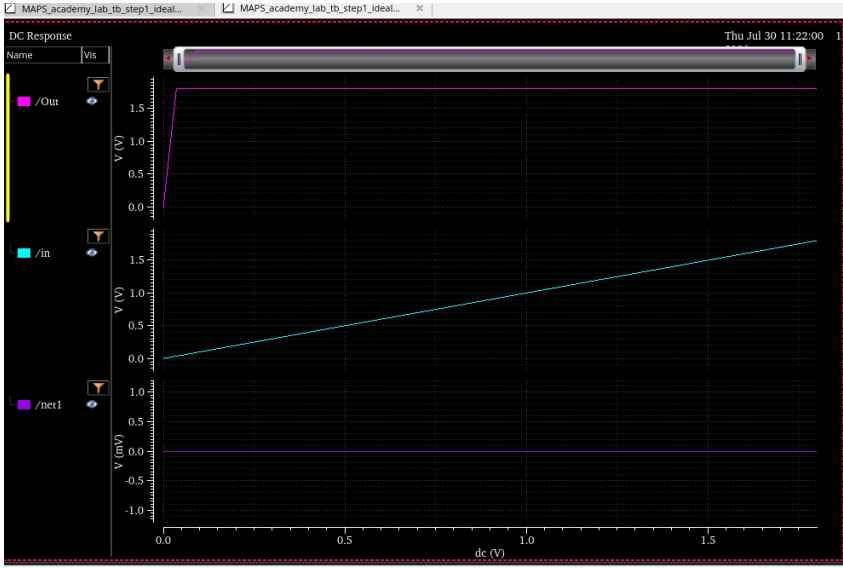


Step 1: Ideal Operational Amplifier

- step c: create a test bench by adding DC source



- step d: run simulation to characterize op-amp by sweeping dc voltages

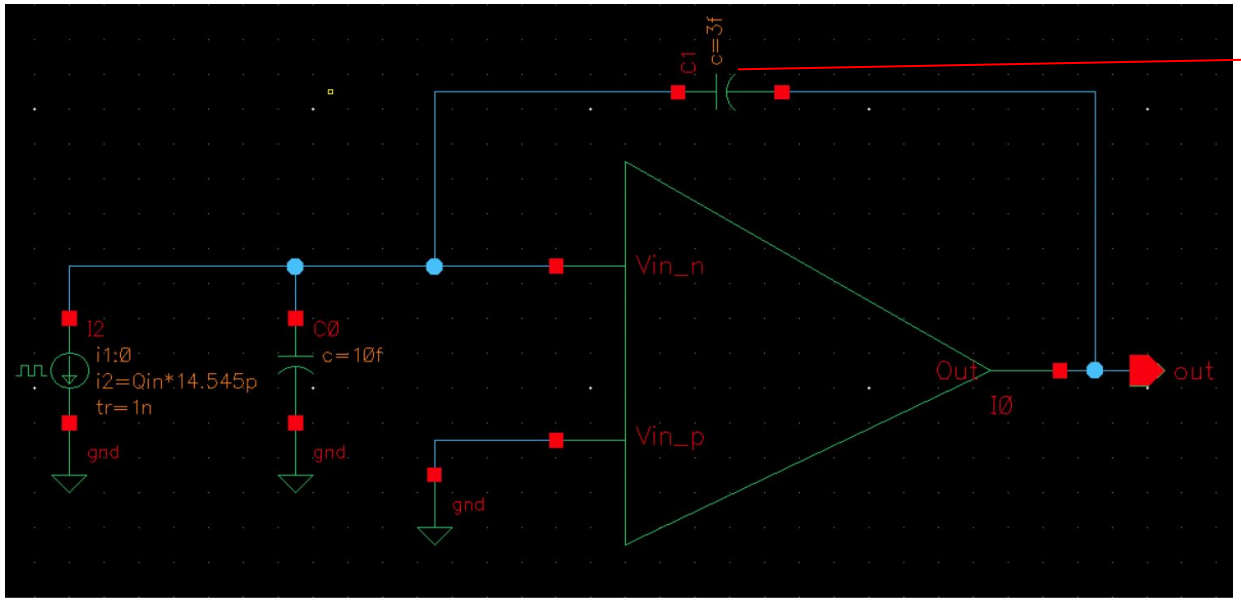


Rest of the hands-on session follows very similar pattern with designing something, creating a symbol, using it downstream in test bench simulation and characterizing properties

Step 2: Ideal Charge Sensitive Amplifier

Goal: to build an ideal charge sensitive amplifier

- A specialized circuit that converts an input charge pulse into a proportional voltage output
- Took the ideal op-amp and added a feedback capacitor



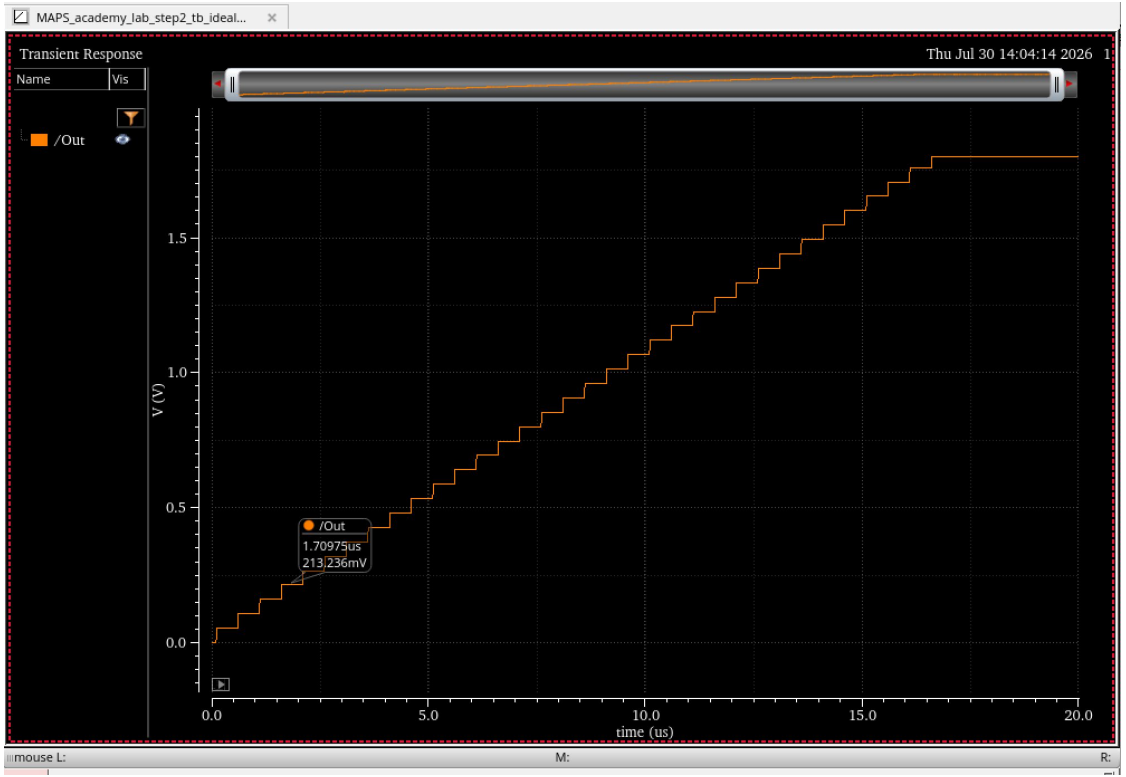
Feedback capacitor

$V_{out} = -Q_{in}/C_f$

Feedback pins the input node near 0V, so no charge can accumulate on C0, it's all forced onto C1 instead, which is why the output only depends on C1.

Step 2: Ideal Charge Sensitive Amplifier

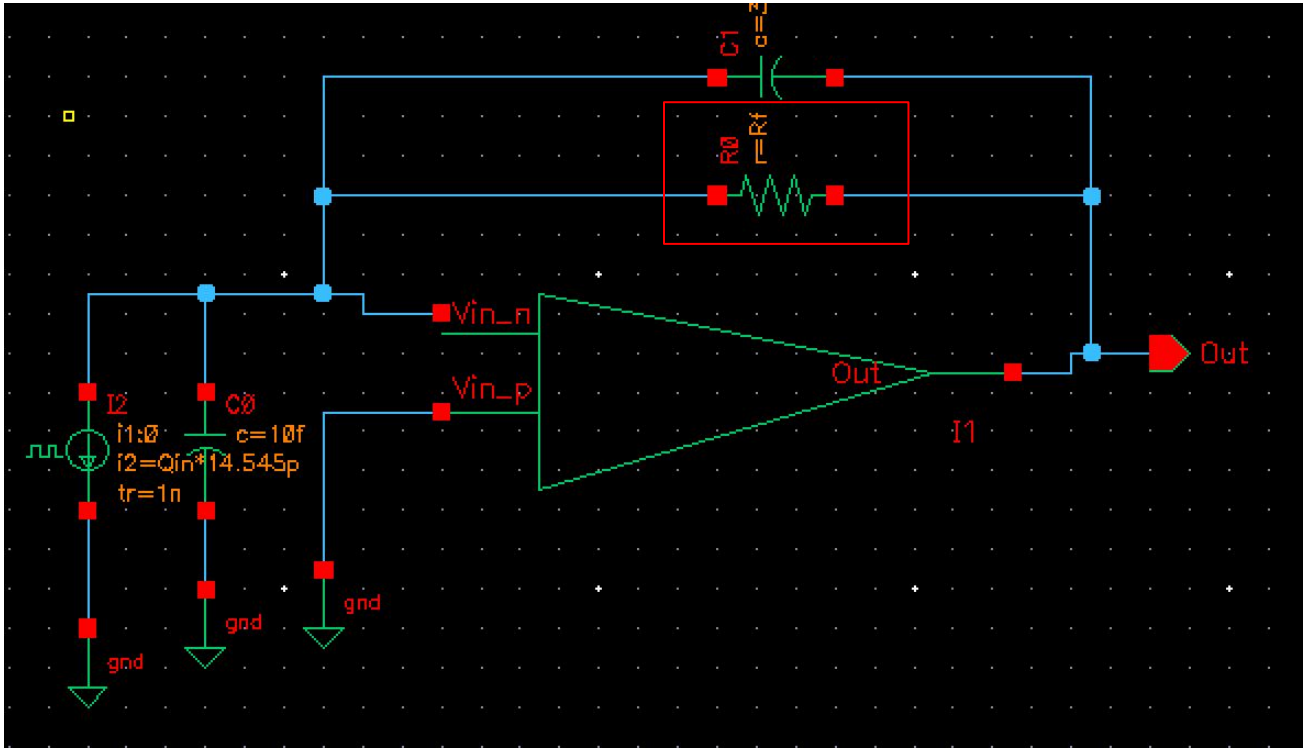
- Ran simulation of ideal CSA to look at the behavior of the circuit over time



- Each pulse has 1ns rise time
- After 1ns output voltage jumps by constant amount as CSA integrates per pulse
- No reset in circuit, output voltage continuously rising

Step 3: Ideal CSA with feedback resistor

Goal: to build an ideal charge sensitive amplifier with feedback resistor



$$V_{out}(t) = \frac{Q_{in}}{C_f} e^{-t/\tau}$$

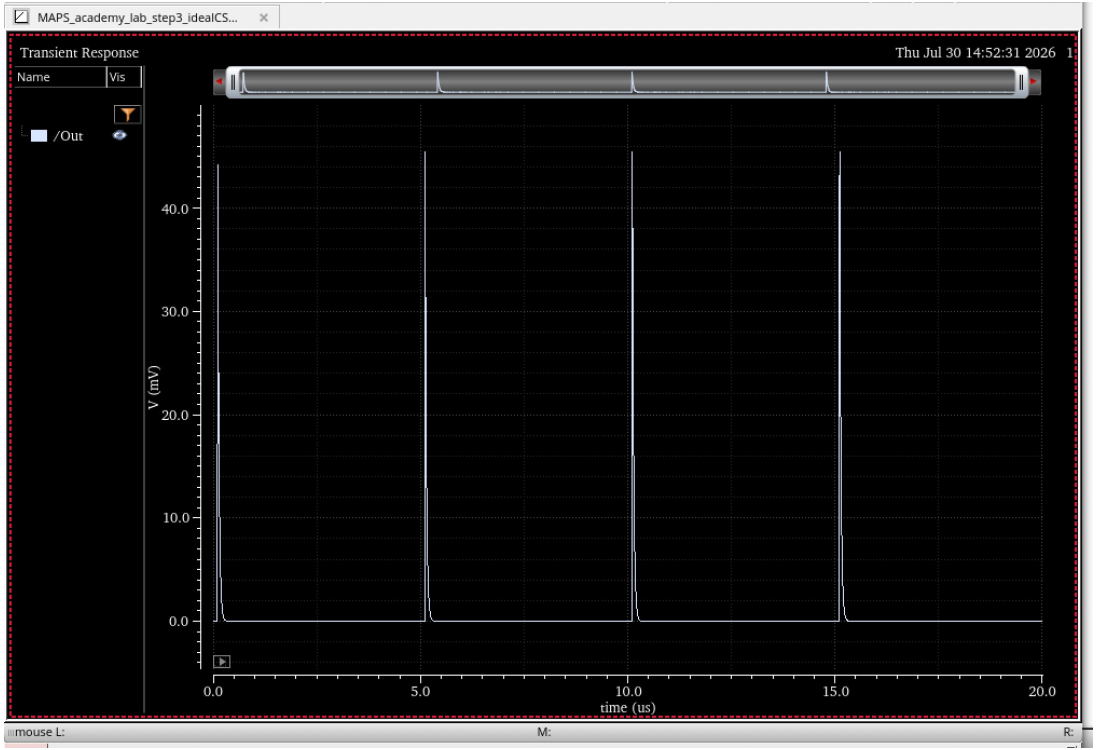
$$\tau = R_f C_f$$

Feedback resistor plays an important role in regulating Vout

Step 3: Ideal CSA with feedback resistor

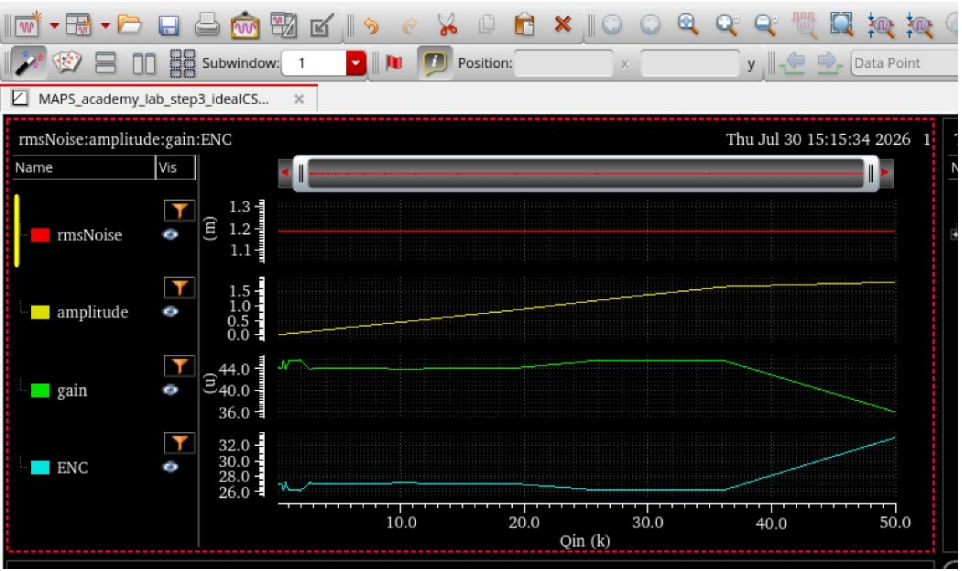
Qin=1000, Rf=10M

- Rf now resets output voltage per pulse
- Transient voltage shows sharp rise and exponential decays



Step 3: Ideal CSA with feedback resistor

Varying Qin, Rf=10M

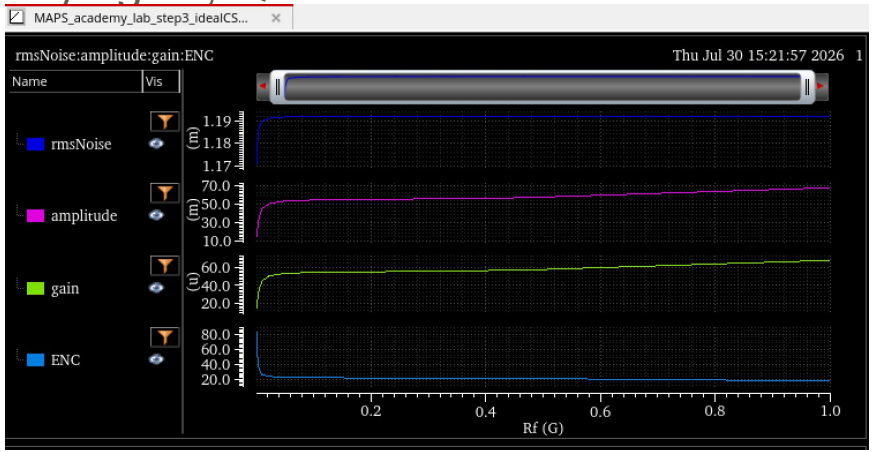


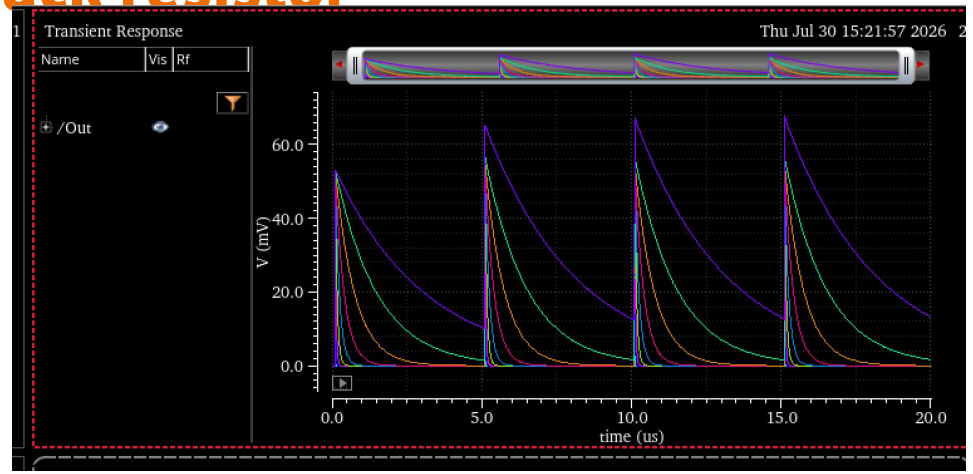
After a certain increase in Qin, gain decrease, ENC increase due to saturation of Vout

- Signal processing parameters defined
  - **rmsNoise**: sqrt of output-referred noise power spectral density 1Hz to 1GHz
  - **Amplitude**: ymax(VT("/out")) - ymin(VT("/out")))
  - **Gain**: amplitude/Qin
  - **Equivalent noise charge (ENC)**: rmsNoise/gain
    - Main figure of merit
    - How much input charge would it take to produce an output fluctuation equal to the noise floor?

Step 3: Ideal CSA with feedback resistor

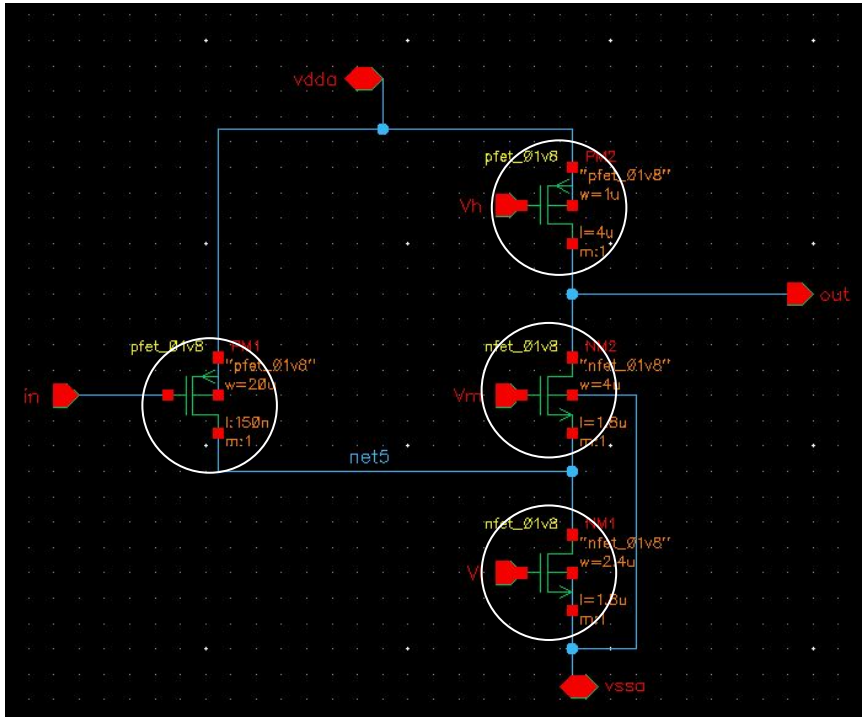
Varying Rf, Qin = 1000





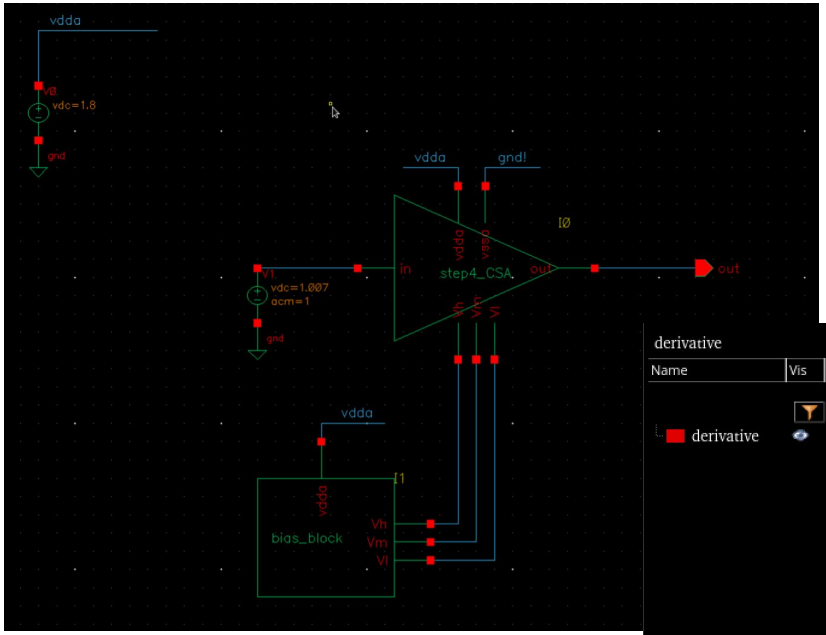
- Large Rf lower equivalent noise charge (thus better)
- But large Rf, slower discharge, more impacted by pileup

Transistor based - Simple CSA Amplifier

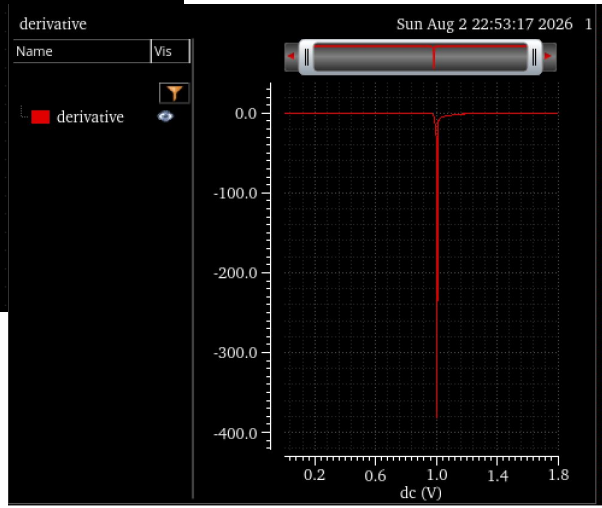


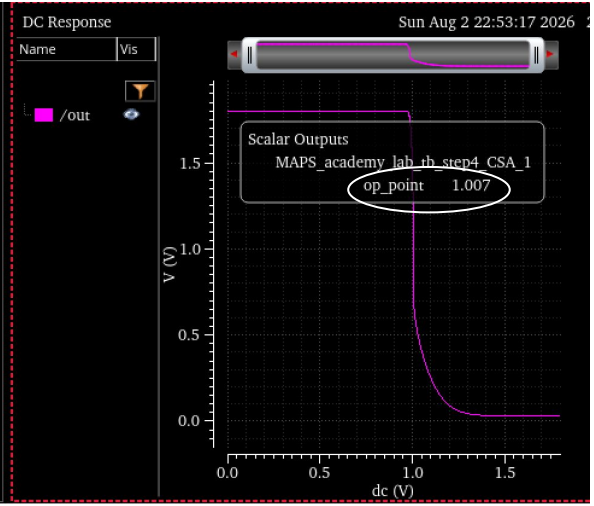
- Transistor-level CSA using Sky130 MOSFETs

Transistor based - Simple CSA Amplifier

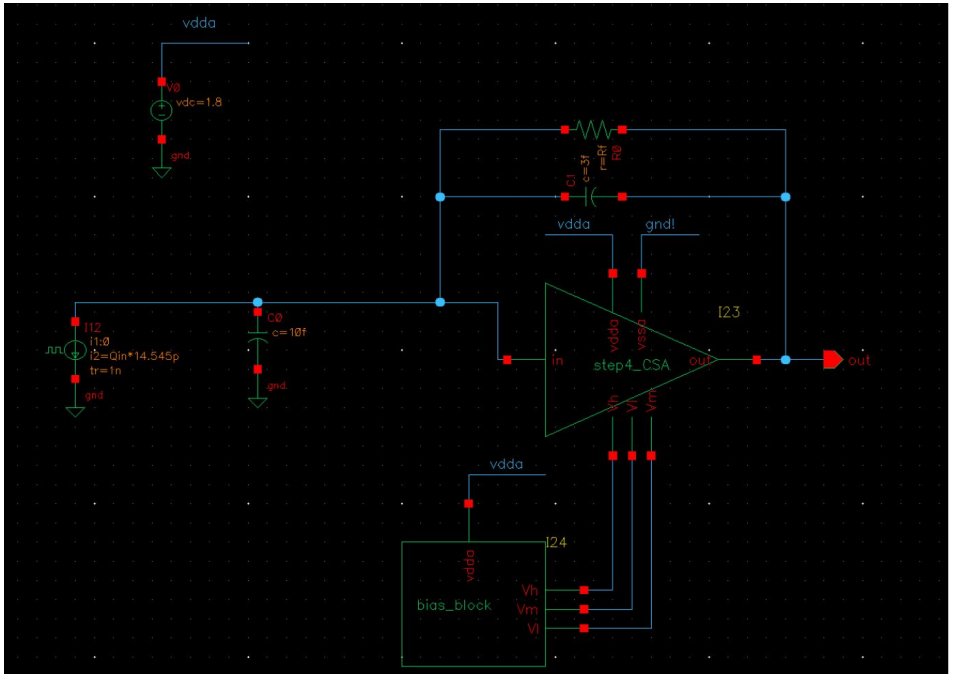


- Transistor-level CSA using Sky130 MOSFETs
- Add the bias block and perform DC analysis
- Optimal DC bias point corresponds to the maximum small-signal gain.
- The highest gain is identified from the maximum slope of the DC transfer characteristic.

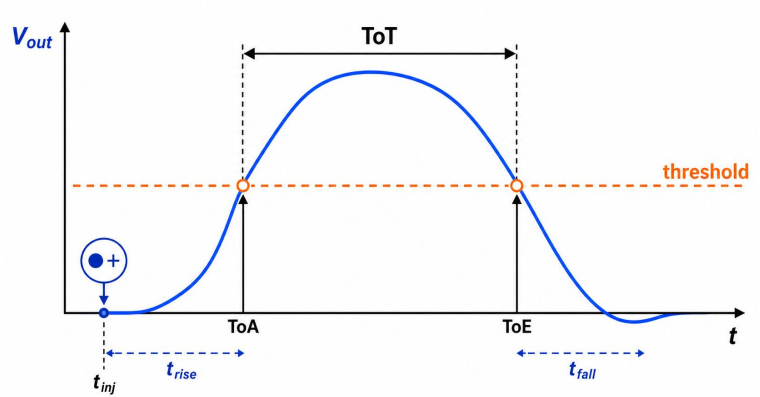




Transistor based - Full CSA simulation

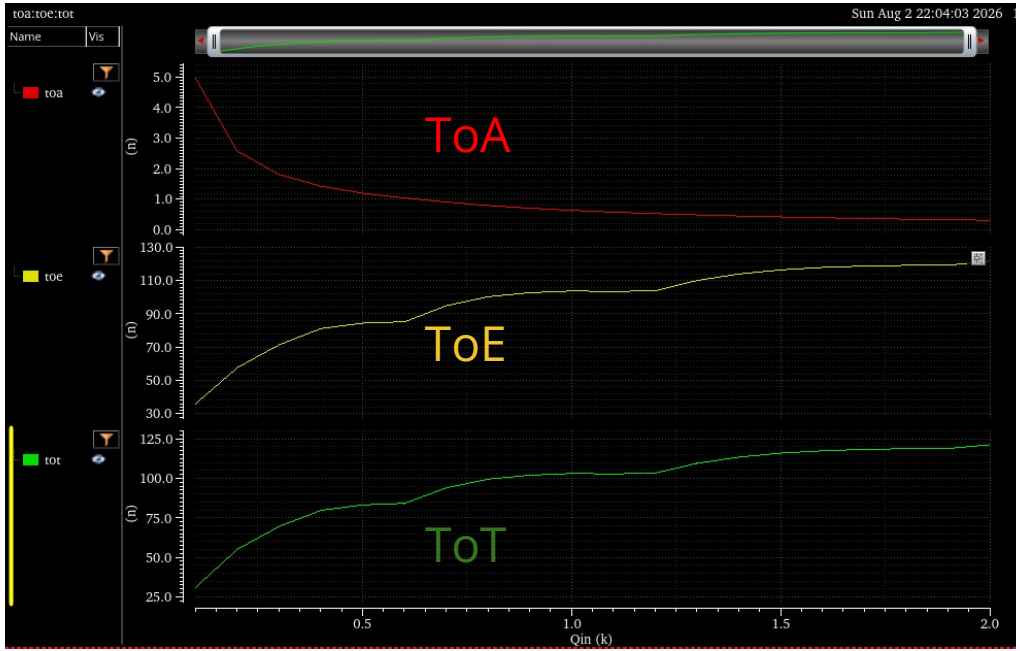


- Replace the ideal op-amp with the transistor CSA
- Add the bias block and reuse the feedback network
- Sweep Qin = 100–2000 e^- (step 100 e^-)
- Measure ToA, ToE and ToT



- ToA: first threshold crossing; sets time-walk behavior.
- ToE: falling-edge crossing after the pulse recovers.
- ToT = ToE − ToA: proxy for pulse amplitude / charge.

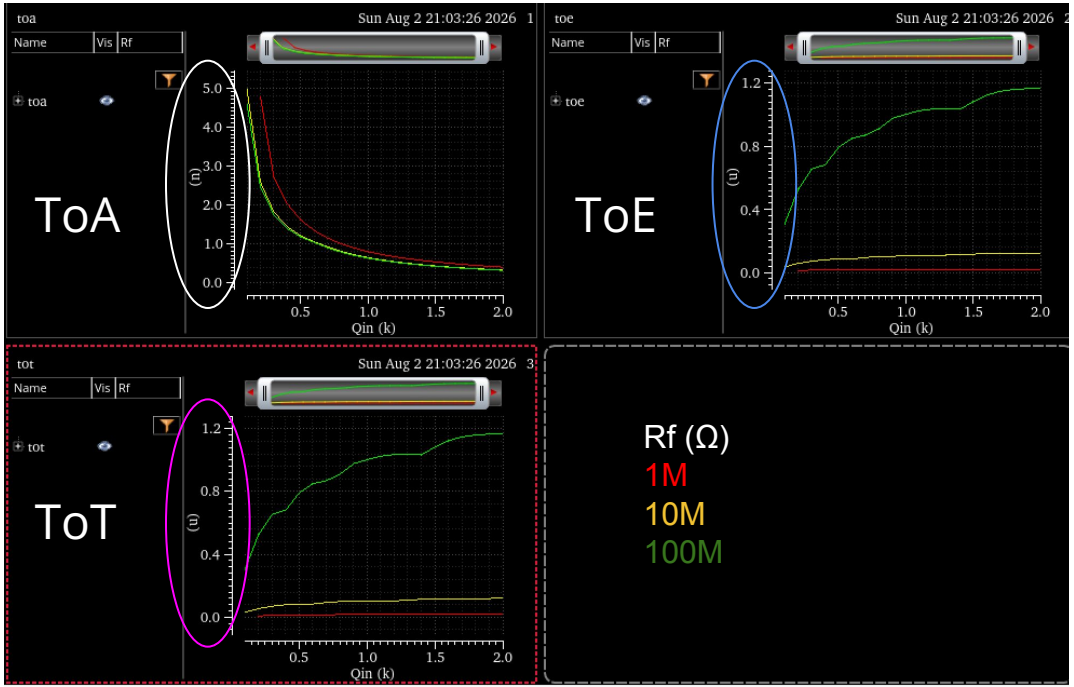
Transistor based - Full CSA simulation



Effect of Injected Charge

- Increasing Qin produces an earlier threshold crossing, reducing ToA.
- Strong ToA dependence at low Qin indicates significant time walk for small signals.
- Larger pulses remain above threshold longer, causing both ToE and ToT to increase.
- At high Qin, the ToT response becomes less sensitive to additional charge

Transistor based - Full CSA simulation



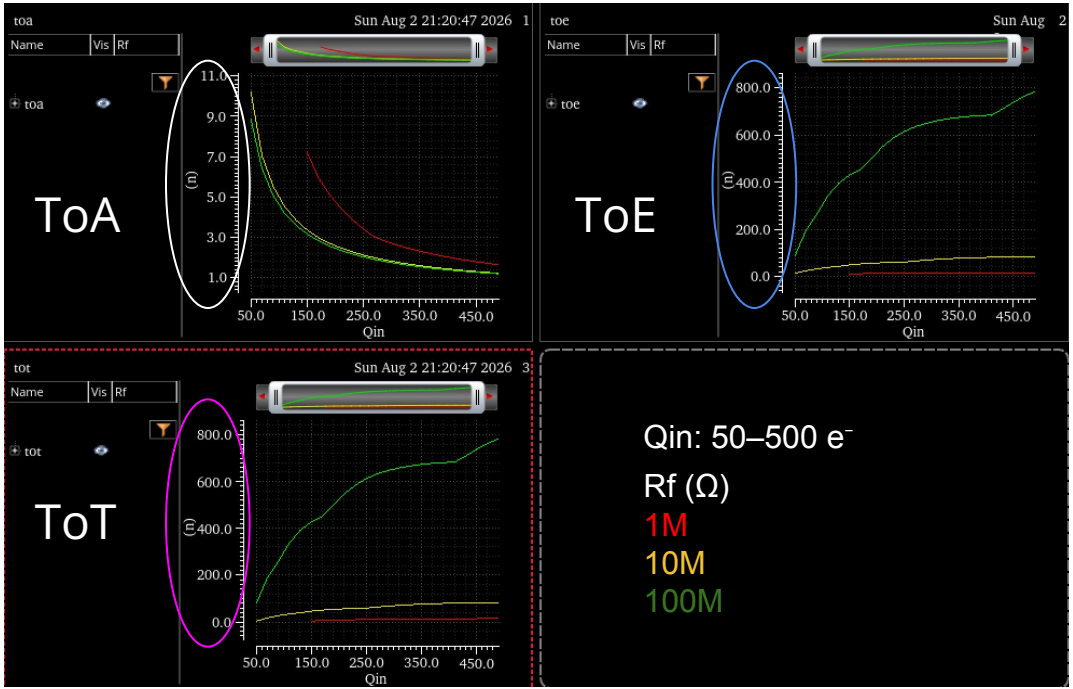
Effect of Feedback Resistance

- ToA changes little with Rf, showing minimal impact on leading-edge timing.
- Increasing Rf delays pulse recovery, resulting in a larger ToE.
- Higher Rf extends the pulse width, leading to a longer ToT.

➔ Low Rf: fast reset and better high-rate performance.

➔ High Rf: longer signal duration but greater pile-up risk

Transistor based - Full CSA simulation

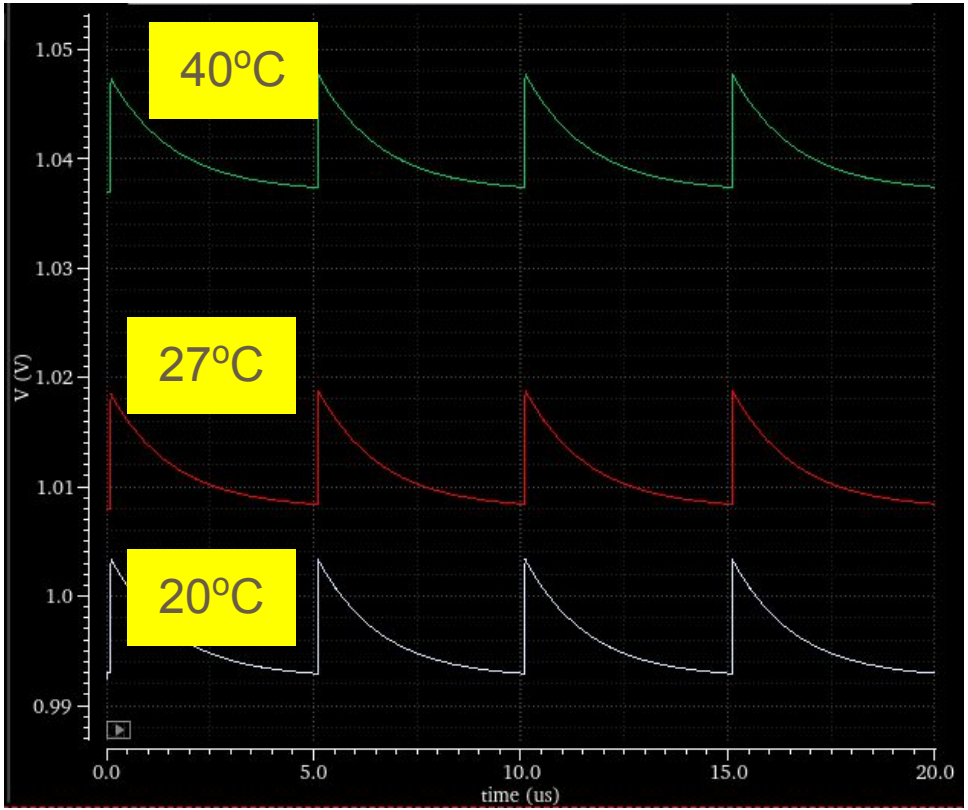


Low-Charge Performance (50–500 e^-)

- Low Qin exhibits significant time walk, as small signals cross the threshold later
- ToT decreases for smaller signals, reflecting the reduced time above threshold
- Higher Rf improves low-charge sensitivity by extending the pulse above threshold
- The low-Qin region defines the practical detection limit of the CSA

Schematic Output Simulation Performance - PVT

Small voltage range in output peaks lead to very strong temperature dependence.

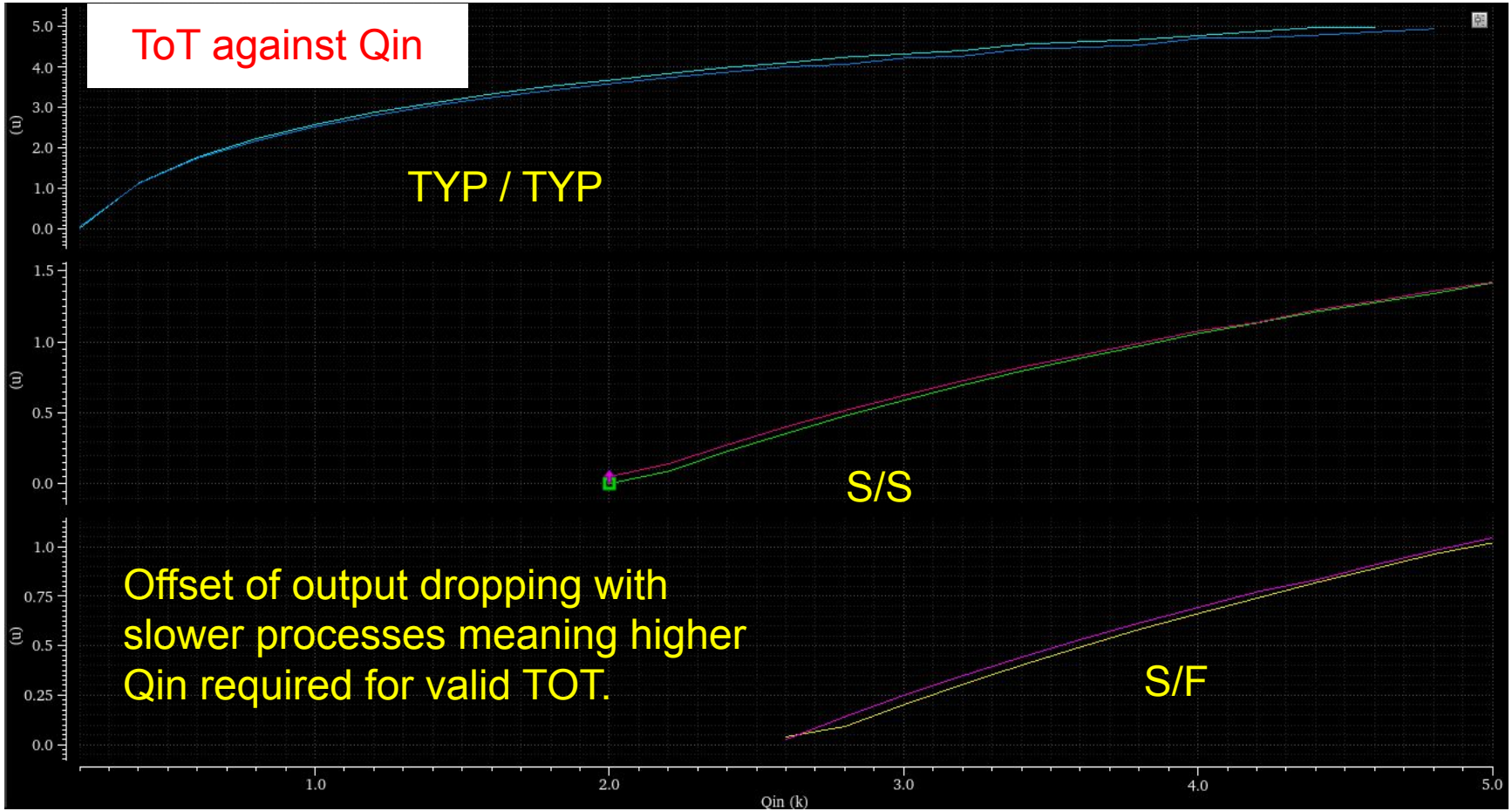


Constant charge injected of 200 e-

Same transistor process corner (typical NMOS / typical PMOS)

Offset is highly temperature-dependent.

Schematic Simulation Performance - PVT



Layout

DRC clean… *Almost (m3 density)* | LVS Clean

Transistor channels follow one direction

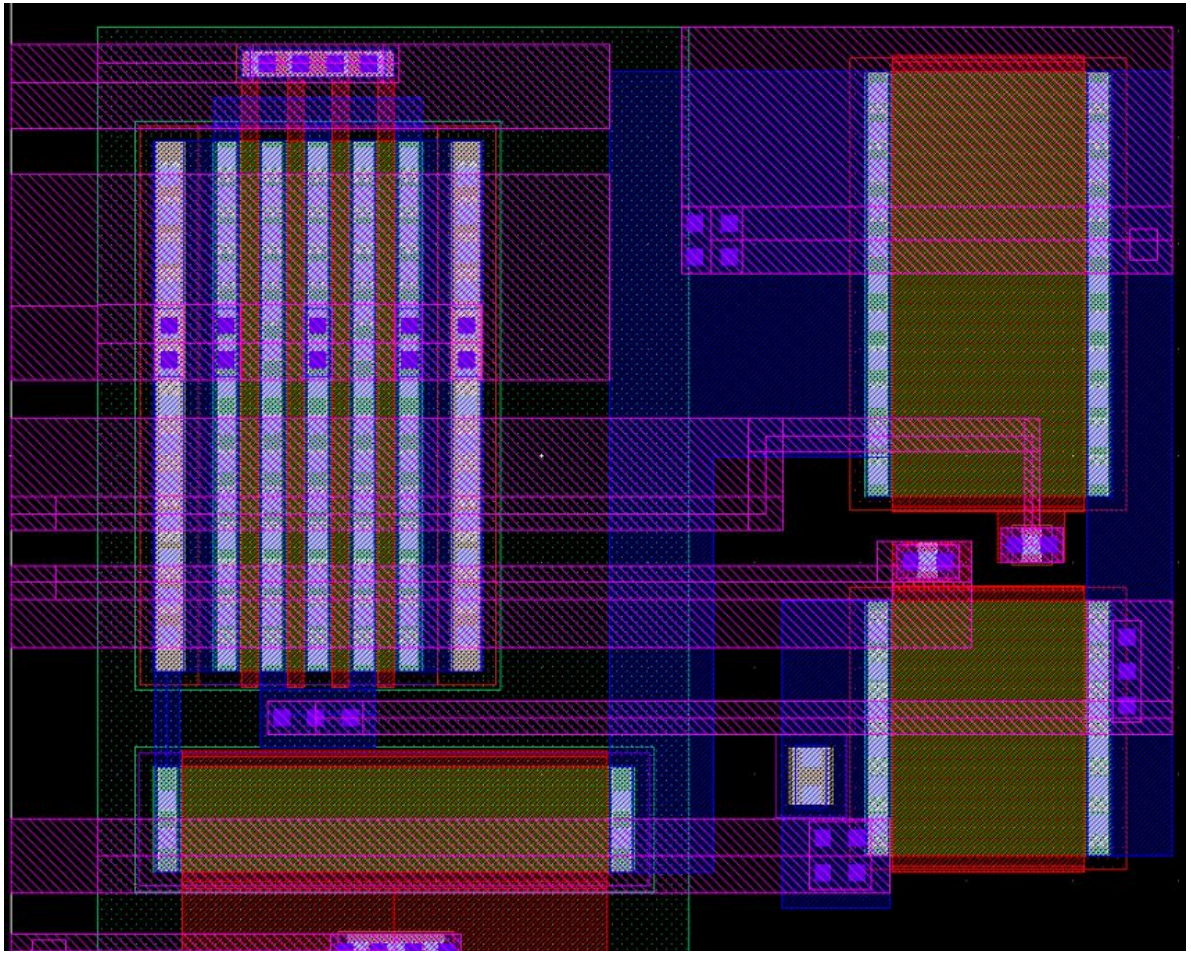
Metal 2 tracks mostly follow one direction

Minimum of two cuts per via for redundancy and .

Large analog metal tracks to reduce resistance and meet local metal density rules.

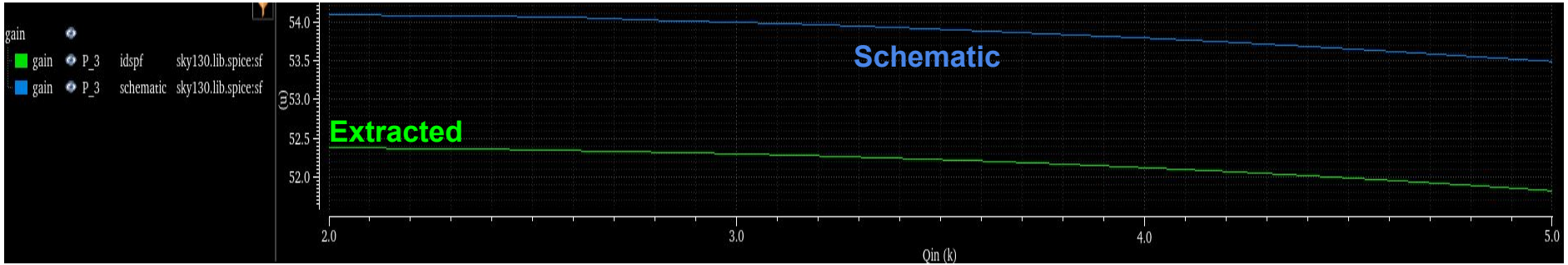
Large power supply metal 2 routing for good via connection from higher-level design.

More than minimum metal spacing between tracks for higher yield (~2x minimum).



Layout Extraction to IDSPF

- Layout introduces parasitics: resistances, capacitances, inductances etc.
- These can slow circuits, reduce power in regions, and impact performance
- Comparison needed before and after

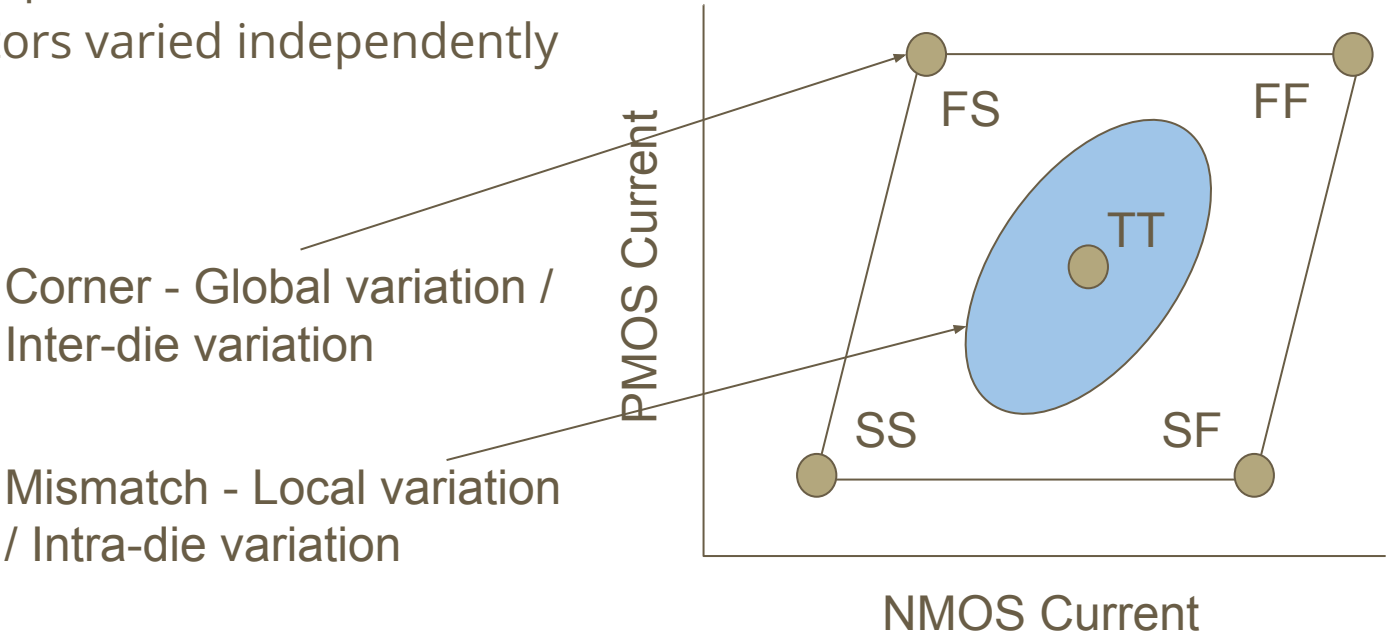


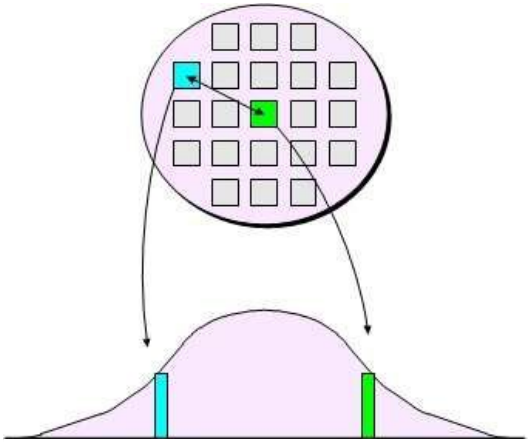
Schematic has consistently higher gain than for the extracted layout. Example given for S/F corner, but true for all.

The open loop gain of amplifier is likely decreasing with increasing charge - causing gain to drop.

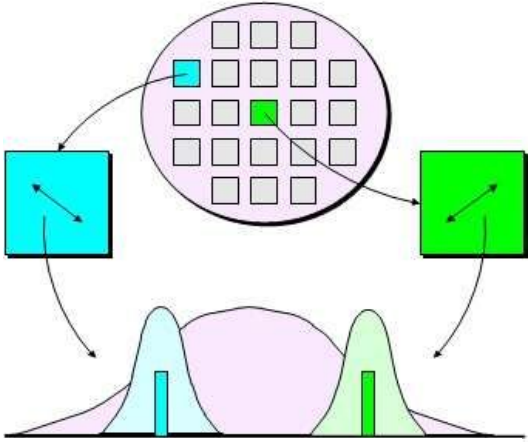
Next Step - Monte Carlo Simulation

- Monte Carlo provide insight to statistical mismatch between devices
- Includes process and mismatch variation
- Transistors varied independently

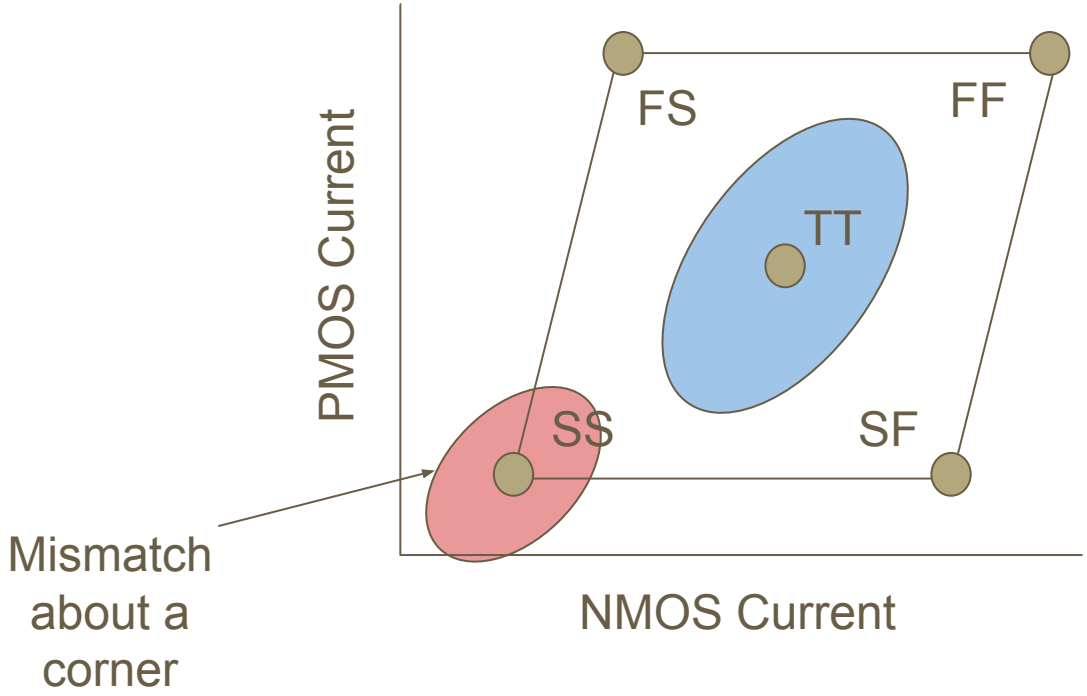




Inter-die variations



Intra-die variations



Maxfield, C. M. (2010, December 3). *Overcoming 32/28-nm IC implementation challenges*. EDN. https://www.edn.com/overcoming-32-28-nm-ic-implementation-challenges/

Summary

- Mini “chip flow” in Cadence Virtuoso with CSA
- Ideal / “Behavioural” → Transistor-level schematic → simulation → layout → post-layout simulation
- ADE environment for expression building and extracting circuit parameters
- Corner sweep to explore effects of process variation