# MAPS for Soft X-rays and Timing detectors

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*On behalf of SLAC Detectors R&D team*

SLAC NATIONAL ACCELERATOR LABORATORY

Stanford University | U.S. DEPARTMENT OF ENERGY

*Note for future readers:*
I've taken some liberty with the chronological order of events

# LCLS-II & LCLS-II-HE: revolutionary tools for X-ray science

- LCLS-II will be the first XFEL to be based on continuous-wave superconducting accelerator technology
- Continuous repetition rate of 1 MHz, with photon energies between 250 eV and 12 keV

# LCLS-II & LCLS-II-HE: revolutionary tools for X-ray science

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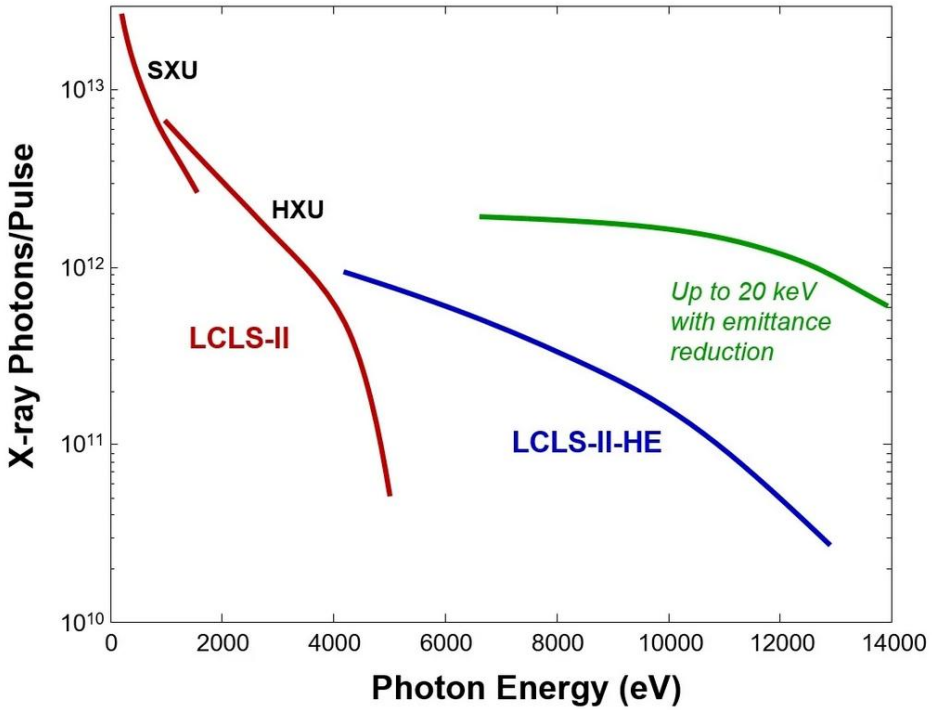
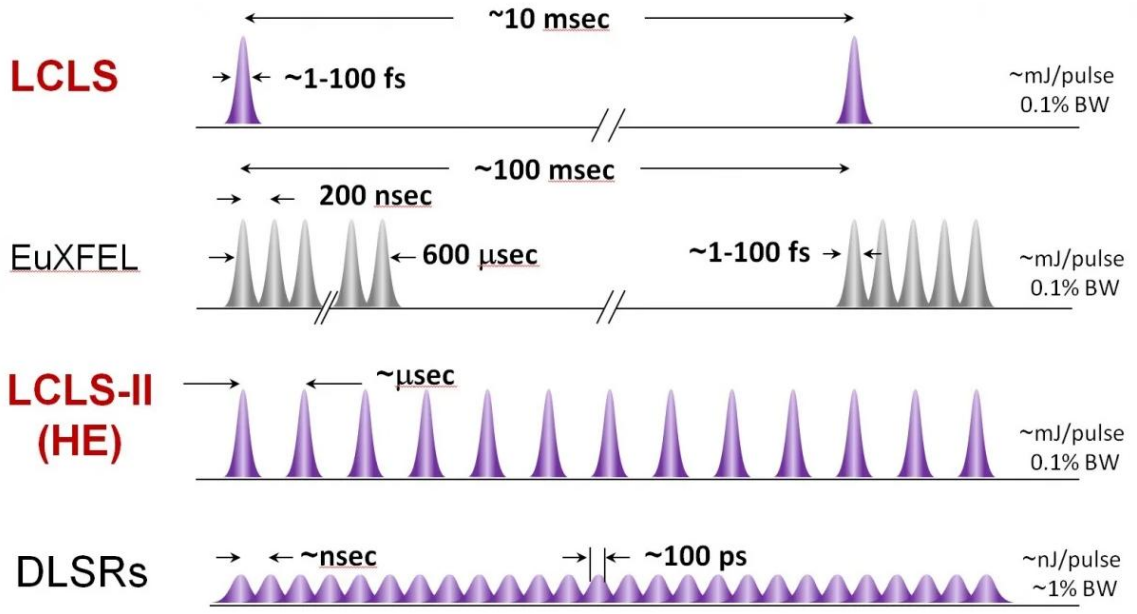
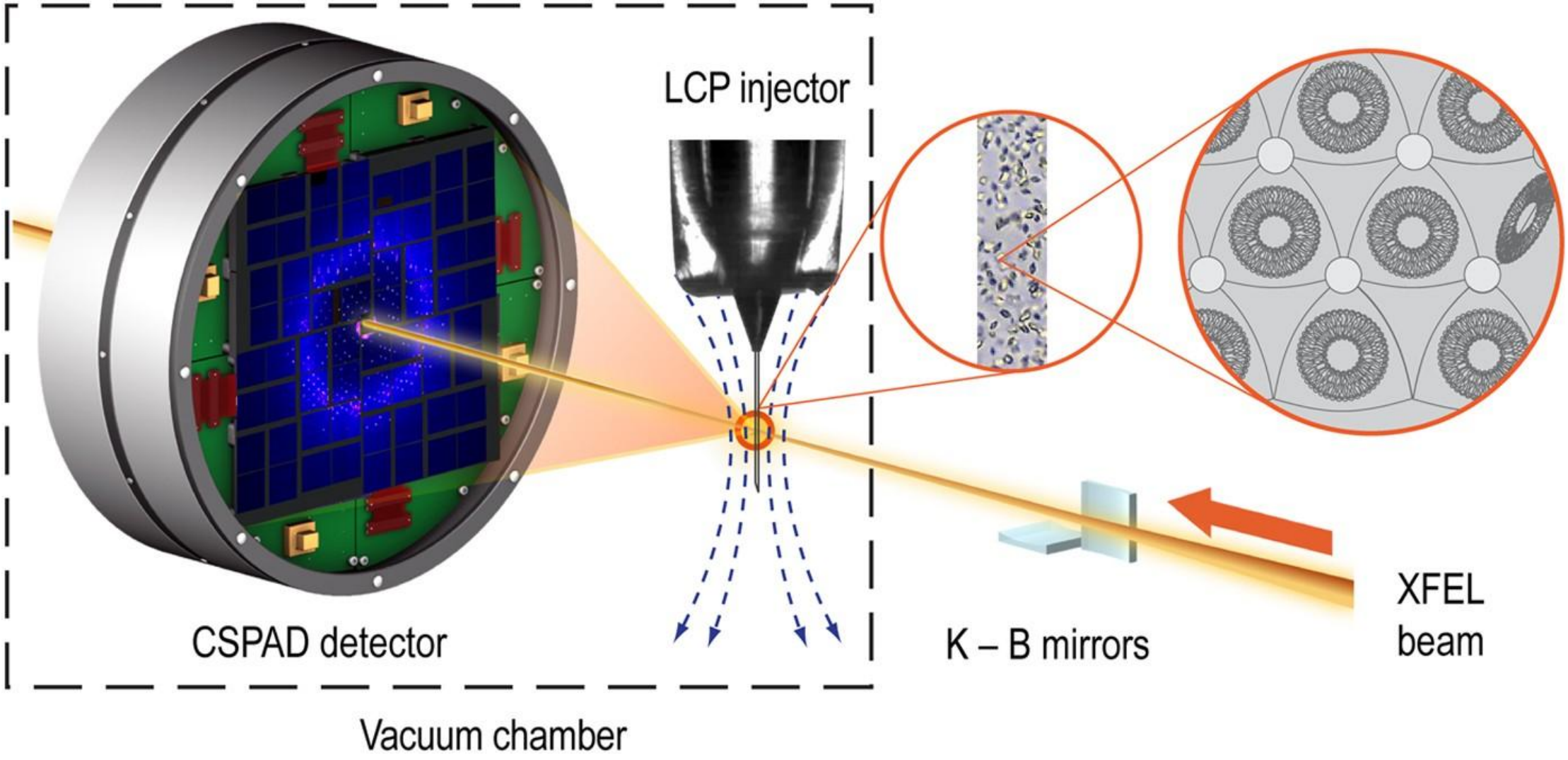


# X-ray detectors



# X-ray detectors for light sources

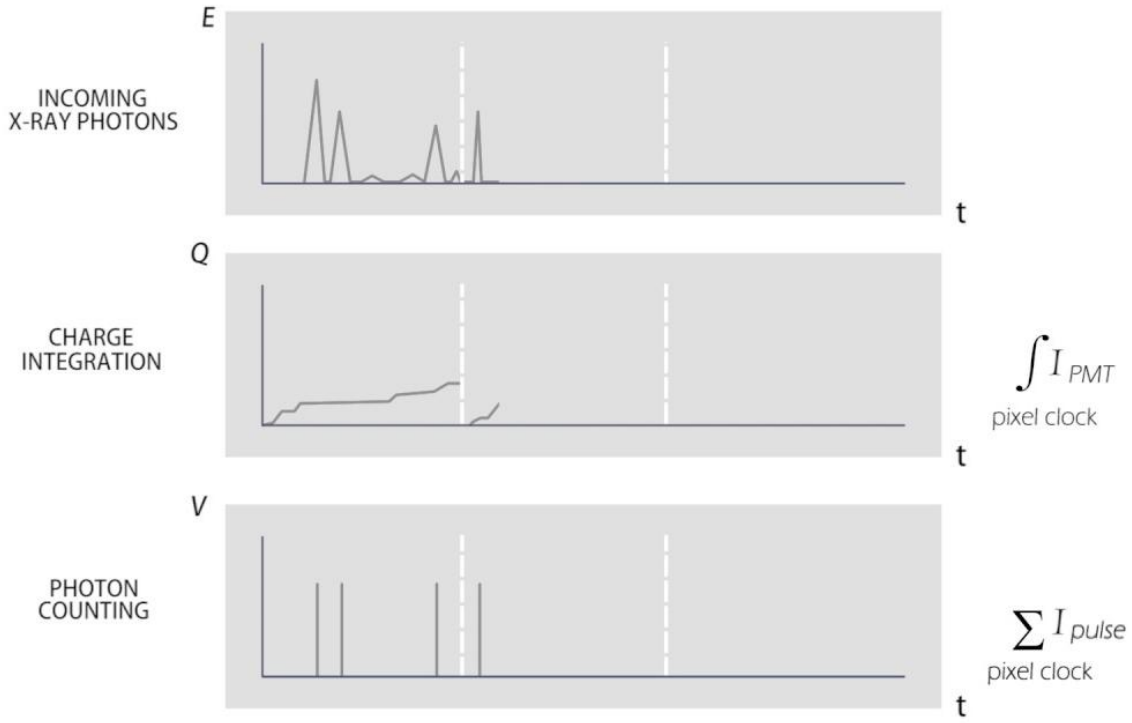
Two main classes of X-ray detectors for light sources:

- **Charge integrating:**
  Integrate Q over C, convert with an A/D
  → *Similar to CMOS image sensors*
- **Photon counting:** count how many times the signal crosses a threshold, single-photon counting
  → *Similar to HEP tracking detectors, but with counter*

PC have been the main technology used in synchrotrons: easier to design, use and calibrate.

However, PC do not perform well at XFELs and 4$^{th}$ gen synchrotrons:

- XFEL produces photons with ~fs spatial separation
- More photons = higher chances of pile-up




**For more information on PC detectors:**
https://www.dectris.com/en/landing-pages/transforming-x-ray-detection/

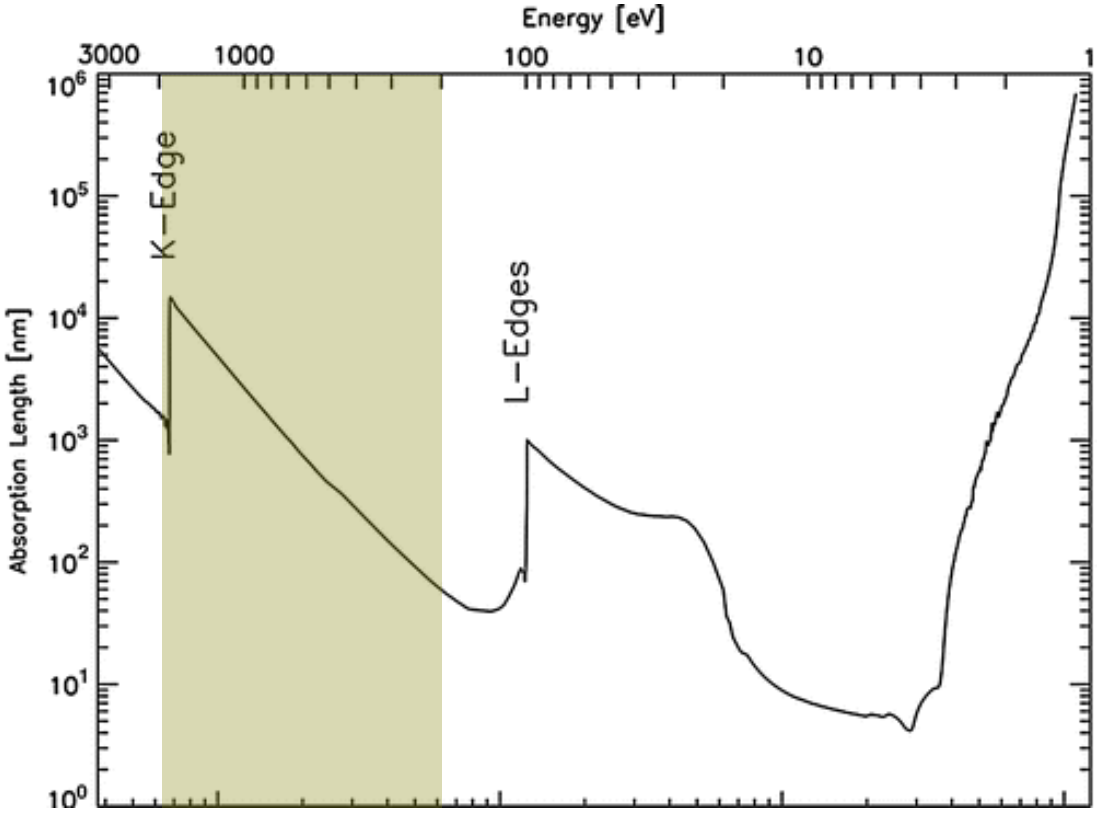
# Designing ePixM: a monolithic detector for soft X-rays

# ePixM detector: specifications

| Parameter | Objective |
|---|---|
| **Quantum efficiency [%, 275eV-2000eV]** | 90 |
| **Pixel Pitch [um]** | 50 |
| **Readout Noise [$e^-$ rms]** | 15 |
| **Well Depth [# photons @ 530eV]** | 3000 |
| **Frame Rate [kHz]** | 5 |
| **Power/pixel [uW]** | 20 |

# X-ray detectors

**Specification: QE > 90% for energies between 250 and 2000 keV**

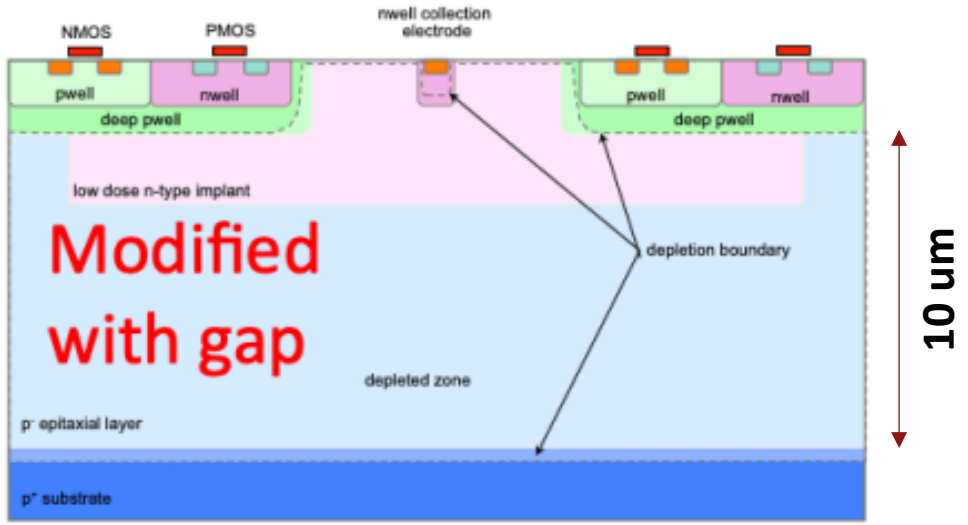


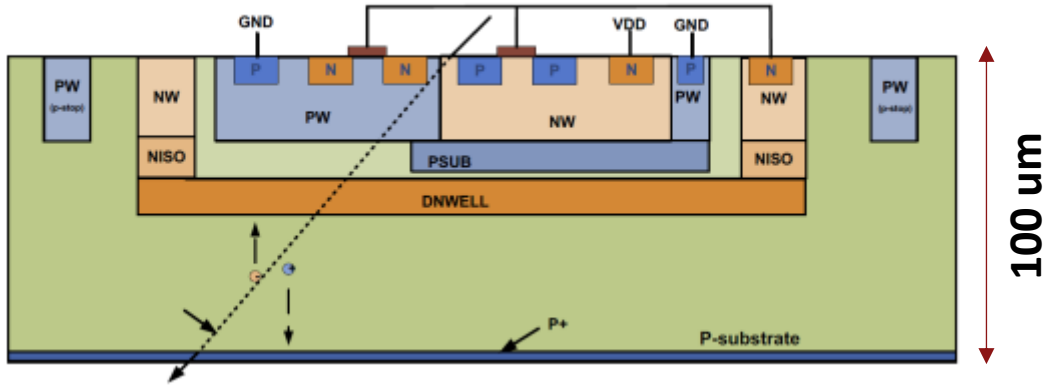

*The **absorption length** is the distance over which the optical intensity in a medium decays to 1 / e (approximately 37%) of its initial value due to absorption*


https://doi.org/10.1007/978-3-319-14394-1_38

# X-ray detectors

**Which technology do you choose to detect 250 to 2keV X-rays?**




**CMOS imaging process, partially depleted**

**HV-MAPS, fully depleted**

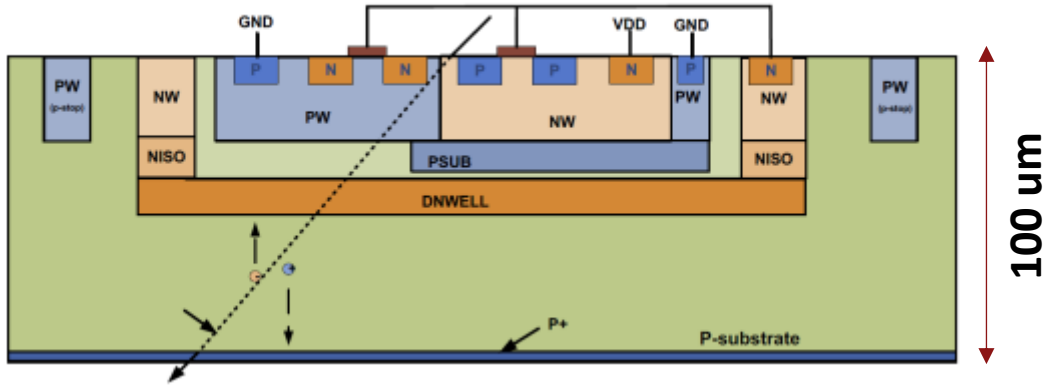
# X-ray detectors

**Which technology do you choose to detect 250 to 2keV X-rays?**

- Large electrode → more uniform E-field, better charge collection and full depletion
- X-ray fully absorbed, electronics shielded from radiation damage

- Requires high-resistivity substrate, special wafer

- Trade-off between area to implement electronics (functionality) & $C_D$
- Large $C_D$ → worse noise performance




**HV-MAPS, fully depleted**

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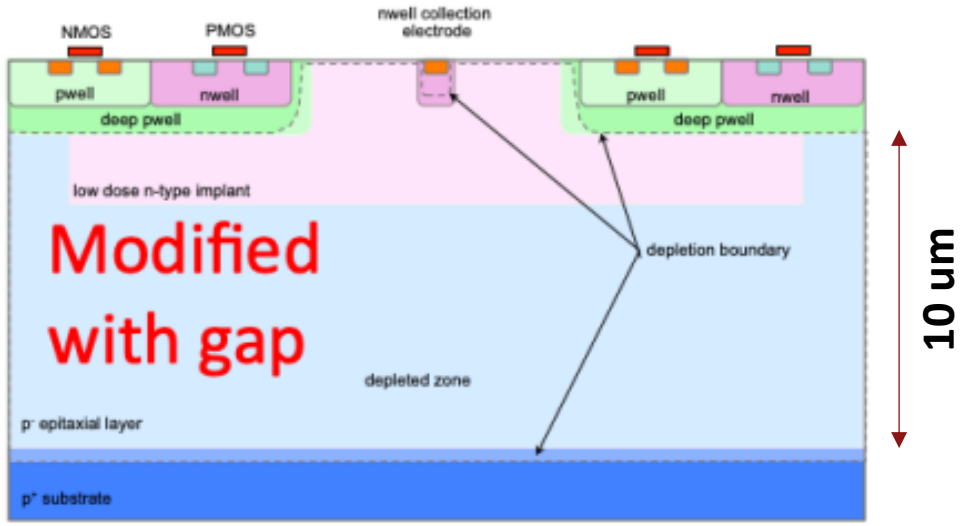


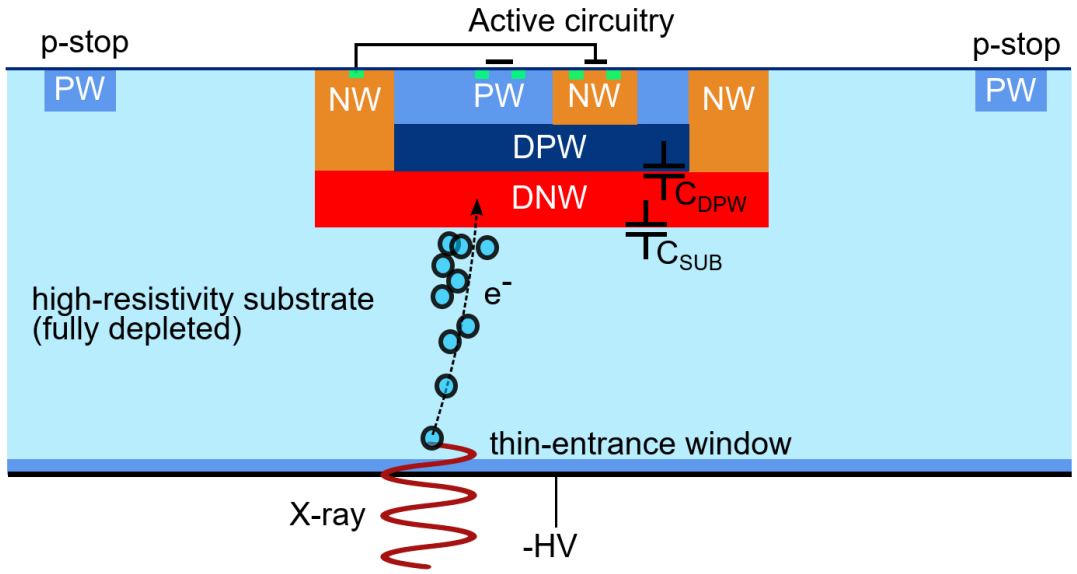

CMOS imaging process, partially depleted

- Small $C_D$ → better noise with same power budget
- Electronic circuit sits outside of collection node

- Charge collection times need to be simulated: <100 ns
- Radiation hardness

- **Requires thinning to 10um for back-side illumination**

# ePixM cross-section: fully depleted HV MAPS




$$C_d = C_{DNW-SUB} + C_{DNW-PSUB}$$

$$\text{ENC} \propto {g_m}/{C_d} \text{ (thermal)}$$

**Trade-off:**
$C_D$ (noise) - Area (complexity)

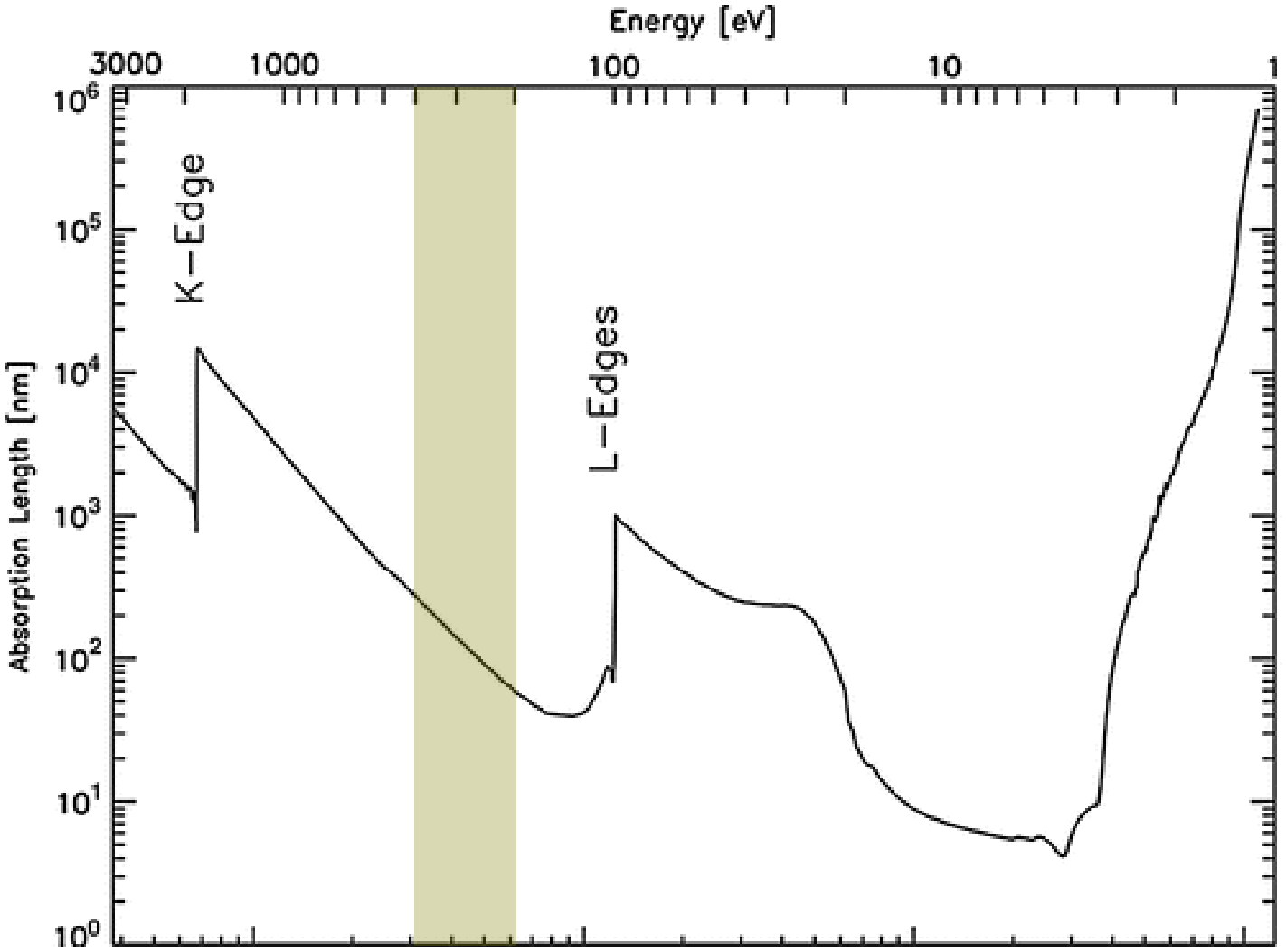
- HV applied on backside: full-depletion, charge collected by drift
- Electronics sits in deep n-well (DNW), which also acts as collection node
- Additional deep p implant (PSUB) isolates NW (PMOS transistors) from DNW
- Wafers thinned and back-processed with thin entrance window

**Why back-side illumination with a thin entrance window?**



[1] Hemperek T., LF-MONOPIX a depleted monolithic CMOS pixel sensor in a 150 nm CMOS technology, FEE2018

# ePixM: thin entrance window

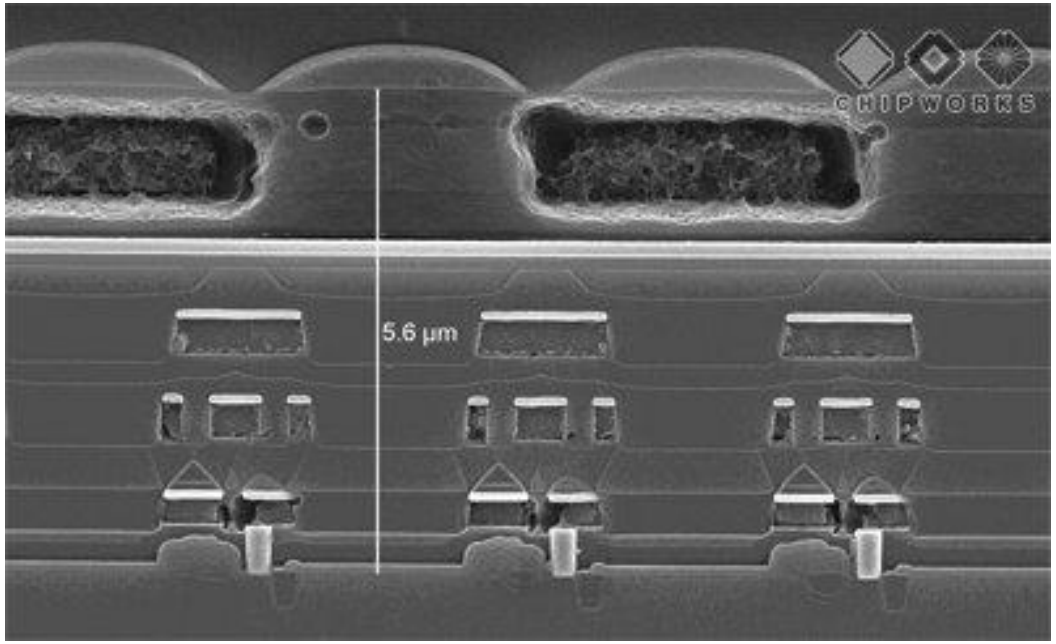


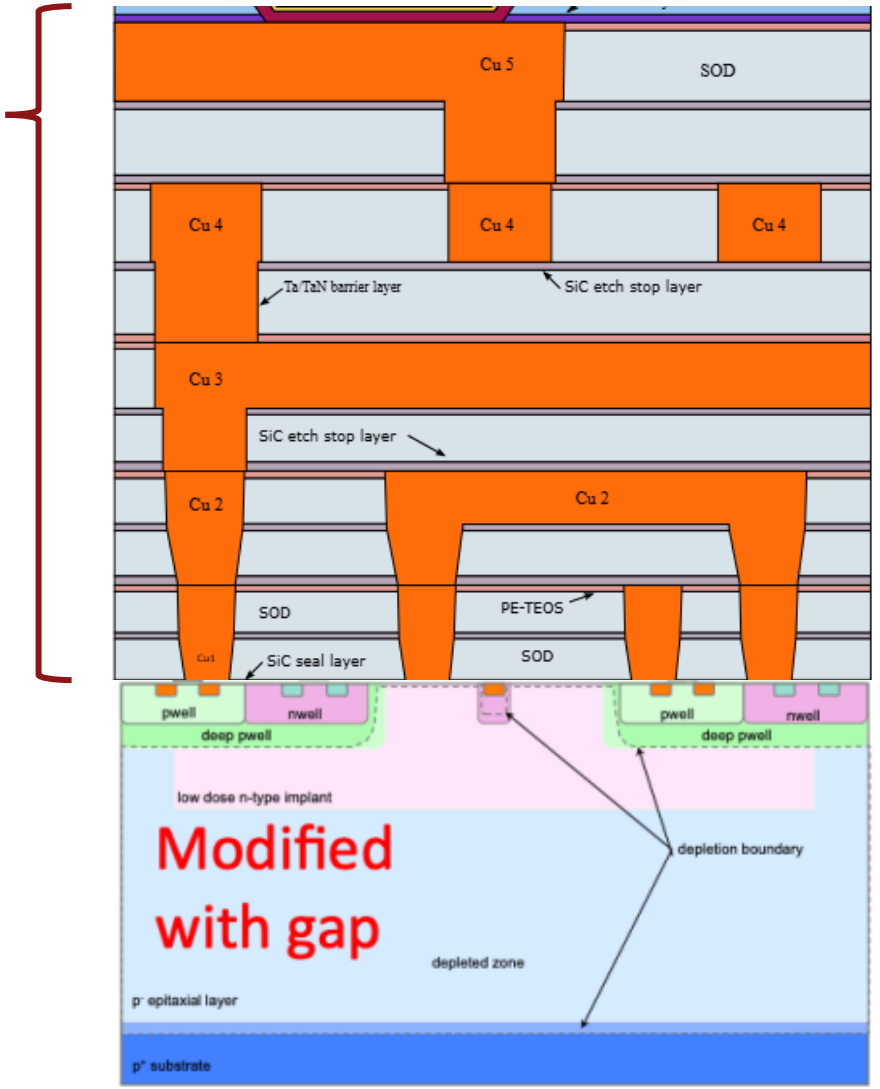



https://doi.org/10.1007/978-3-319-14394-1_38

# Why back-side illumination?

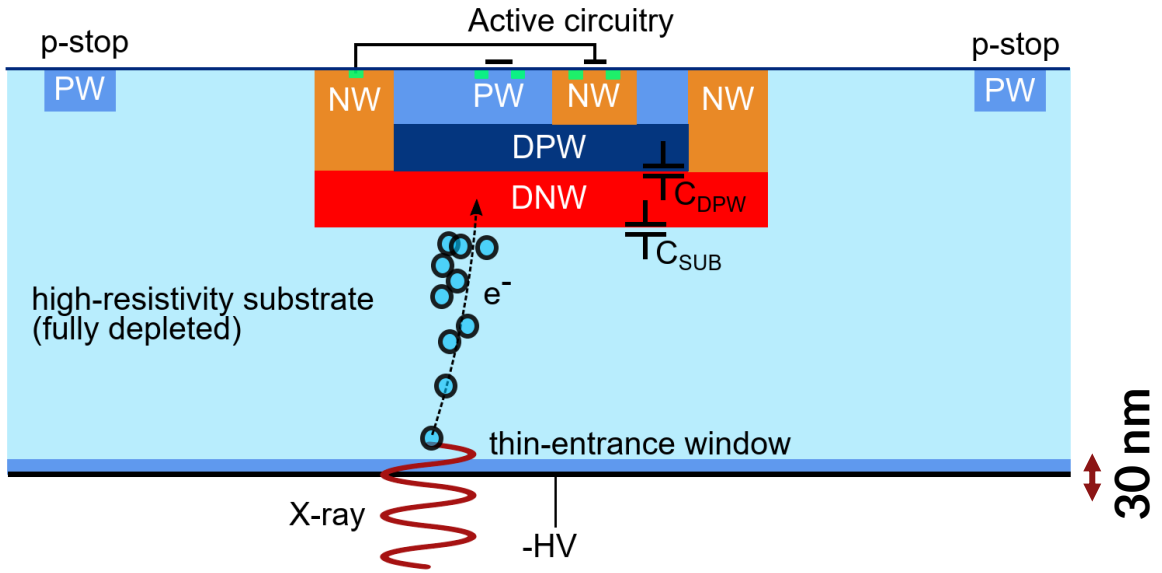
**Metal stack: ~6 metals, typically Cu in modern CMOS processes, plus dielectric layers…**

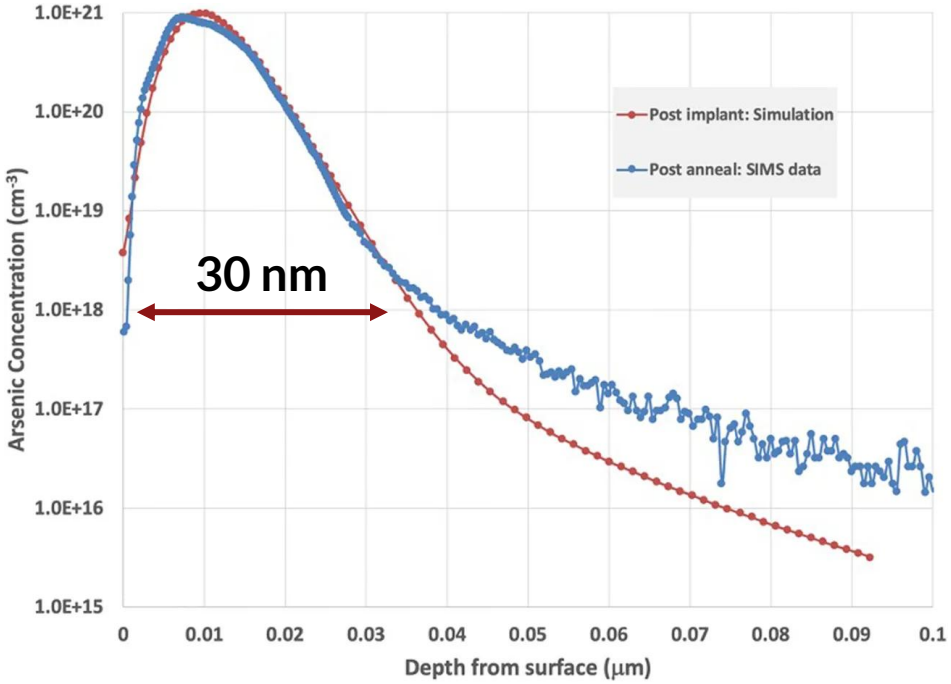


# ePixM: thin entrance window

- Need doping on the backside to apply -HV and deplete the sensor
- Depth of the doped region need to be small to avoid degrading QE at lowest energies
- Shallow entrance windows is challenging: the high Temp anneal needed to activate the dopant also drives the dopant profile deeper, growing the region that is insensitive to soft X-rays
- Also *nice-to-have*: do not destroy the CMOS side already (if already done by fab)
- Novel technique based on microwave annealing developed by J. Segal, C. Kenney



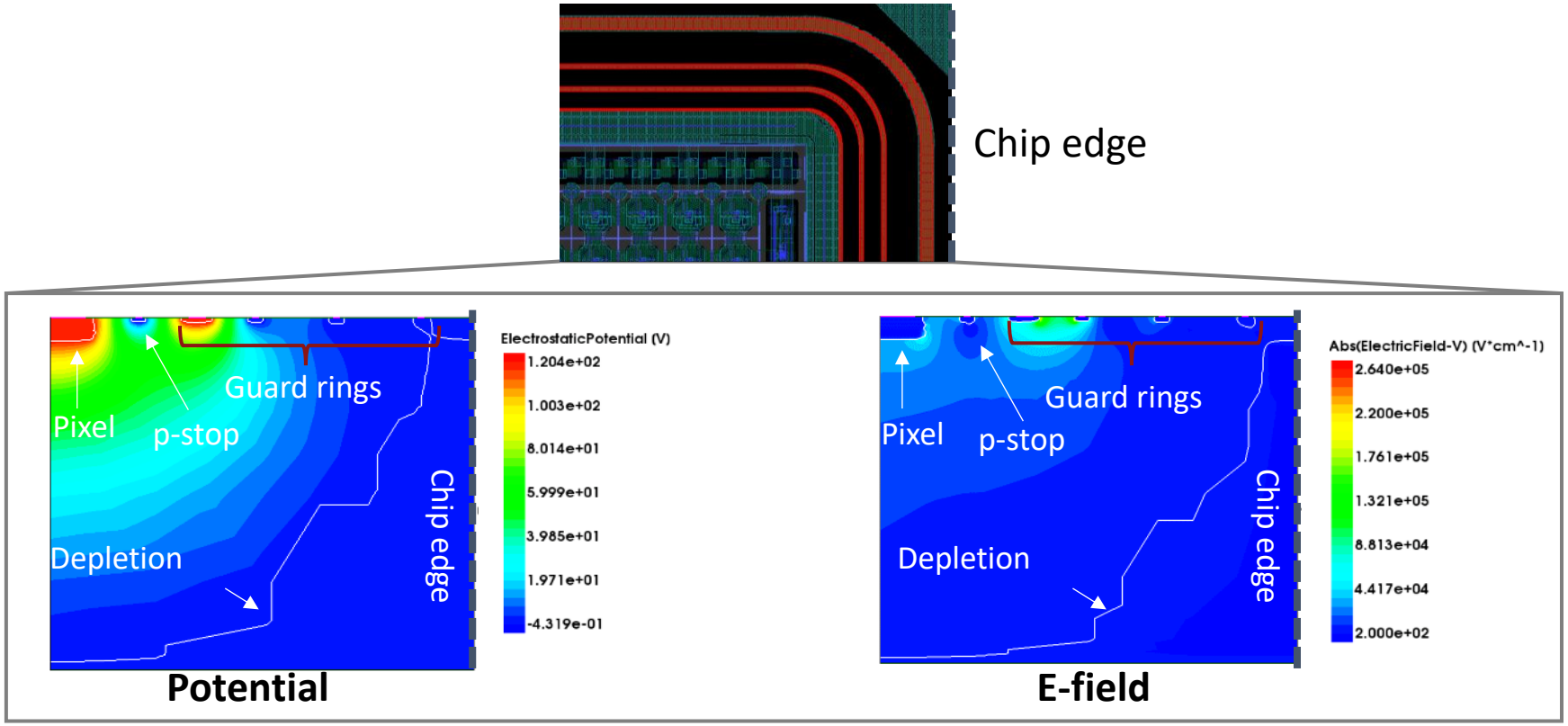





https://doi.org/10.3389/fphy.2021.618390

# ePixM: guard-rings

- Guard rings at chip boundaries to limit $I_{leak}$
- p-stop structures with metal overhangs to isolate each pixel
- Rounded edges at corners to reduce peak E-field and enable 100-200V bias applied






TCAD simulations by J. Segal

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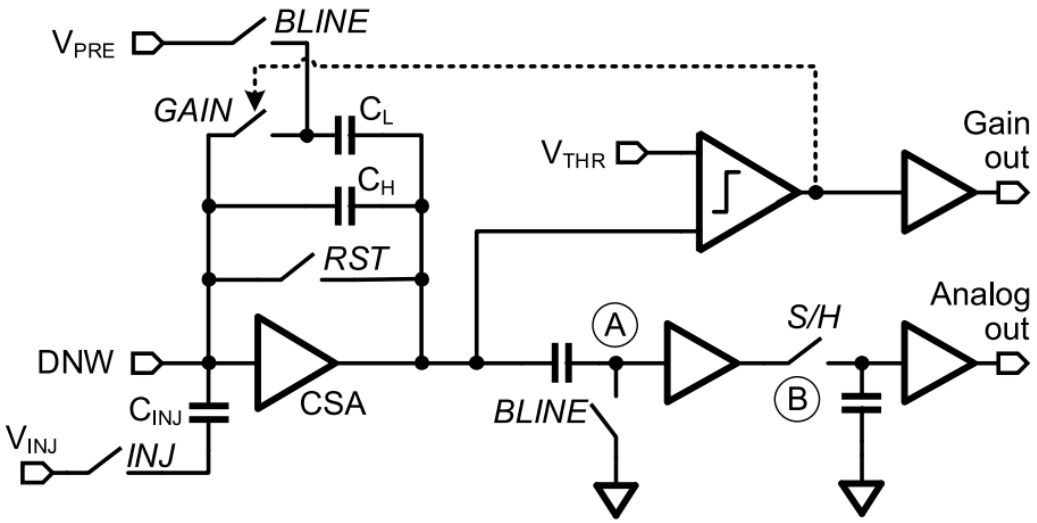
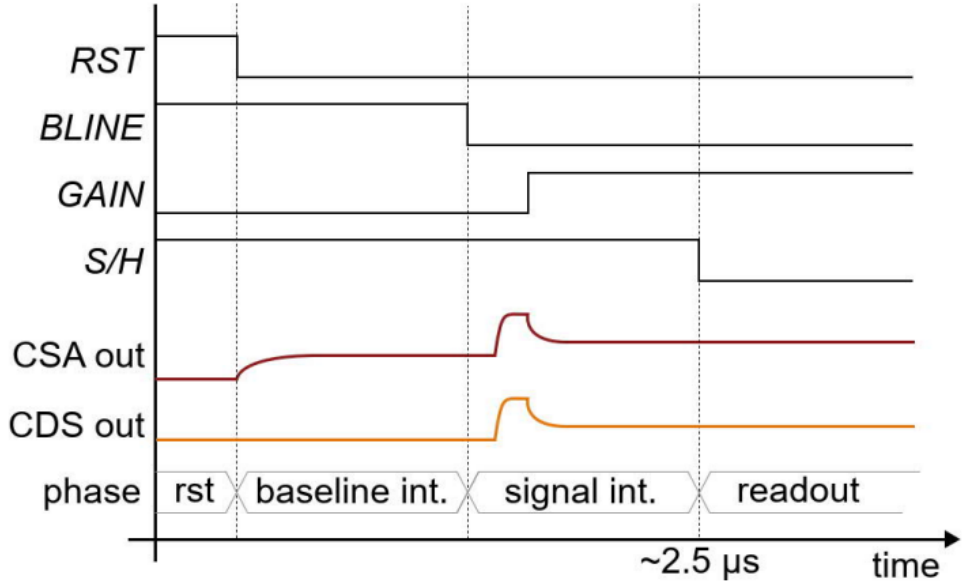
# ePixM: circuits




- Time-variant circuit with switched reset *(similar to CMOS imagers)*
- In-pixel noise shaper implemented with Correlated Double Sampling (CDS)
- Automatic gain-switching to extend dynamic range

# ePixM: capacitances

**Performed TCAD simulations to characterize detector capacitance:**

- TCAD design kit from foundry with doping profiles
- Many iterations between circuit and device simulations:
  TCAD to sim $C_D$ → Schematics → Layout → Noise sims →
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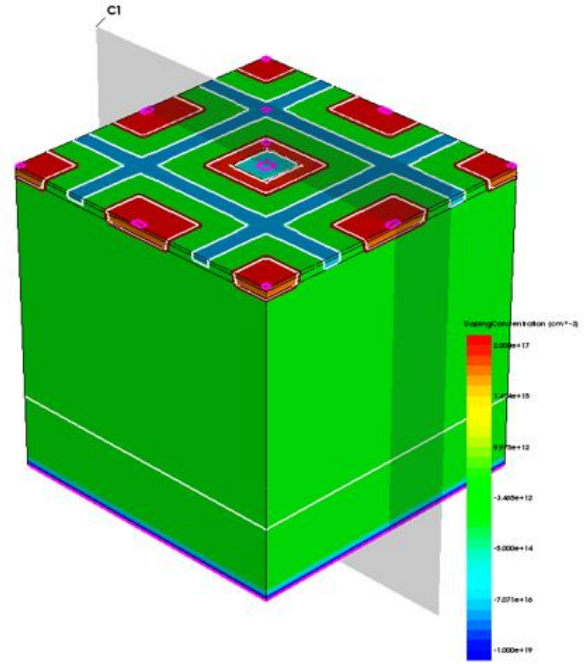
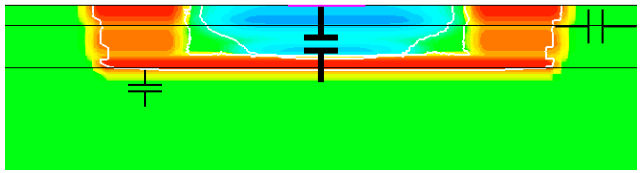



**Pixel doping profile:**



| | Capacitance [fF] |
|---|---|
| **adjacent pixel (x 4)** | 0.16 |
| **internal p-well** | 45 |
| **p-guard ring** | 8.6 |
| **backside** | 2.2 |
| **Total (summed)** | **56.4552** |

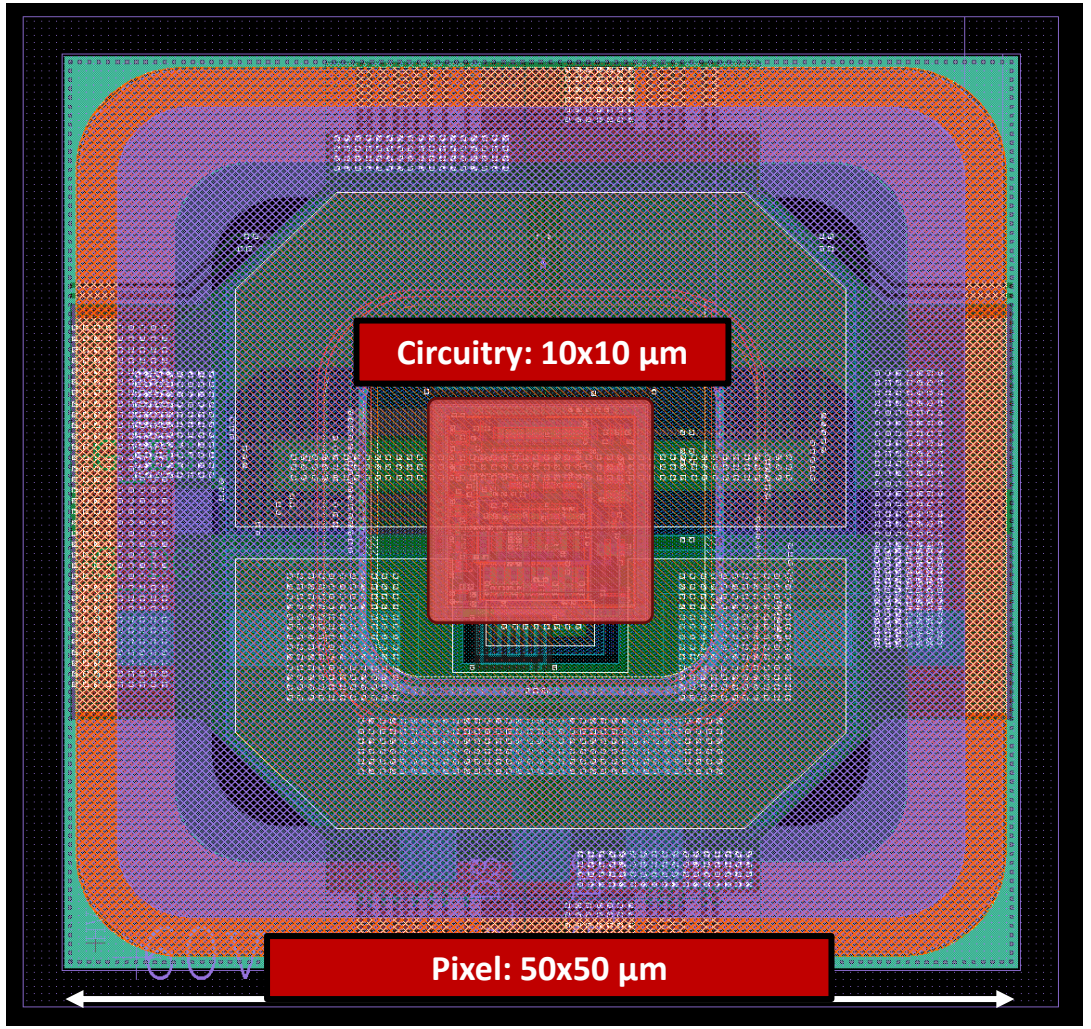
# ePixM v1: pixel layout

**Trade-off:**
$C_D$ (noise) - Area (complexity)

**Design strategies:**
- Full custom layout:
  minimum spacing/distance of every DRC rule
- Minimize size of transistors
- Reduce area of DNW & DNW/PW overlap

**Post-layout noise simulations:**
- ENC ~11 el. ✅
- Dynamic range 600 keV ✅

**Layout of one pixel**



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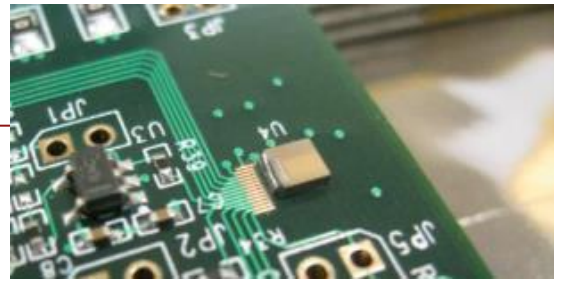
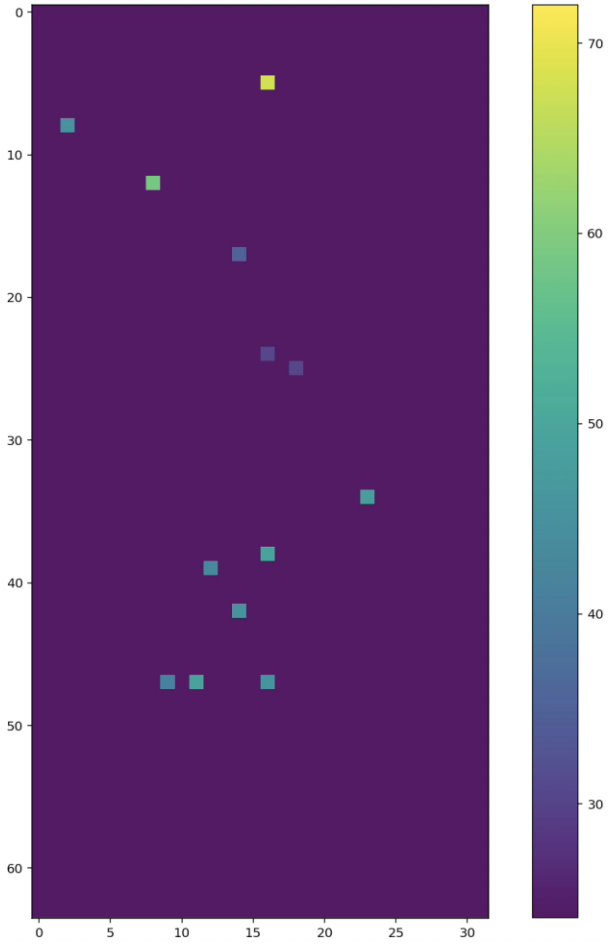
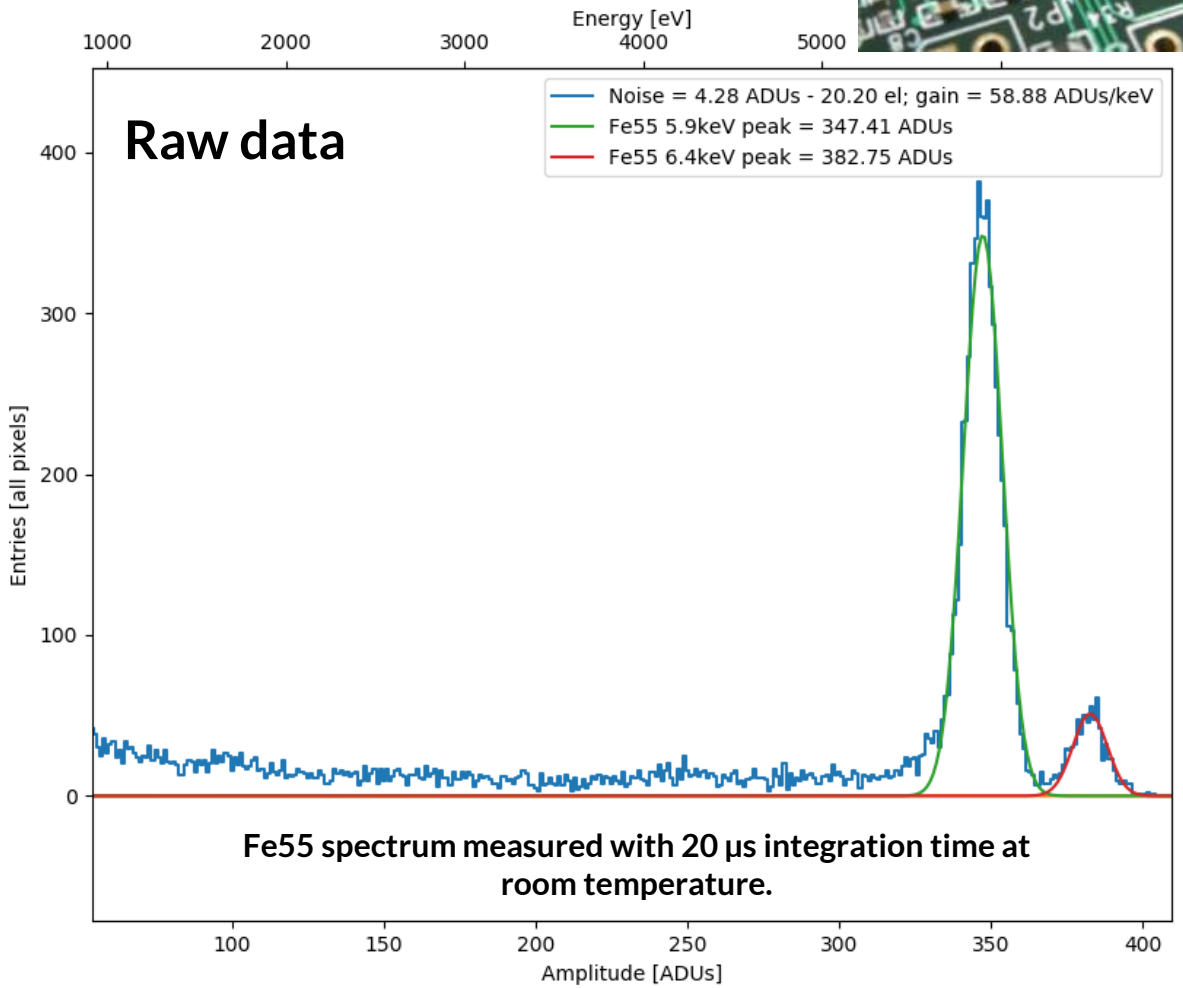
# ePixM first measurements

Small pixel matrix prototype



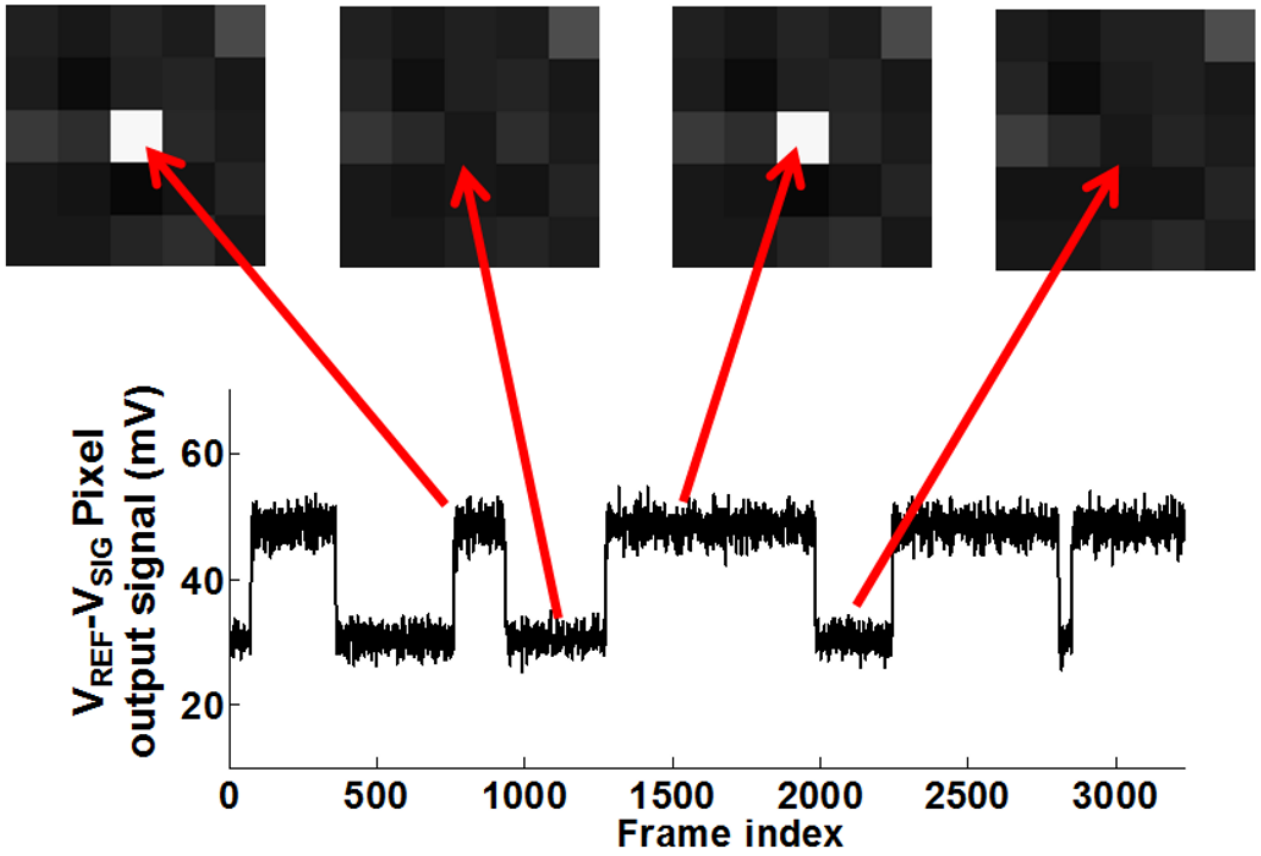
Fe55 live acquisition



# ePixM first measurements

- A good number of pixels showed an excess of noise…
- Upon further investigation, data looked like the following plot…






https://pagespro.isae-supaero.fr/vincent-goiffon/

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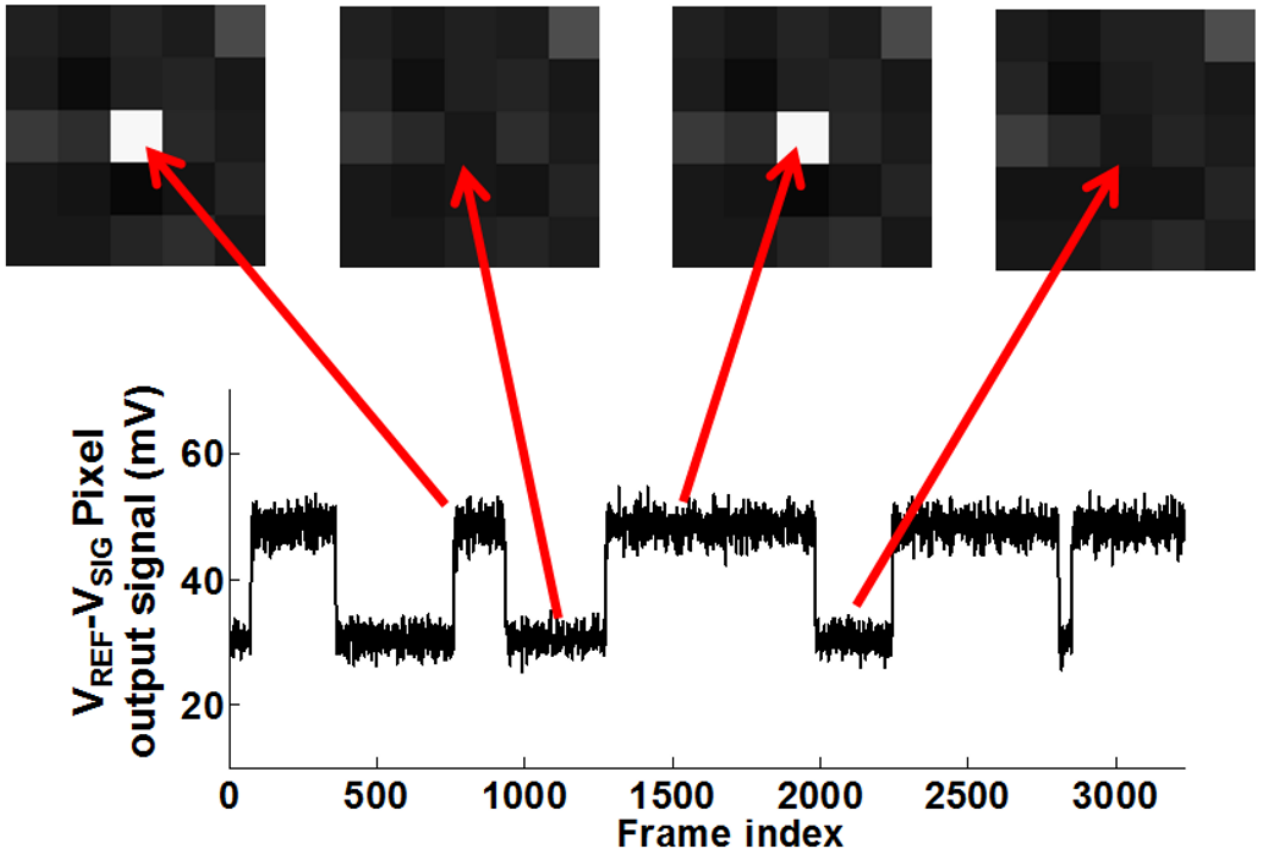


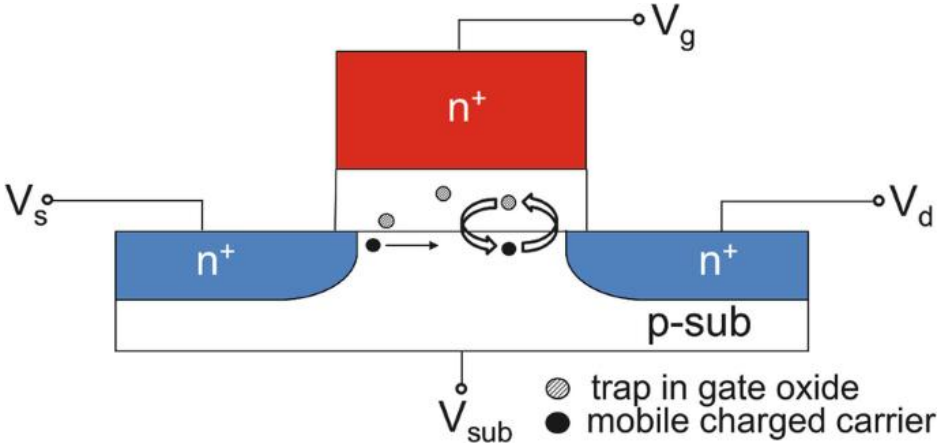




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# MAPS & RTS

**Do not trust simulations (blindly)!**

**Avoid minimum sized transistors in amplification stages!**

Jinst

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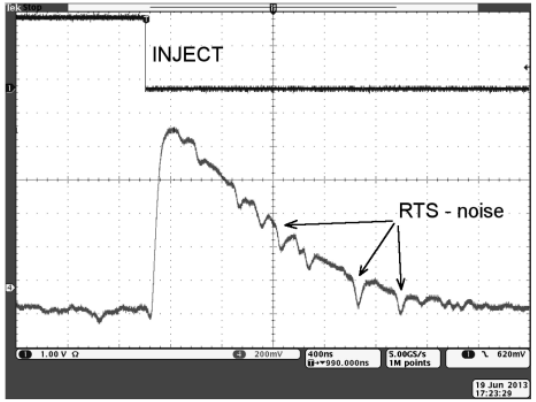
ACCEPTED: *January 18, 2015*
PUBLISHED: *February 27, 2015*

**DMAPS: a fully depleted monolithic active pixel sensor — analog performance characterization**

M. Havránek,[1,2] T. Hemperek, H. Krüger, Y. Fu, L. Germic, T. Kishishita, C. Marinas, T. Obermann and N. Wermes

*Physikalisches Institut, Universität Bonn, Nußallee 12, 53115 Bonn, Germany*[3]

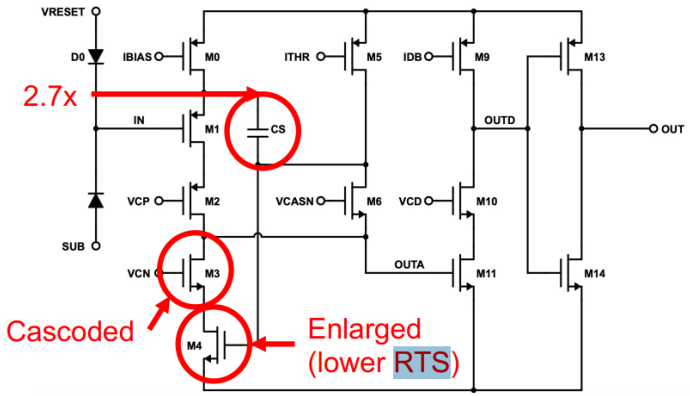
*E-mail:* miroslav.havranek@cern.ch




Random Telegraph Signal noise (RTS) represents a significant noise component of all variants of the DMAPS pixels in EPCB01. Spikes caused by the RTS are clearly visible in figure 10. RTS noise is not a speciality of EPCB01 only. The RTS noise often appears in monolithic pixels as described for example in [13] and [14].

**Latest Developments and Results of Radiation Tolerance CMOS Sensors with Small Collection electrodes**

I. Asensi Tortajada[1,2,*], P. Allport[3], M. Barbero[4], P. Barrillon[4], I. Berdalovic[1,5], C. Bespin[6], S. Bhat[4], D. Bortoletto[7], P. Breugnon[4], C. Buttar[8], R. Cardella[1], F. Dachs[1,13], V. Dao[1], Y. Degerli[12], H. Denizli[10], M. Dyndal[1], L. Flores Sanz de Acedo[1,8], P. Freeman[3], L. Gonella[3], A. Habib[4], T. Hemperek[6], T. Hirono[6], T. Kugathasan[1], I. Mandić[9], M. Miku[9], K. Moustakas[6], M. Munker[1], K.Y. Oyulmaz[10], P. Pangaud[4], H. Pernegger[1], F. Piro[1], P. Riedler[1], H. Sandaker[11], E.J. Schioppa[1], P. Schwemling[12], A. Sharma[1,7], L. Simon Argemi[8], C. Solans Sanchez[1], W. Snoeys[1], T. Suligoj[5], T. Wang[6], N. Wermes[6]




## 2. Evolution of MALTA and Mini-MALTA

The analog Front-end (FE) of MALTA and Mini-MALTA is shown in Fig. 1. Measurements on MALTA sensor revealed significant Random Telegraph Signal (RTS) noise, preventing lower threshold settings which was attributed to the ”M3” transistors being too small . To verify this assumption, the Mini-MALTA sensor includes sectors with the same ”M3” size as on MALTA and with a larger transistor. Measurements with Mini-MALTA confirmed that the RTS noise was decreased due to the larger transistor size, before and after irradiation.

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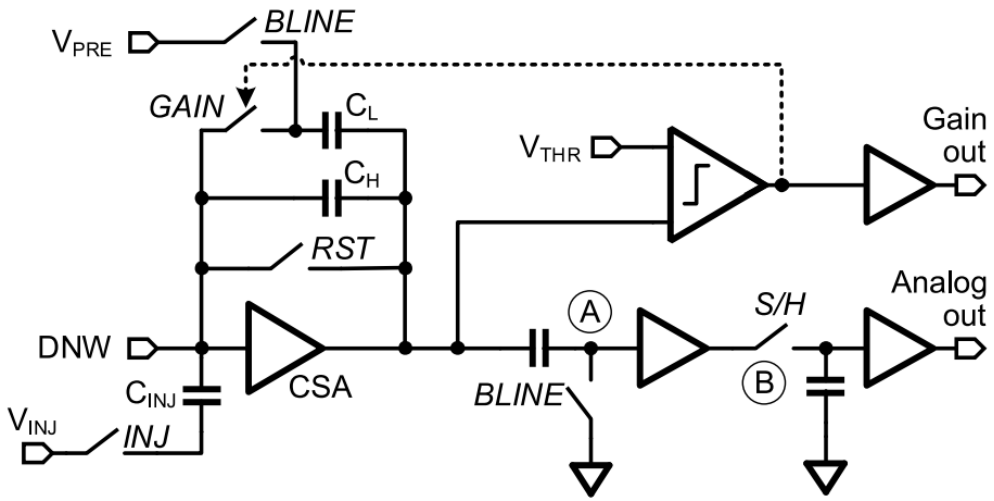
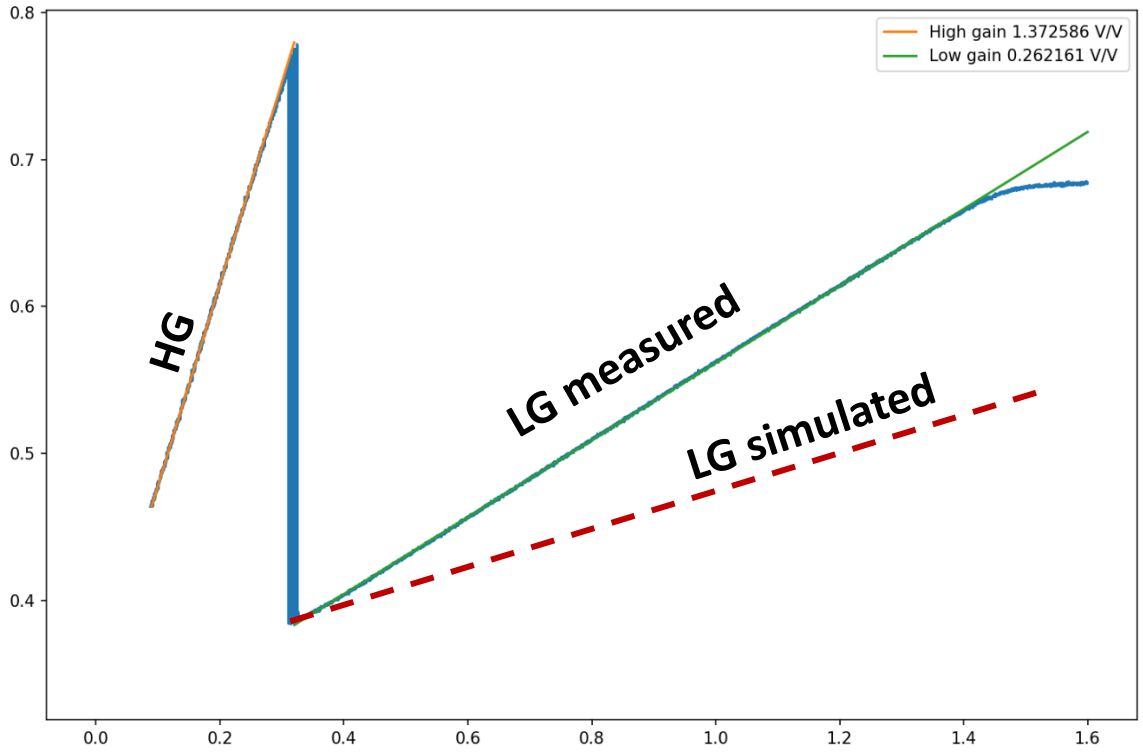
| Power/pixel [uW] | 20 ✅ |

# ePixM first measurements

- Gain in low-gain was off by a factor of 2
- Issue was later identified…



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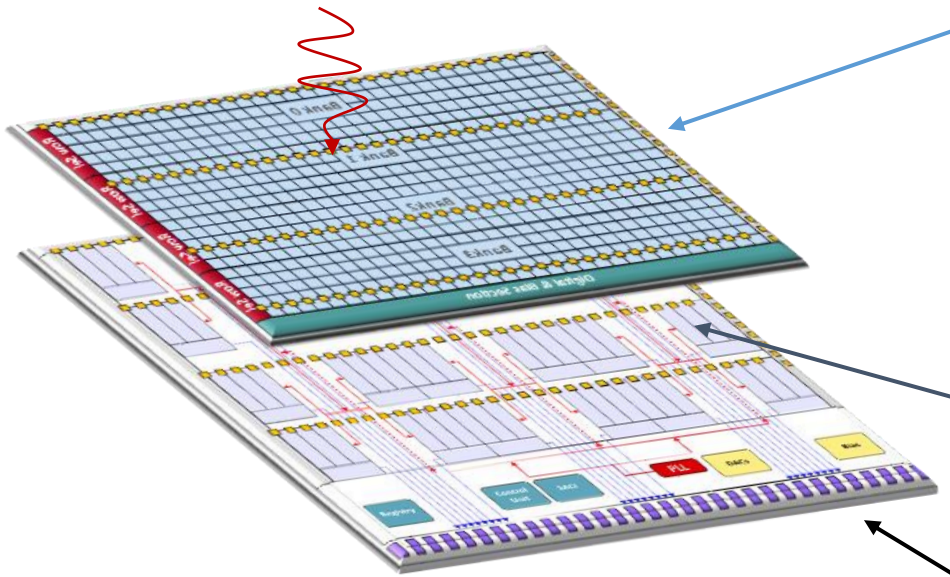
# ePixM camera

- In order to achieve high-frame rate, we parallelize the readout: multiple A/D converters
- Hard to implement in MAPS layer, so we de-coupled the problem…

X-rays $E_\gamma$ = 250 eV – 2keV



ePixM Monolithic Active Pixel Sensor (MAPS)

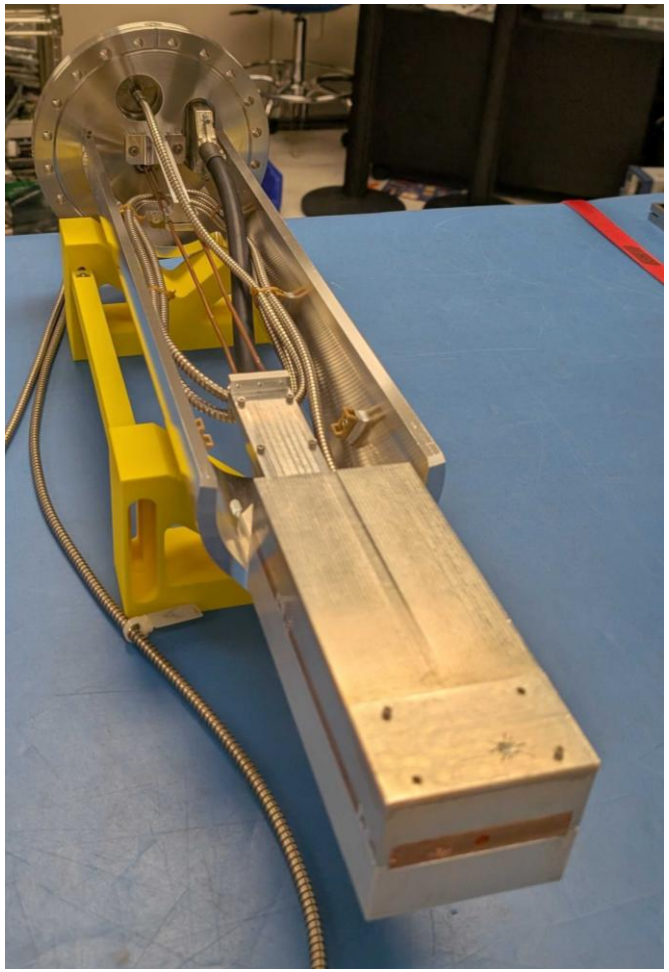
Standard micro-bumps

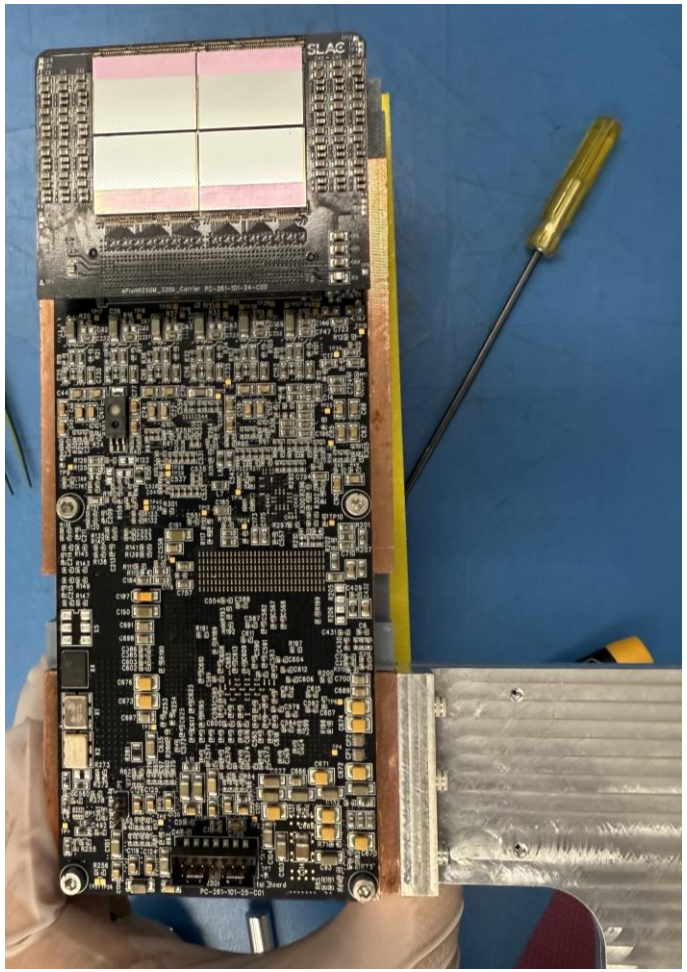
ePixHR-M Readout ASIC:
Analog-Digital converters, synchronization, biasing…

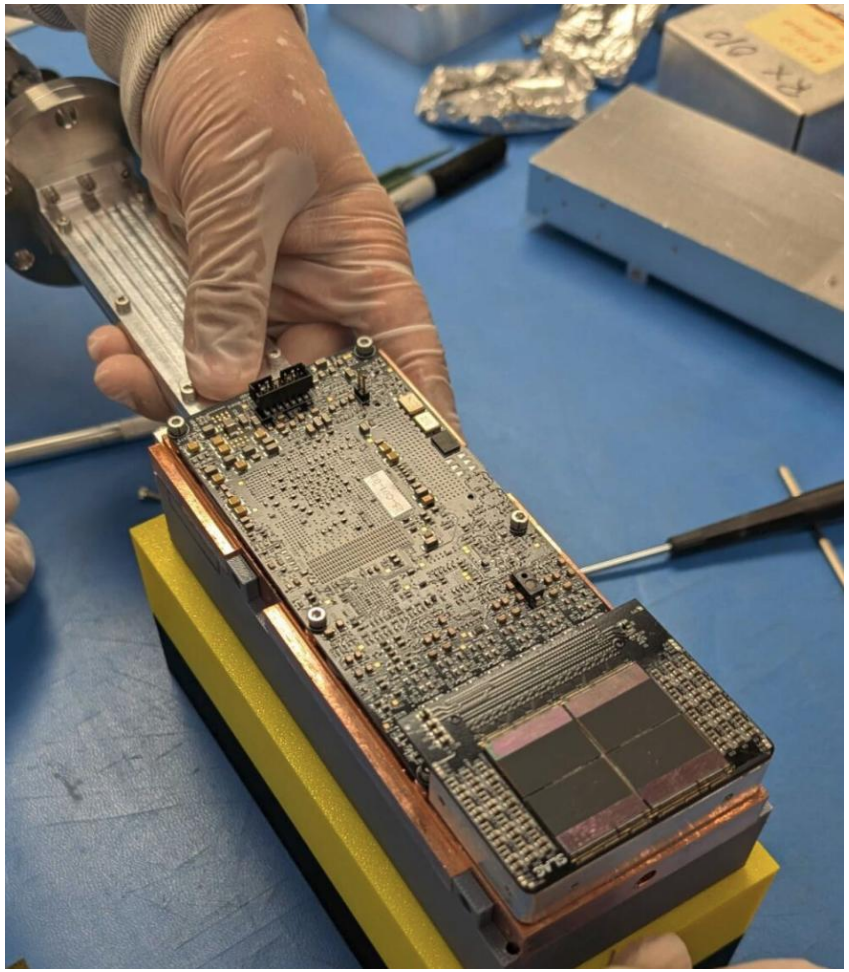
# ePixM camera

*… many years of works, with lots of challenges…*

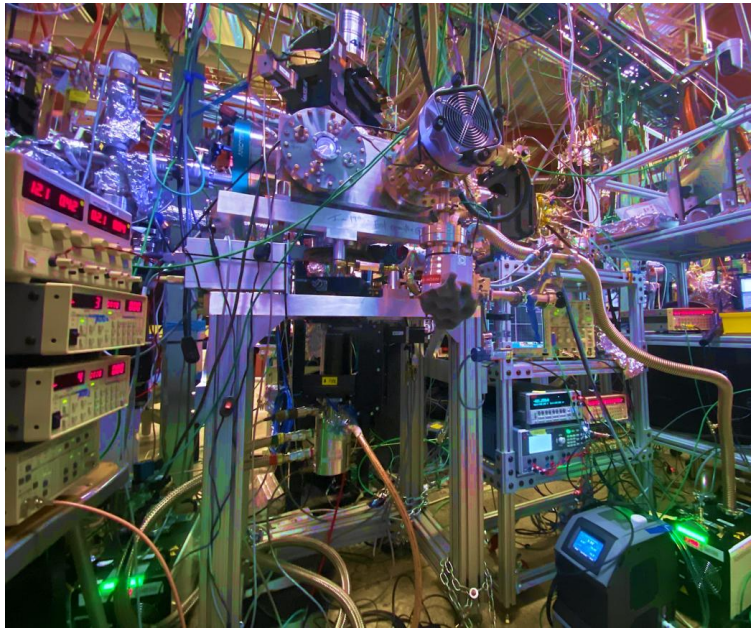
# ePixM camera

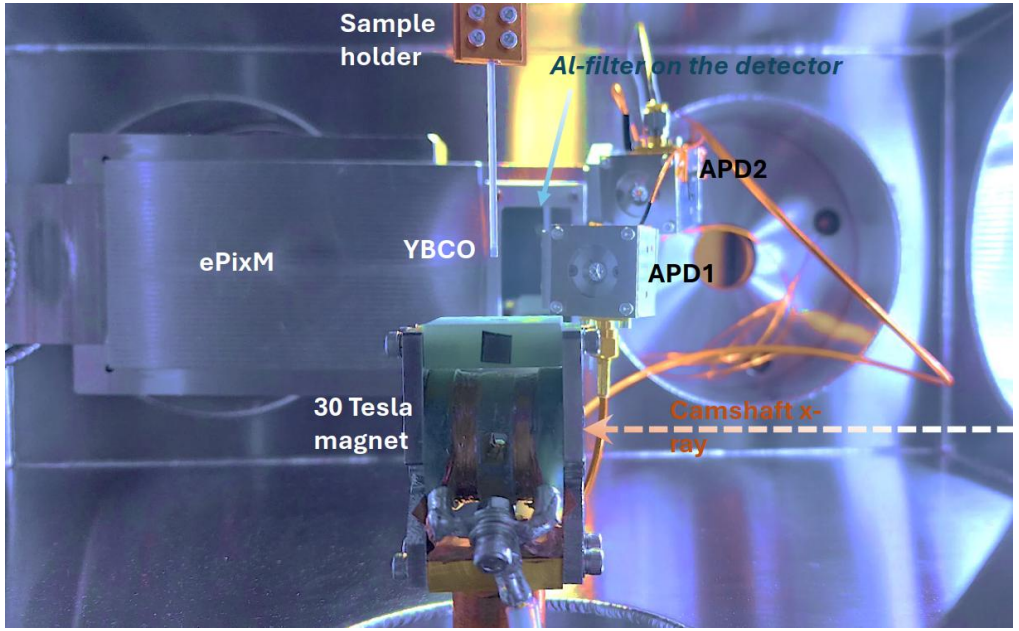


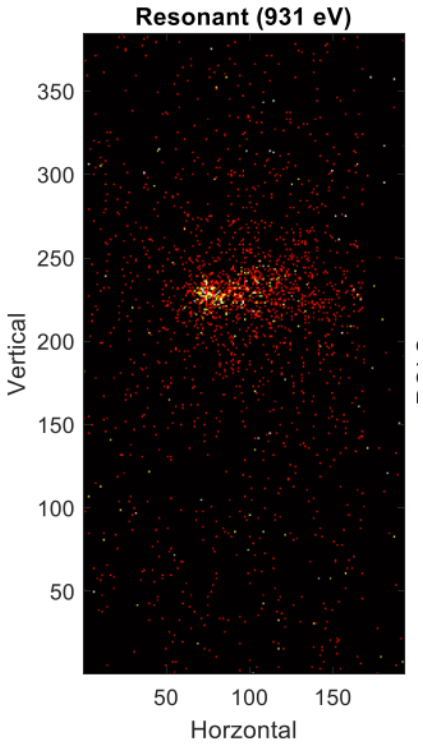




# ePixM camera



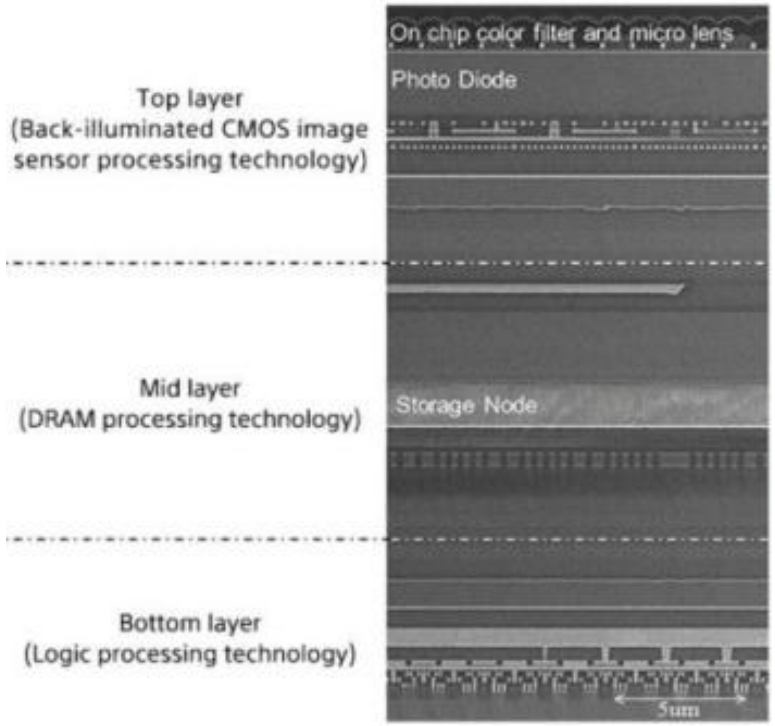


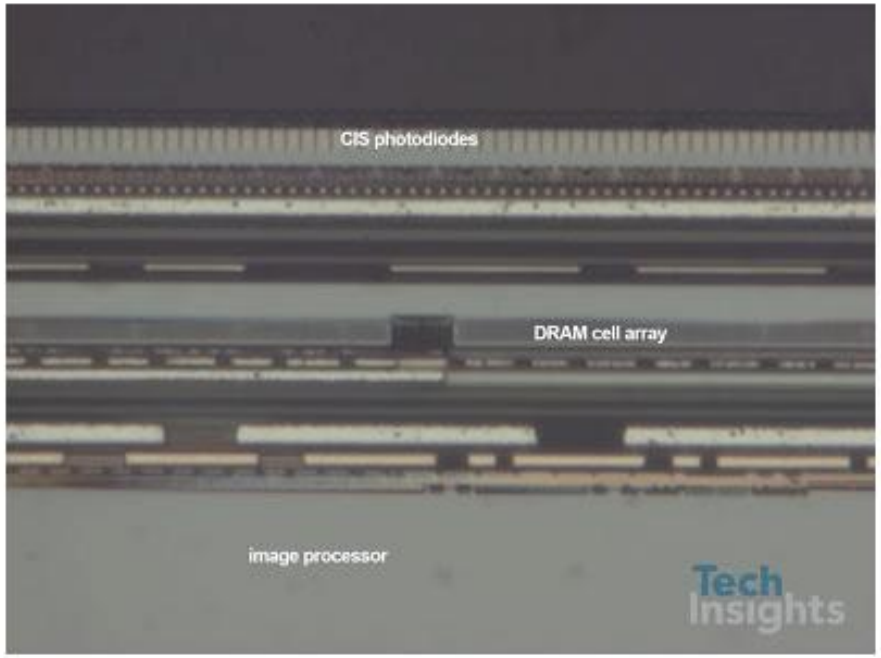
# Emerging technologies – 3D stacking

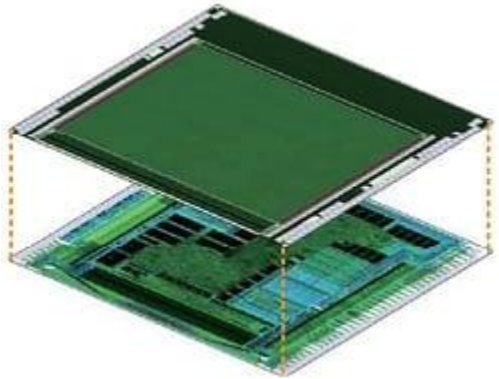
# 3D stacking in CMOS imaging technology

- 3D stacking at wafer level is now an established technology at major CIS fabs: Sony, Canon, TowerJazz, STMicroelectronics, *etc.*
- Wafer bonding can reduce interconnection capacitance between layers



Sectional view of 3-layer stacked CMOS image sensor with DRAM

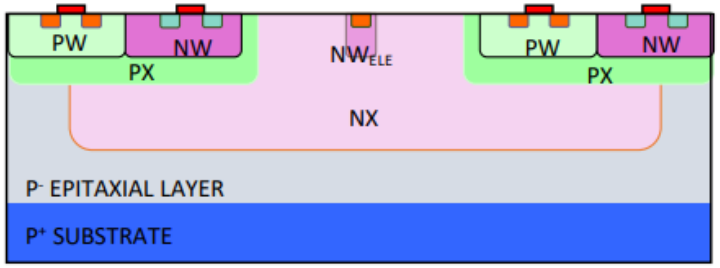


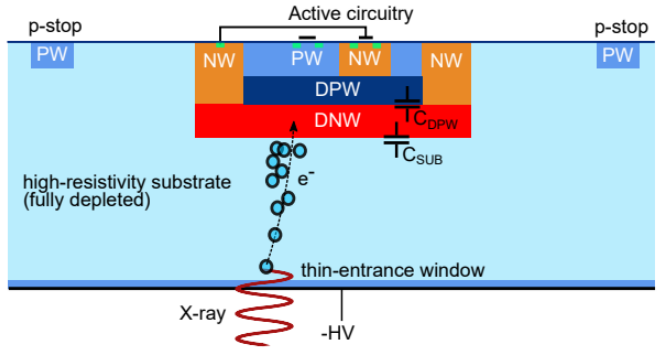





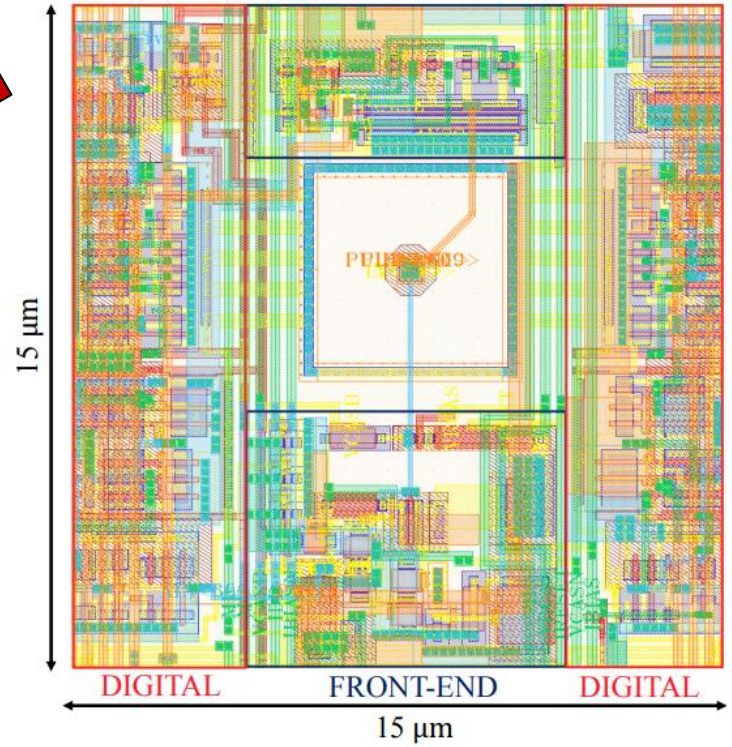
https://semiengineering.com/cmos-image-sensors-cis-past-present-future/
Sony ISSCC 2017

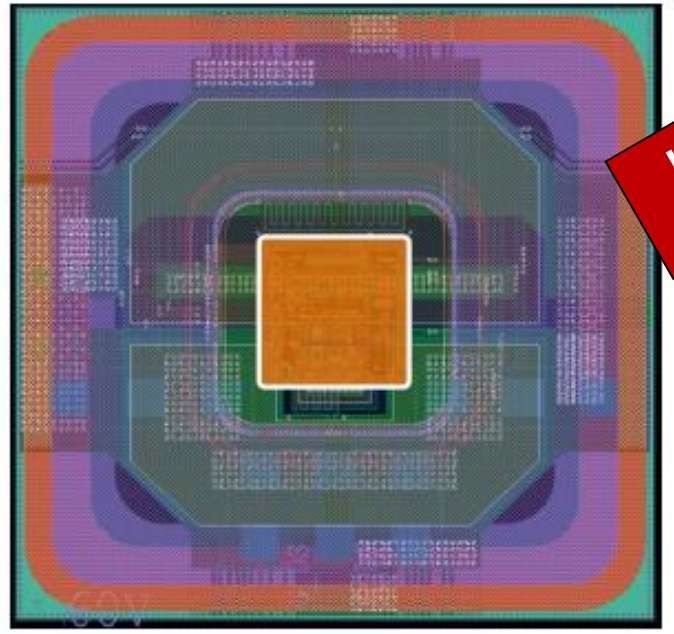
# Why 3D stacking?




Small collection electrode



Large collection electrode



T. Hatsui, Deployment status of CITIUS: https://www.bnl.gov/ifdeps/files/talks/takakihatsuis3.pdf

# Why 3D stacking?

- Optimized processes:
  - Top = imaging / detection layer
  - Bottom = analog / digital layer

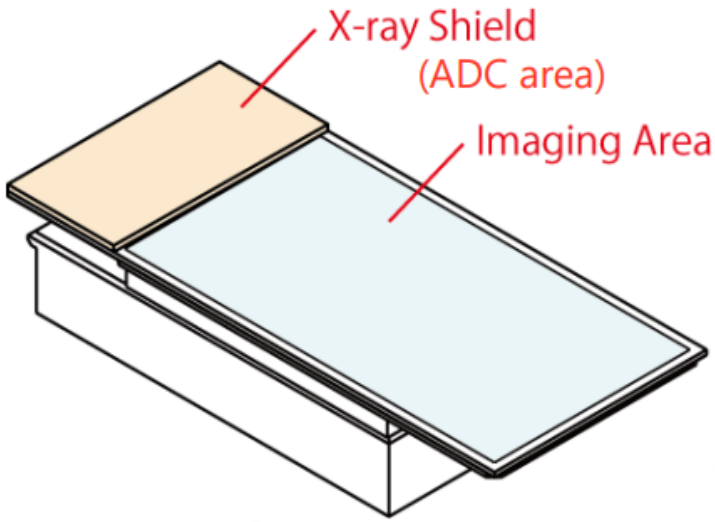
- **Strongly reduce trade-offs between layout of sensing node and readout electronics**
- **More metals for routing:**
  - **Better power supply**
  - **More logic density**

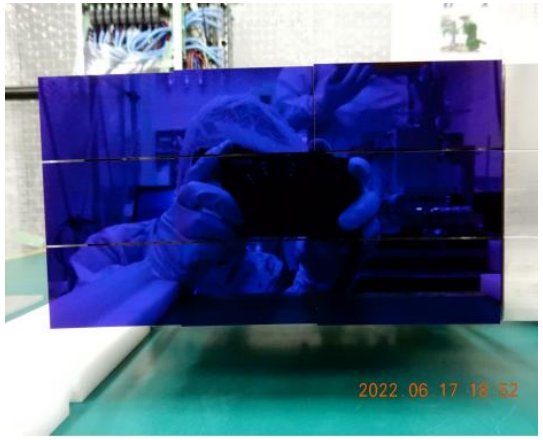
- **$$$, complexity, access to prototyping and small volume fabrication**



T. Hatsui, Deployment status of CITIUS: https://www.bnl.gov/ifdeps/files/talks/takakihatsuis3.pdf

# 3D stacking in X-ray imagers: CITIUS detector




## Stitching Lithography and 3D integration (by Sony Semiconductor Solutions)

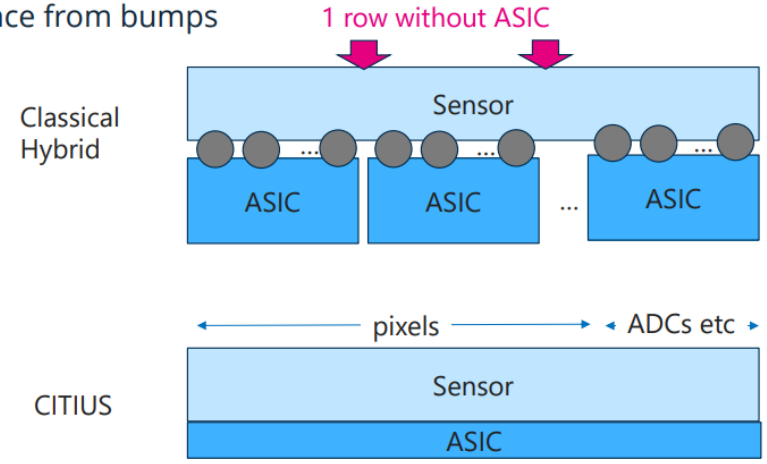
### Stitching Lithography

- technique to make chips larger than on lithography shot (> 30 mm)
- Widely used for camera with 35mm Full-frame Image Sensor

from https://electronics.sony.com/

### 3D integration

- no bumps results in uniform response for high-energy X-rays
- no fluorescence from bumps



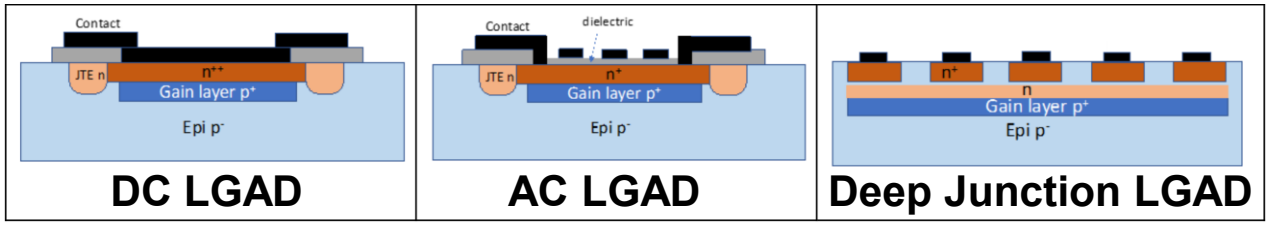


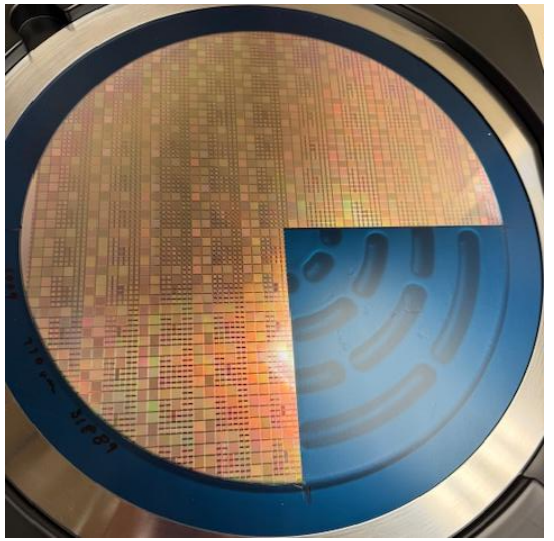


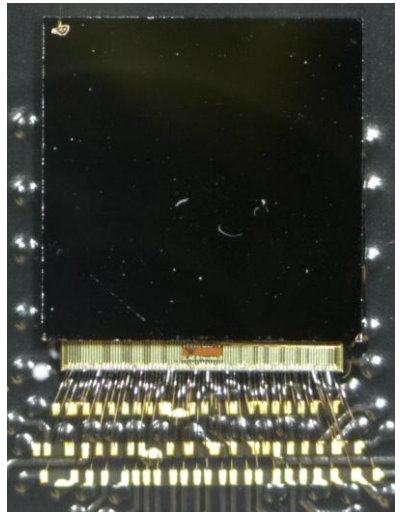

T. Hatsui, Deployment status of CITIUS: https://www.bnl.gov/ifdeps/files/talks/takakihatsuis3.pdf

# 3D stacking in HEP detectors: the ACCELERATE project

- **Goal: stack LGAD sensor with gain-layer + readout ASIC on advanced CMOS node**
- Development in partnership with Tower Semiconductor, FNAL, LLNL
- Full wafer run on 12” process: first time done with LGADs
- ~50 separate sensor structures: **pixel** arrays; **strip**; device **test structures**
- LGAD variants: **AC**, **Deep Junction (DJ)**, **Reach Through (RT)**

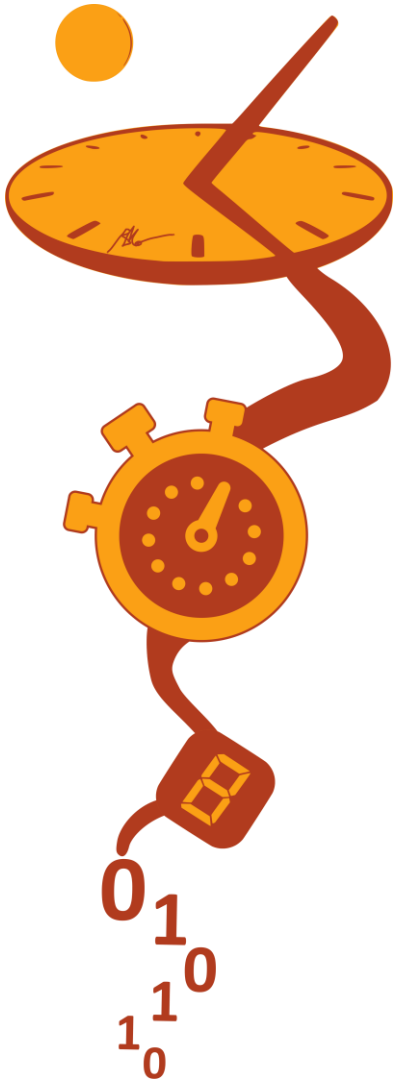




# MAPS for timing detectors

HEPiC Summer Week 2025



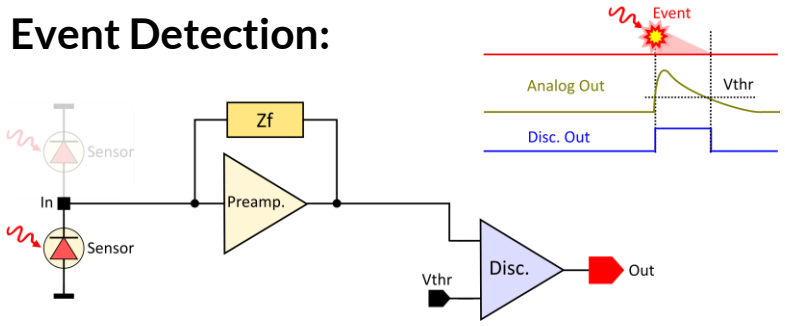

# Timing detectors for HEP

Bojan Markovic, SLAC National Accelerator Laboratory
*markovic@slac.stanford.edu*

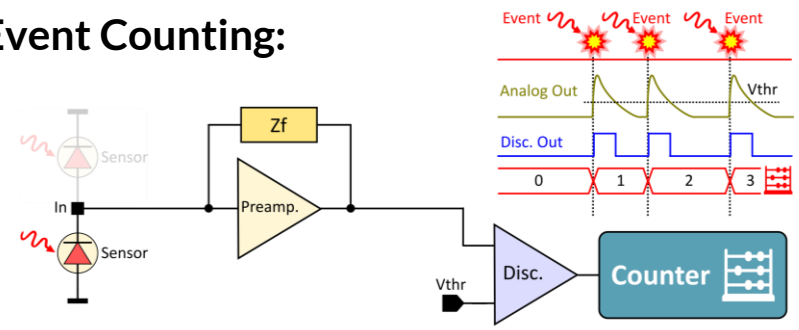
24 June 2025

# Detector front-end: what are we measuring?

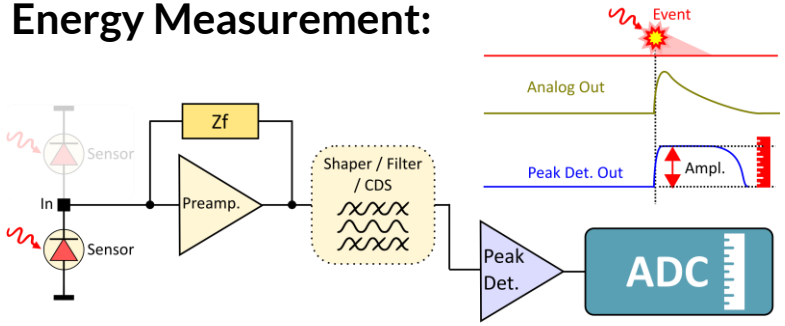
## Event Detection:



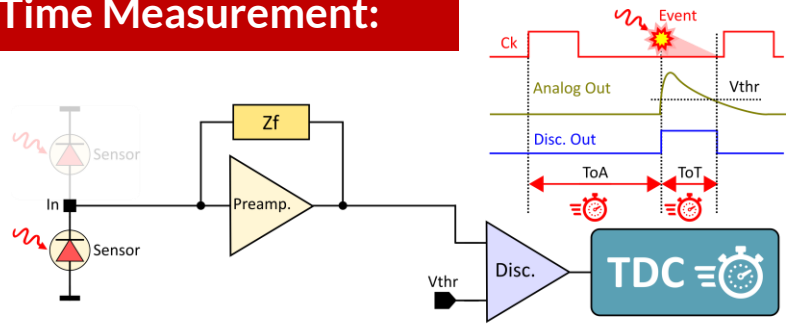

## Event Counting:




## Energy Measurement:

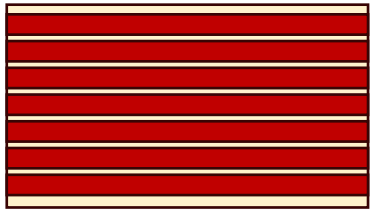



## Time Measurement:

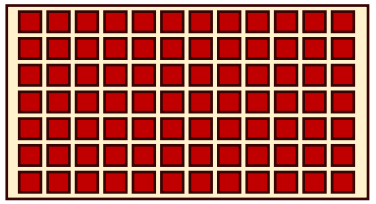



## Spatial Position:

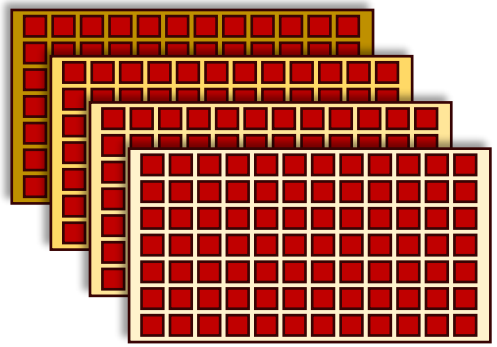
- Strips → 1D



- Pixels → 2D

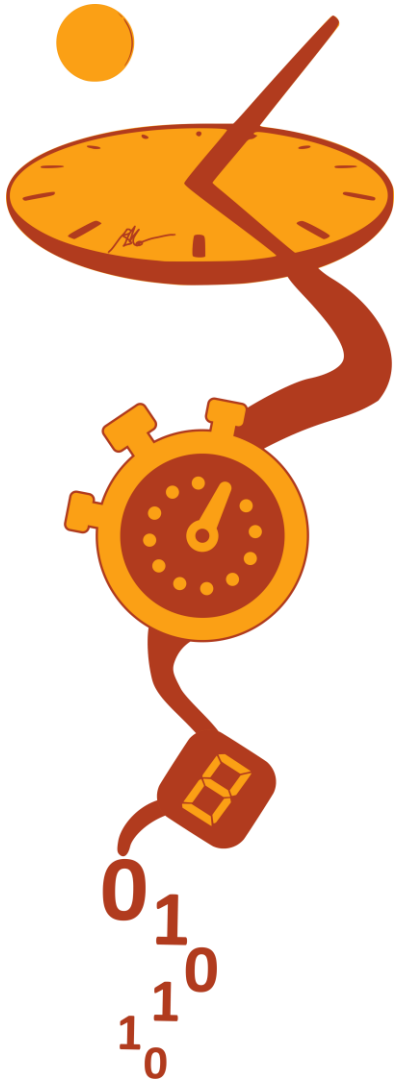


- Layers of pixels / strips → 3D

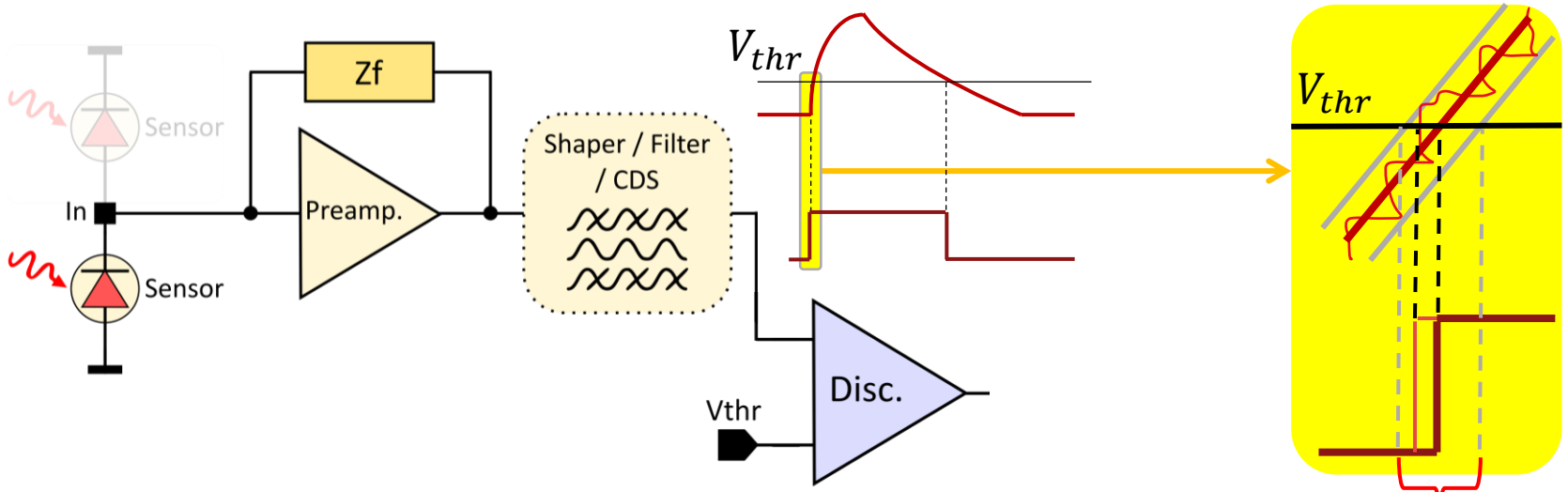


# Some terminology…

- **Time Measurement** is a lose term as time has no absolute physical properties to measure.
- What we are really measuring is the duration separating two events; thus, a more accurate term is **Time Interval Measurement**.
- Electronic high-precision time measurement circuits are called by different names: Time Interval Meters (TIM), time counters, time digitizers, **Time-to-Digital Converters (TDC)**.



# Detector front-end: time measurement







Temporal uncertainty; time noise → **jitter**

$$Jitter_{rms} = \frac{\sigma_V}{slope} \approx \frac{v_n G_v \sqrt{BW}}{\frac{Q_{in}/Z_f}{t_r}} \sim \frac{v_n (C_d + C_{in})}{Q_{in}} \frac{t_r}{\sqrt{t_p}} \sim \sqrt{t}$$

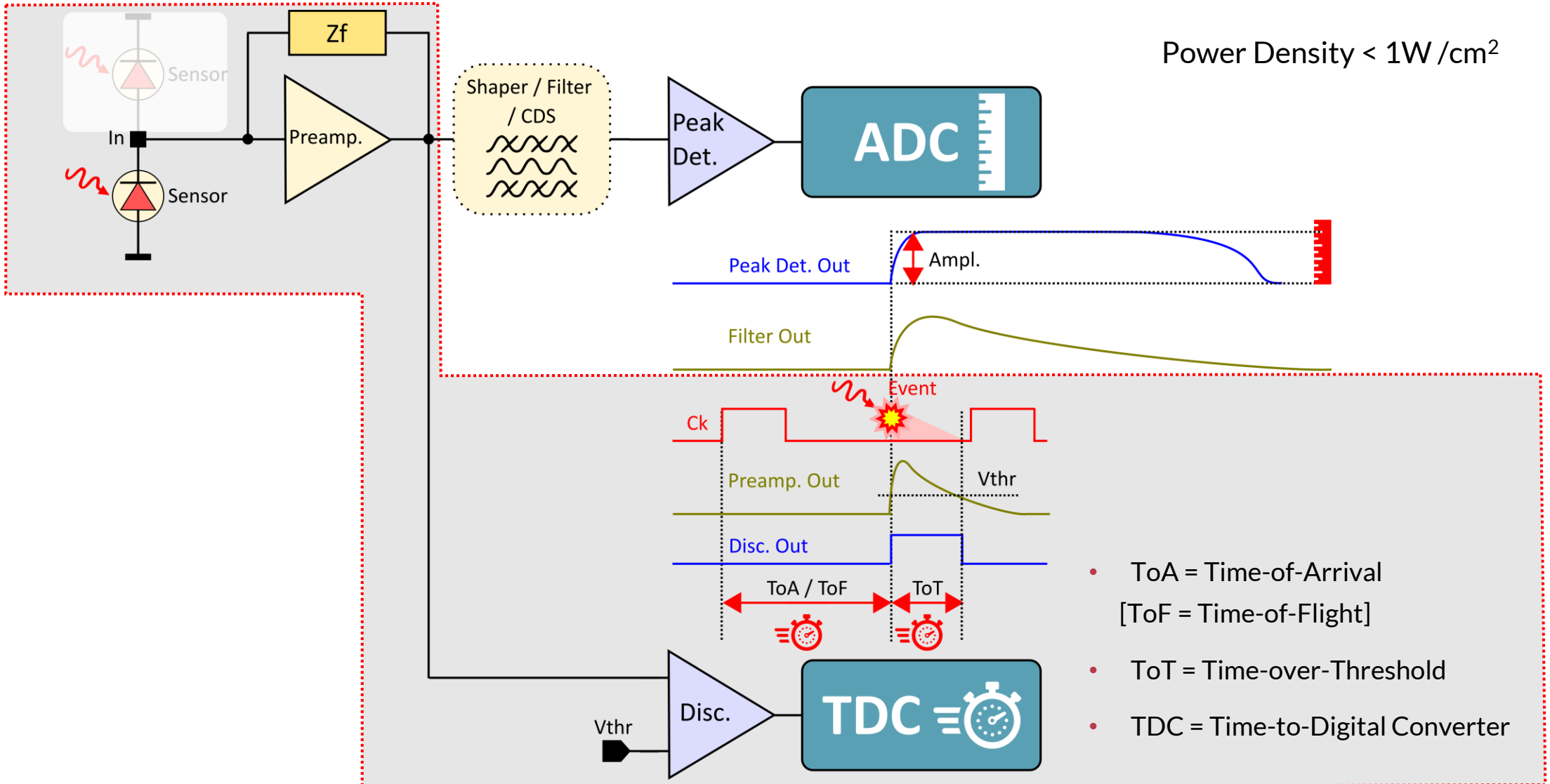
$\sqrt{t}$ → Faster = better

*up to what point?*

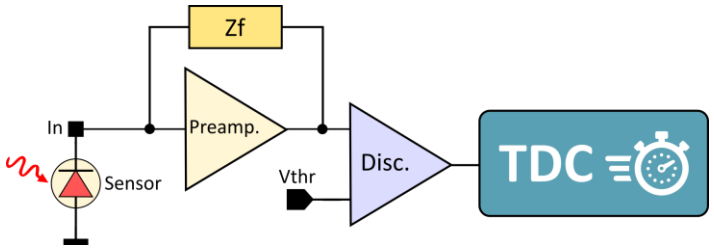
$$\frac{t_r}{\sqrt{t_p}} = \sqrt{\frac{t_p^2 + t_c^2}{t_p}} \quad \xrightarrow{minimum\ for:} \quad t_p = t_c$$

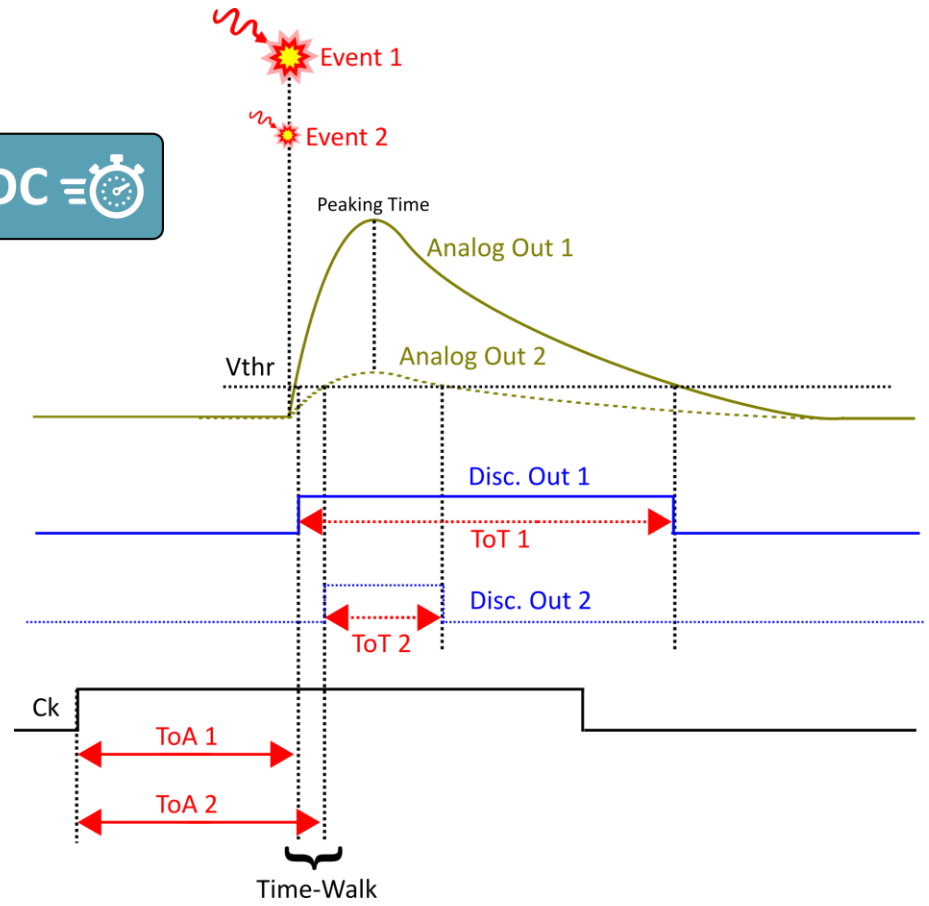
front-end shaping time equal charge collection time

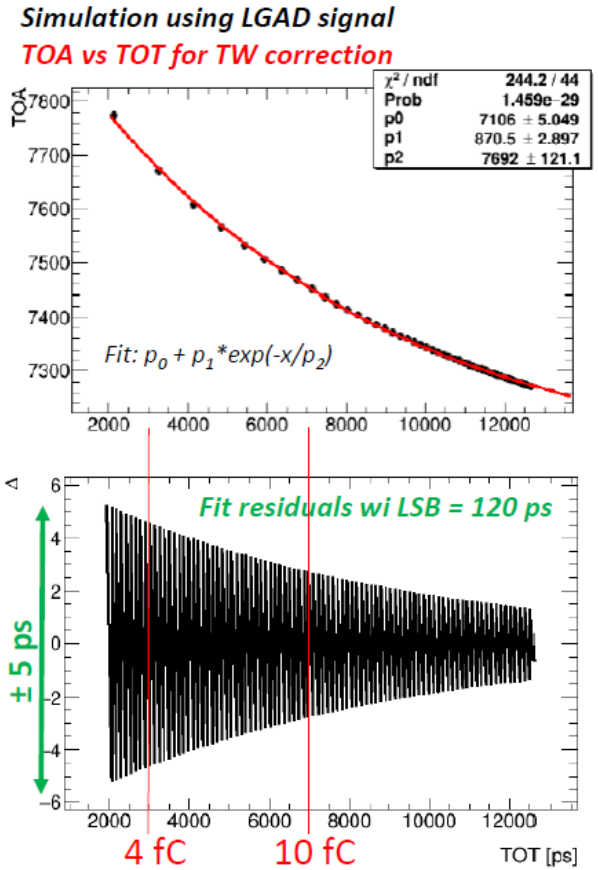
# Detector front-end: time / amplitude measurement



# Time-Walk, Time-over-Threshold (TOT)



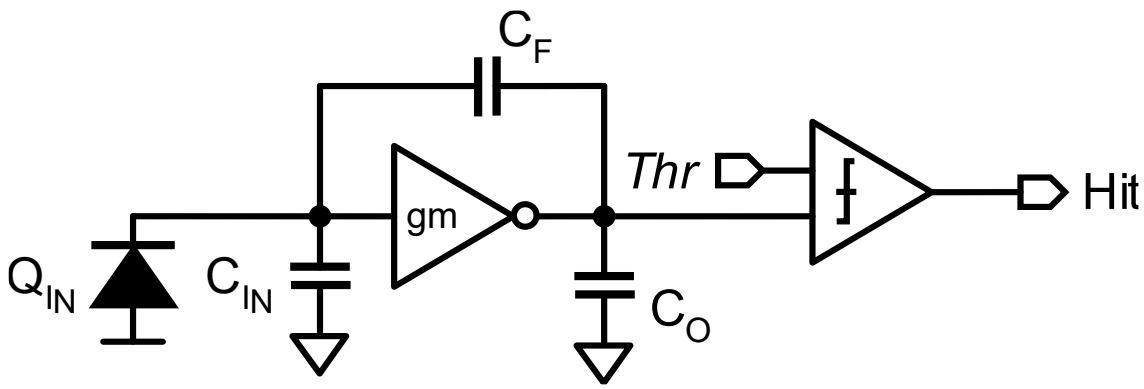




- ToT measurement (i.e., an indirect coarse measurement of amplitude) is used for offline Time Walk correction.
- Other ways of dealing with Time Walk exist (example: multiple thresholds) but are rarely used.

# Back to MAPS for timing detectors…

# Pixel front-end: timing basics




- Jitter in a front-end architecture with CSA [1]: $$Jitter = \frac{1}{Q_{\mathrm{in}}} q\, Enc \frac{C_O}{g_m}(1 + C_{\mathrm{IN}}/C_{\mathrm{FB}})$$
- Reducing jitter:
  - Increase power consumption → **limited power budget**
  - Reduce noise
  - Decrease ratio $C_{IN}/C_{FB}$

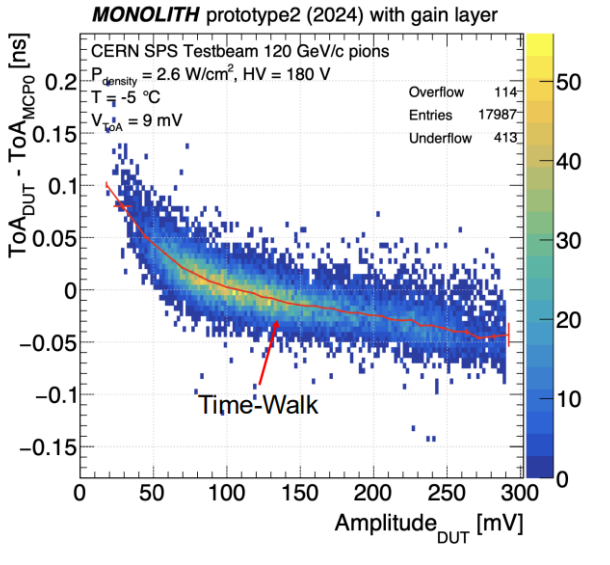
  **Trade-off: noise, timing performance, threshold dispersion**
  - Reduce capacitance at CSA output → **optimize circuit & adopt scaled CMOS nodes**
  - Time-walk is also reduced → **important if we want to gate the front-end**

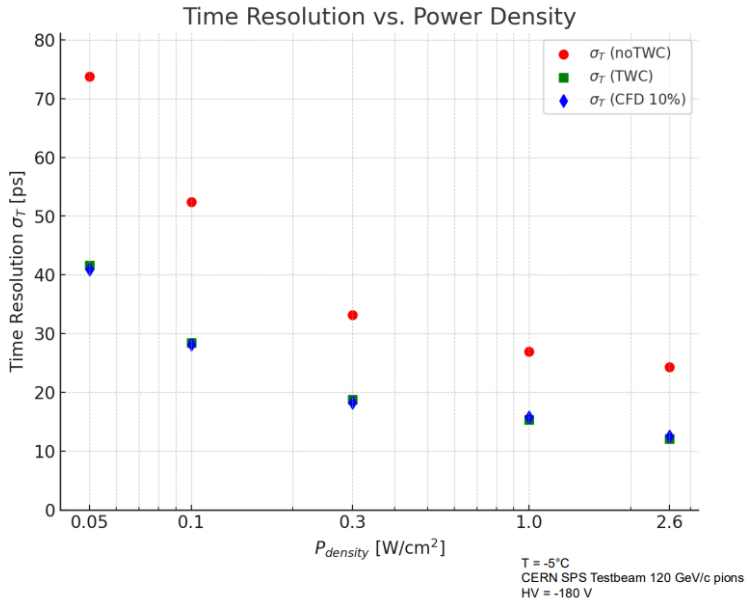


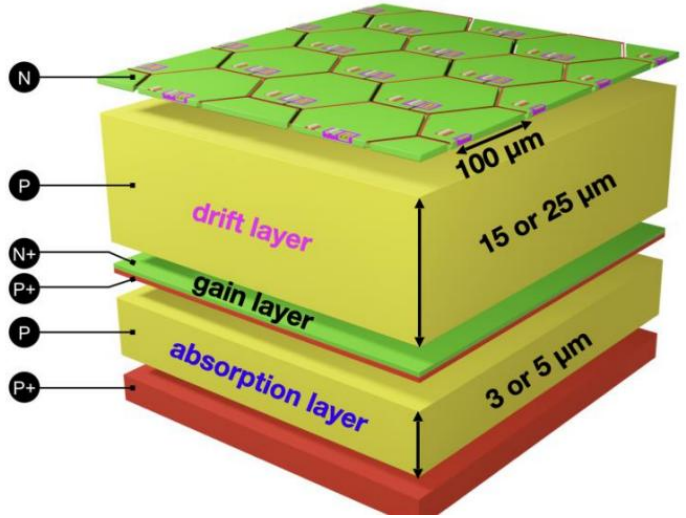
[1] https://doi.org/10.1016/j.nima.2022.167489
* assuming signal at CSA output >> threshold

# Timing MAPS: MONOLITH

$$Jitter = \frac{1}{Q_{\mathrm{in}}} q\, Enc \frac{C_O}{g_m}(1 + C_{\mathrm{IN}}/C_{\mathrm{FB}})$$




- IHP 130nm process with deep implants to implement gain layer in substrate
- SiGe HBT process offers higher efficiency: better $g_m$ for same current
- Monolith prototype 2, with electronics outside the pixels, achieved excellent timing performance: **<30 ps time resolution** even without Time Walk Correction

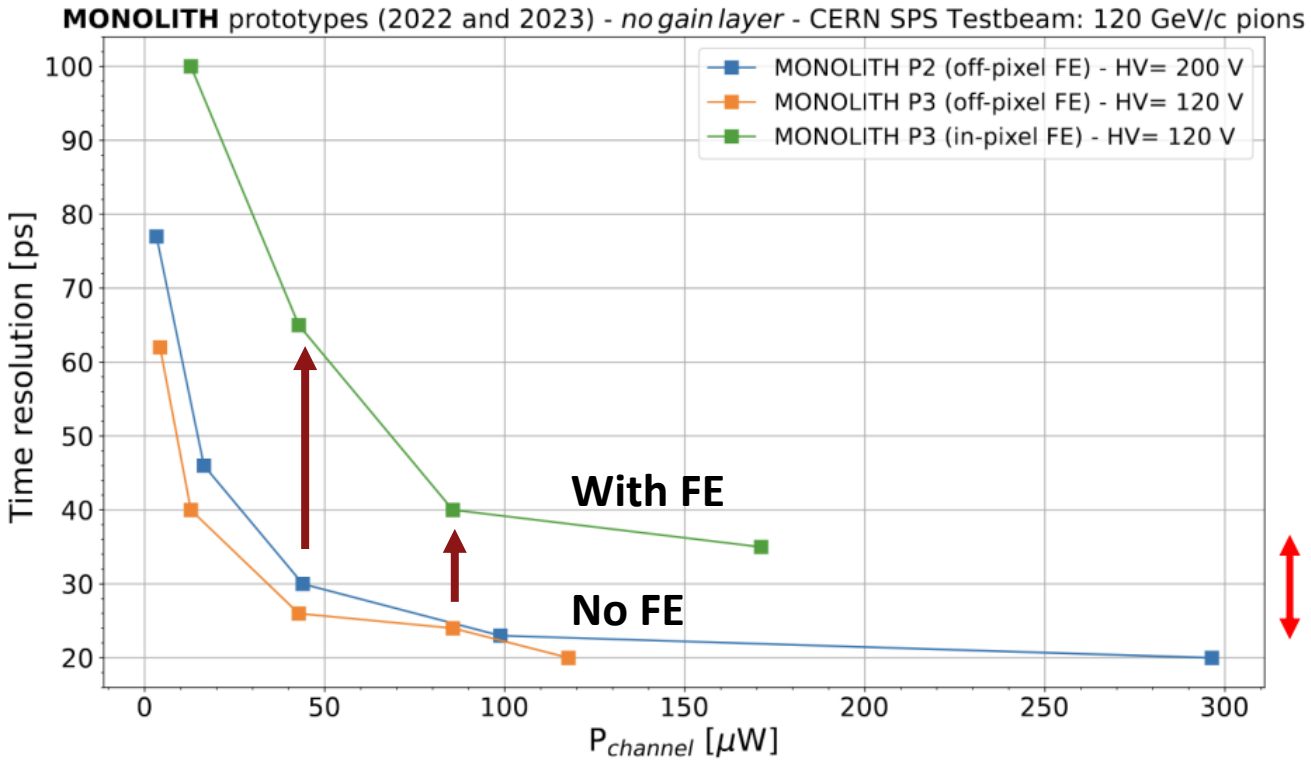


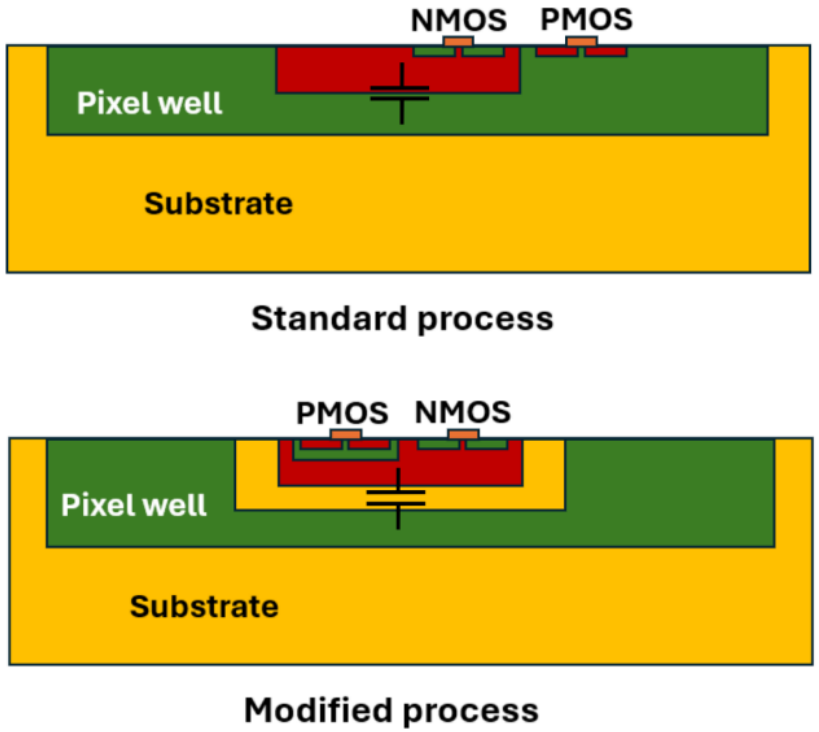
[1] L. Paolozzi, Front-End Electronics Workshop 2026

**30 ps @ 300 mW/cm²**

# Timing MAPS: MONOLITH

$$Jitter = \frac{1}{Q_{in}} q\, Enc \frac{C_O}{g_m}(1 + C_{IN}/C_{FB})$$




- When front-end circuitry is implemented inside the pixel, performance is affected
- Solution to mitigate by additional well to isolate transistors well from collecting electrode

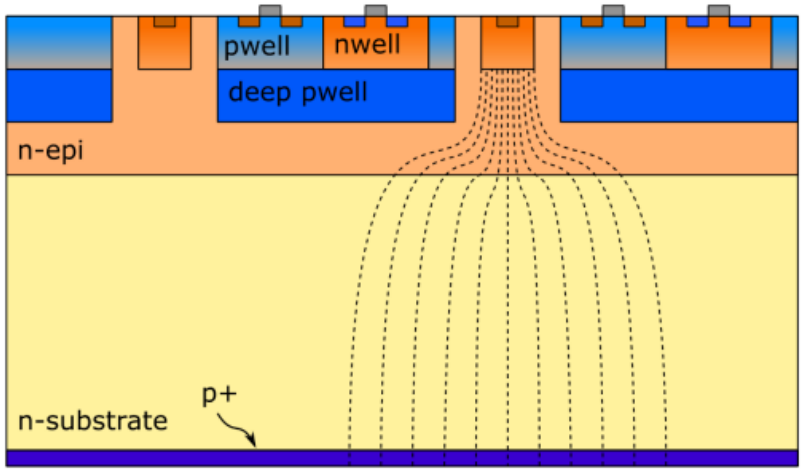


[1] L. Paolozzi, Front-End Electronics Workshop 2026

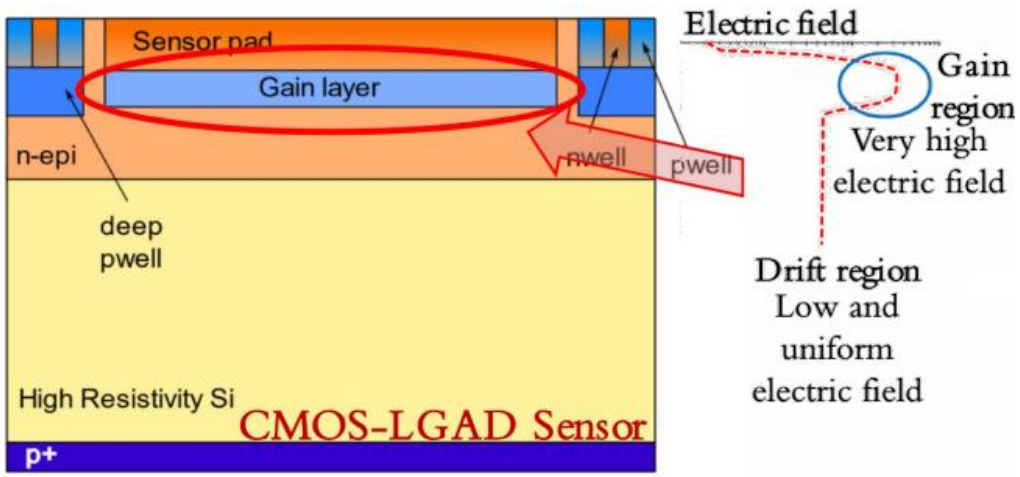
**~30 ps @ 700 mW/cm²**

# Timing MAPS: MadPix / Arcadia

$$Jitter = \frac{1}{Q_{\mathrm{in}}} q\, Enc \frac{C_O}{g_m}(1 + C_{\mathrm{IN}}/C_{\mathrm{FB}})$$




Standard ARCADIA sensor, small collection electrode




MadPix sensor with large electrode and gain layer

- LFoundry 110nm process, modified for timing applications: ALICE 3 TOF layer
- Achieved 80ps, working towards 20ps with 15um thickness and better control of gain layer

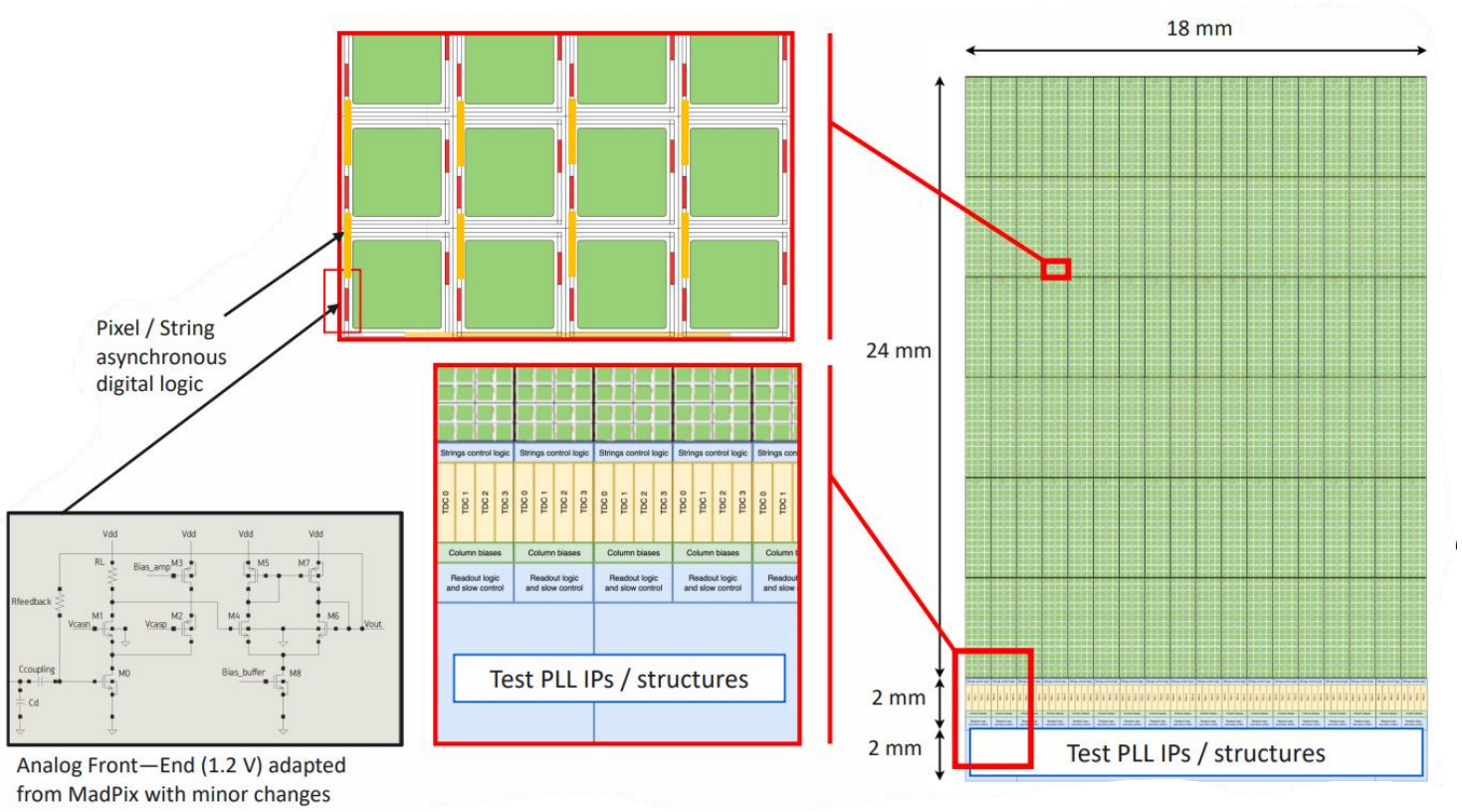


[1] V. Pagliarino, Front-End Electronics Workshop 2026

**~30 ps @ 320 mW/cm$^2$ (planned)**

# Timing MAPS: MadPix / Arcadia

$$Jitter = \frac{1}{Q_{in}} q\, Enc \frac{C_O}{g_m}(1 + C_{IN}/C_{FB})$$




**200 uA / pixel**

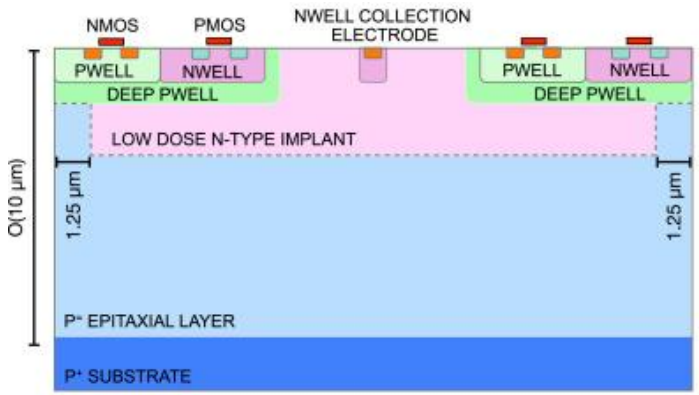
- Large collection electrode with gain layer does not allow to place circuitry inside the pixels (250um pitch)
- Approach: move circuitry in-between collection pads, implement TDCs at the periphery

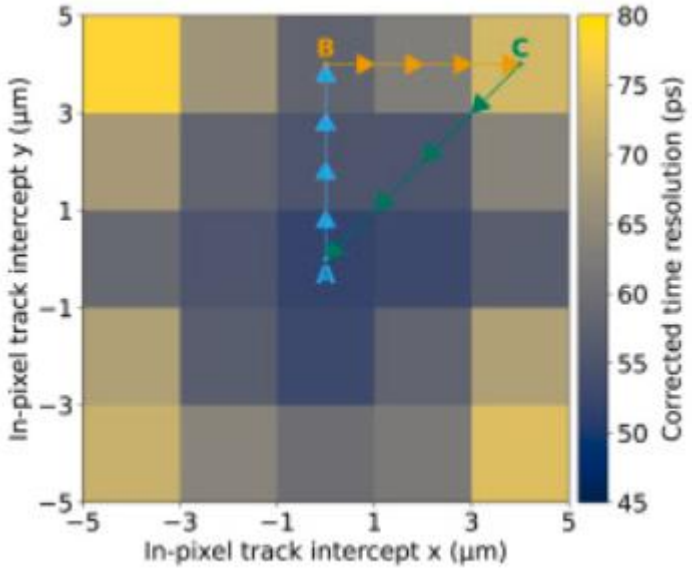
[1] V. Pagliarino, Front-End Electronics Workshop 2026

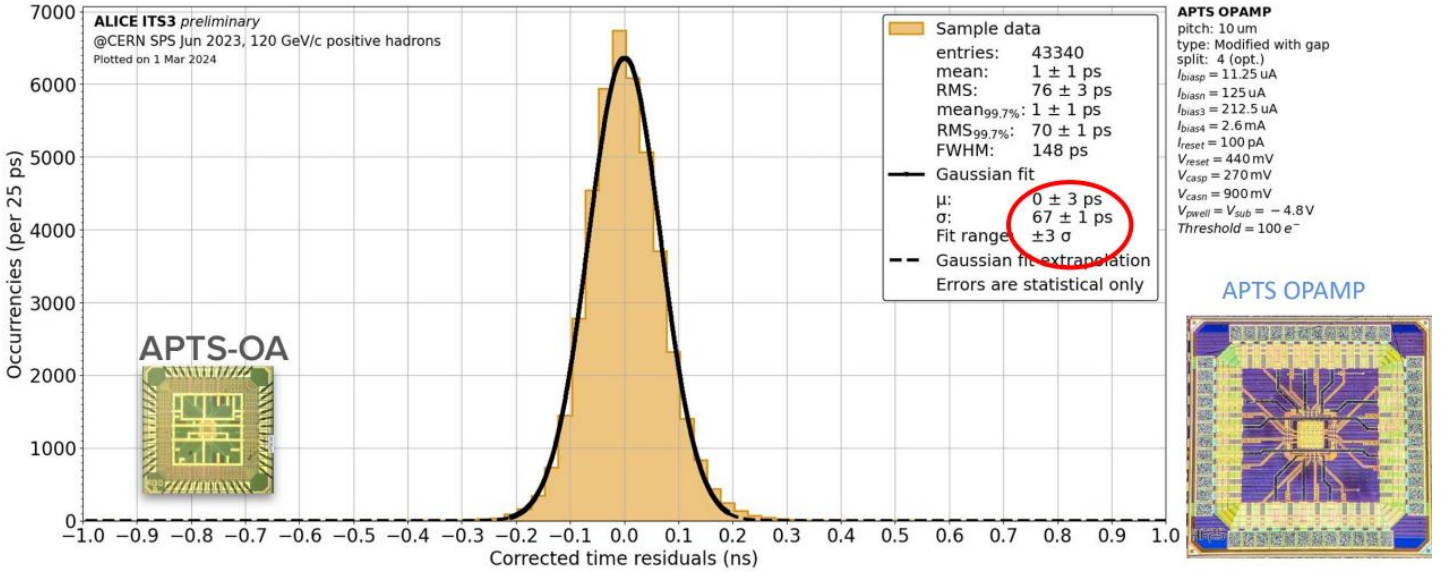
**~30 ps @ 320 mW/cm$^2$ (planned)**

# Timing MAPS: TPSCo 65nm?

$$Jitter = \frac{1}{Q_{\mathrm{in}}} q \boxed{Enc} \frac{C_O}{g_m} (1 + \boxed{C_{\mathrm{IN}}}/C_{\mathrm{FB}})$$




APTS OPAMP



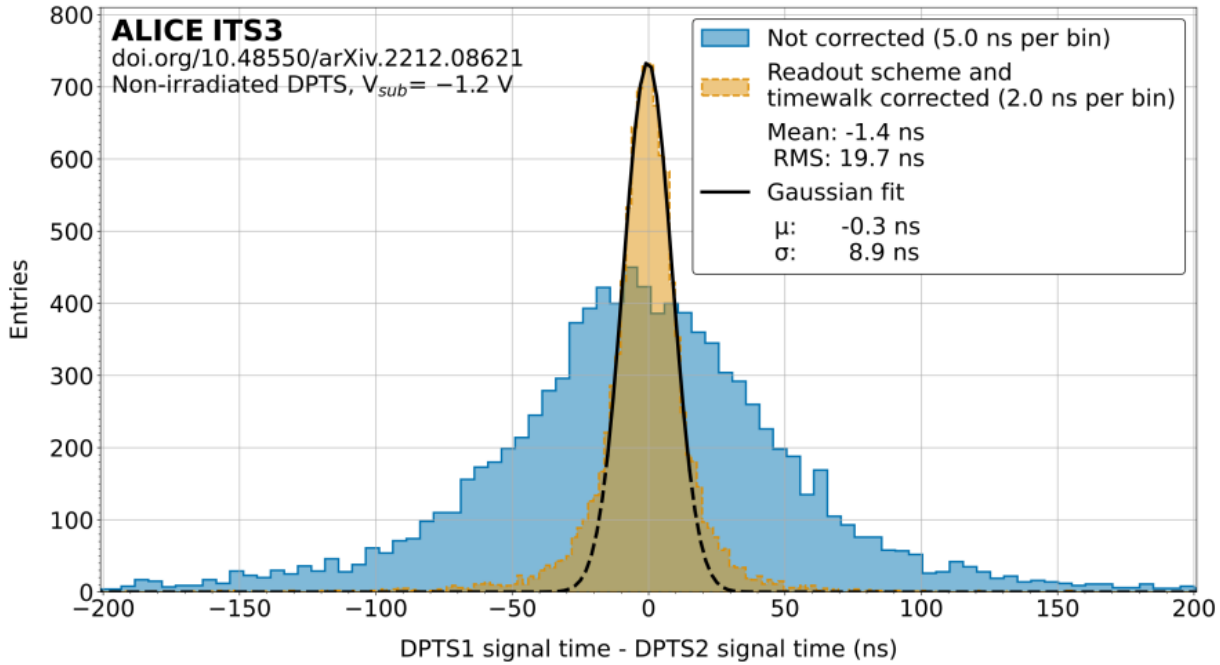
doi/10.1016/j.nima.2024.170034

- 10 um pixel, sensor only
- Time-walk and cluster size correction to correct for non-uniformity of electric field

# Timing MAPS: TPSCo?

$$Jitter = \frac{1}{Q_{\mathrm{in}}} q \boxed{Enc} \frac{C_O}{g_m} (1 + \boxed{C_{\mathrm{IN}}}/C_{\mathrm{FB}})$$

## Sensor + Front end (DPTS)



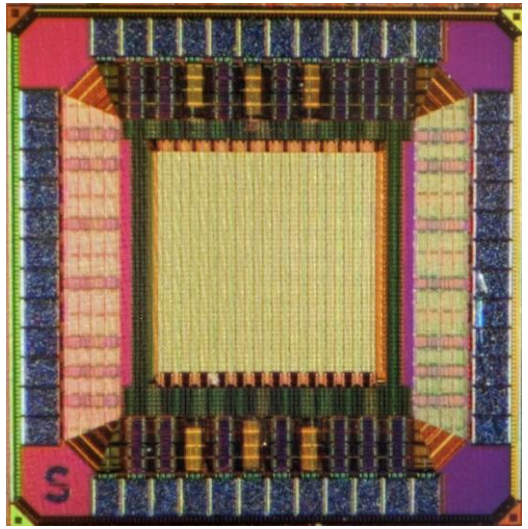

**~6 ns timing resolution** **(~30 ns not corrected)**

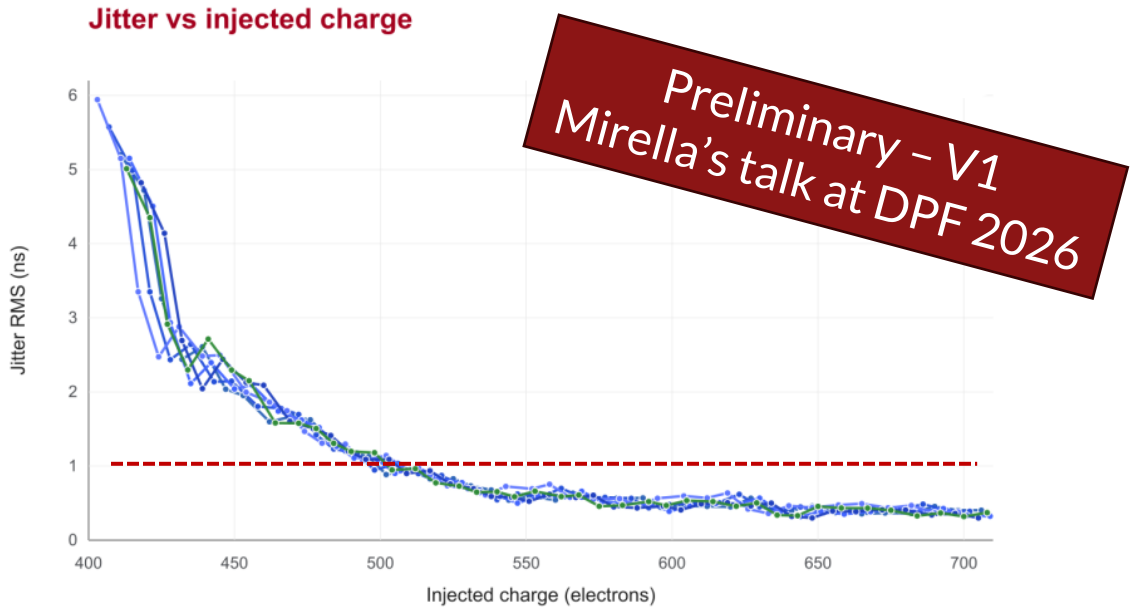
**~120 nW in-pixel**

- Note: DPTS is not a Front-End optimized for timing

# NAPA: exploring timing on TPSCo

$$Jitter = \frac{1}{Q_{\text{in}}} q \, Enc \frac{C_O}{g_m} (1 + C_{\text{IN}}/C_{\text{FB}})$$

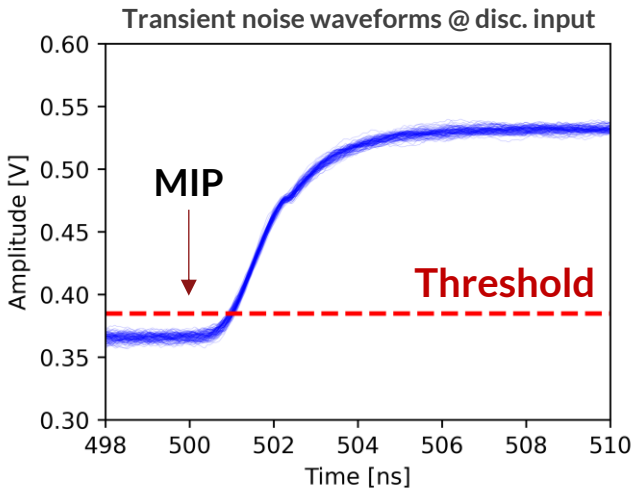


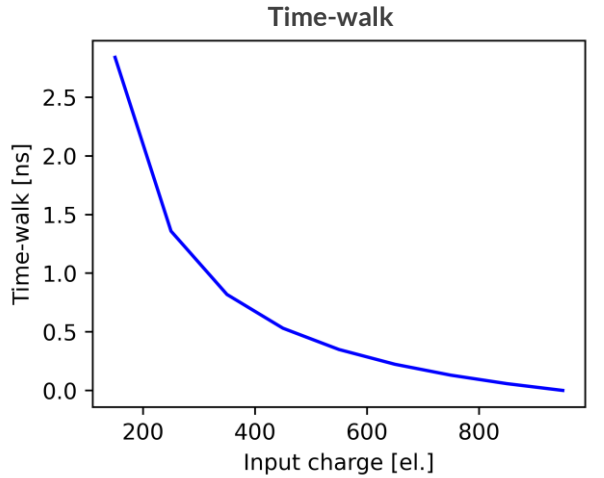



- **Goal of NAPA project @ SLAC:**
  - explore timing resolution with TPSCo 65nm technology
  - Focus on long term R&D targeting requirements at e+e- colliders, in particular O(ns) timing
  - Power consumption compatible with large area, low material budget

# NAPA: can we get to sub-100 ps timing?

- **Pushing the pixel front-end towards fast timing:**
  - ENC: 16 $e^-$
  - Jitter: 36.8 ps
  - Current: **2.6 µA / pixel**
  - Timewalk: 3 ns → **sets the "gating" / "integration time" accuracy**





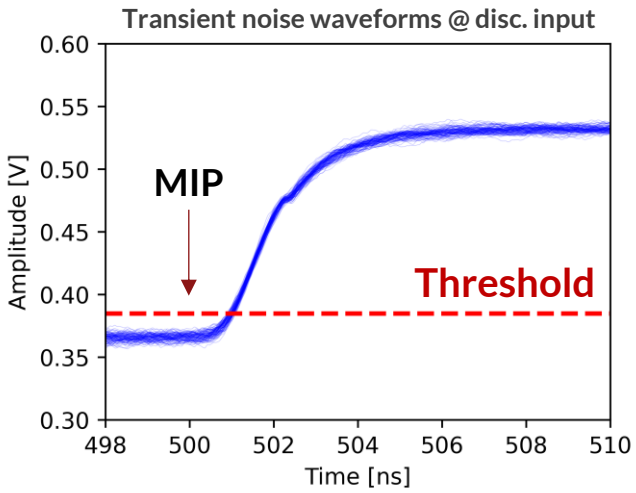

* $Q_{in}$ = 550 $e^-$ with $t_{rise}$=1ns, $C_{FB}$ = 0.35 fF, $C_{DET}$ = 2.5 fF, typical, 100 MC tnoise with noise$f_{max}$ 20 GHz, no Landau

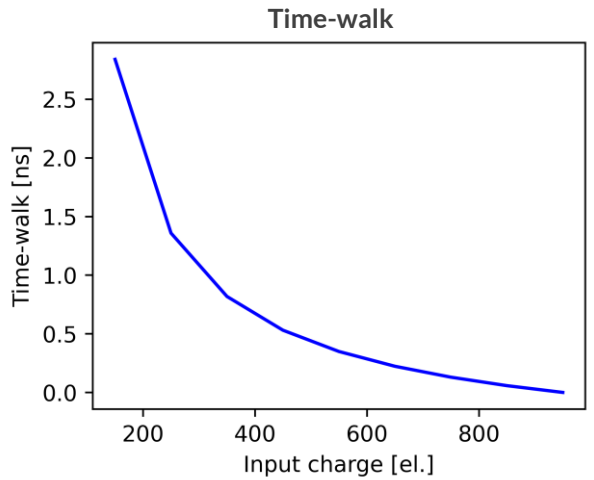
# NAPA: can we get to sub-100 ps timing?

- **Pushing the pixel front-end towards fast timing:**
  - ENC: 16 $e^-$
  - Jitter: 36.8 ps
  - Current: **2.6 µA / pixel**
  - Timewalk: 3 ns → sets the "gating" / "integration time" accuracy

→ **At 10 um pixel pitch: 3 W/cm$^2$ !!!!!!**

Need further optimization of sensor and/or power-pulse the chip



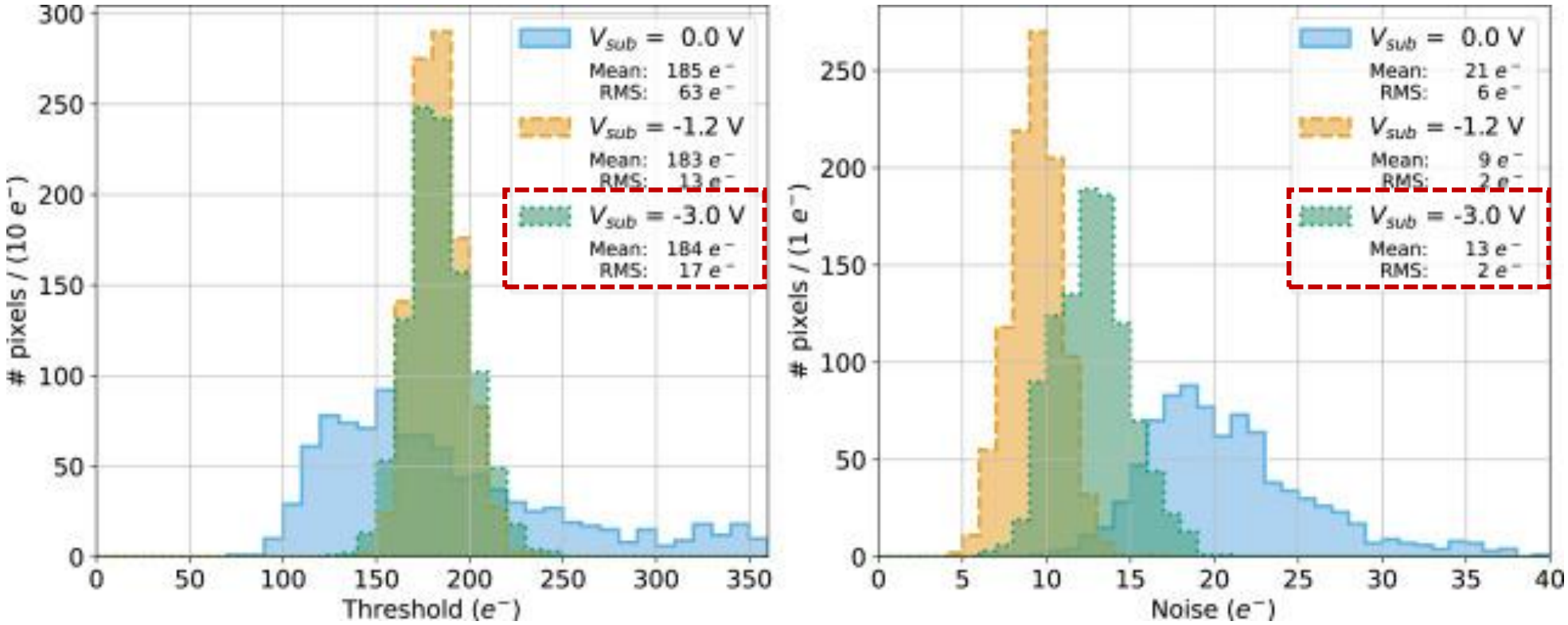






* $Q_{in}$ = 550 $e^-$ with $t_{rise}$=1ns, $C_{FB}$ = 0.35 fF, $C_{DET}$ = 2.5 fF, typical, 100 MC tnoise with noise$f_{max}$ 20 GHz, no Landau

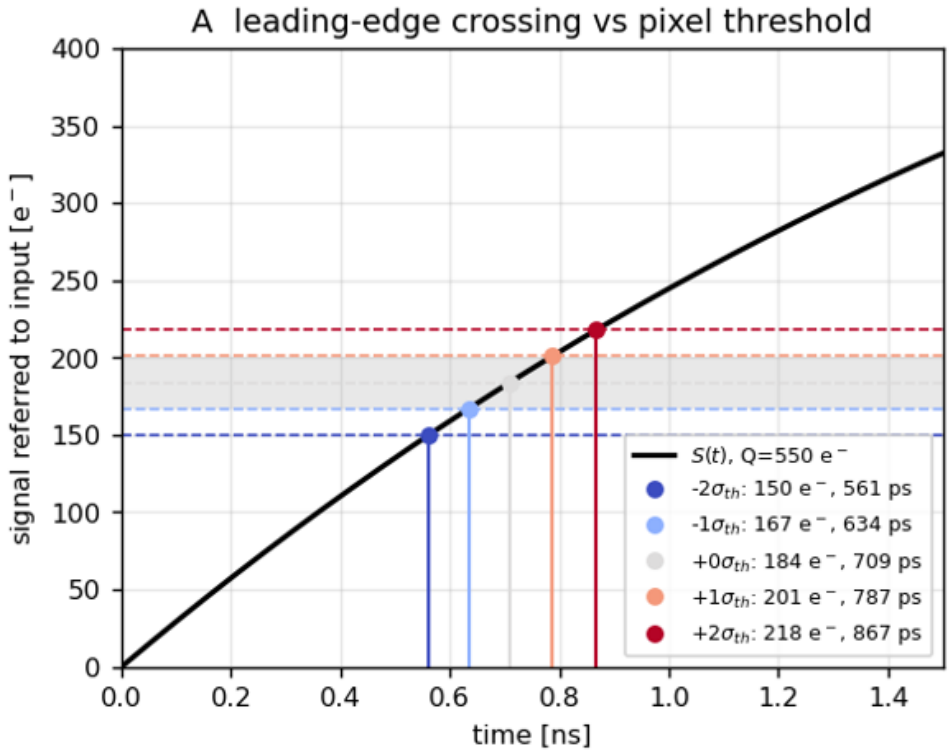
# Can we get sub-100ps timing on the whole pixel matrix?

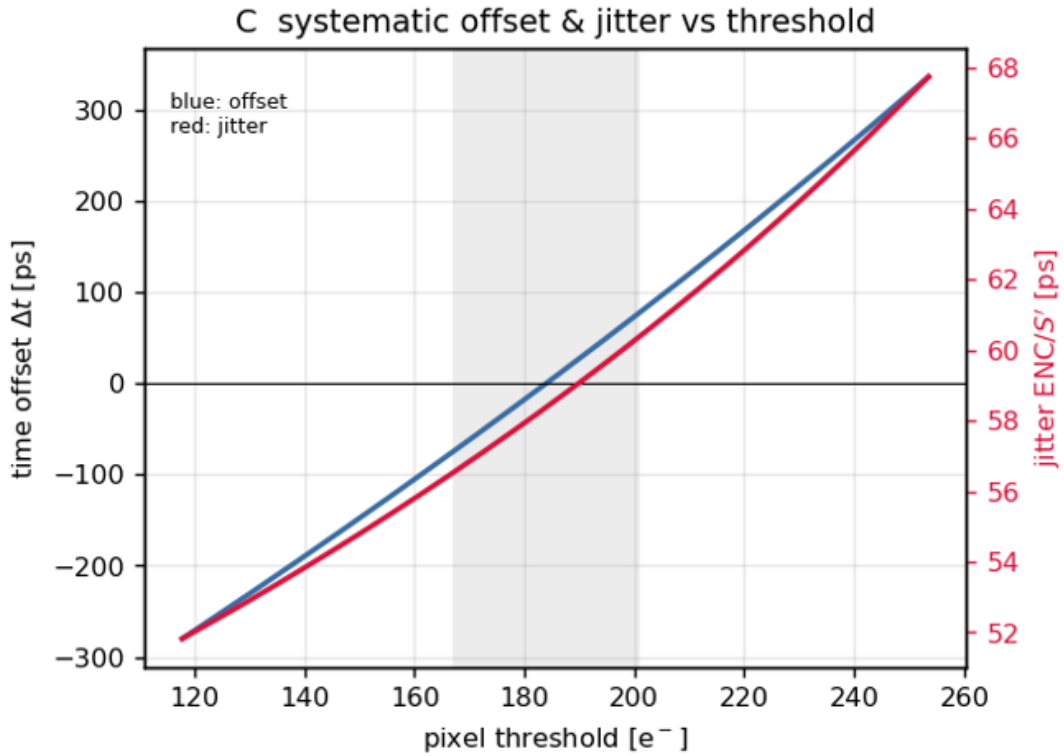
Let's take the numbers from DPTS as starting point to estimate what happens over a large area…



# Sub-100ps timing on the whole pixel matrix?

A quick numerical simulation…



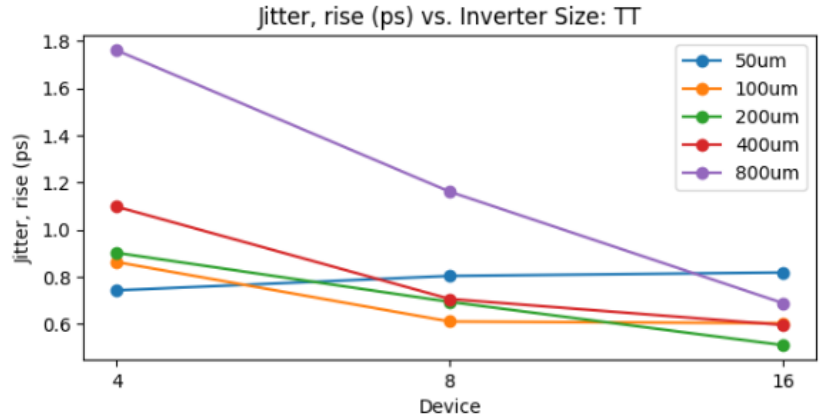




**Controlling precisely the threshold in every pixel is a must in timing detectors!**

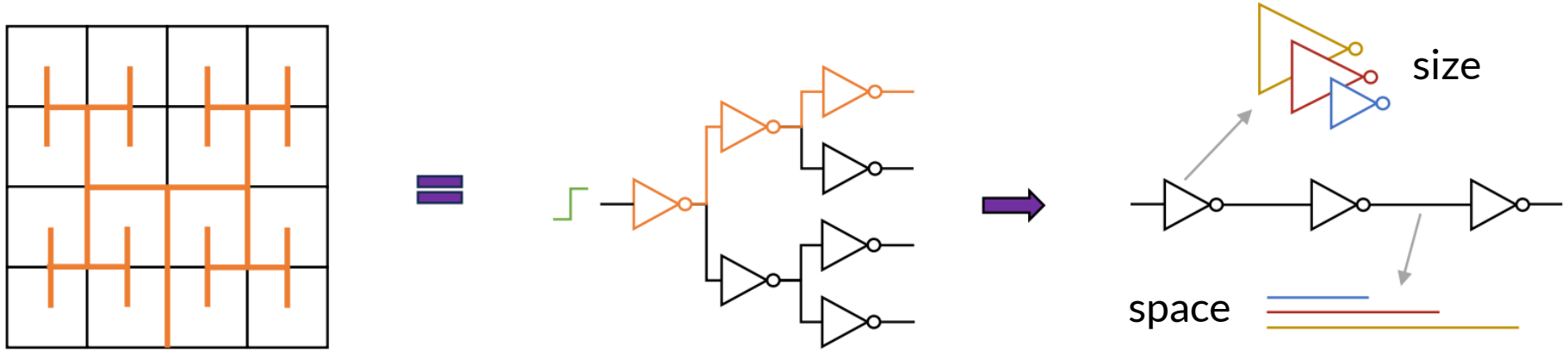
# Clock & timing signal distribution

*M. Zeng (Stanford - HEPIC), B. Markovic*

- Clock & signal distribution network strategy based on H-tree
- Evaluate performance for different buffer size & spacing
- Assuming a 256x256 matrix of 50 µm “macro pixels”:
  - Jitter*: **<2 ps**
  - Power consumption @ 100 kHz clock freq: **0.1 mW/cm$^2$**
  - **Power scales linearly with frequency!**




| | 4 | 8 | 16 |
|---|---|---|---|
| 50um | 0.7434 | 0.8045 | 0.8192 |
| 100um | 0.8632 | 0.6114 | 0.6040 |
| 200um | 0.9024 | 0.6945 | 0.5111 |
| 400um | 1.0980 | 0.7067 | 0.5967 |
| 800um | 1.7607 | 1.1616 | 0.6896 |





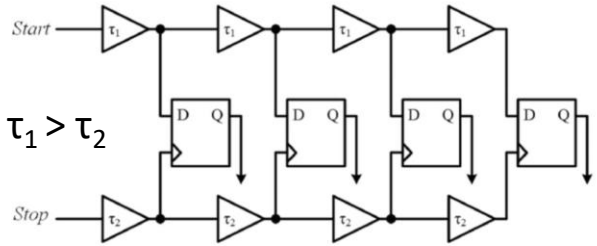

**simulated <2ps at post-layout & transient noise on supply/ground nets*

# TDC Architecture

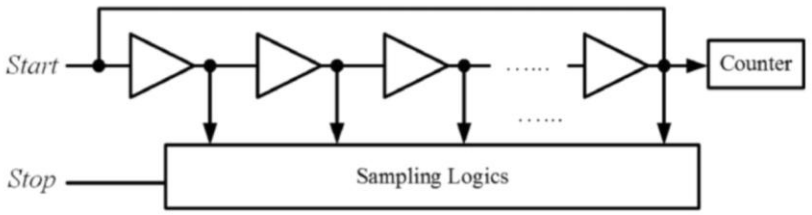
*A. Duncanson, M. Zeng (Stanford - HEPIC), B. Markovic*

- Multiple pixel analog front-ends connected to one TDC
- HIT information from pixel → **START conversion signal**
- Clock → **STOP signal**
- Time-to-Digital Converter (TDC) architecture [1]:
  - Vernier Delay line: high resolution ($\tau_1$ - $\tau_2$)
  - Ring Oscillator: large dynamic range due to counter

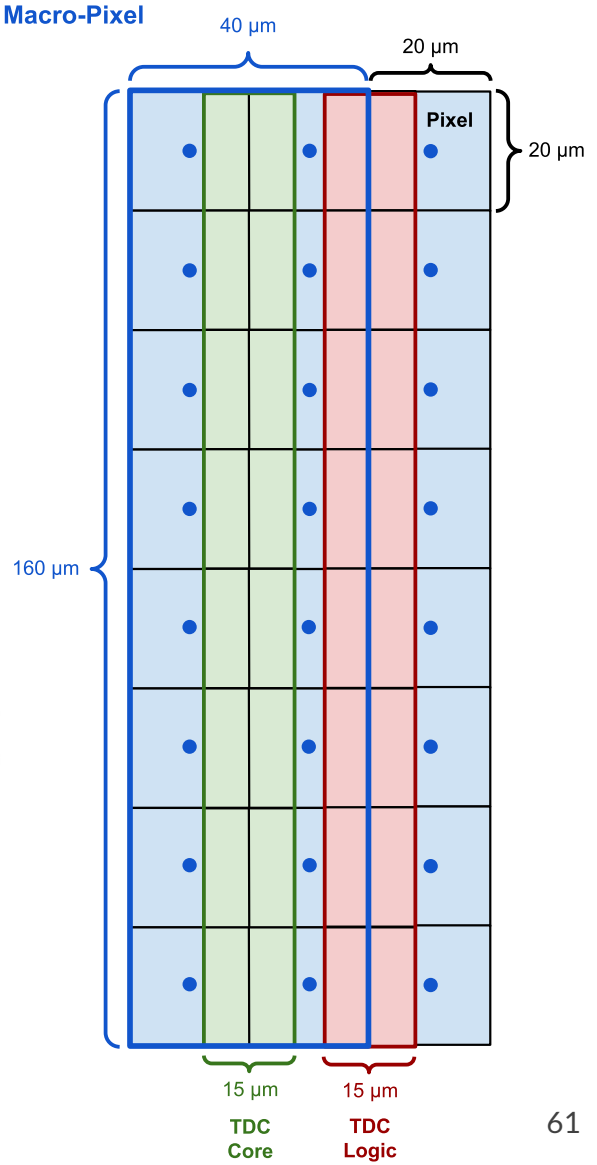
**Why?**




**Vernier Delay Line**




**Ring Oscillator (RO)**

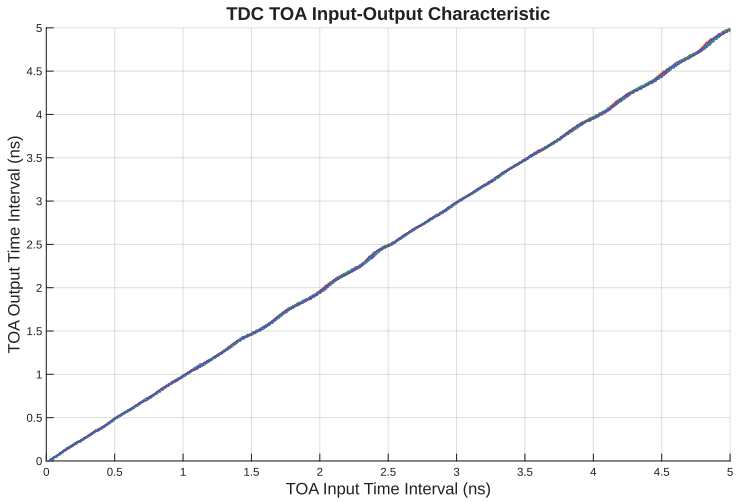


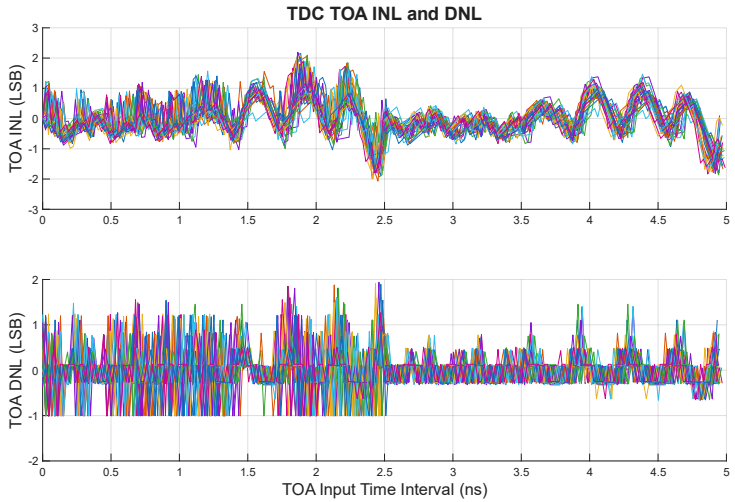

[1] Chang et al. 2016

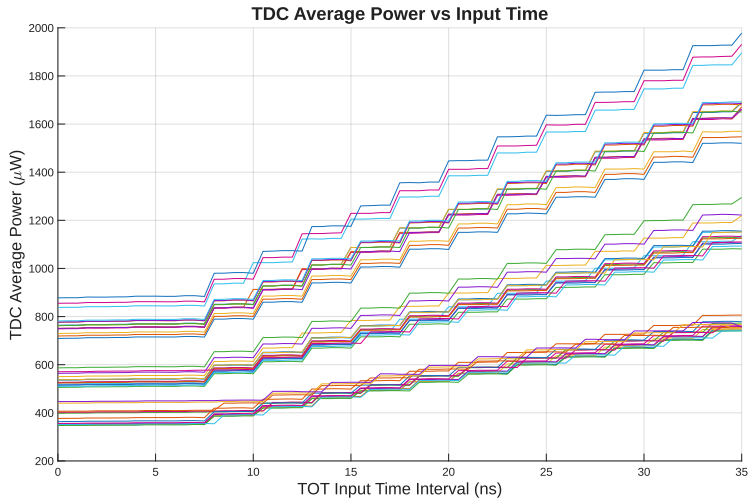
# TDC: Post-layout simulations

*A. Duncanson (Stanford - HEPIC), B. Markovic*

## TOA Simulations Across Corners[1]




- **TOA resolution:** 20 ps
- **TOT resolution:** 2.5 ns
- **Power consumption:**
  - If no HIT: only static power consumption due to leakage
  - If HIT: 6 µW assuming continuous conversion every 10 µs → scaled by macro-pixel occupancy

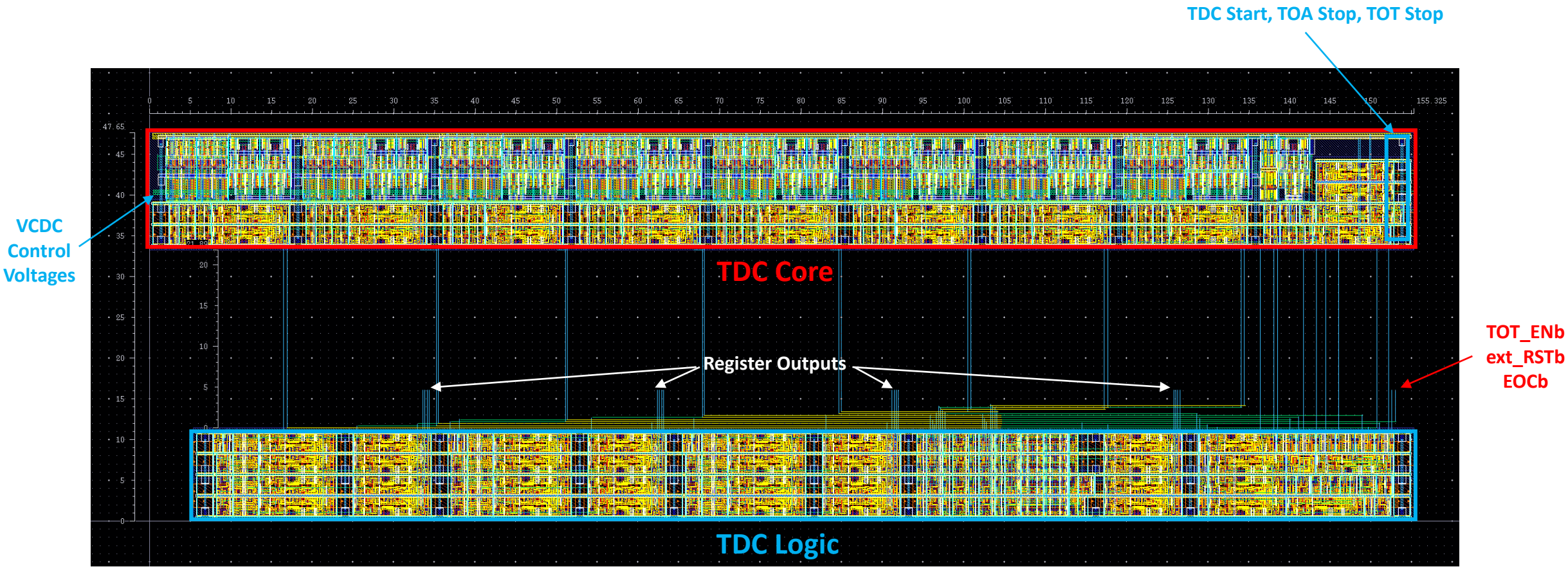
**TDC Power Consumption is dynamic, depends on: how often & how long the conversion is!**

[1] A. Duncanson, DRD7.6a meeting

# TDC: Layout

*A. Duncanson, M. Zeng (Stanford - HEPIC), B. Markovic*

## Full TDC area: TDC Core + TDC Logic = 4,250 μm$^2$

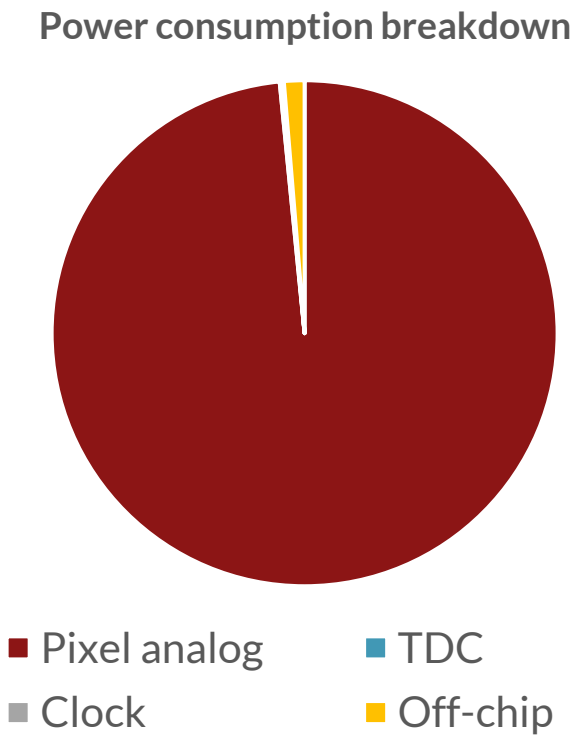



[1] A. Duncanson, DRD7.6a meeting

# Putting it all together: power breakdown at 100 kHz BX

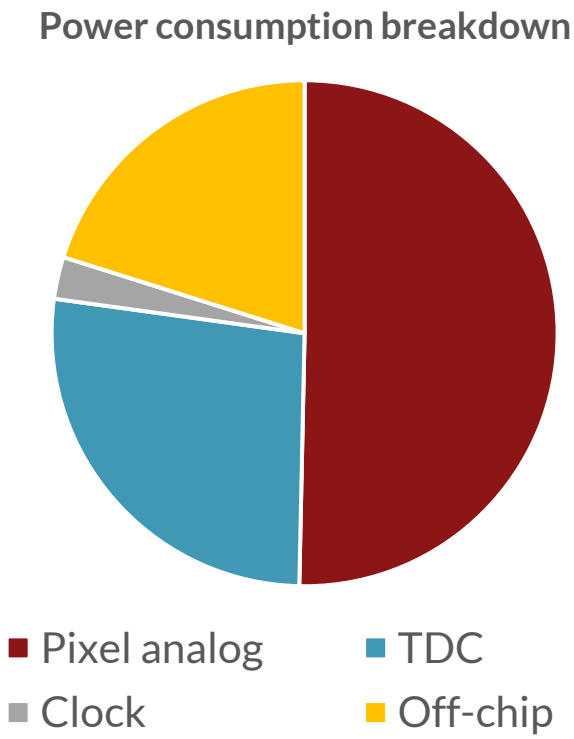
- **Assumptions:**
  - Bunch-crossing: **10 µs**
  - Occupancy: **100 hits / cm² / BX** (assuming in-pixel timing cuts)
  - Macro-pixel pitch: 200×60 µm
  - Pixel pitch*: 20 µm **(!!!)**
- Estimated power consumption:
  - Analog front-end: 750 mW (2.6 µA/pixel @ 25um pitch)
  - TDC: 1 mW
  - Clock distribution: 1 mW
  - Off-chip data link: 10 mW

- **Power in pixel analog front-end dominates power consumption**



# Putting it all together: power breakdown at 40 MHz BX

- **Assumptions:**
  - Bunch-crossing: **25 ns (x400)**
  - Occupancy: 100 hits / $cm^2$ / BX
  - Macro-pixel pitch: 200×60 µm
  - Pixel pitch*: 20 µm **(!!!)**
- **Estimated power consumption:**
  - Analog front-end: 750 mW (2.6 µA/pixel)
  - TDC: 400 mW
  - Clock distribution: 40 mW
  - Off-chip data link: 300 mW
- **Dynamic power consumption matches the analog front-end**



# Final thoughts on MAPS for timing

- Several approaches towards MAPS with improved timing performance are being proposed
- No one has yet delivered an HEP timing detector based on MAPS:

  - **Heavy modified process with custom doping profiles to implement gain layers (<50 ps):**
    ☺ Excellent sensor performance, uniform electric field for better timing
    ☹ No advanced nodes, availability, circuit performance, effect of circuits on sensor performance

  Large pixel size, low occupancy?

  - **TSPCO 65nm approach – Small collection electrode**
    ☺ More advanced CMOS, more real estate for circuits, low detector capacitance
    ☹ Current sensor performance not optimized for timing, small pitch is a draw-back

  Small pixel size, O(ns) timing?