

MAPS Matrix Readout Architectures & Periphery

MAPS Academy, SLAC

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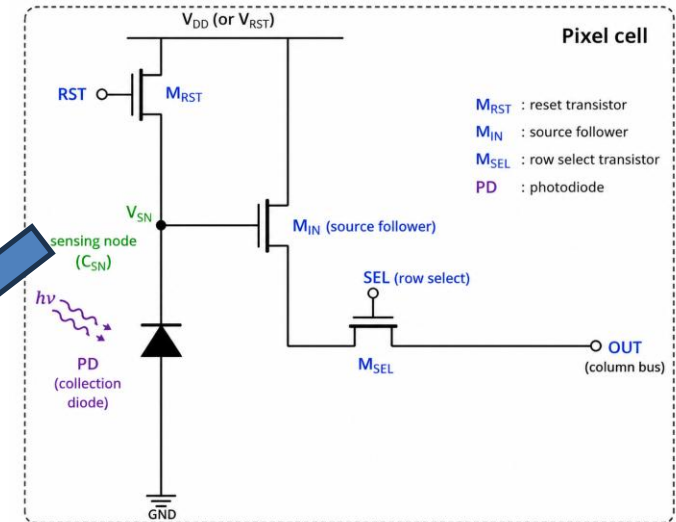
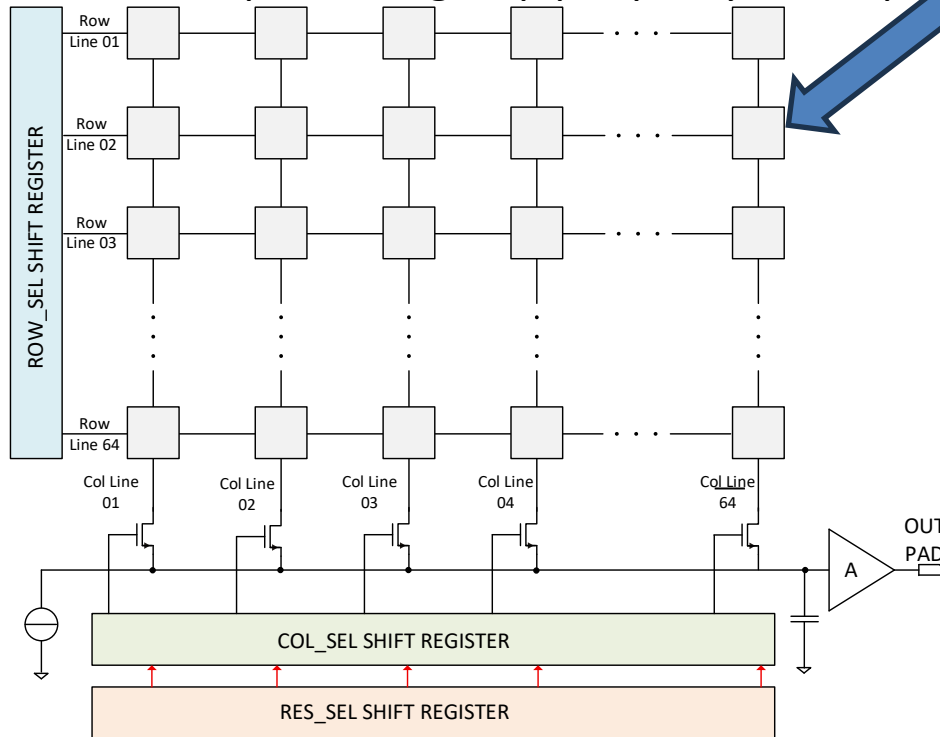
- Matrix Readout Architectures
 - Rolling Shutter
 - Zero Suppression
 - Asynchronous / Event-Driven
- Stitching
- Periphery
 - LVDS
 - DAC
 - Bandgap
 - Regulator

Key Performance Metrics

- Hit Rate Capability – Maximum particle flux that can be processed without data loss.
- Time Resolution – Precision with which the arrival time of a hit can be determined.
- Power Consumption – Total power required for pixel matrix, periphery, and I/O.Readout
- Bandwidth / Throughput – Maximum rate at which hit data can be transferred off-chip.
- Dead Time – Time during which the detector or parts of it are unable to record new hits.
- Latency – Time from hit occurrence to data availability at the chip output.
- Integration Time – Duration over which charge is accumulated before readout.
- Scalability – Ability to scale the architecture to larger matrices while maintaining performance.
- Pixel Area / Fill Factor – Impact of in-pixel circuitry on pixel size and sensing efficiency.
- Periphery Area – Silicon area occupied by readout electronics outside the pixel matrix.
- Output Data Volume – Amount of data generated and transmitted after sparsification and zero suppression.
- Design Complexity – Complexity of the architecture, implementation, and verification.
- Radiation Tolerance – Robustness against TID and SEE effects.

Serial Analog Readout

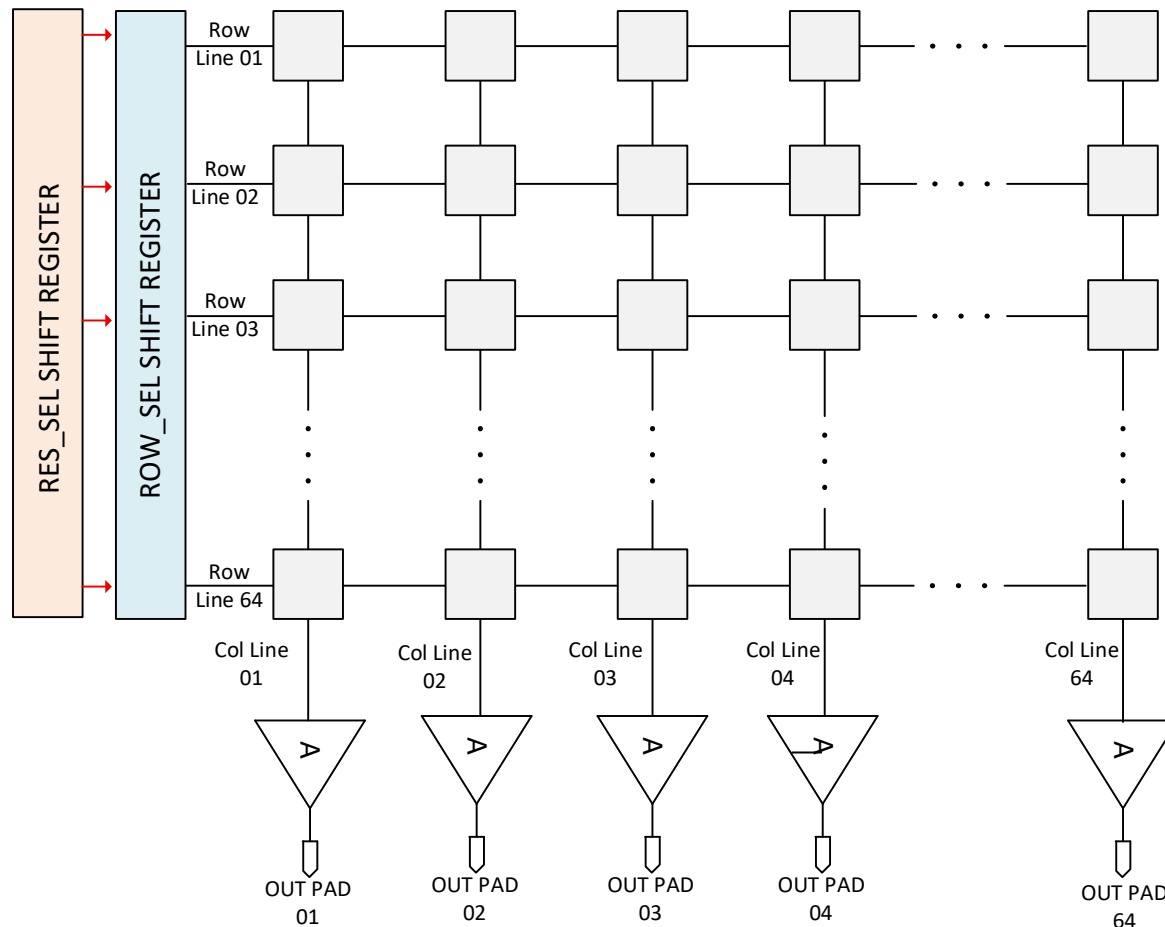
- Restrictions of early MAPS sensors
 - low integration density (600-350nm)
 - usage of PMOS transistor prohibited
 - no in-pixel digital logic
- Only feasible option: analog pixel readout
 - Further processing chip periphery off-chip



- Advantages
 - Simplicity
 - high fill factor
- Disadvantages
 - Limited frame rate
 - Long integration time
 - Increases pile-up probability

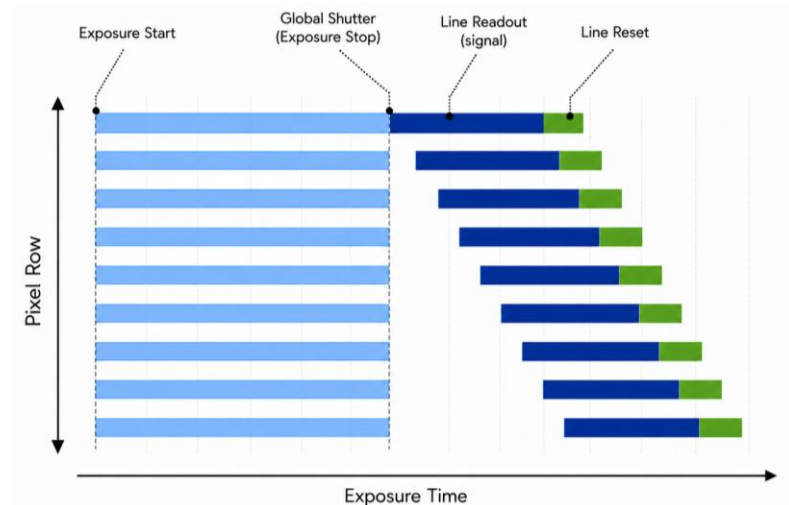
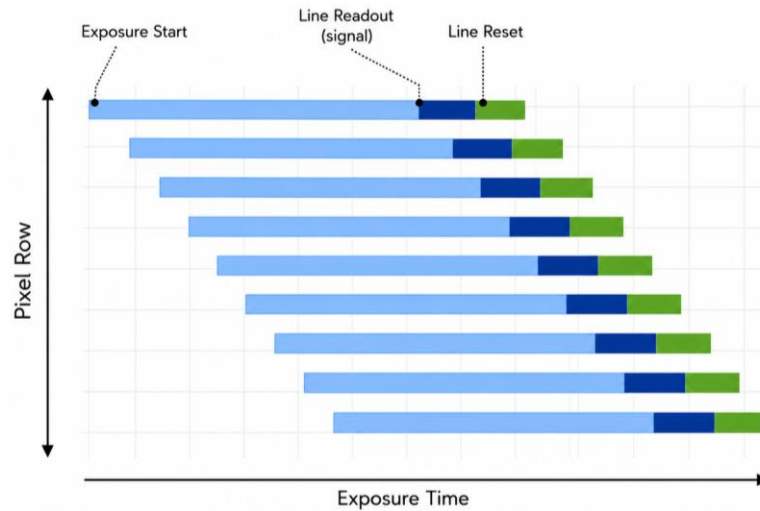
Collum Parallel Readout

- Obvious option to speed up readout is reading out all columns in parallel



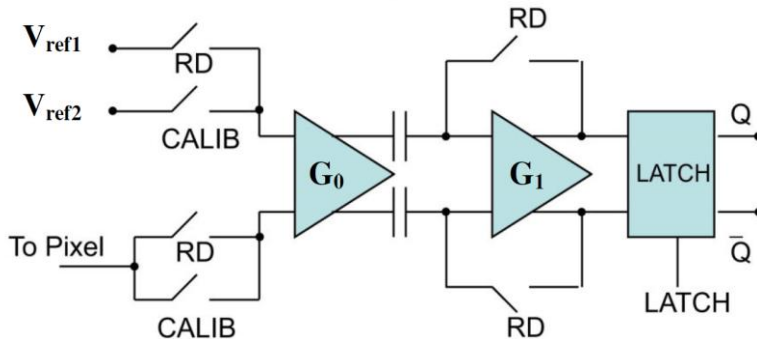
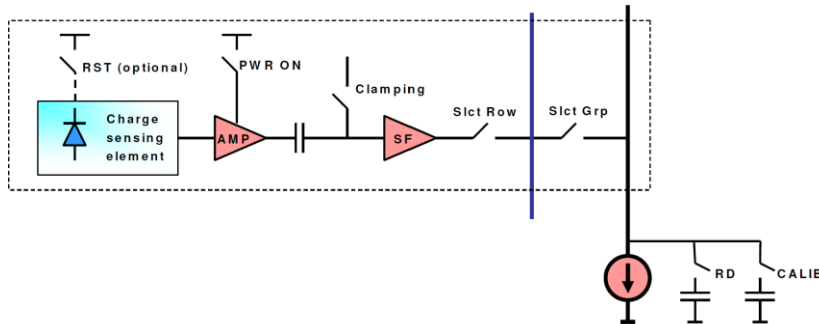
- Advantage
 - Col x higher frame rate
- Disadvantage
 - Col x higher power consumption in periphery
- Limitations (so far)
 - Data is readout independent of pixel hit occupancy
 - DC-offset varies strongly
 - Signal is very small

Rolling vs Global Shutter



- **Rolling Shutter:**
 - Addressed row transfers signal to periphery while other rows continue signal integration
 - The selected row is reset and immediately starts a new integration period
 - The Next row is selected, resulting in a continuously moving ("rolling") shutter
 - Preferred option in HEP applications due to pile-up probability
- **Global Shutter**
 - Signal integration of all rows happens synchronously
 - Increased dead-time with respect to rolling shutter approach
 - Used in high-speed imaging to mitigate imaging artefacts

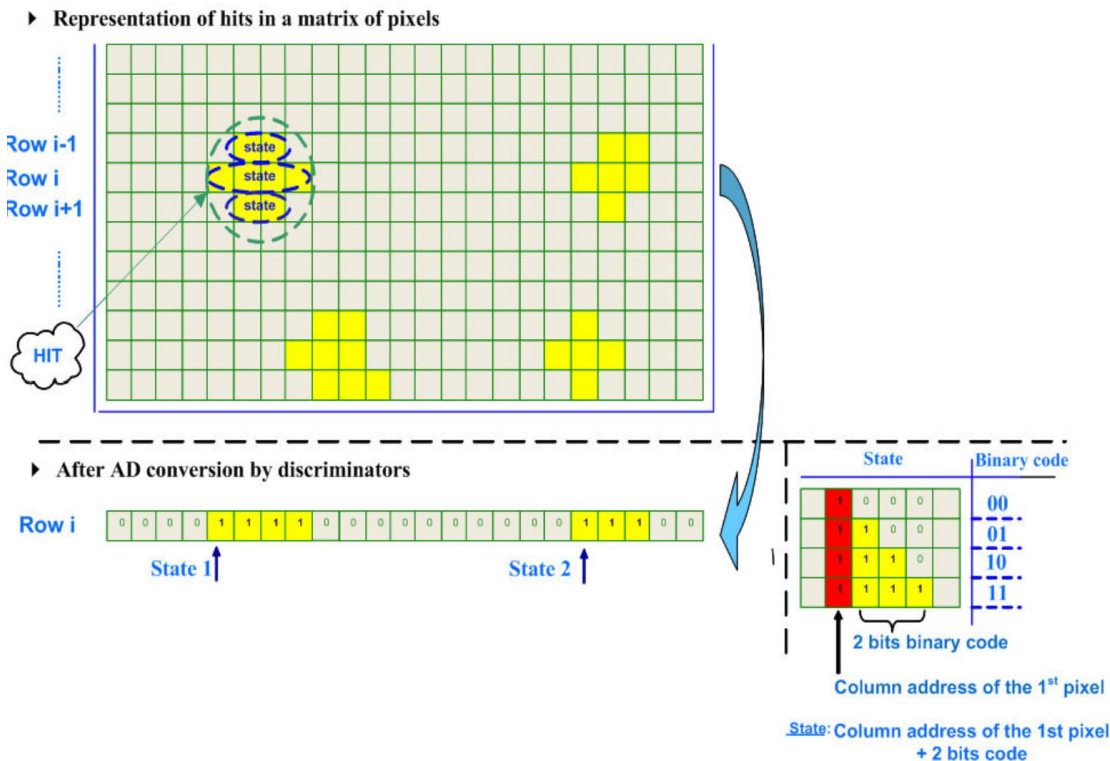
Binary Readout



- at the chip periphery column parallel-wise
- discrimination against a threshold
- very challenging
 - **Very small input signals** (tens of mV)
 - **Pixel-to-pixel offsets**
 - **Comparator offset**
- „Double“ CDS
 - In-pixel CDS
 - Comparator autozeroing
- autozero phase:
 - Stores pixel and comparator offsets together with the threshold for offset-compensated comparison.

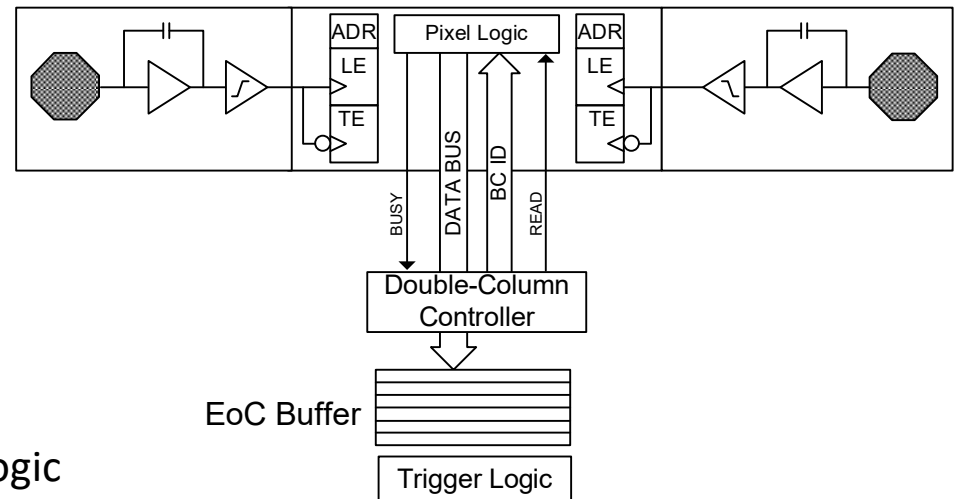
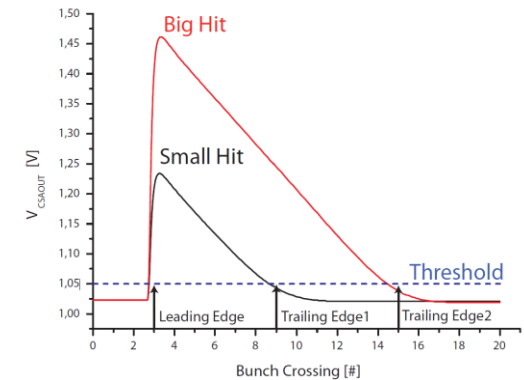
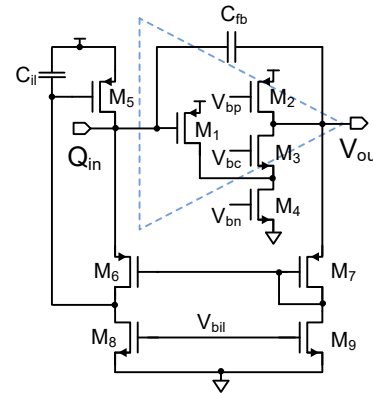
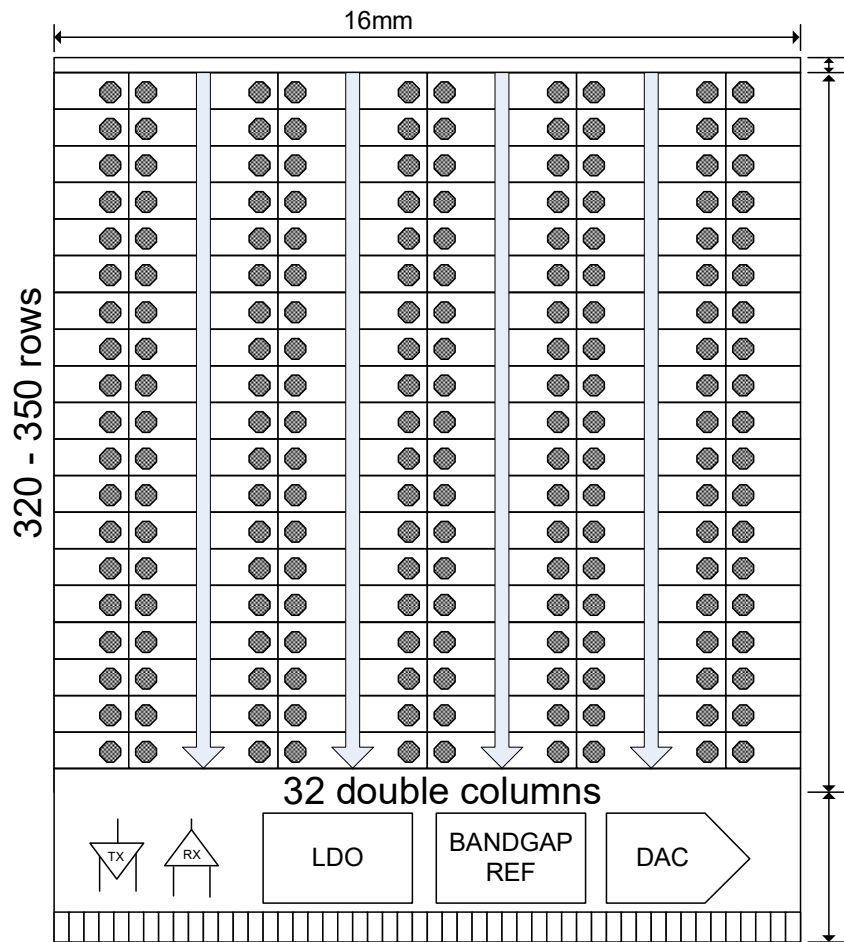
Y. Degerli et al., "A Fast Monolithic Active Pixel Sensor with Pixel-Level Reset Noise Suppression and Binary Outputs for Charged Particle Detection," IEEE Transactions on Nuclear Science, vol. 52, no. 6, pp. 3186–3193, Dec. 2005.

Zero Suppression Logic



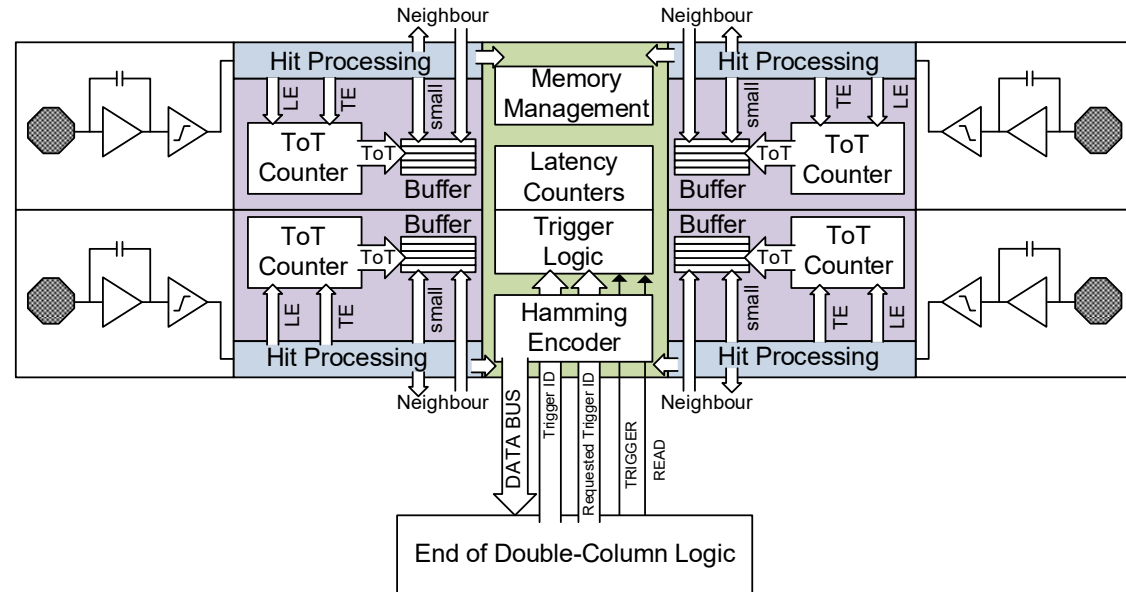
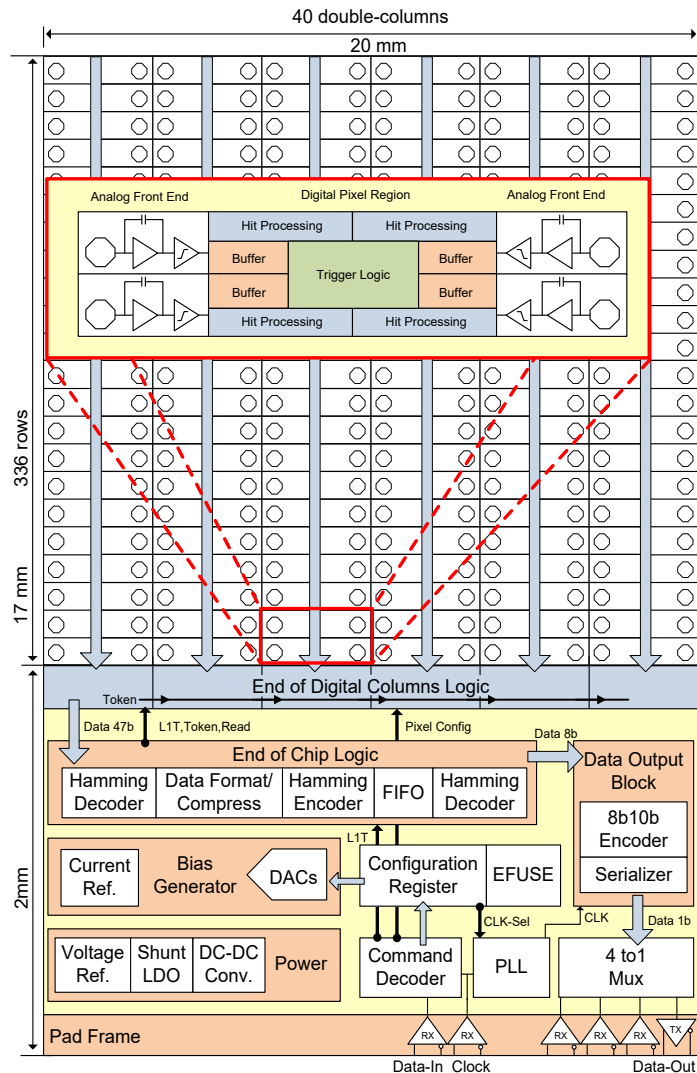
- reduces output bandwidth and power consumption by transmitting only hit information.
- Scans each binary row after discrimination and identifies hit clusters.
- Assigns row and column addresses to the first pixel of each cluster.
- Encodes the cluster size (up to 4 adjacent pixels) using a 2-bit code.
- Compression efficiency increases as hit occupancy decreases

Architecture FE-I3 Hybrid Pixel Detector Readout Chip



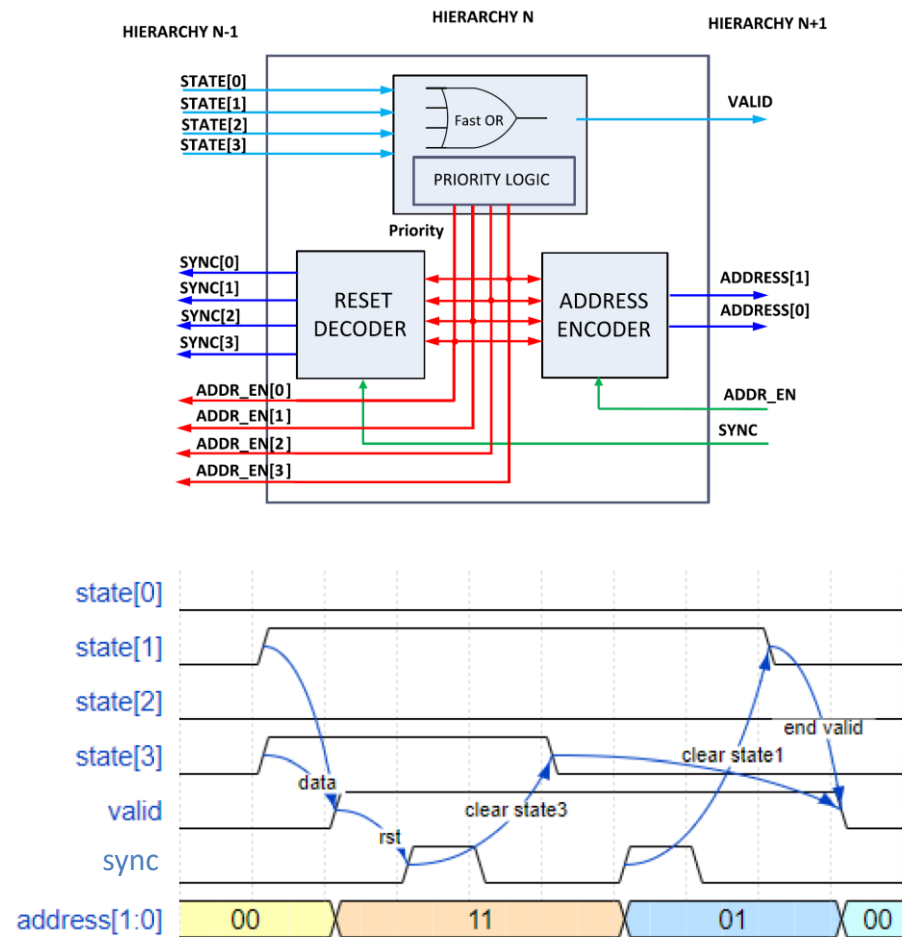
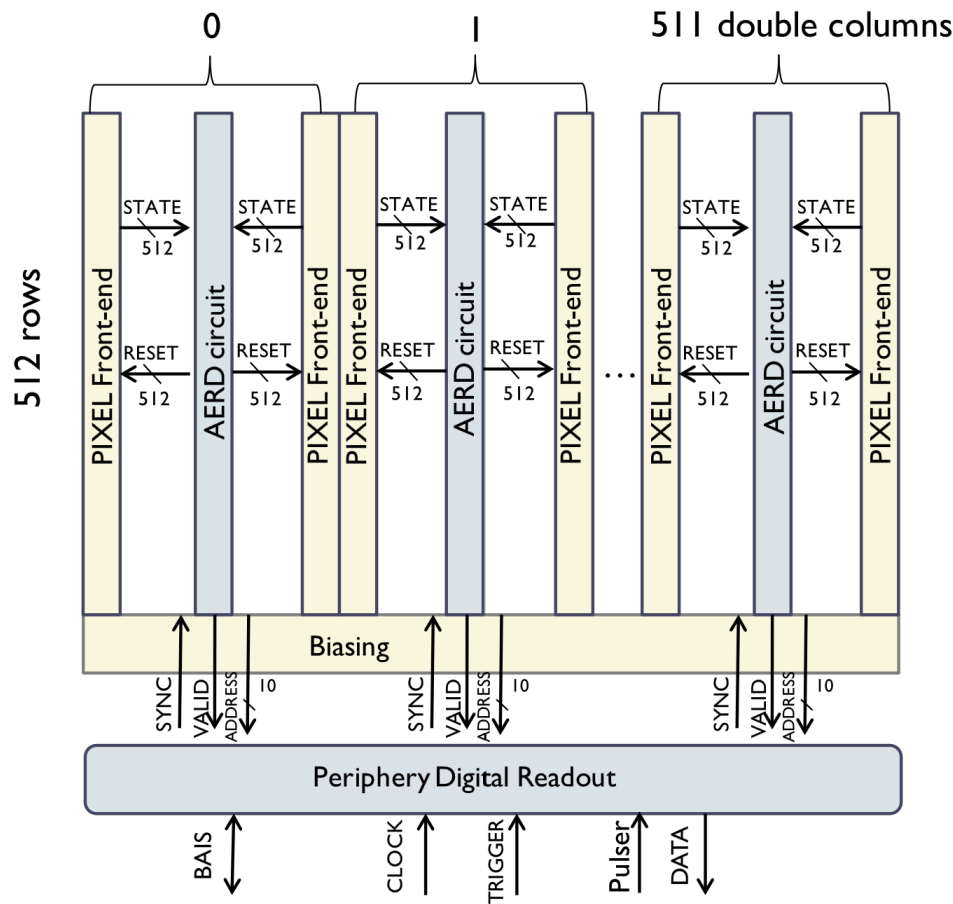
- Every pixel has a discriminator and its own logic
- All hits are read out by token mechanism
- Data is stored in EOC buffers

Architecture FE-I4 Hybrid Pixel Detector Readout Chip

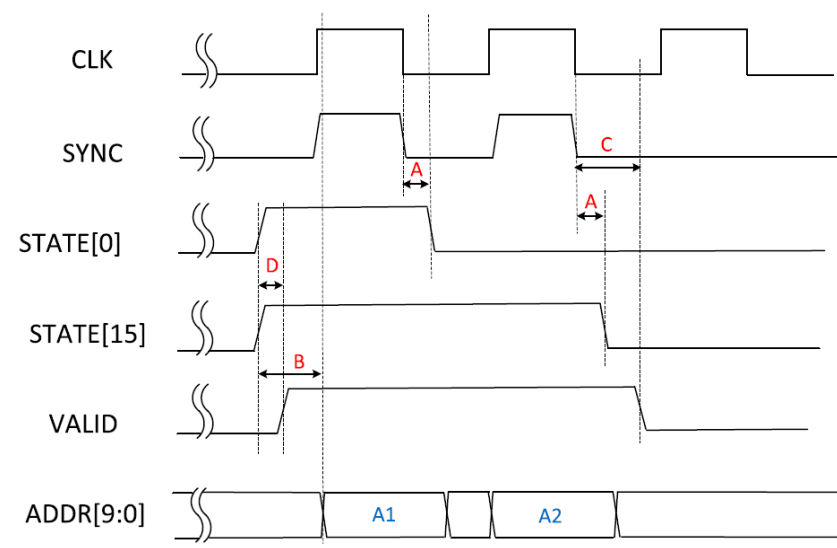
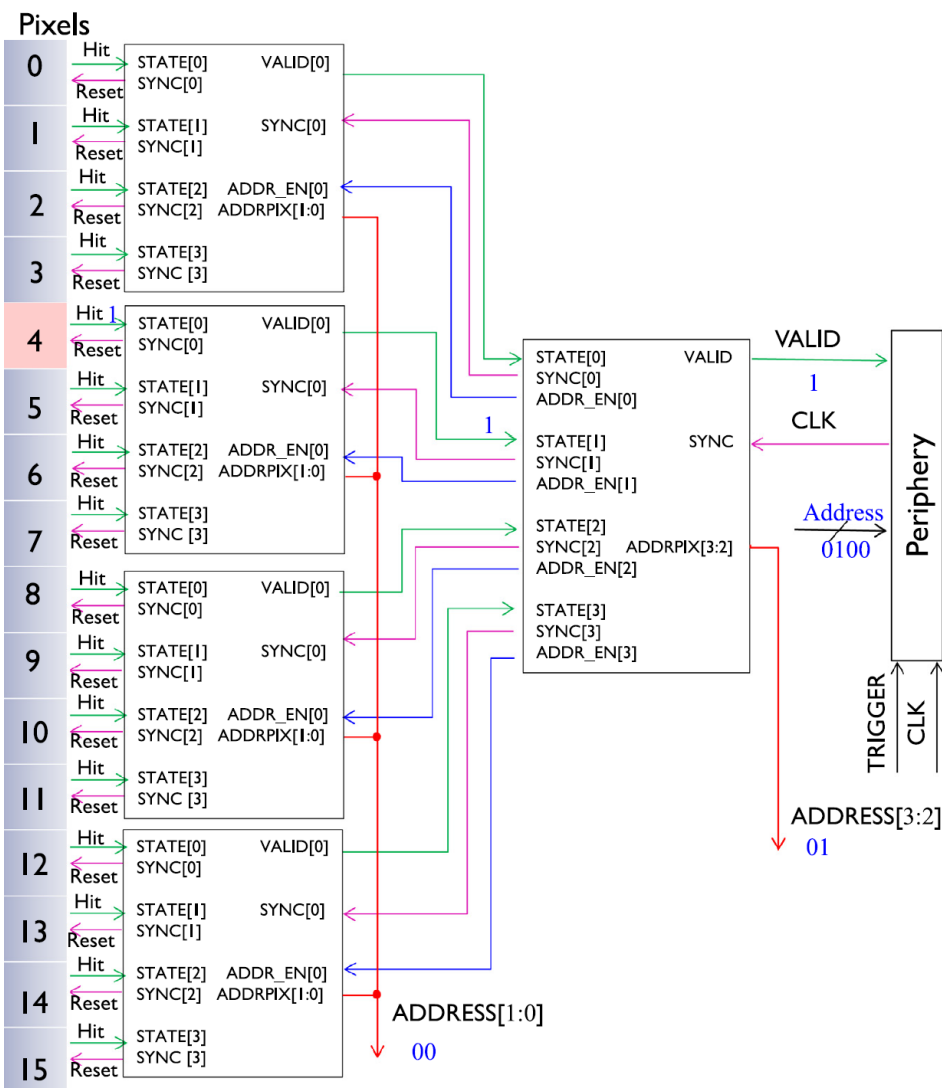


- Shared logic between pixels of same region
- Hits stored in local buffers
- Only triggered data is read out

ALPIDE Asynchronous/Data Driven Readout Architecture

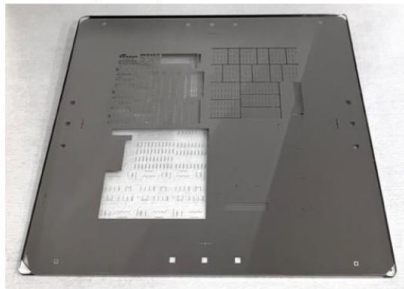


Arbiter Tree with Hierarchical Address Encoder & Reset Decoder

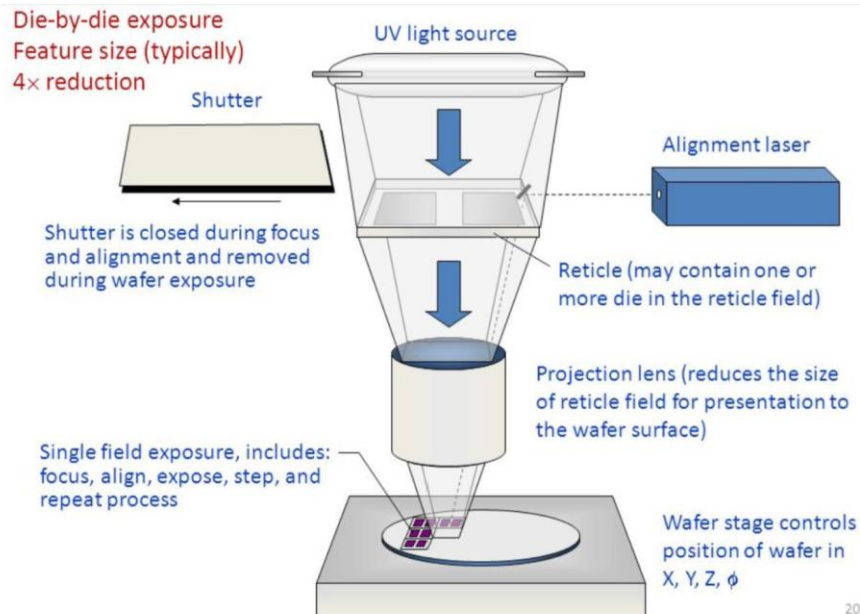


Maximum Die Size Restriction

Mask Plate: Also known as a “**Reticle**”, is a transparent glass plate with your pattern printed on it in opaque chrome.



- projection optics expose only one reticle field at a time.
- conventional dies cannot extend beyond a single reticle field.
- reticle defines the maximum area of a die
 - e.g. 26 mm × 33 mm



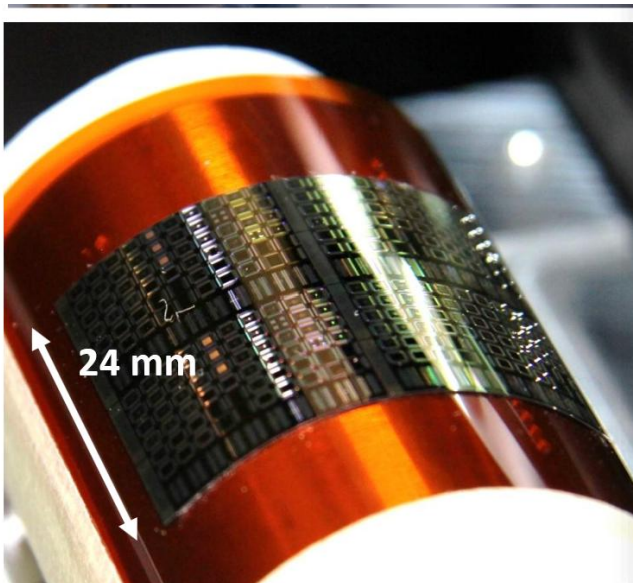
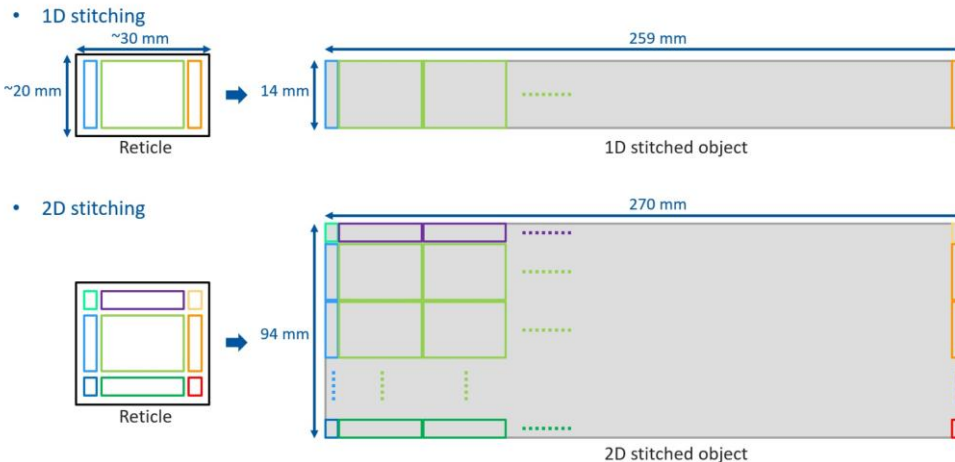
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Impact of Readout Architecture on Key Performance Metrics

Metric	MIMOSA-1	MIMOSA-26	FE-I3	FE-I4	ALPIDE
Pixel size	20×20 μm^2	18.4×18.4 μm^2	50×400 μm^2	50×250 μm^2	27×29 μm^2
Matrix size	64×64 pixels	576×1152 pixels	160×18 pixels	336×80 pixels	512×1024 pixels
Pixels/chip	4.1k	663k	2.9k	26.9k	524k
Readout principle	Serial analog	Rolling shutter	Triggered column-drain	Triggered local buffering	Asynchronous data-driven
Frame/Event time	10–100 ms	185.6 μs	Trigger dependent	Trigger dependent	Continuous
Time resolution	10–100 ms	185.6 μs	25 ns	25 ns	~2 μs
Max. trigger/event rate	<100 Hz	5.4 kframes/s	100 kHz	100 kHz	>100 kHits/s
Output bandwidth	<10 Mb/s	1.6 Gb/s	40 Mb/s	160 Mb/s	1.2 Gb/s
Power density	100–200 mW/cm ²	250 mW/cm ²	700 mW/cm ²	160 mW/cm ²	40 mW/cm ²
Clock in pixel matrix	No	Row scan only	Yes	Yes	No
On-chip discrimination	No	Column	Pixel	Pixel	Pixel
Priority encoder	No	No	Column arbitration	Regional arbitration	Hierarchical asynchronous

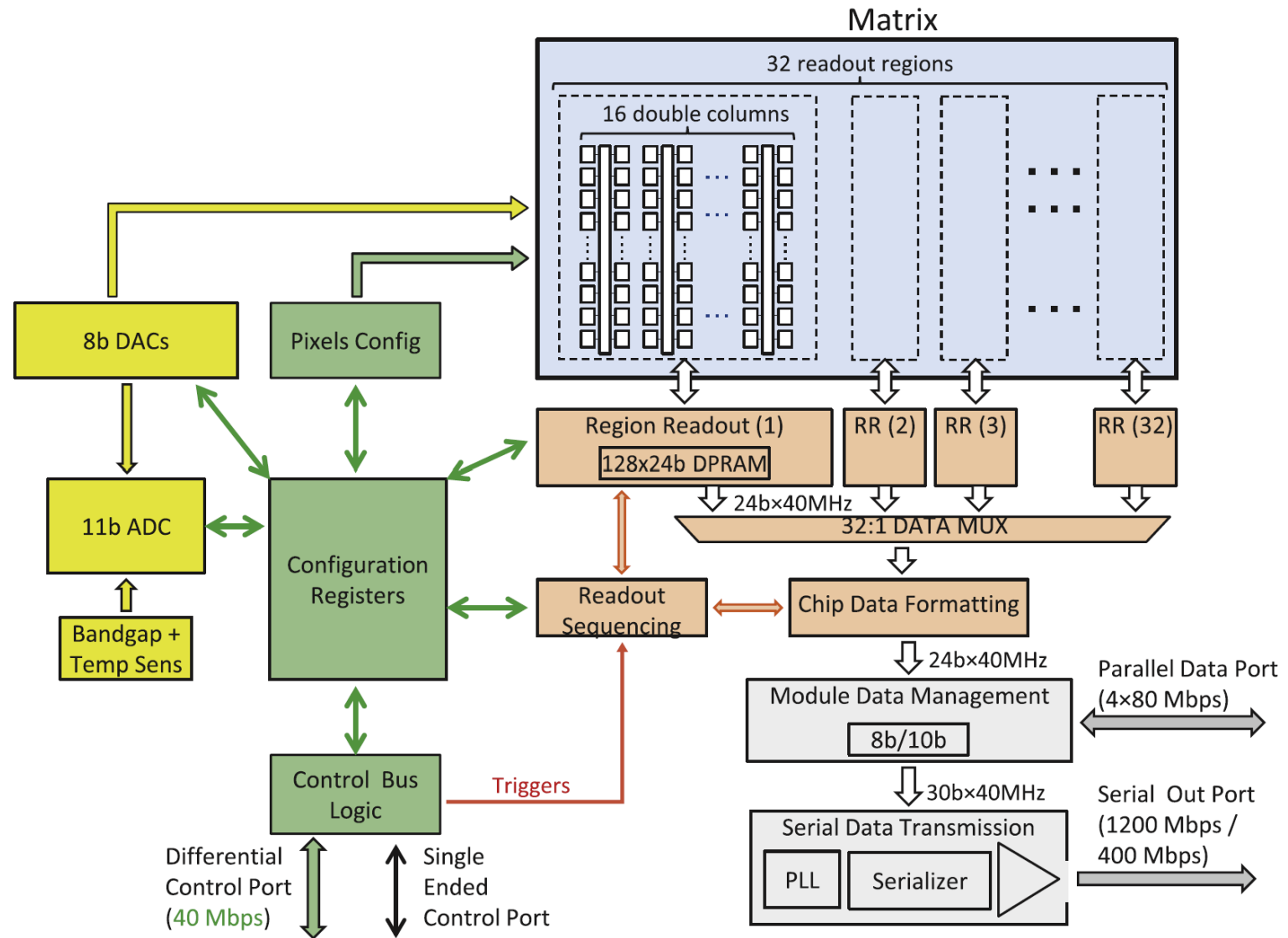
- Readout intelligence gradually moves **from the periphery into the pixel**.
- Sparse, data-driven readout **reduces latency, bandwidth, and power**.
- Architectural innovations enable **larger matrices and higher hit rates**.
- Modern MAPS combine **high integration with efficient on-chip data processing**

Stitching for Larger Sensor Areas



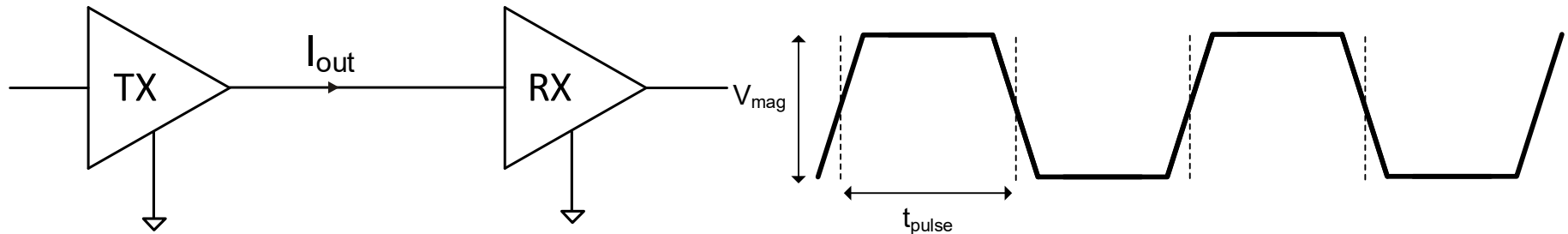
- stitching allows for larger sensors
 - recticle is reused several times
 - Exposures are not treated as separate dies but single
 - wires, devices, etc. continue
 - Sensors could even be bent
-
- Stitching affects yield
 - nanometer alignment required
 - The larger the device the higher the probability for defects

Crucial Blocks at the Chip Periphery



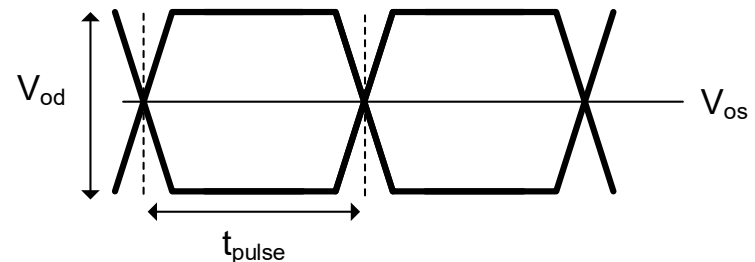
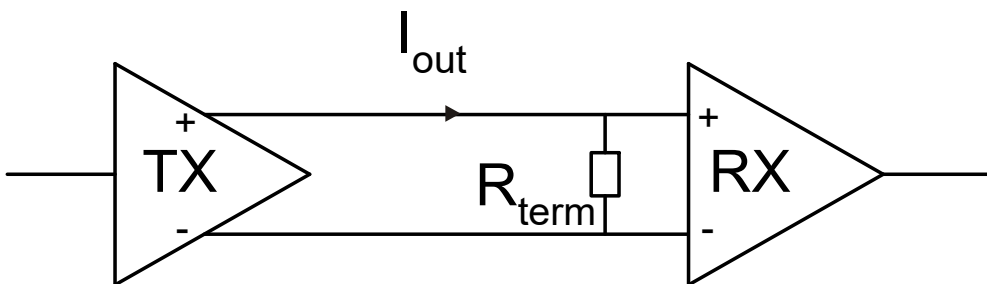
Single-Ended Signaling

- All electrical signal circuits require a loop or return path.
- Single ended signal is affected by distortion and noise.
 - Ground or reference may move due to switching currents
 - Electromagnetic interference can impose voltage on a single ended signal.
 - Signal passing from one board to another are subject to the local ground disturbance.
- Can be counteracted effect by widening ground plane.

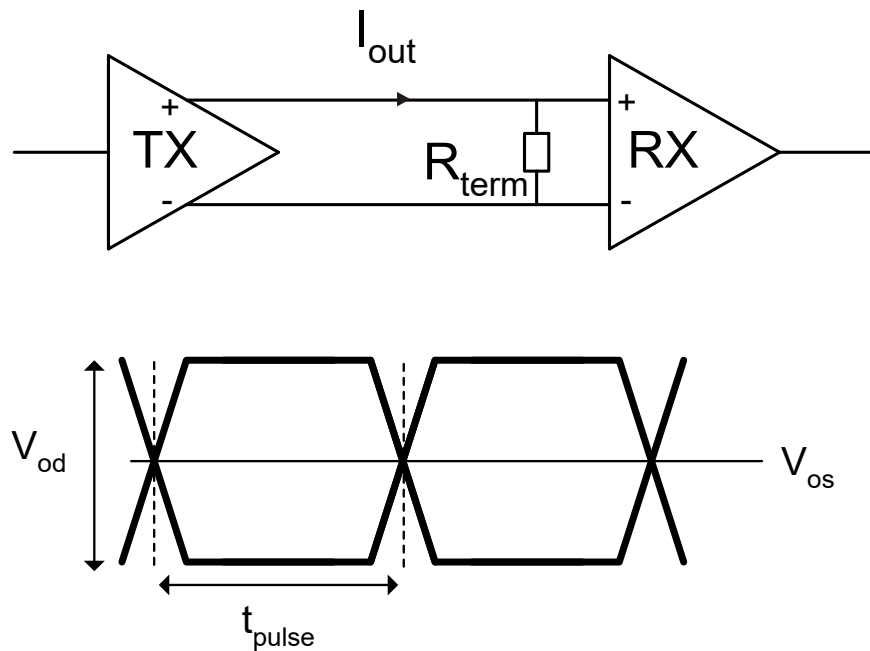


Differential Signaling

- Does not use the ground plane as current return path to close the loop
- Two dedicated conductors are used instead
 - The transmitter translates the single input signal into a pair
 - of outputs that are driven 180° out of phase.
 - The receiver, a differential amplifier, recovers the signal as the difference in the voltages on the two lines.
- Advantages of differential signaling can be summed up as follows
 - Differential Signaling is not sensitive to ground noise or shifts.
 - electromagnetic interference imposes the same voltage on both signals and the difference cancels out the effect.
 - Since the currents in the “wires” are equal but opposite and proximal, EMI is reduced.



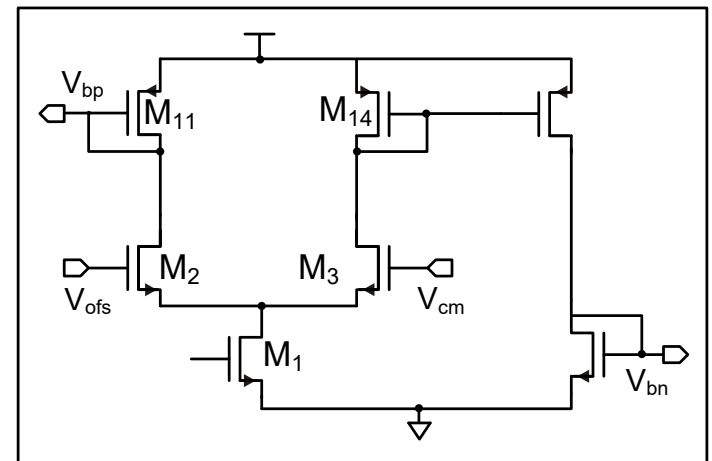
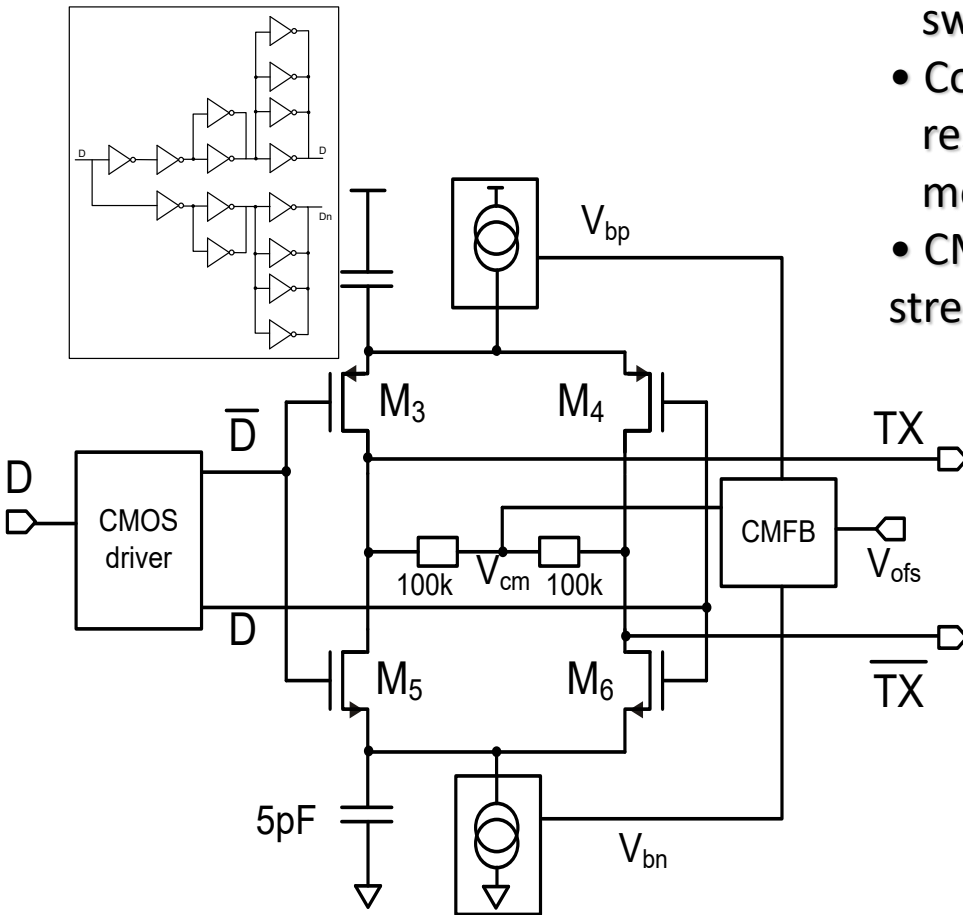
Low Voltage Differential Signaling (LVDS)



I_{out}	3.5 A
R_{term}	100Ω
V_{os}	1.20V
V_{od}	350 mV
V_{odth}	100 mV
$V_{cm-range}$	0-2.4V

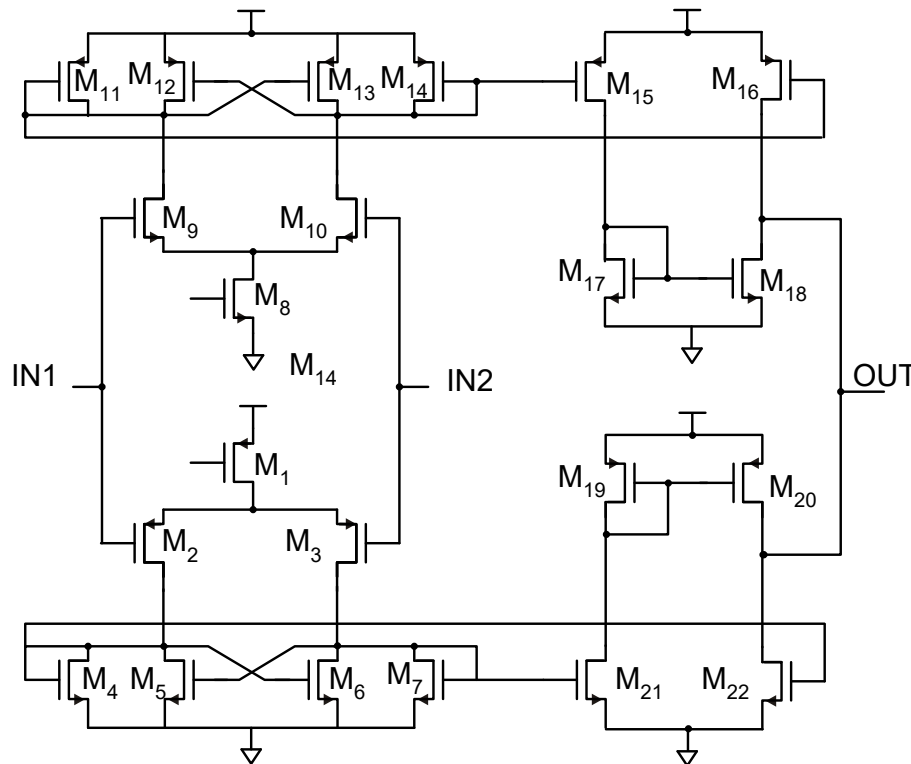
LVDS Driver

- Current is routed to/from the output by four switches M3-M6
- Common-mode voltage is measured by a resistive divider and controlled by a common-mode feedback circuit
- CMOS signal is provided with significant driver strength to speed-up switching



Boni et al., IEEE JSSC VOL. 36 NO. 4, 2001

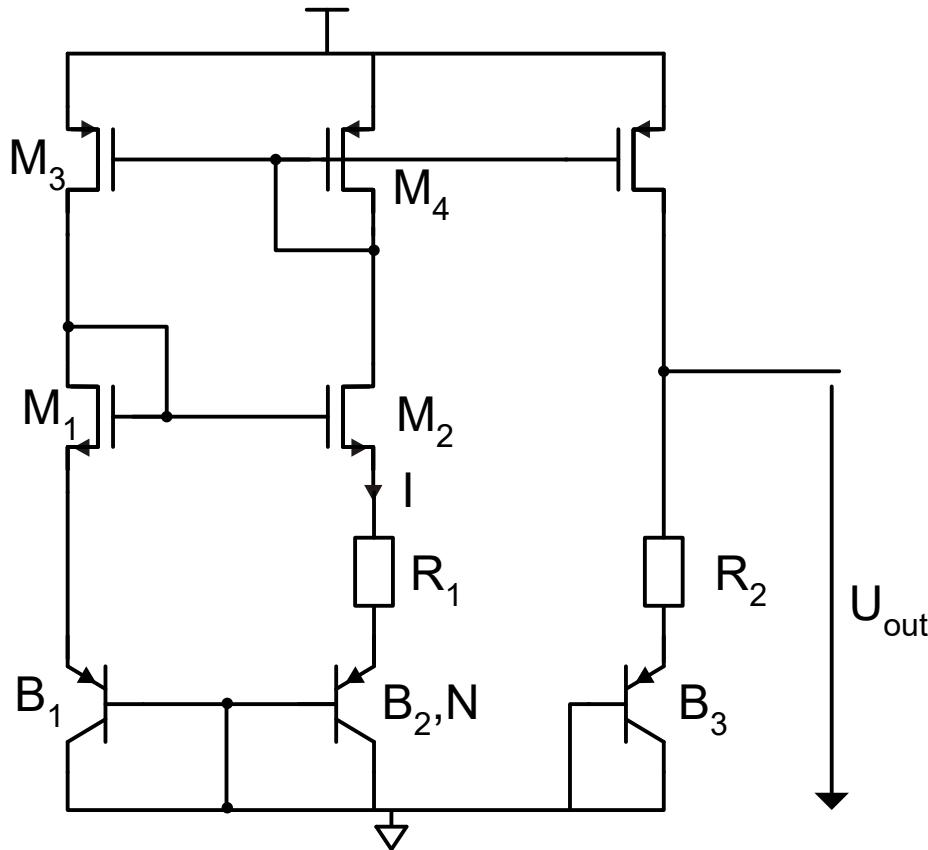
LVDS Receiver



- parallel PMOS/NMOS comparator input stages allow operation in a **wide range of common-mode** voltages
- cross coupled positive feedback structure allows introduction of hysteresis
- second stage sums signals from both input stage and converts them to a CMOS output signal

Tyhach et al., A 90-nm FPGA I/O Buffer Design With 1.6-Gb/s Data Rate for Source-Synchronous System and 300-MHz Clock Rate for External Memory Interface, IEEE JSSC, Sept. 2005

“High”-Supply Voltage Bandgap Voltage Reference

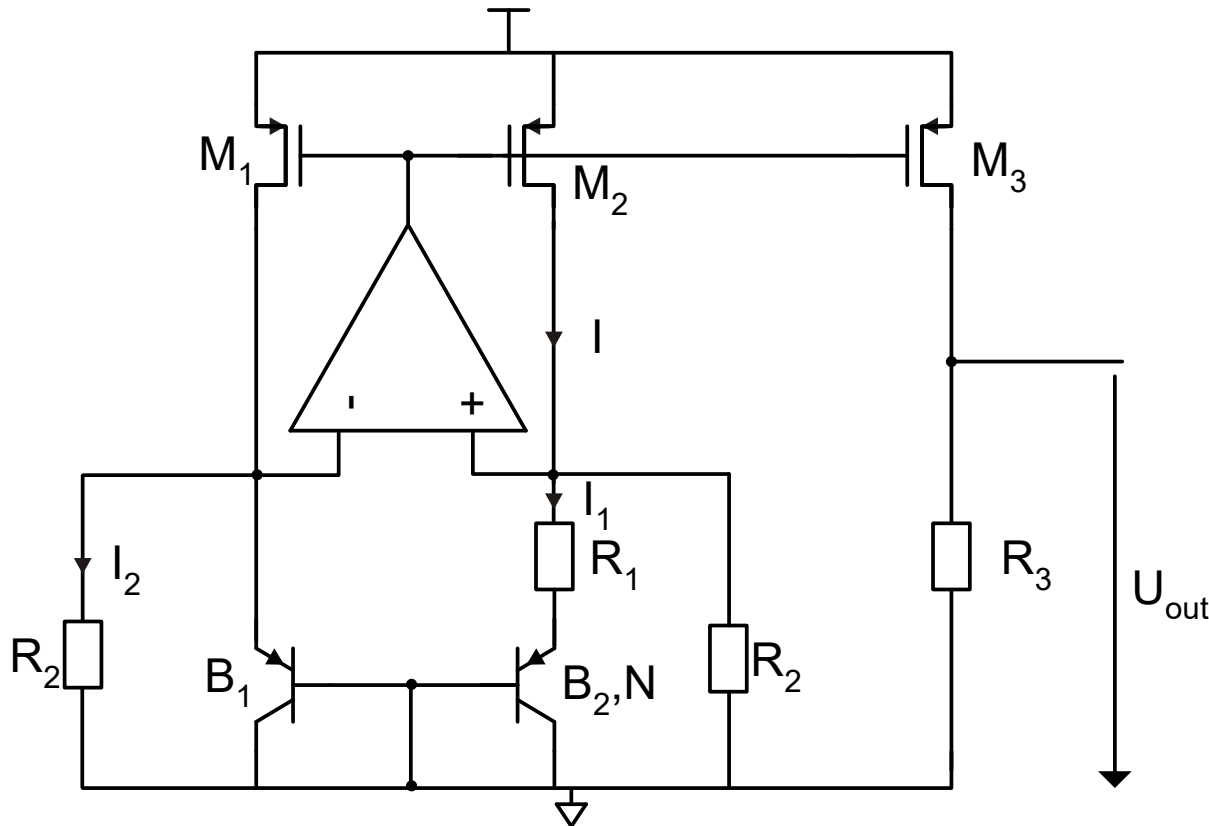


$$I = \frac{\Delta V_{BE}}{R_1} = \frac{V_T \ln N}{R_1}$$

$$V_{out} = V_T \frac{R_2}{R_1} \ln N + V_{BE} \\ \approx 1.2V$$

- Most radiation sensitive circuit part in pixel periphery
- „Bipolars“ implemented as MOS in weak inversion
- enclosed gate-layout

“Low”-Supply Voltage Bandgap Voltage Reference



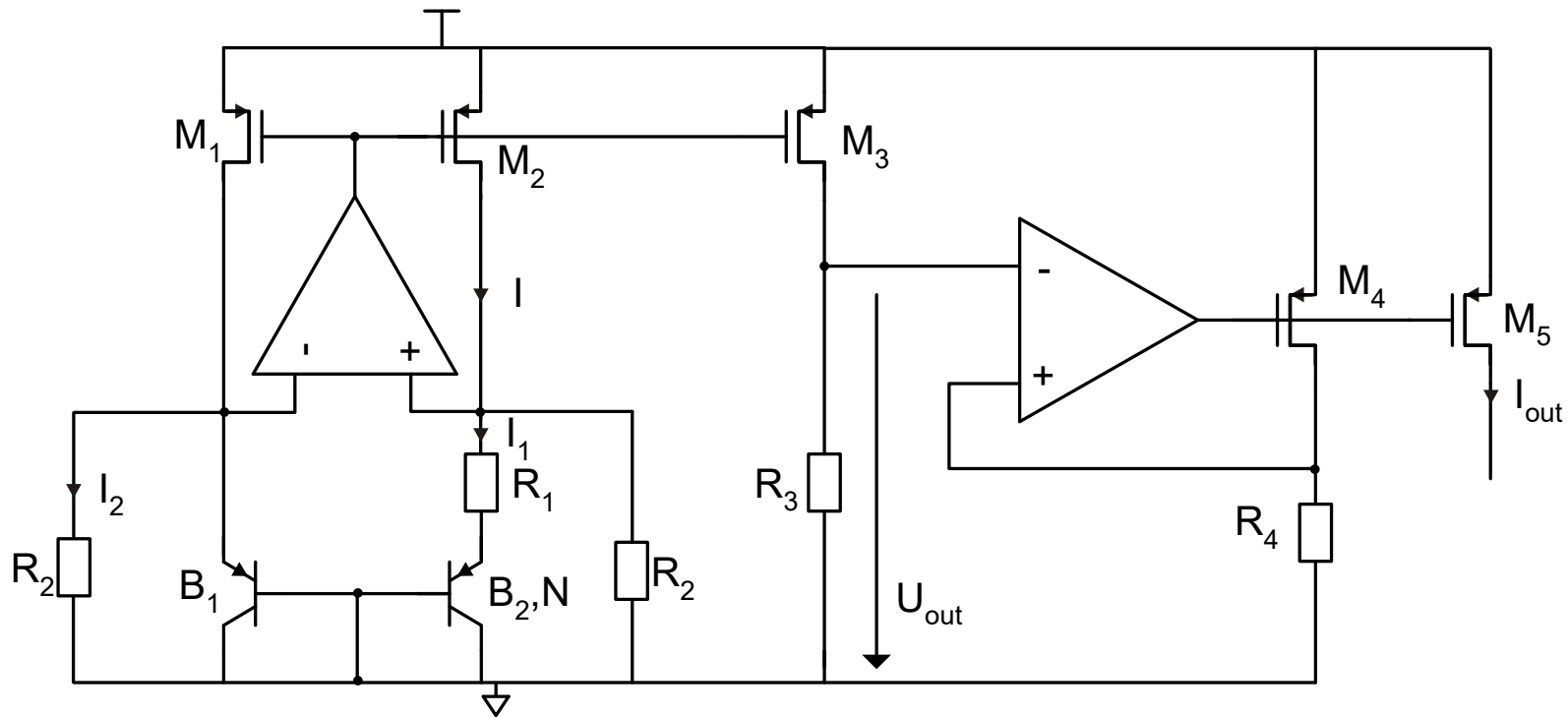
$$I = I_1 + I_2$$

$$I_1 = \frac{\Delta V_{BE}}{R_1} = \frac{V_T \ln N}{R_1}$$

$$I_2 = \frac{U_{BE1}}{R_2}$$

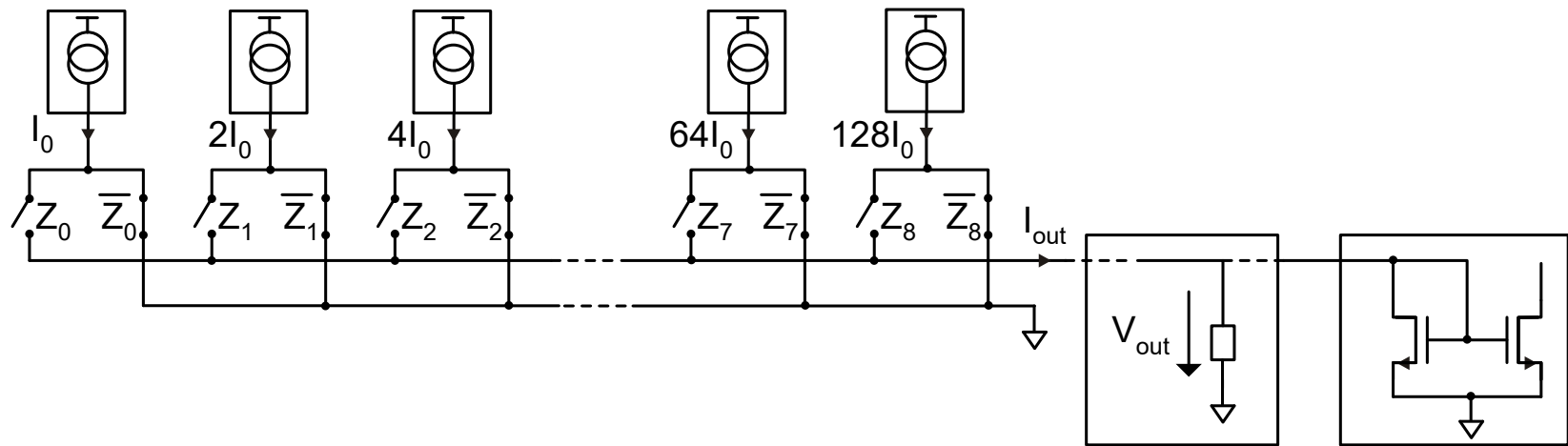
$$V_{out} = \frac{R_3}{R_2} \left(V_{BE} + \frac{R_2}{R_1} V_T \ln N \right)$$

Reference Current Generator



- Usage of external resistor R_4 with zero-temperature coefficient
- Choice of R_2/R_1 to compensate for R_4

Current Steering DAC Architecture

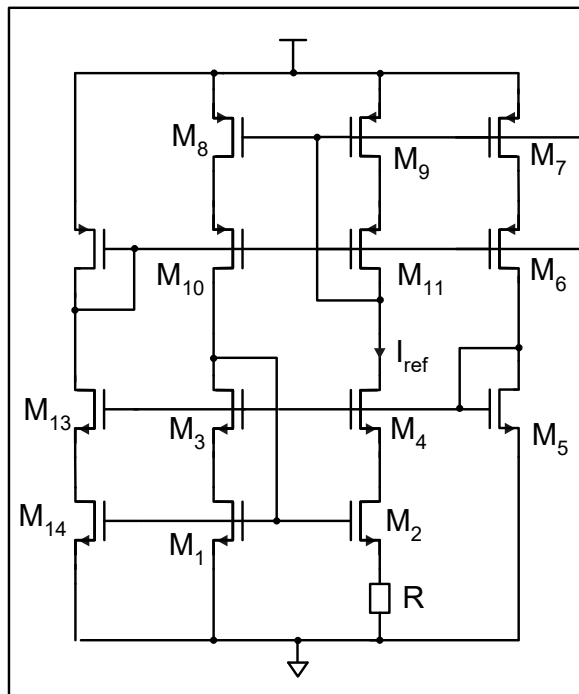


Current steering architecture

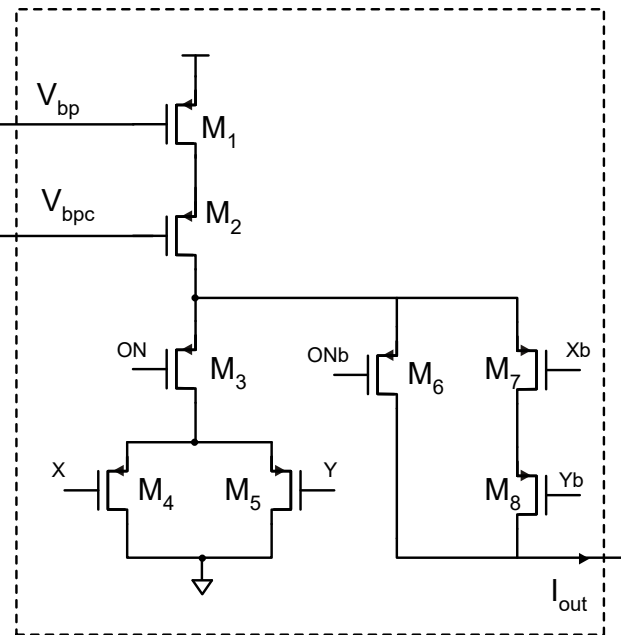
- Amount of current flowing to DAC output is steered by DAC setting
- Output current can be used for biasing or the generation of a voltage by use of a resistor
- Constant current consumption of $255 \cdot I_0$ (for 8 Bit DAC)

DAC Unit Cell

Reference
Circuit



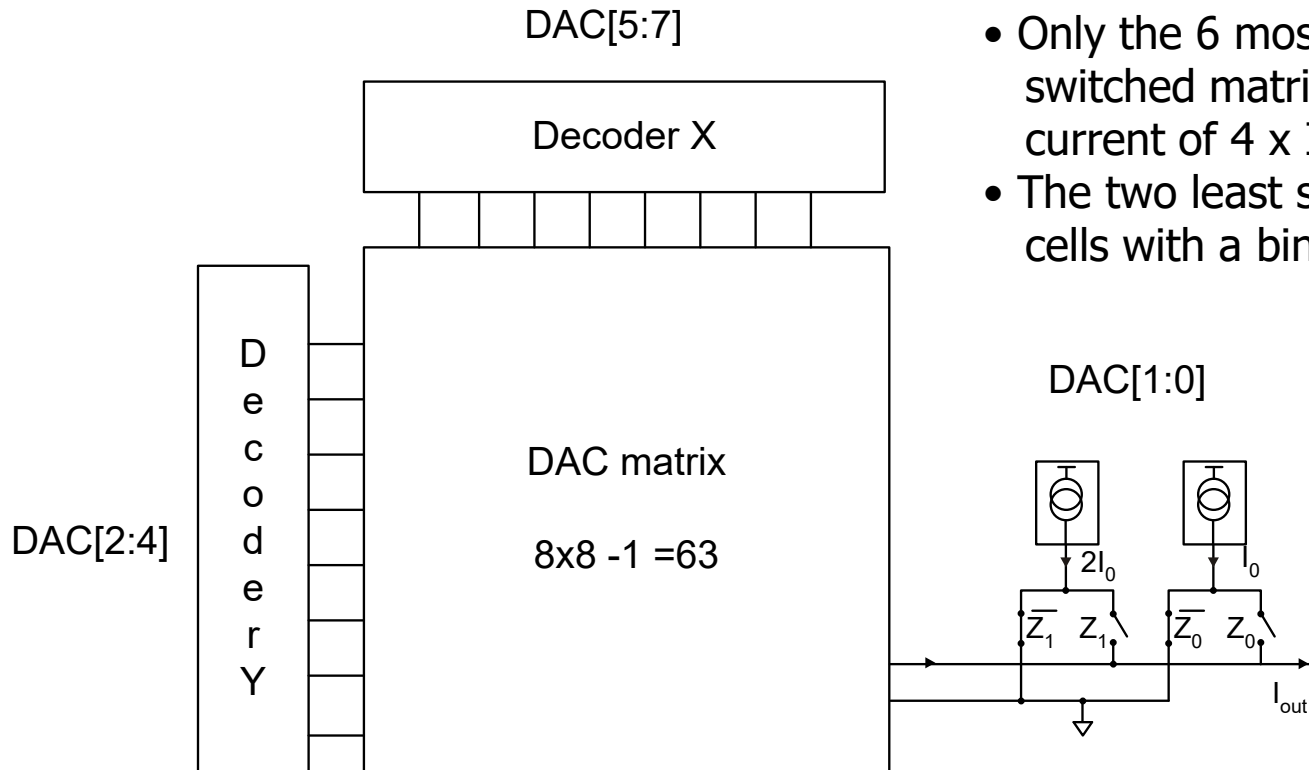
DAC Unit Cell



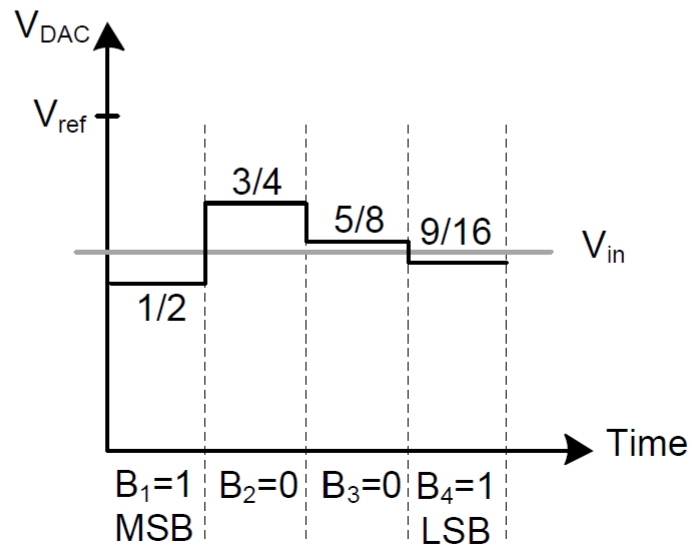
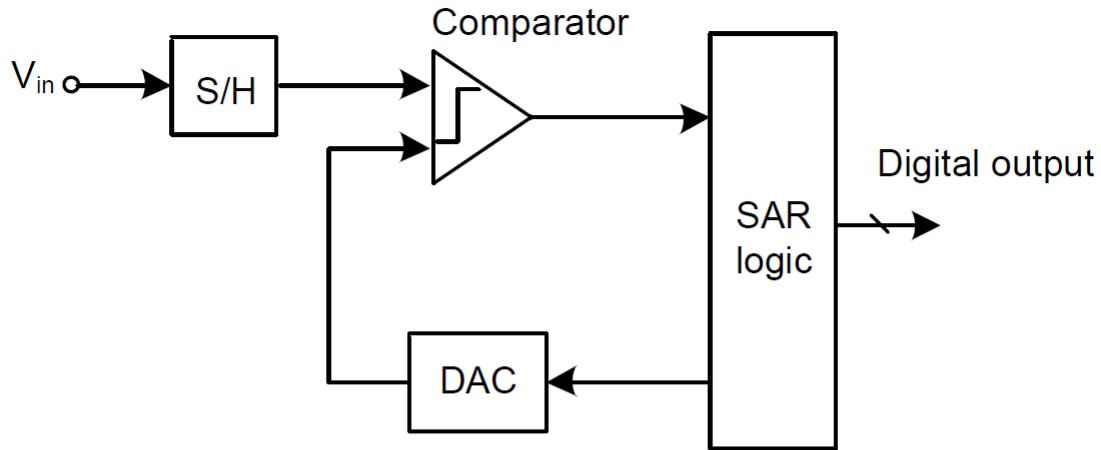
- cascoded current source
- biasing voltages extracted from the reference circuit
- switching scheme for DAC matrix arrangement

DAC matrix

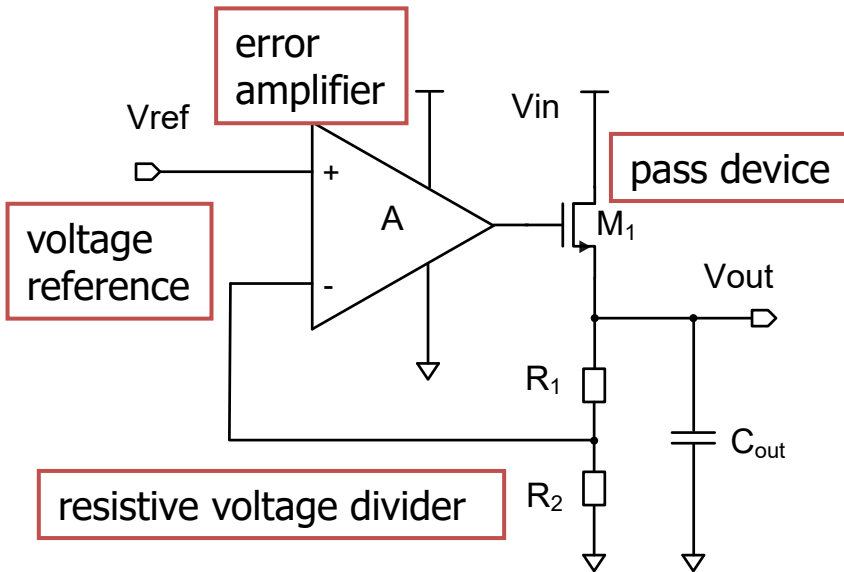
- cells are switched on one after another to have inherent monotonic DAC characteristic
- Only the 6 most significant are realized as a switched matrix of unit cells with unity current of $4 \times I_0$ to save area.
- The two least significant bits are realized as cells with a binary weighted current.



Successive Approximation ADC



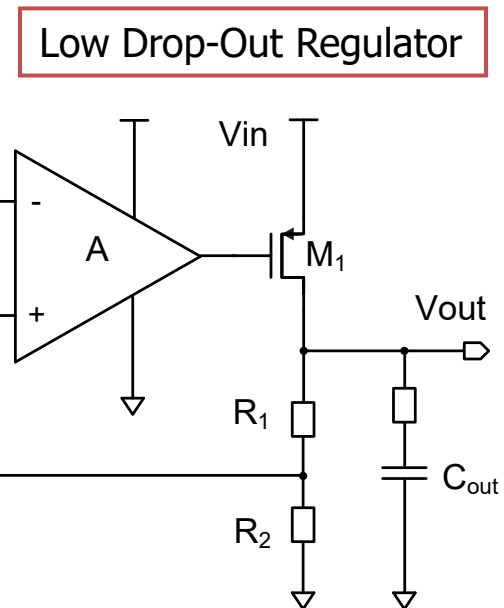
Linear Voltage Regulator



Drop-Out Voltage

$$V_{drop} = V_{out} - V_{in} = V_{DSSAT} + V_{th}$$

Easier to stabilize



$$V_{drop} = V_{DSSAT}$$

More difficult to stabilize

Take-Home Message

- **Matrix Readout Architectures**

- Readout intelligence has continuously moved closer to the pixel.
- Sparse, data-driven architectures maximize hit rate while minimizing power and bandwidth.
- Stitching enables large-area monolithic sensors beyond the reticle limit.

- **Periphery**

- High-performance MAPS require more than an optimized pixel matrix.
- Robust chip operation relies on **interfaces, reference generation, DACs, ADCs, voltage regulators, and clock generation.**
- Periphery circuits largely determine **signal integrity, power efficiency, and radiation tolerance.**

- **Outlook**

- Future MAPS will integrate increasing levels of **on-chip intelligence** for data processing and detector control.
- Power Management get lately more attention