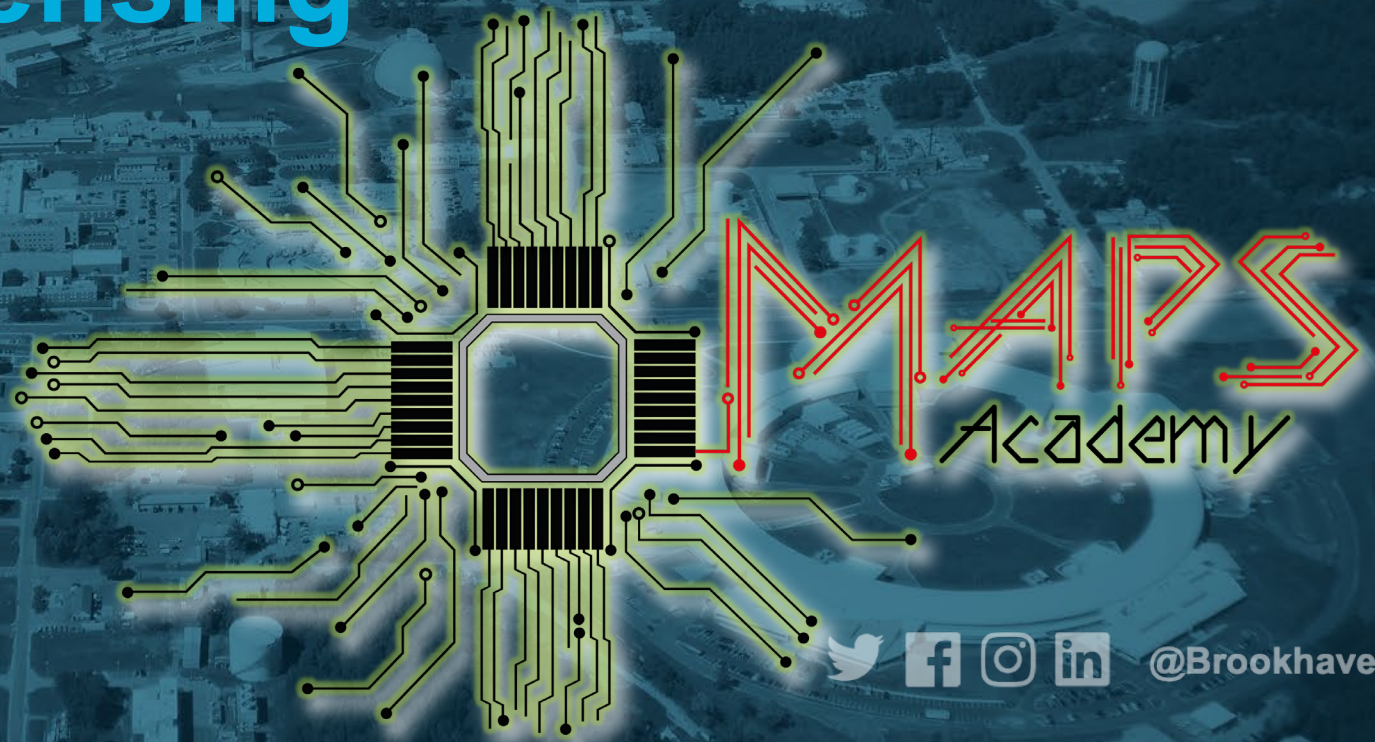
Introduction to MAPS: Concepts, Detection & Sensing

Grzegorz W. Deptuch,
gdeptuch@bnl.gov

Brookhaven National Laboratory

U.S. DEPARTMENT OF ENERGY



@BrookhavenLab

MAPS ACADEMY, SLAC, Stanford, July 28 - August 4, 2026

MAPS, Where?

PAST:

STAR HFT
MAPS

PRESENT:

ALICE ITS2	ALICE ITS3	EIC ePIC
MAPS	MAPS	MAPS

FUTURE:

ALICE 3	BELLE II	ILD	SiD	CLD	IDEA	Allegro	LHeC	FCC-hh
MAPS	MAPS	MAPS	MAPS	MAPS	MAPS	MAPS	MAPS	MAPS

Diffusion MAPS

Modified Process MAPS

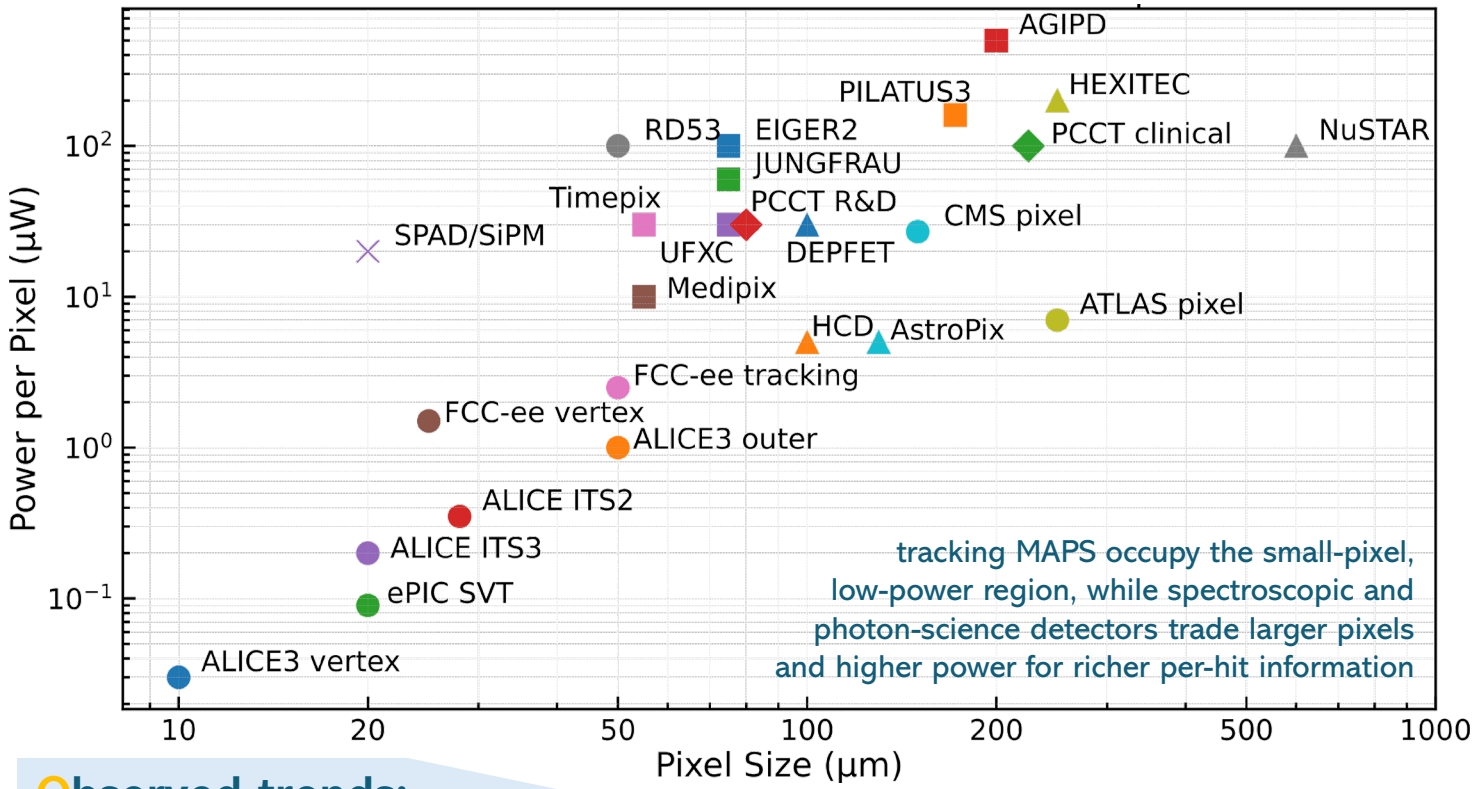
SOI MAPS

HV Depleted MAPS

Historical message: STAR proved MAPS could work in colliders; ALPIDE/ITS2 made MAPS the technology of choice for large-area precision vertexing.

Brookhaven National Laboratory

Pixel-Detectors in Pixel-Size–Power Space



Domain	Name	Size of Pixel	Power / Pixel
HEP/ NP	ALICE 3 Vertex Detector	~10×10 μm² (R&D)	<0.05 μW
	ALICE 3 Middle/Outer tracker	~50×50 μm² (concept)	~0.75–1.25 μW
	ePIC Silicon Vertex-Tracking (EIC)	20×22.5 μm²	< 0.1 μW
	ALICE ITS2 (ALPIDE)	27×29 μm²	~0.3–0.4 μW
	ALICE ITS3 (MOSAIX)	~20 μm (18–22.5 μm)	~0.1–0.25 μW
	FCC-ee Vertex Detector	~25×25 μm (concept)	~1–2 μW
	FCC-ee Tracking Detector	CLD (50×50 μm²)	~2–3 μW
	RD53 / HL-LHC	50×50 μm² / 25×100 μm²	~50–150 μW
	ATLAS pixel (LHC / IBL era)	50×250 μm²	~5–10 μW
	CMS pixel (Run-2/3)	100×150 μm²	~20–35 μW
Photon Science	EIGER2	75×75 μm²	~100 μW
	PILATUS3	172×172 μm²	~160 μW
	JUNGFRAU	75×75 μm²	~60 μW
	AGIPD (FEM/mod.-derived, XFEL)	200×200 μm²	~450–600 μW
	UFXC	50-100 μm pitch	~10–50 μW
	Medipix3 / Medipix4	55×55 μm²	~5–20 μW
	Timepix3 / Timepix4	55×55 μm²	~10–50 μW
Astro-Physics	NuSTAR (Caltech)	600 × 600 μm²	~50–200 μW
	HEXITEC (RAL)	250 × 250 μm²	~100–300 μW
	AstroPix	~130 × 40 μm²	~1–10 μW
	DEPFET (eROSITA/Athena WFI)	~100 μm (75–130 μm) pitch	~10–50 μW
	HCD (HxRG family)	IR: 18–36 μm, X: ~100 μm	~1–10 μW
Medical Imaging	PCCT clin. CdTe/CZT – NAEOTOM α	225 μm (R&D: 150 μm)	~50–200 μW
	PCCT (R&D / Medipix-based)	55–110 μm pitch	~10–50 μW
	Energy-integrating CT (legacy)	mm-scale scintillator	n/a
Other	SPAD arrays / SiPM pixels	10–50 μm pitch	~1–100 μW

Observed trends;

- Power / pixel spans more than 4 orders of magnitude across detector architectures.
- Pixel pitch alone does not determine power; timing, noise, digitization, buffering, radiation tolerance, and data transmission are often dominant.
- Per-link throughput commonly approaches practical limits of order 10^8 –10^9 hit words or data items / second,
- At low occupancy, sparsified and event-driven readout use available bandwidth more efficiently than continuous full-frame readout.

Brookhaven National Laboratory

Values are approximate and not always directly comparable

Pixel detectors

HEP-NP: [1] CERN Yellow Rep. (2022–2024); [2] BNL ePIC SVT Indico, event 19823 (2023); [3] NIM A 824 (2016) 434; J. Phys. G 41 (2014) 087002; [5] CERN-LHCC-2022-012; [6] JINST 16 (2021) P02015; [7] EPJ ST 228 (2019) 261; [8] CERN-ACC-2018-0057; [9] arXiv:1911.12230; [10] EPJ Tech. Instrum. 10 (2023) 16; [11] CERN-LHCC-2010-013; [12] JINST 3 (2008) P07007; [13] CERN-LHCC-2012-016; [14] JINST 16 (2021) P02027; [15] NIM A 565 (2006) 188; [16] JINST 13 (2018) C01041; [17] NIM A 924 (2019) 217; [18] CERN-LHCC-2017-009; [19] CMS-TDR-014 (2017); [20] CERN-LHCC-2017-021; Photon Science: [21] Springer (2016); [22] NIM A 607 (2009) 247; 23] Dectris EIGER2 Docs (2020–2024); [24] JSR 13 (2006) 30; [25] Dectris PILATUS3 Specs (2016); [26] PSI JUNGFRAU TDR (2015); [27] JSR 25 (2018) 119; [28] NIM A 633 (2011) S11; [29] Front. Phys. 11 (2023) 1329378; [30] IEEE TNS 58 (2011) 2432; [31] JINST 9 (2014) C05026; [32] NIM A 581 (2007) 485; [33] JINST 8 (2013) C02016; [34] JINST 17 (2022) C01044; [35] CERN Medipix Docs; Astrophysics: [36] ApJ 770 (2013) 103; [37] NIM A 531 (2004) 18; [38] RAL HEXITEC Docs; [39] JINST 15 (2020) C01042; [40] AstroPix Reports (2020–2023); [41] A&A 588 (2016) A1; [42] NIM A 253 (1987) 365; [43] SPIE Press (Janesick); [44] Teledyne HxRG Docs; Medical Imaging: [45] Med. Phys. 40 (2013) 100901; [46] Radiology 289 (2018) 293; [47] Phys. Med. Biol. 52 (2007) 4679; [48] Radiology 298 (2021) 273; Other: [49] IEEE JSSC 43 (2008) 2977; [50] Phil. Trans. R. Soc. A 372 (2014) 20130100; [51] NIM A 926 (2019) 16; [52] Opt. Express 22 (2014) 17573

Basic Principles of Operation of Detectors

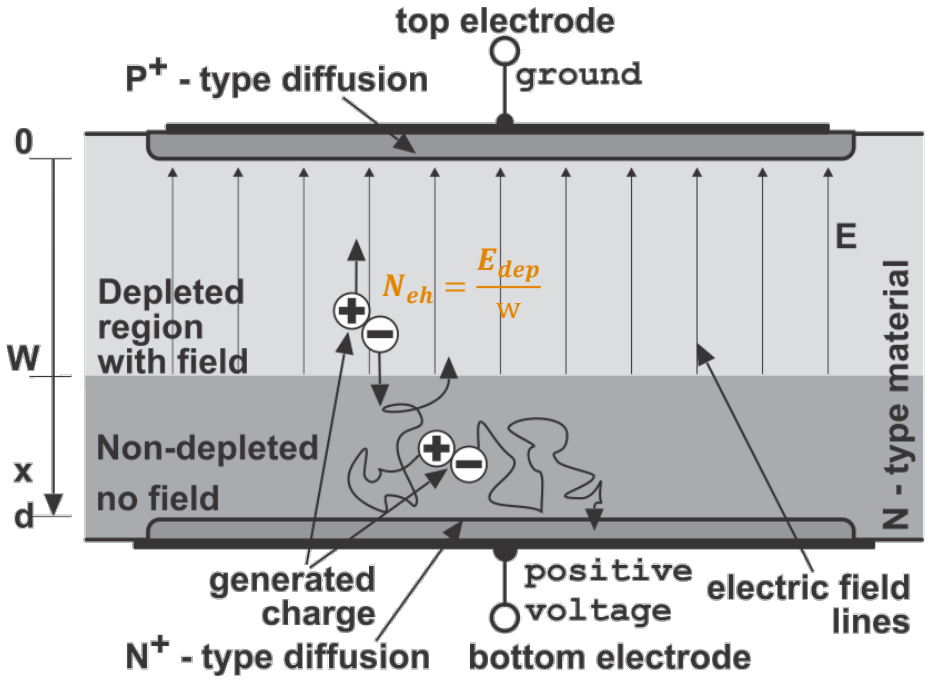
Operation of Semiconductor Radiation Detector 1

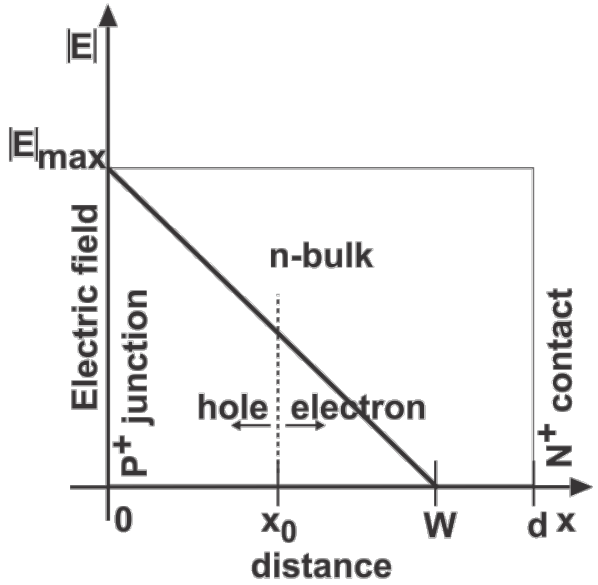
Ionization, transport and charge collection

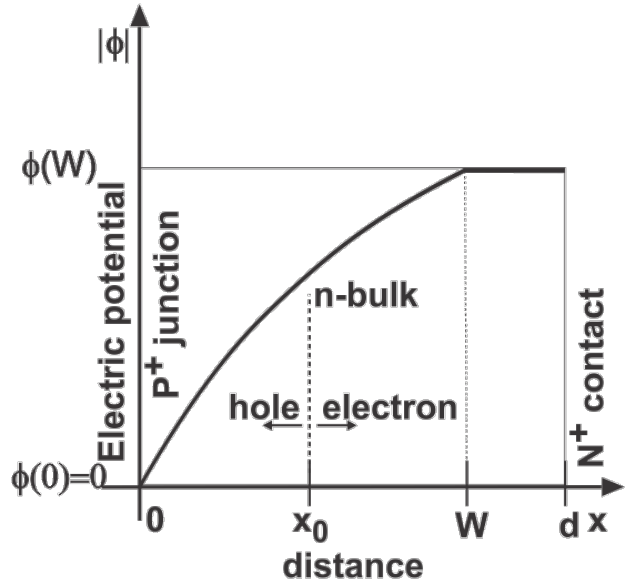
Radiation deposits energy → electron–hole pairs are created

→ electric field separates and transports them

→ diffusion transports (recombination and trapping)







x_0 – depth (from top) where the electron–hole pair is generated

⊕ holes drift toward the top electrode (directed by the electric field)

⊖ electrons drift toward the bottom electrode (if $x_0 < W$, initially by field; below W, by diffusion)

$$|\boldsymbol{E(x)}| = \begin{cases} |E(x)| = \frac{qN_D}{\varepsilon_{Si}}(W-x) = |\boldsymbol{E}|_{\boldsymbol{MAX}}\left(\boldsymbol{1-\frac{x}{W}}\right) & for \quad 0 < x \le W \\ 0 & for \quad W < x \le d \end{cases}$$

$$W \approx \sqrt{\frac{2\varepsilon_{Si}(V_{bi}-V_d)}{qN_D}} \quad for \quad V_{bi} = \frac{kT}{q}\ln\frac{N_A N_D}{n_i^2}$$

$$\boldsymbol{\varphi(x)} = \begin{cases} \varphi(x) = \frac{qN_D}{\varepsilon_{Si}}\left(Wx - \frac{x^2}{2}W\right) = \boldsymbol{E_{MAX}}\left(\boldsymbol{x - \frac{x^2}{2W}}\right) & for \quad 0 < x \le W \\ \frac{E_{MAX}W}{2} & for \quad W < x \le d \end{cases}$$

$w \approx 3.6\ {}^{eV}/_{e^-h^+}$

x – depth from top surface

x_0 – position of generation $(0 \le x_0 < d)$

W – depletion depth (edge of field)

d – thickness of detector

$|E|_{max}$ – maximum field at p^+ junction

N_D – donor concentration in n-bulk

Brookhaven National Laboratory

Operation of Semiconductor Radiation Detector 2

Charge generation - ionization

Deposited energy is converted into mobile electron–hole pairs

$$N_{e,h} = \frac{E_{dep}}{w} \qquad w \approx 3.6\ {}^{eV}/_{e^- h^+}$$

Transport

At high field, add only verbally that velocity eventually saturates.

$$v_{e,h} = \mp \mu_{e,h} E$$

Drift

→ driven by electric field

→ directed and fast

→ reduced trapping and spreading

Diffusion

→ driven by concentration gradient

→ random and slower

→ produces lateral charge sharing

Collection

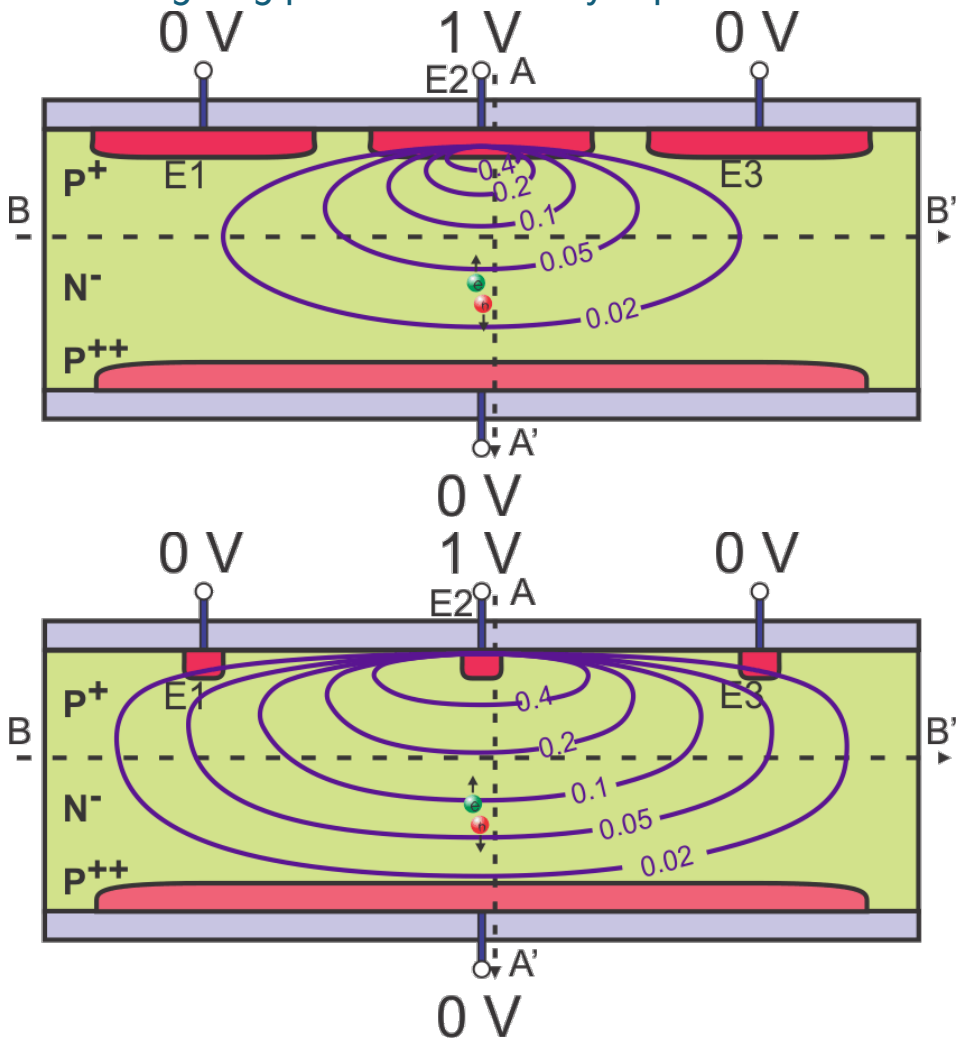
Carriers terminate on electrodes, but the electrical signal begins while they are moving, not only when they arrive.

Brookhaven National Laboratory

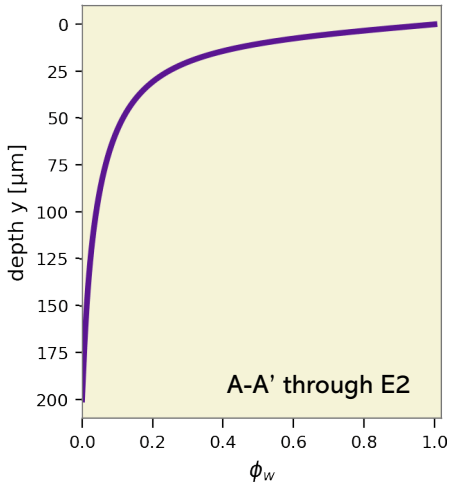
Operation of Semiconductor Radiation Detector 3

Signal induction → physical electric field transports charge; how that motion is observed by particular electrode is defined by weighting field.

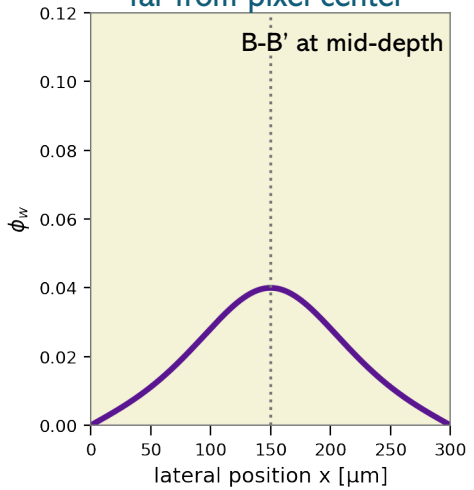
weighting potential is auxiliary Laplace solution



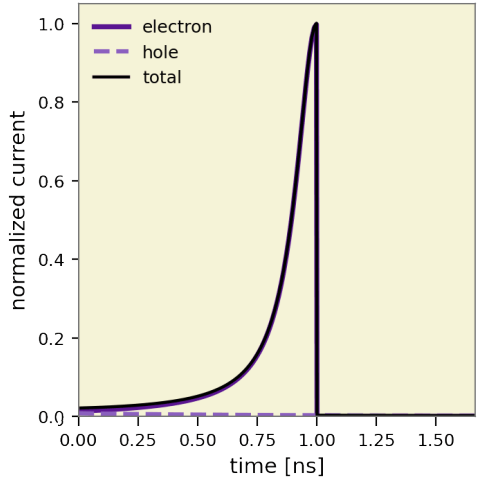
most of potential change occurs near E2



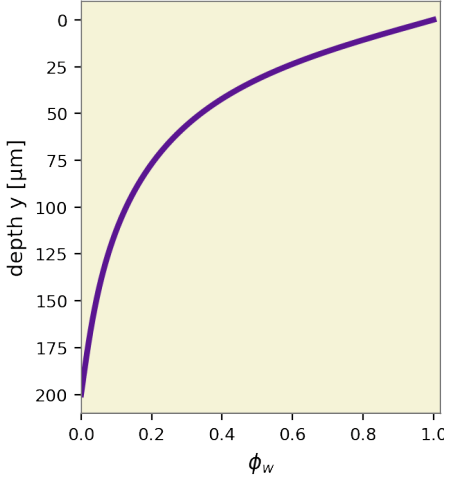
very week sensitivity far from pixel center



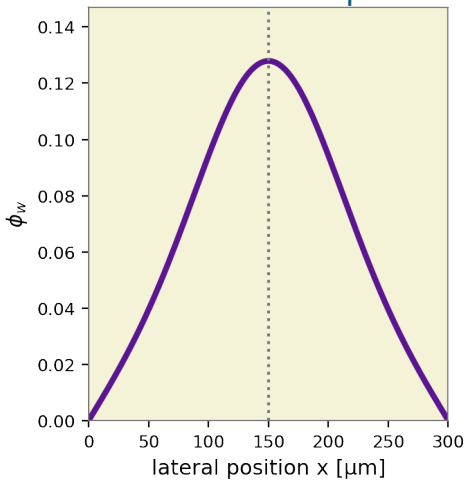
electron pulse is concentrated near collection



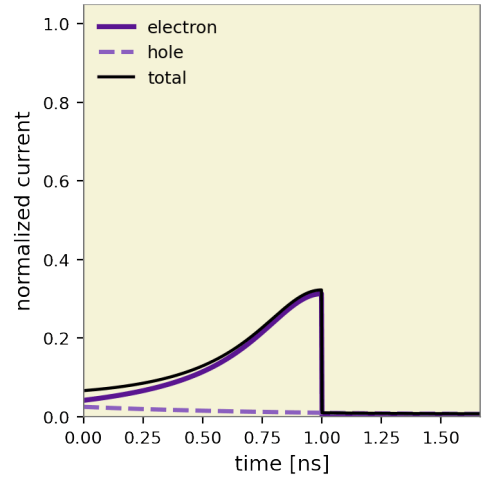
weighting potential penetrates farther into bulk



broader lateral sensitivity at the same depth



signal develops over more of drift; hole motion contributes more strongly



Ex: pitch =100 μm, d=200 μm, w_{small}=20 μm, w_{large}=70 μm

Brookhaven National Laboratory

$$i_k = q\mathbf{v} \cdot \mathbf{E}_{w,k} \qquad \mathbf{v} = q\mathbf{E}$$

$$\Delta Q_k = -q\left(\varphi_{w,k}(f) - \varphi_{w,k}(i)\right)$$

i_k— instantaneous current induced on electrode k q— moving carrier charge, $\mathbf{v}$— instantaneous drift velocity of carrier, $\mathbf{E}_{w,k}$— weighting field of electrode k, Q_k— total induced charge on electrode k, $\phi_w(i)$— weighting potential at where carrier is created, $\phi_w(f)$— weighting potential where the carrier disappears

E-Field Engineering for Semiconductor Detectors 1

From depletion engineering to electrostatic potential engineering

1) p-n junction

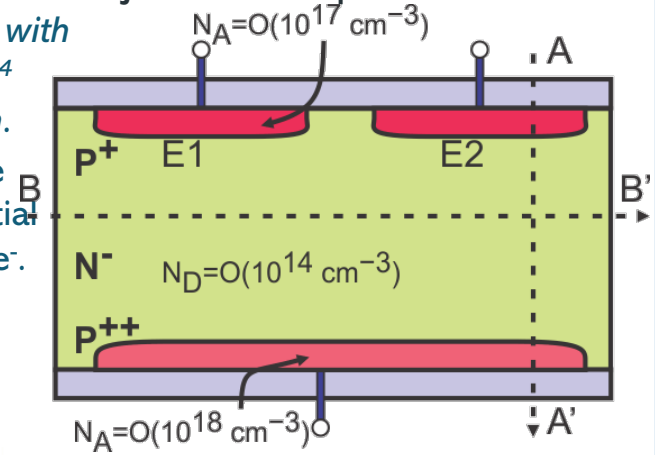
electrons and holes diffuse across junction → potential barrier

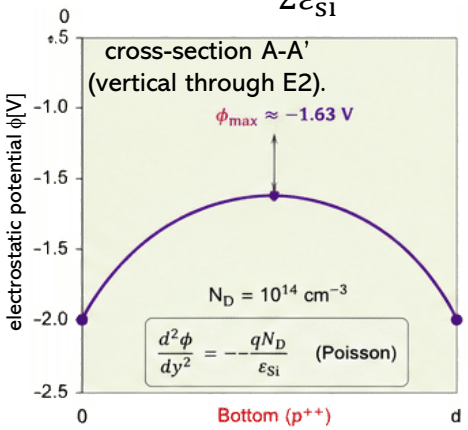
Ex: P^+ E1 *(-1 V) and* P^+ E2 *(-2V) with* P^{++} *implants in* N^- *layer* ($N_D=10^{14}$ cm^{-3}) *at 300 K) – thickness 4*μm.

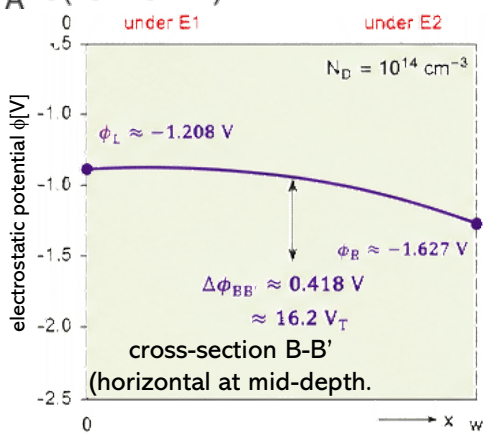
Applied electrode biases + space charge shape electrostatic potential → drift field transporting signal e^-.

$$\nabla^2\varphi = -\frac{qN_D}{\varepsilon_{si}}$$

$$\varphi_{A\text{-}A'}(y) = -2 + \frac{qN_D}{2\varepsilon_{si}}(y^2\text{-}dy)$$







Entire N^- acts as drift region guiding carriers to electrode of higher potential → e- drift towards E1, h^+ are collected by P implants.

How about current flow? for depleted N^- layer, only leakage and transients.

$$\varepsilon_{Si} = 11.7\varepsilon_0(1.036\times10^{-12}\ {}^{F}/_{cm});\ V_T = \frac{kT}{q} = 25.9\ mV$$

E. Gatti and P. Rehak, Nucl. Instrum. Methods Phys. Res. 225 (1984) 608

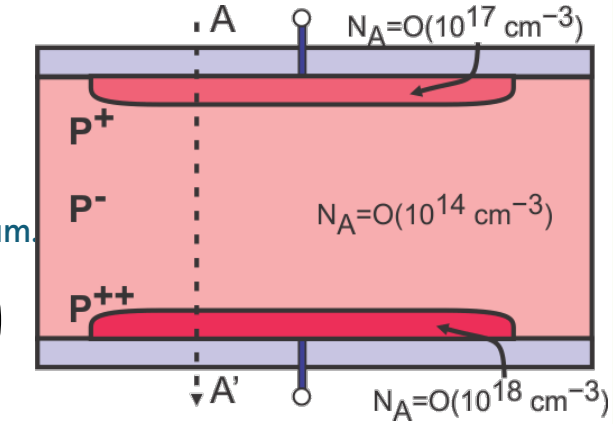
2) Same type but different doping concentration

majority carriers diffuse to regions of lower concentrations → potential barrier

Ex: P^+ *(-1 V) and* P^{++} *(-2V) implants in* P^- *layer* ($N_A=10^{14}$ cm^{-3}) *at 300 K).*

To equalize Fermi level, electrostatic potential adjusts at thermal equilibrium.

$$\Delta\varphi_{12} = \varphi_2 - \varphi_1 = V_T \ln\left(\frac{N_{A1}}{N_{A2}}\right)$$

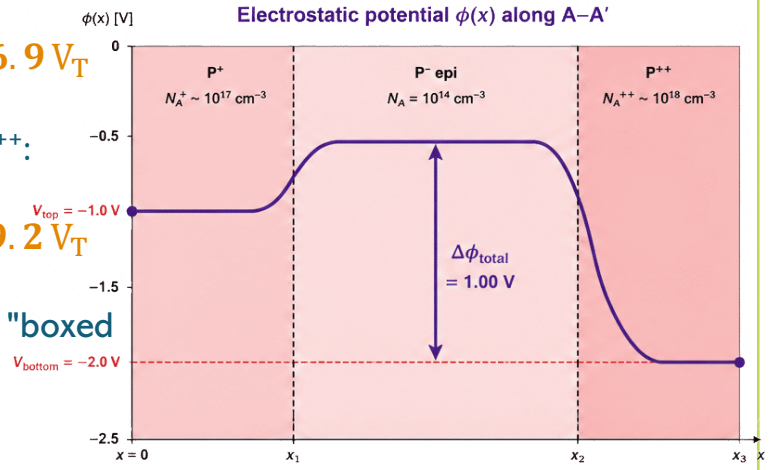


- Barrier between P^+ and P^-:

$$\Delta\varphi_{P^+P^-} = V_T \ln\left(\frac{10^{17}}{10^{14}}\right) \approx 6.9\ V_T$$

- Barrier between P^- and P^{++}:

$$\Delta\varphi_{P^+P^-} = V_T \ln\left(\frac{10^{18}}{10^{14}}\right) \approx 9.2\ V_T$$



P^- region is electrostatically "boxed in" by 2 potential barriers for minority e^-.

How about current flow?

- for undepleted, uniformly doped P^- layer, current density is approximately:

$$J_p = q\mu_p N_A E \approx q\mu_p N_A \frac{\Delta V}{L} = \rho_p^{-1}\frac{\Delta V}{L} \approx \frac{1}{139L} \quad J_p \approx 7.2\ {}^{A}/_{cm^{-2}}\Big|_{L=10\mu m}$$

Holes are majority carriers everywhere, they drift through entire structure

E-Field Engineering for Semiconductor Detectors 2

From field shaping to controlled charge storage and transfer

3) MOS structure - photogate

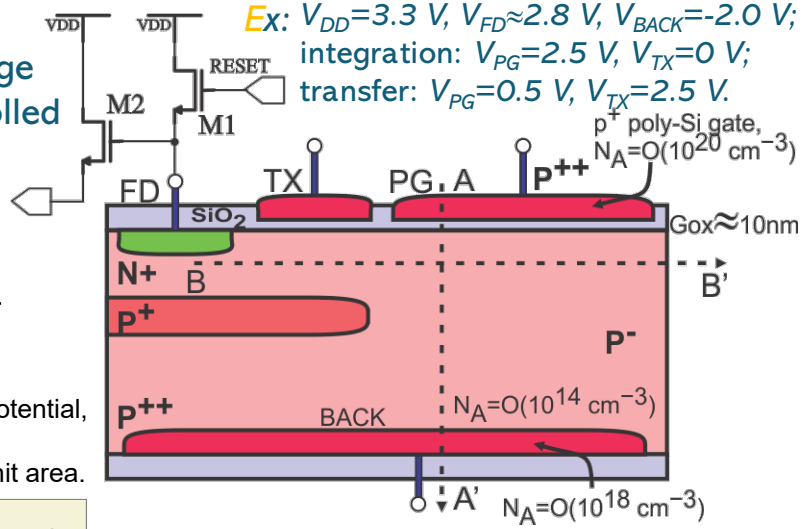
Electrically controlled potential well → storage well is primarily controlled dynamically by gate voltage

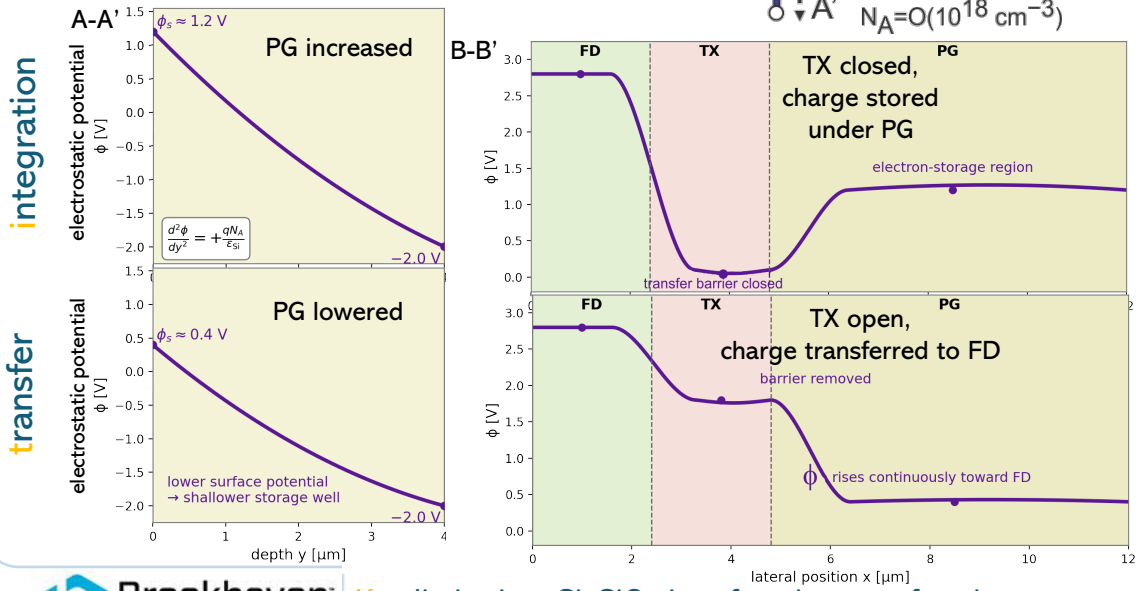
$$V_{PG} = V_{FB} + \psi_s - \frac{Q_s}{C_{ox}}$$

$$Q_d = -\sqrt{2q\varepsilon_{Si}N_A\psi_s}$$

V_{FB} = flat-band voltage,
ψ_s = semiconductor surface potential,
Q_s = semiconductor charge,
C_{ox} = oxide capacitance per unit area.

Ex: V_{DD}=3.3 V, V_{FD}≈2.8 V, V_{BACK}=-2.0 V; integration: V_{PG}=2.5 V, V_{TX}=0 V; transfer: V_{PG}=0.5 V, V_{TX}=2.5 V.



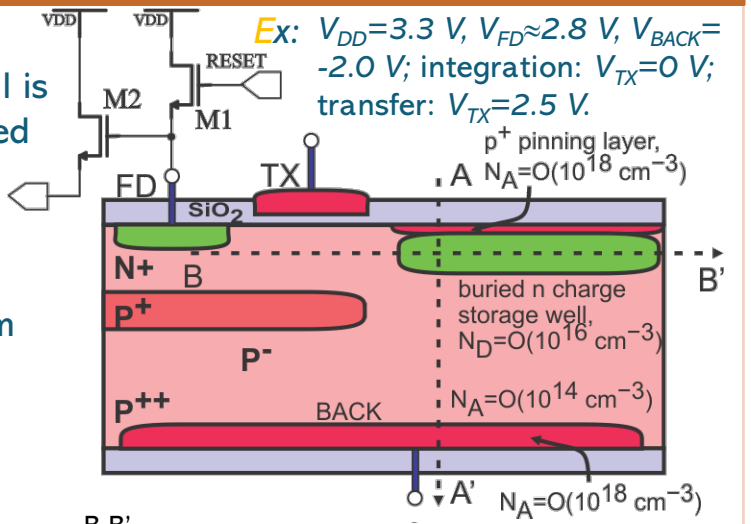


Key limitation: Si–SiO_2 interface is part of active storage region → dark current and interface-state noise important.

4) Pinned PhotoDiode

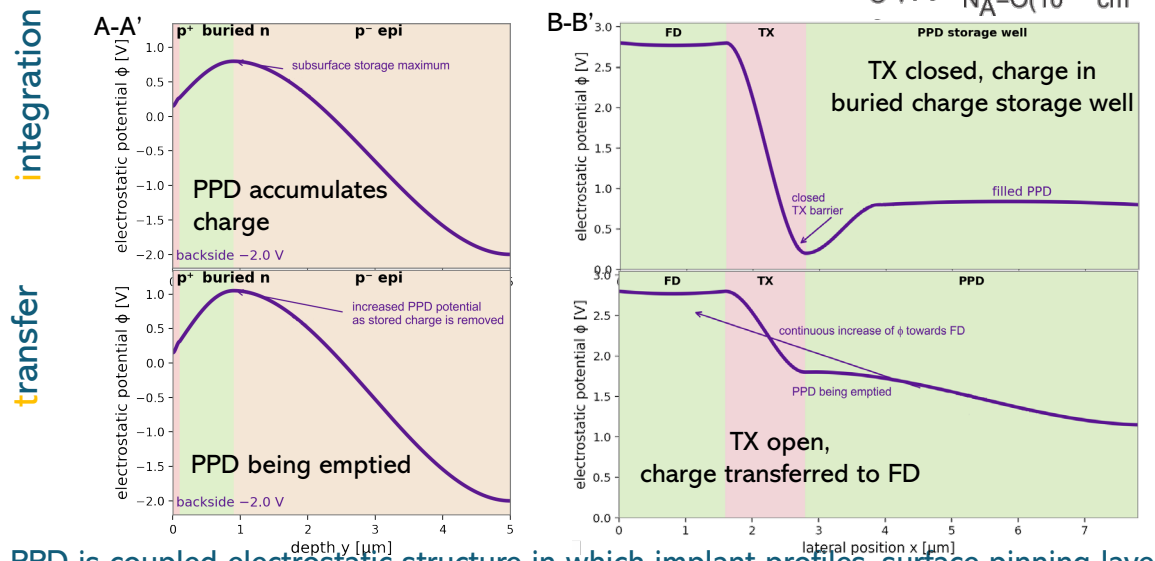
Technological control of potential well → storage well is primarily defined by implanted doping profiles + pinned surface potential

Ex: V_{DD}=3.3 V, V_{FD}≈2.8 V, V_{BACK}=-2.0 V; integration: V_{TX}=0 V; transfer: V_{TX}=2.5 V.



Representative dimensions:

- P+ pinning layer =100 nm
- Buried N well = 0.8 μm
- Depleted P- epi = 5 μm
- TX gate length = 1.2 μm



PPD is coupled electrostatic structure in which implant profiles, surface pinning layer, transfer gate and floating diffusion are designed to yield storage and complete transfer
Result: low dark current, low image lag and low-noise charge transfer.

N. Teranishi, Y. Ishihara, and H. Shiraki, Japanese Patent JP 1,728,783, 1990

E-Field Engineering for Semiconductor Detectors 2

Comparative: Photogate vs. Pinned PhotoDiode

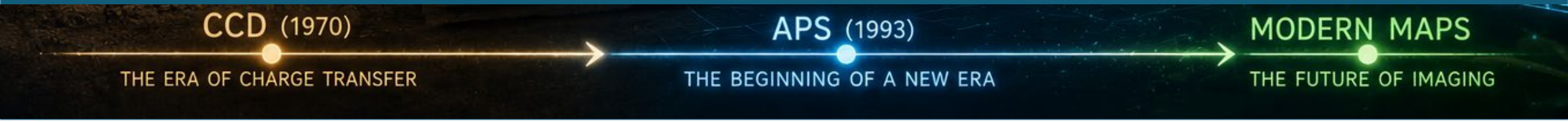
Photogate	Pinned PhotoDiode
Potential well created mainly by gate voltage	Potential well created mainly by implants
Charge stored close to oxide interface	Charge stored below the surface
Well depth dynamically adjustable	Surface potential pinned
Interface dark current can be significant	Surface dark current strongly suppressed
Transfer controlled by clocked gates	Transfer controlled by dedicated transfer gate
Voltage-defined storage	implant-defined storage with voltage-controlled transfer

Photogates create charge-storage wells electrically;

Pinned PhotoDiodes embed well in doping profile and use gate only for controlled transfer.

Brookhaven National Laboratory

Introduction



CCDs vs. MAPS: Charge Transfer vs. In-Pixel Readout

CCDs

Charge-domain signal transport

Signal charge is transferred pixel-to-pixel and converted at one or a few output nodes.

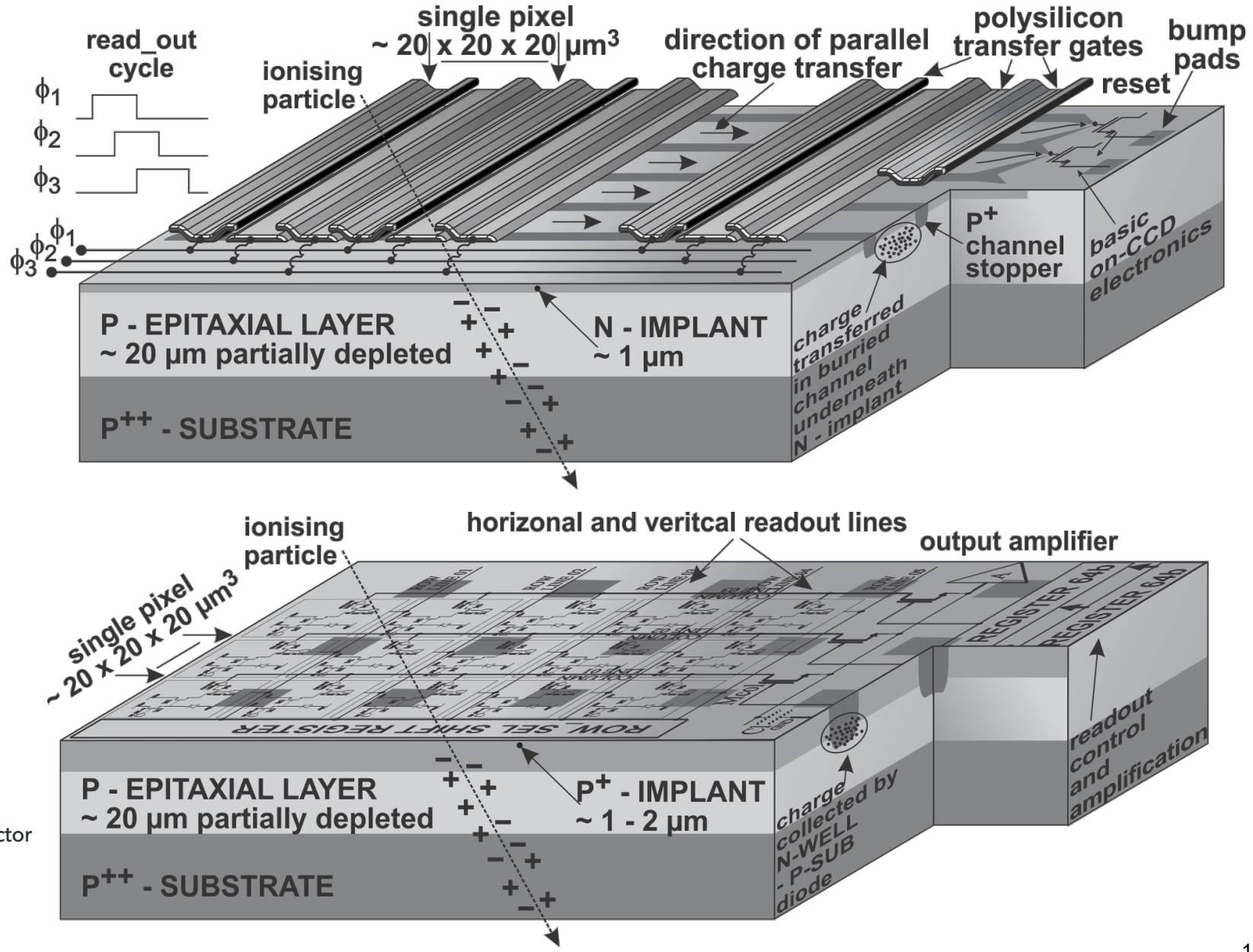
Readout	mostly sequential
Electronics in pixel	none
Strengths	excellent uniformity, lowest read noise, large-area imaging
Main limitation	serial charge transfer; clock complexity; transfer inefficiency especially after irradiation

MAPS

Local charge-to-voltage conversion

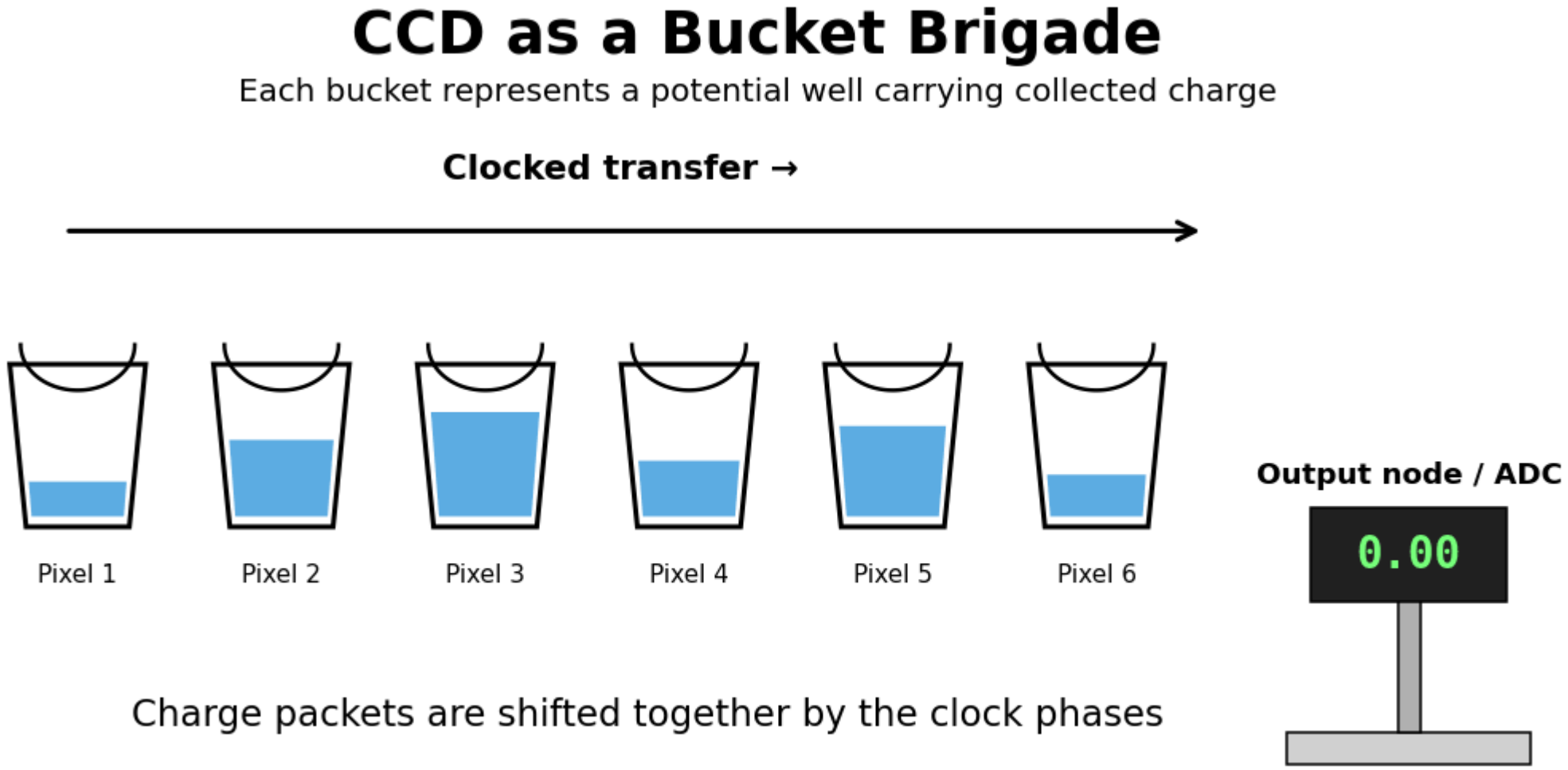
Charge is collected and converted locally; pixels are addressed through electrical interconnects.

Readout	rolling shutter, global shutter, ROI or event-driven
Electronics in pixel	analog front-end, discrimination, timing, memory, ADC, intelligence
Strengths	parallelism, integration, speed, functionality, scalable systems
Main limitation	pixel nonuniformity, analog/digital coupling, fill-factor trade-offs



Brookhaven National Laboratory

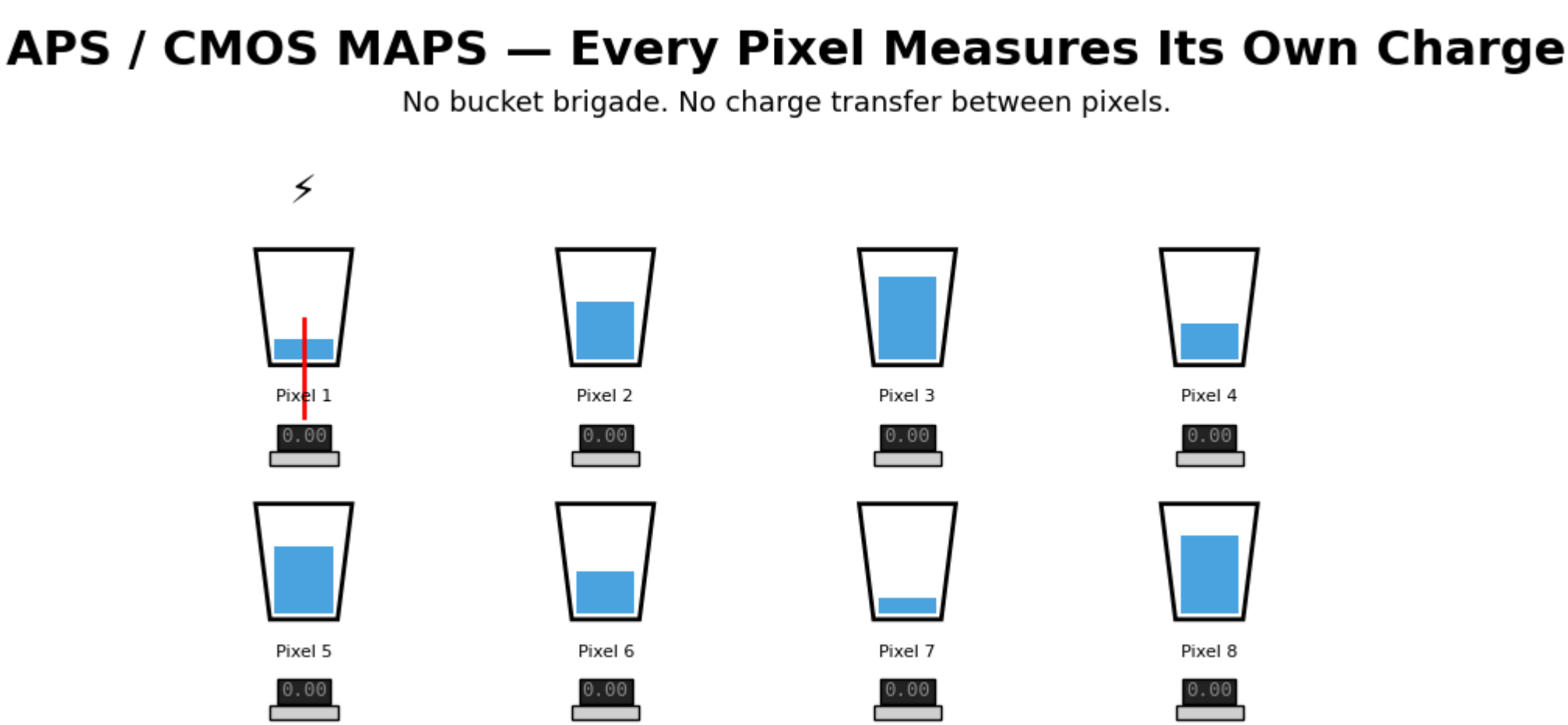
CCDs v.s. MAPS (CMOS Image Sensors) - 1



CCD: Charge Moves

Brookhaven National Laboratory

CCDs v.s. MAPS (CMOS Image Sensors) - 2



MAPS: Charge Stays – Information Moves

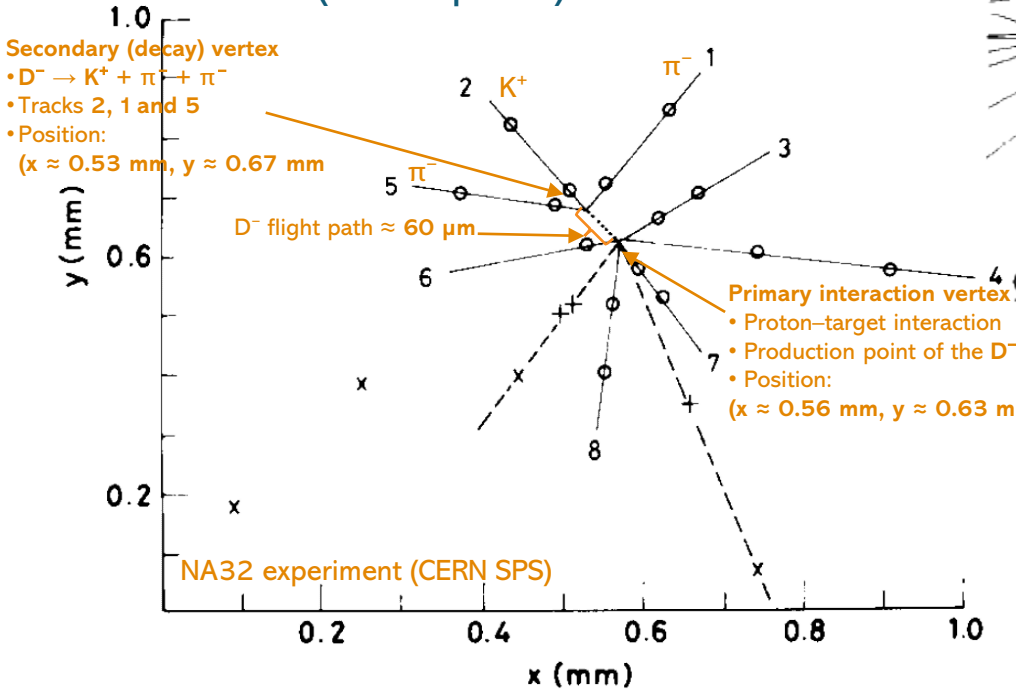
Brookhaven National Laboratory

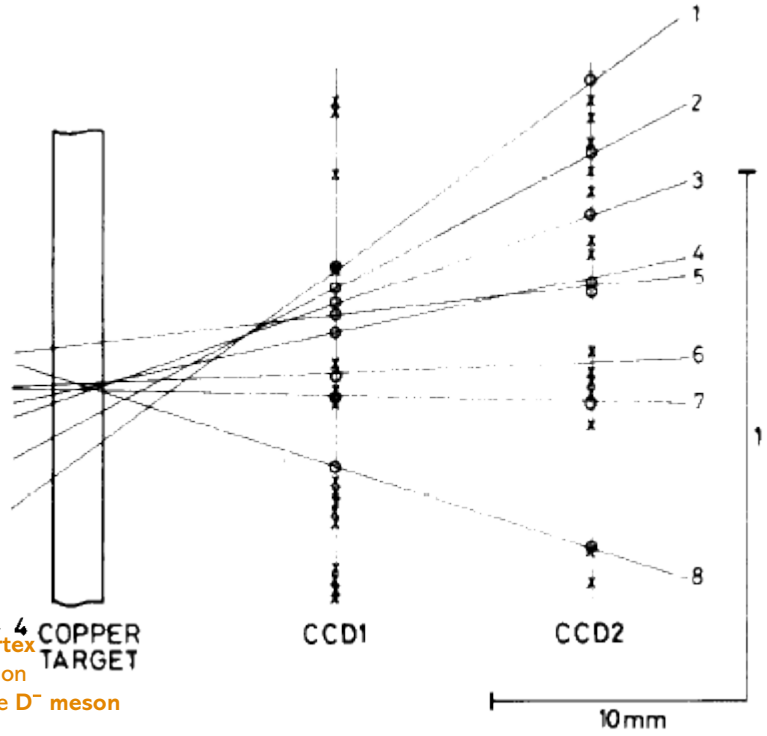
CCDs v.s. MAPS (Origins of Si Pixel Tracking)

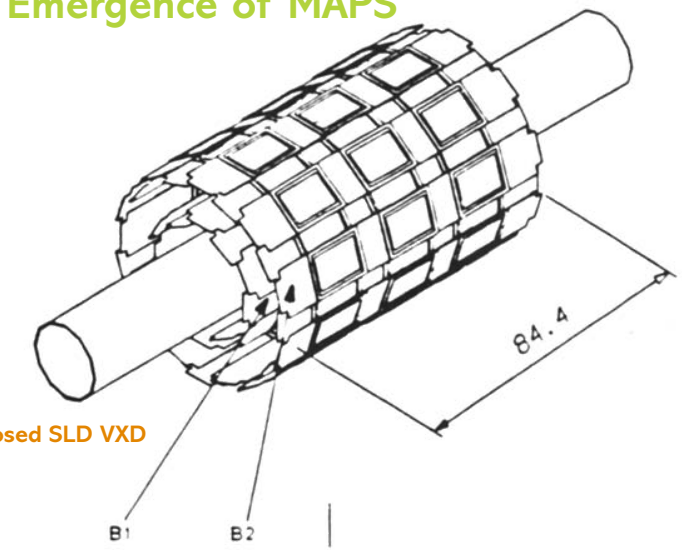
Before MAPS, CCDs proved that a fine-pitch silicon imager could also be an extraordinarily precise tracking detector.

Historical Timeline:

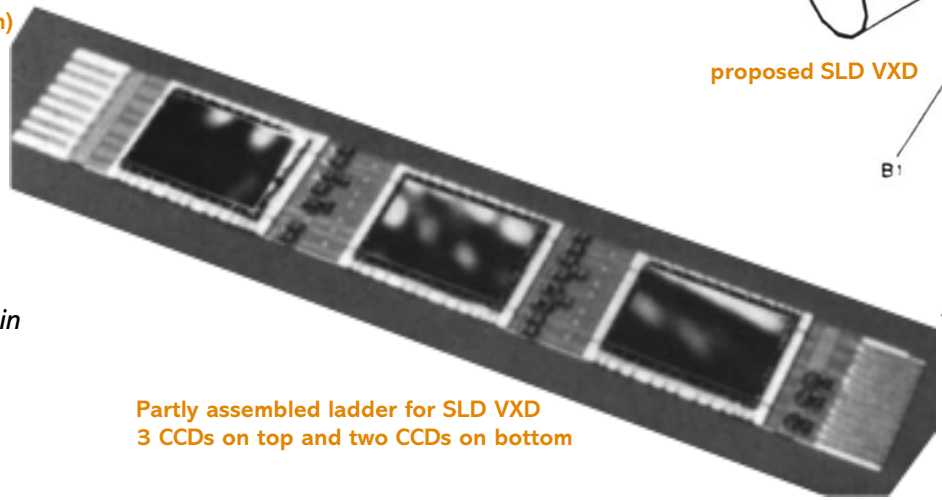
- 1970 – CCD invented in Bell Labs (optical)
- 1981 – Particle tracking proposed
- 1981/1983 – CERN beam test
- 1984/1985 – ACCMOR NA32 (first tracking)
- 1987 SLD CCD VXD proposal
- 1990 VXD1 (120 Mpixels)
- 1990–1998 – SLD VXD2/VXD3
- 1992–95 VXD2
- 1996–98 VXD3 (307 Mpixels)
- 1998-2005 CPCCD, ISIS, thin ladder for future Linear Collider
- ~2000 GLCvertex, LCFI, US LC vertex collabs
- Emergence of MAPS



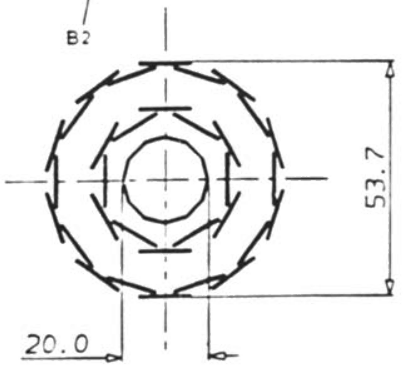




proposed SLD VXD



Partly assembled ladder for SLD VXD
3 CCDs on top and two CCDs on bottom

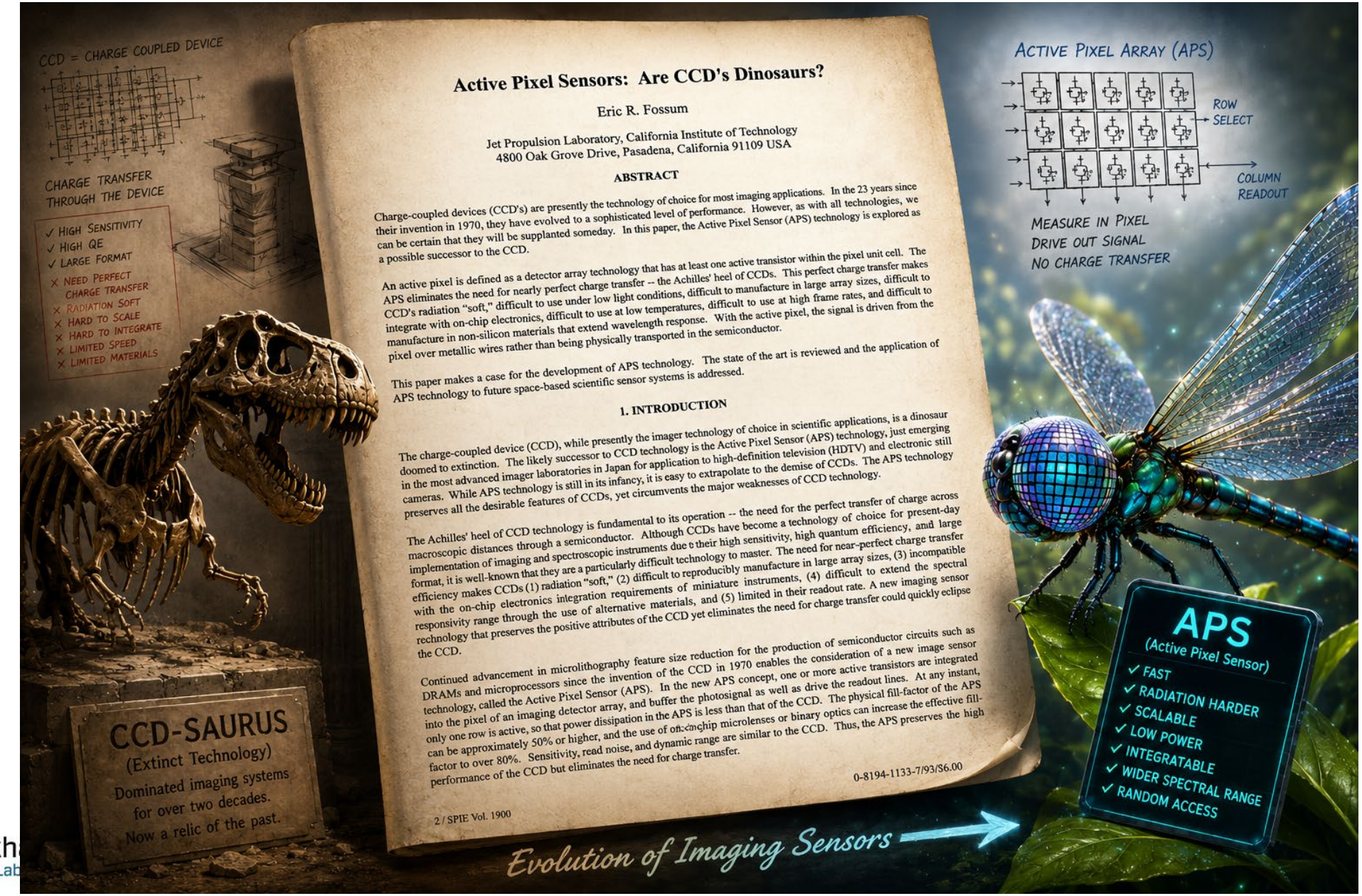


first charm decay seen with Si detector by ACCMOR Collaboration in 1984, using thin target followed by CCDs at 1 and 2 cm beyond (view along beam direction).

Brookhaven National Laboratory

C.J.S. Damerell *et al.*, **NIM A 253 (1987) 478–481.**
C.J.S. Damerell, **NIM A 541 (2005) 178–188**

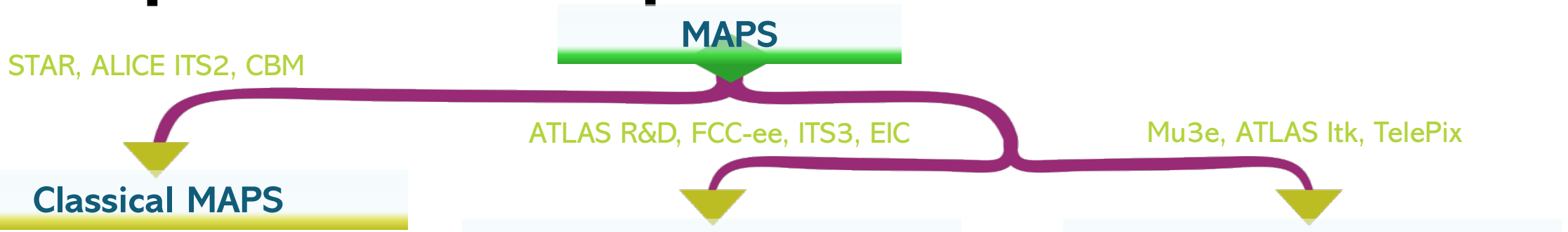
CCDs v.s. MAPS (Turning Point)



paper real,
image AI-generated

Families of MAPS Detectors

Non-Nepleded v.s. Depleted Q Collection Volume



Classical MAPS

charge collection primarily by diffusion

Small collection electrode (typically n-well diode)

↓

Electronics outside sensing node

↓

Medium capacitance (10–30 fF, medium Q/C)

↓

Low radiation resistance

AMS 0.6 µm, AMS 0.35 µm OPTO — IReS/IPHC

MIMOSA 1 → 28 (Ultimate) → STAR PXL → CBM → MIMOSIS

first MAPS system used in experiment

NP (STAR PXL in HFT in STAR at RHIC)

TowerJazz 180 nm — CERN ALICE ecosystem

FSBB-MO, MISTRAL → ASTRAL → ALPIDE → ALICE ITS2

ALPIDE = culmination of classical MAPS.

- Sparse data-driven RO replaced rolling shutter
- Q collection still mostly diffusion-based.

Small Collection Electrode

charge collection by diffusion/drift

Small collection electrode (typically n-well diode)

↓

Electronics outside sensing node

↓

Very low capacitance (2–5 fF, high Q/C)

↓

Very low analog power

↓

Very low noise

↓

Low-Voltage operation (partially – depleted or fully depleted)

↓

Excellent energy resolution

↓

Potential for precise timing

↓

Need sophisticated electric-field engineering

↓

Radiation hardness relies on electric-field optimization

Large Collection Electrode

charge collection primarily by drift

Large collection diode (typically n-well or p-well diode)

↓

Electronics inside collection well

↓

High capacitance (100 fF and 400 fF not unusual, small Q/C)

↓

Higher analog power

↓

Hich voltage operation (depleted)

↓

Much stronger electric field

↓

Very short drift

↓

Excellent radiation hardness

↓

Uniform timing

↓

Lower gain

↓

Lower energy resolution

Small Electrode v.s. Large Electrode MAPS

Depleted MAPS

Small Collection Electrode

low capacitance and power

Tower Semiconductor 180 nm CIS — CERN / Bonn / CPPM / Oxford / Birmingham

TJ-Monopix 1 → 2 → OBELIX — Belle II VTX derivative, MALTA mini → 2 → 3, CLICTD-demo

LFoundry 110 nm CIS — INFN

ARCADIA ER1 → ER2 → ER3; MD1 → MD2 → MD3

Tower Semiconductor 65 nm CIS — CERN-ALICE ecosystem / RAL / INFN / DESY / IPHC Strasbourg – U. Frankfurt / CEA / BNL / SLAC

APTS, DPTS, CE65, FASTPIX, MOSS → MOSAIX, TANGERINE, MANTA, CACTUS, OCTOPUS, CE-TPiX

OBELIX = Belle II upgrade
MOSAIX = ALICE ITS3 upgrade and ePIC Inner Barrel SVT for EIC

third family

SOI

separate technology branch for fully depleted monolithic sensing FD-SOI

Wafer-bonded high-resistivity substrates

↓

Variants with small and large collection electrode (substrate diode with connection through BOX)

↓

Electronics above sensing volume

↓

Low radiation resistance and couplings

OKI / LAPIS Semiconductor 200 nm FD-SOI CMOS — SOIPIX Collaboration KEK

CPIX, INTPIX, SOFIST, SOIPIX, XRPIX, SOFI X-ray, Astrophysics, Synchrotron

Large Collection Electrode

LFoundry 150 nm HV-CMOS — Bonn / CPPM / CERN

LF-CPIX, LF-Monopix 1 → 2, RD50 - MPW1 → MPW2 → MPW3 → MPW4

AMS / TSI 180 nm HV-CMOS — Heidelberg / KIT / PSI

MuPix 7 → 8 → 10 → 11 — final Mu3e sensor, ATLASPix 1 → 2 → 3 → 3.1, AstroPix, TelePix

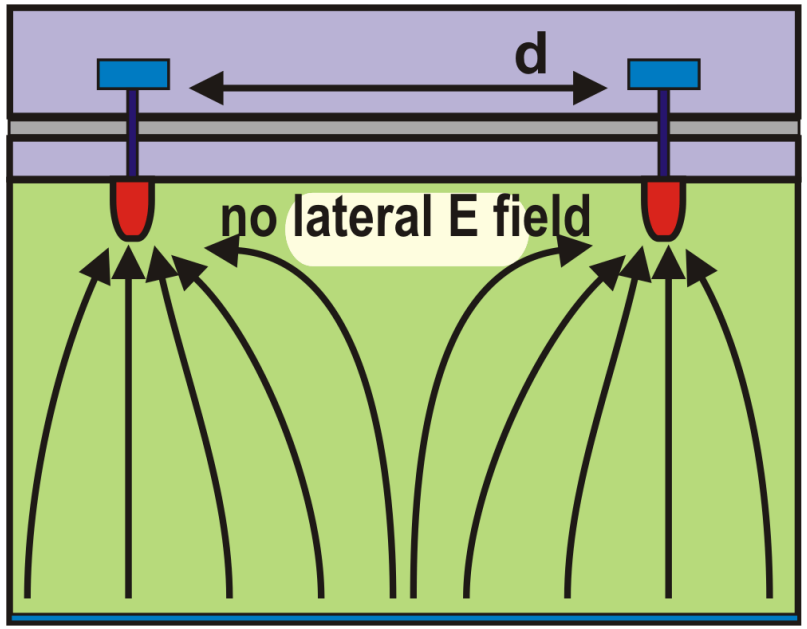
AMS 180 nm HV-CMOS — Heidelberg / KIT / CERN-RD50

H35DEMO, H18 / CCPD prototypes, HV2FEI4, ATLASPix precursors

Brookhaven National Laboratory

Role of Large Electrode in Charge Collection

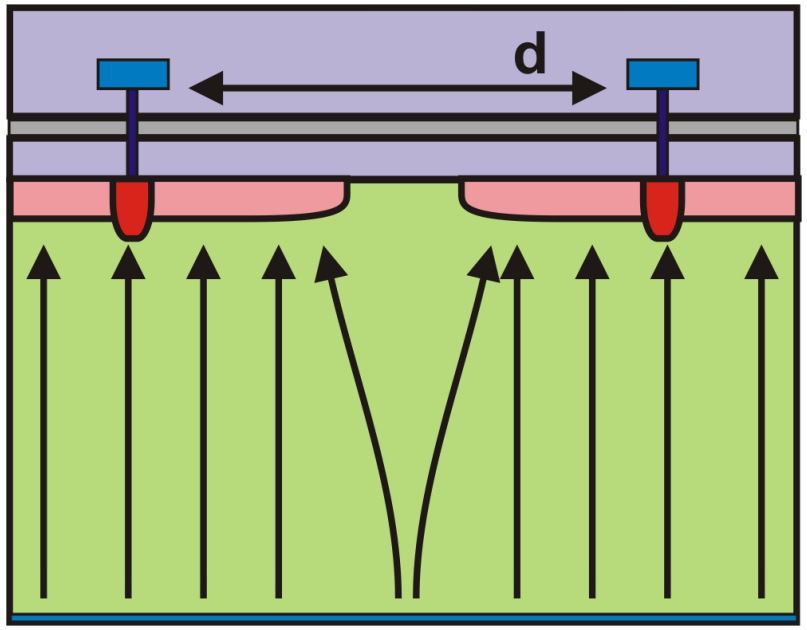
Small Collection Electrode



Generally electric field in p-on-n (/ n-on-p) sensor is not uniform in case of very small p-type (/n-type) implants separated by large lateral distance:

- potential pockets can be created,
- no electric field areas – thus no/slow charge collection from some regions

Large Collection Electrode



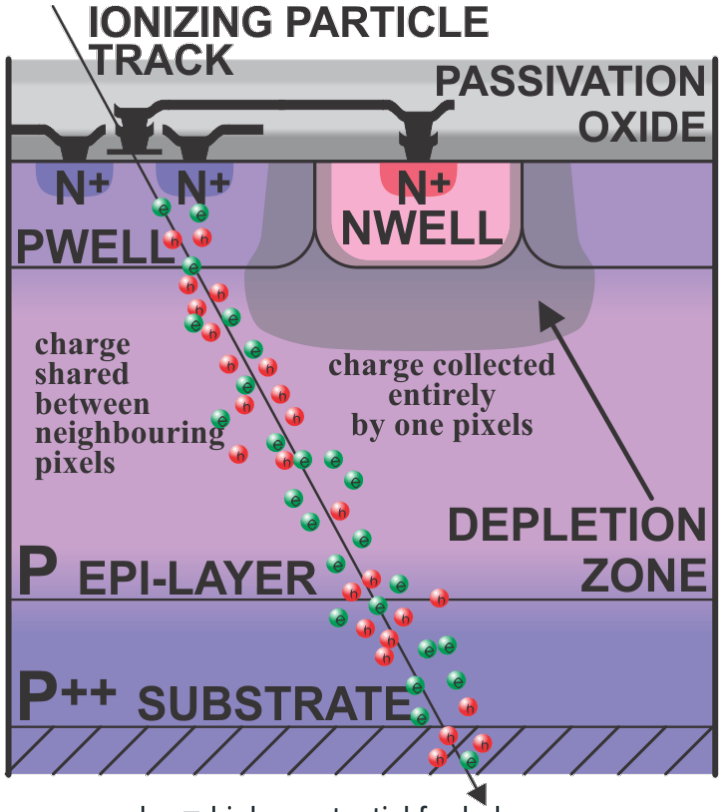
Distribution of electric field can be improved by increasing effective sizes of implants:

- smaller distances between implantation islands may lead to shorts, especially if inversion / accumulation charge gets trapped at interface,
- large charge collection implants "steal" real estate from transistors in bulk MAPS and not deep internal electrode available.

Brookhaven National Laboratory

Overview of MAPS Detectors

Early MAPS: Charge Collection by Diffusion (2000) 1



warmer color = higher potential for holes

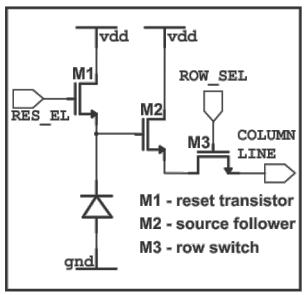
Key idea: Thin, lightly doped p-type epitaxial layer of standard CMOS process serves as sensitive volume. Small n-well/p-epi diodes collects charge (e-).

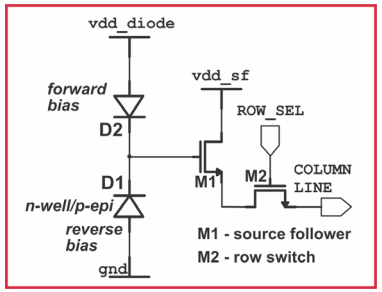
Strengths:

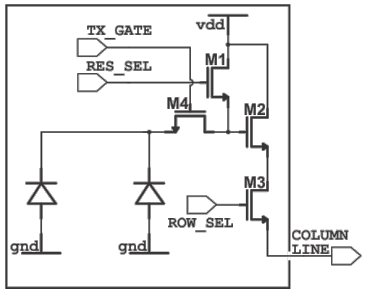
- **Monolithic integration:** no bump bonding or separate sensor wafer → low material budget
- **Small pixel pitch:** typically $10–30\ \mu m$.
- **Low input capacitance:** small collection diode → low noise (after CDS).
- **Commercial CMOS fabrication:** low cost and high yield, access to stitching.
- **Charge sharing:** supports spatial resolution better than binary pitch/$\sqrt{12}$.

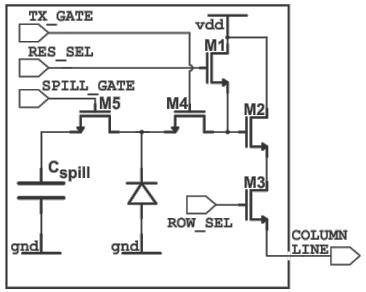
Main issues:

- **Mostly undepleted epi-layer:** thermal diffusion dominates charge collection.
- **Slow and position-dependent collection:** increased recombination and trapping sensitivity → limited radiation tolerance (TID≈150 krad, NIEL>10_{13} n_{eq}/cm_2) and timing performance.
- **Charge spreads over several neighboring pixels:** clusters produced → Q single diode ↘.
- **Rolling-shutter or raster-scan readout:** long frame integration times and pile-up
- **Standard twin-well CMOS:** restricts full CMOS circuitry because PMOS n-wells compete for charge → limited choices of circuit solutions, i.e. 3T, 3TSB or 4T pixels.

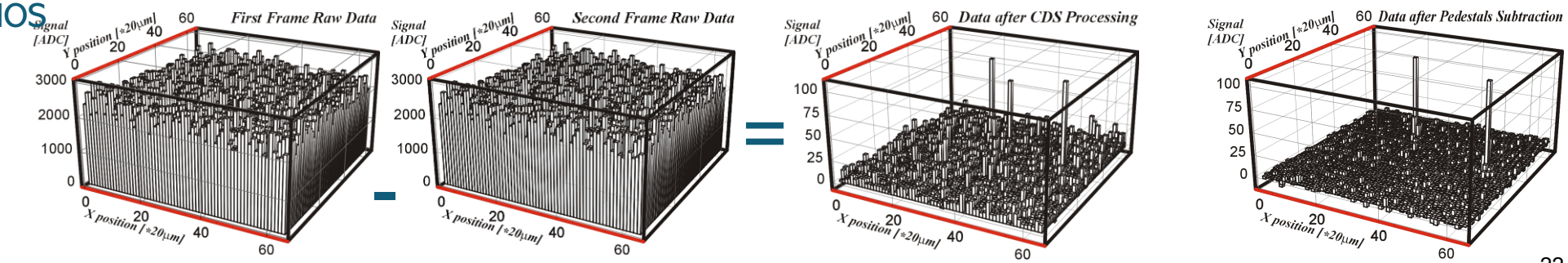








- **Lack of amplification in pixel:** Fixed Pattern Noise dominating → frame CDS



Brookhaven National Laboratory

G. Deptuch et al., IEEE Trans. Nucl. Sci. 49 (2002) 601 , M. Deveaux, JINST 14 (2019) R11001, C. Hu-Guo et al., Nucl. Instrum. Methods Phys. Res. A 623 (2010) 480–482

Early MAPS: Charge Collection by Diffusion (2000) 2

Diffusion-Dominated Charge Collection: Why It Takes ~100 ns

For diffusion over a characteristic distance L: $\boxed{\langle r^2 \rangle = 2nDt}$,

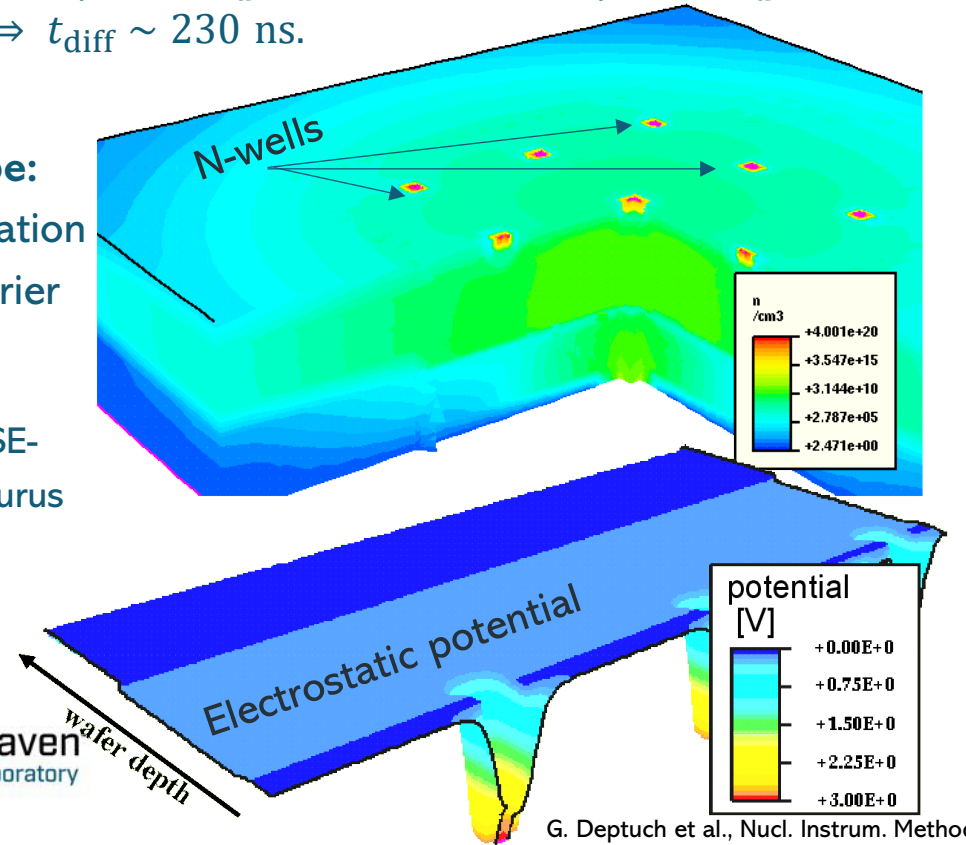
where n = # dimensions; for 1D estimate: $\boxed{t_{\text{diff}} \sim \frac{L^2}{2D}}$.

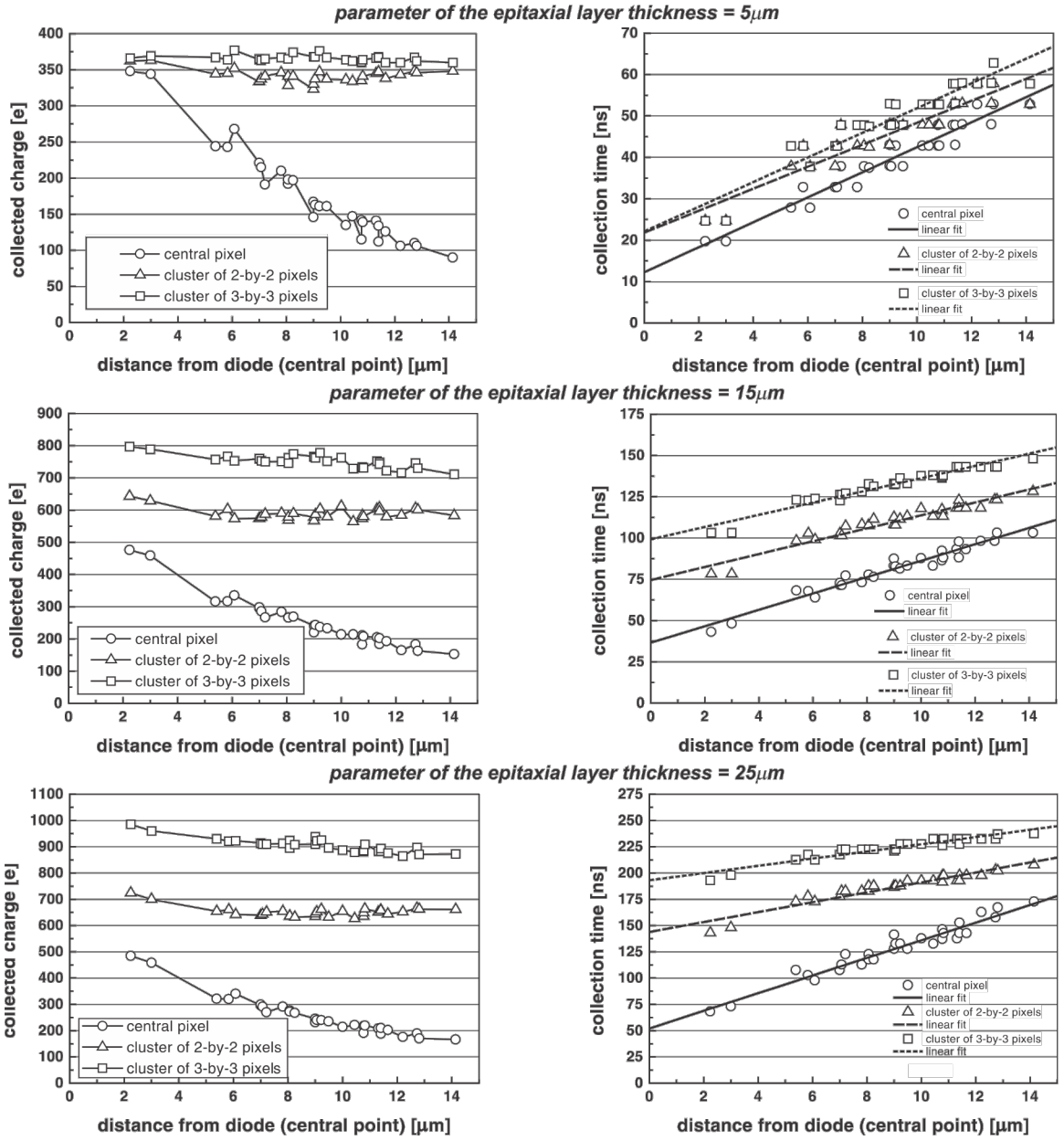
For e⁻ in Si at RT: $D_e = \mu_e \frac{kT}{q}$

and using: $\mu_e \approx 1{,}350\ \text{cm}^2\ \text{V}^{-1}\text{s}^{-1}$, and $D_e \approx 35\ \text{cm}^2/\text{s}$,
one gets: $L = 20\ \mu\text{m} \Rightarrow t_{\text{diff}} \sim 57\ \text{ns}, L = 30\ \mu\text{m} \Rightarrow t_{\text{diff}} \sim 130\ \text{ns}$,
$L = 40\ \mu\text{m} \Rightarrow t_{\text{diff}} \sim 230\ \text{ns}$.

Simulation type: transient simulation of minority carrier density

Former DESSIS ISE-TCAD now Sentaurus Dvice Simulator (Synopsys)

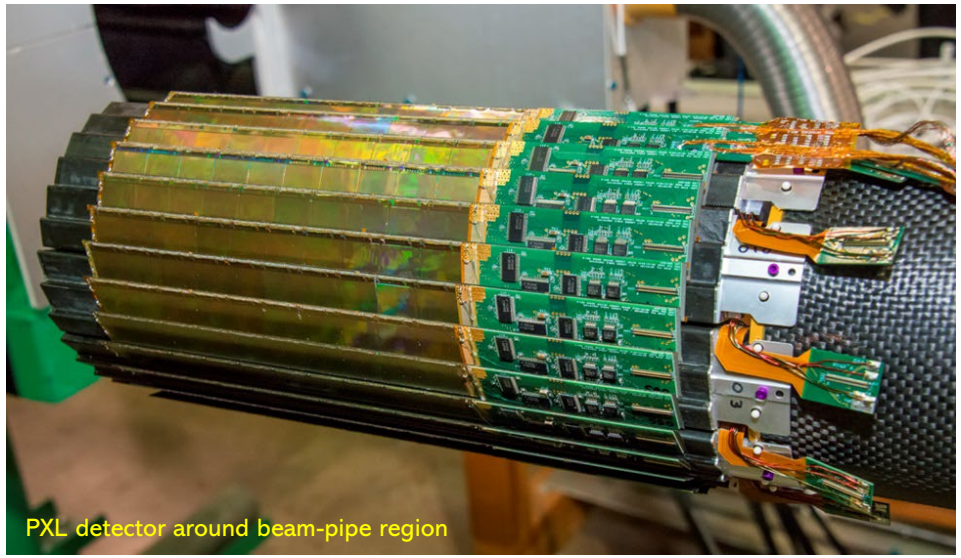




G. Deptuch et al., Nucl. Instrum. Methods Phys. Res. A 465 (2001) 92–100

Early MAPS: Charge Collection by Diffusion (2000) 3

Diffusion-based MAPS went from sensor prototypes to working low-mass vertex detector at RHIC STAR


PXL detector around beam-pipe region

PXL system scale

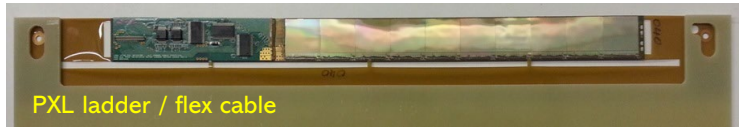
- 2 innermost layers at r = 2.8 and 8 cm
- 10 sectors, 40 ladders / 400 sensors ≈ 356 million pixels
- ≈ 0.16 m² active area, sensors thinned to 50 µm
- Air cooling, low material ≈ 0.37% X_0 per layer
- Frame integration time (rolling shutter): 185.6 µs

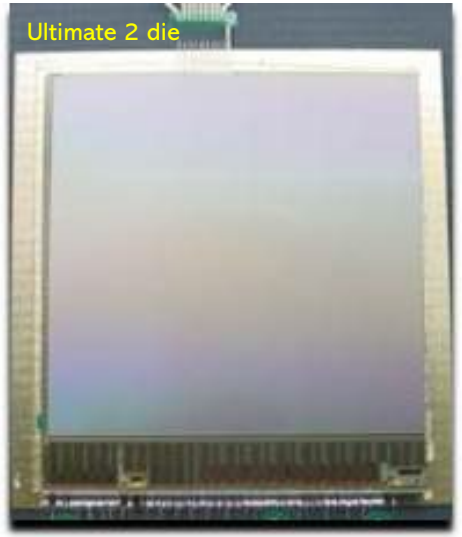
Ultimate-2 (MIMOSA-28)

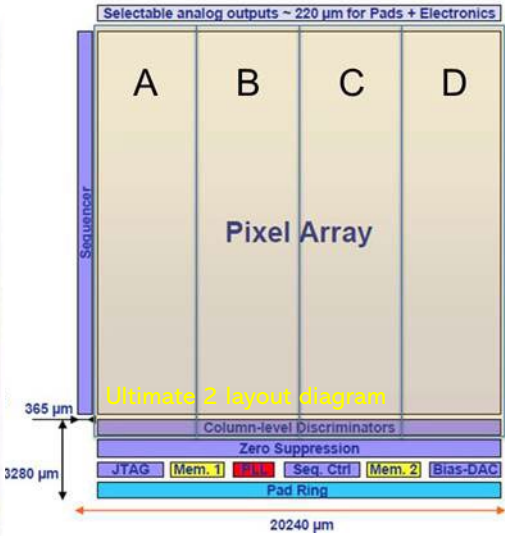
- 0.35µm CMOS OPTO
- 20.7 × 20.7 µm² pixels; 928 × 960 matrix
- 50 µm sensor thickness
- ENC = 10–12 e^- ; S/N ≈ 30, >99% efficiency
- On-chip discrimination + sparsification

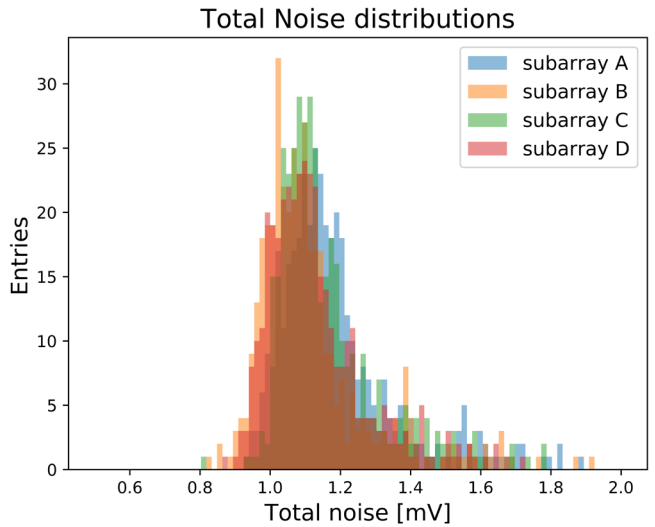
What STAR demonstrated

- First large-scale thin-MAPS vertex detector at a collider
- >99% hit efficiency and ≈ 4 µm single-point resolution
- Reliable operation with air cooling and ultra-low material
- Direct topological reconstruction of open-charm decays


PXL ladder / flex cable


Ultimate 2 die





Why STAR needed MAPS

- Reconstruct displaced charm-hadron decay vertices ($D^0 \rightarrow K^-\pi^+$, $c\tau \approx 123$ µm)
- Improve track pointing from millimeter scale to a few ×10 µm
- Minimize multiple scattering with thin, air-cooled detector layers

Brookhaven National Laboratory

STAR PXL detector demonstrated for the first time that MAPS could operate reliably as large-scale collider vertex detector, paving the way for MAPS in ALICE ITS2, ITS3 R&D, ePIC, FCC-ee, and many future experiments.

L. Greiner et al., "The STAR MAPS-based PiXeL detector," Nucl. Instrum. Methods Phys. Res. A 845 (2017) 573–578; STAR PXL technical paper, arXiv:1710.02176

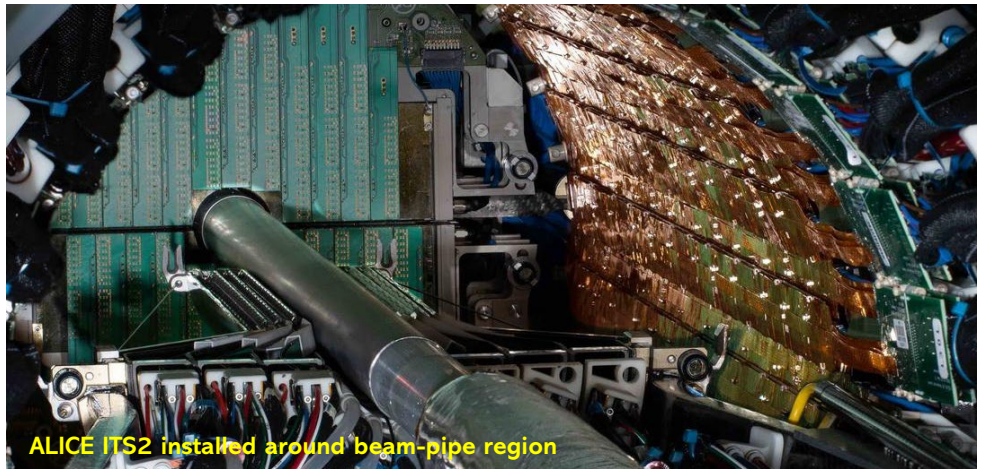
Next Gen MAPS: Collection by Drift/Diffusion

MIMOSA / Ultimate diffusion MAPS → **STAR PXL** large-system proof → **Remaining limits** diffusion + rolling shutter → **TowerJazz CIS** HR epi + deep P-well

STAR proved diffusion-based MAPS could deliver a low-mass, high-granularity vertex detector; the next step was to move from diffusion collection toward engineered depletion and full-CMOS pixels.

Technology evolution and bridge

- ALPIDE: localized depletion + diffusion in HR epi; much better than early MAPS but not optimal.
- RAL spearheaded TowerJazz deep implant modification.
- Deep p-well made full-CMOS pixel logic possible; ≈40 mW/cm², ≈5 µm resolution, >99% efficiency.



ITS2 system scale

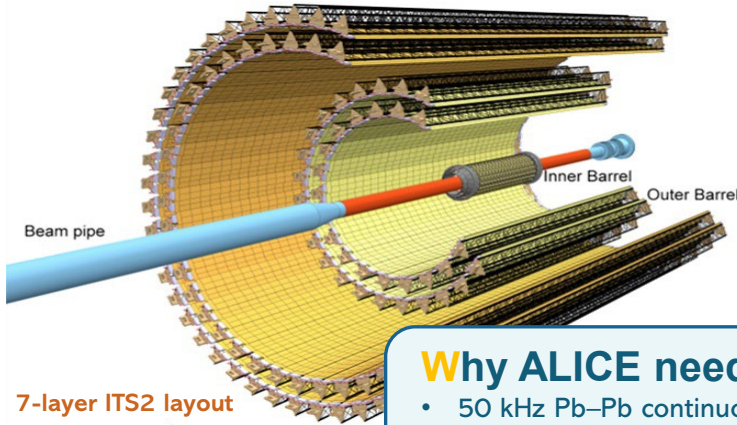
- 7 cylindrical layers
- 24,120 ALPIDE chips
- ≈12.5 billion pixels
- ≈10 m² active area
- radii ≈ 22–405 mm
- 50 – 100 µm thick sensors
- ≈ 0.35% X_0 inner layers
- Event time >2 µs

ALPIDE

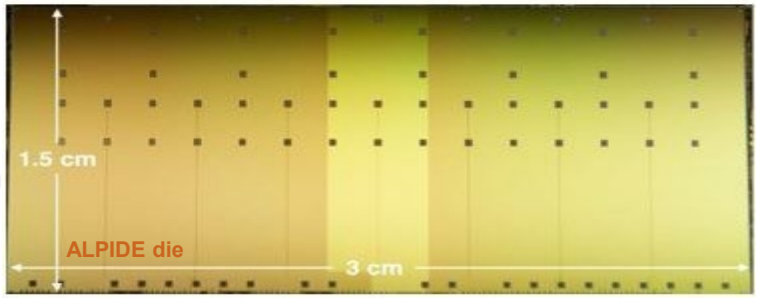
- 15 × 30 mm² chip
- 512 × 1,024 pixels
- 29.24 × 26.88 µm² pitch
- TowerJazz 180 nm CIS
- HR p-epi, deep p-well
- In-pixel amplification + discriminator
- Hit-driven sparse readout

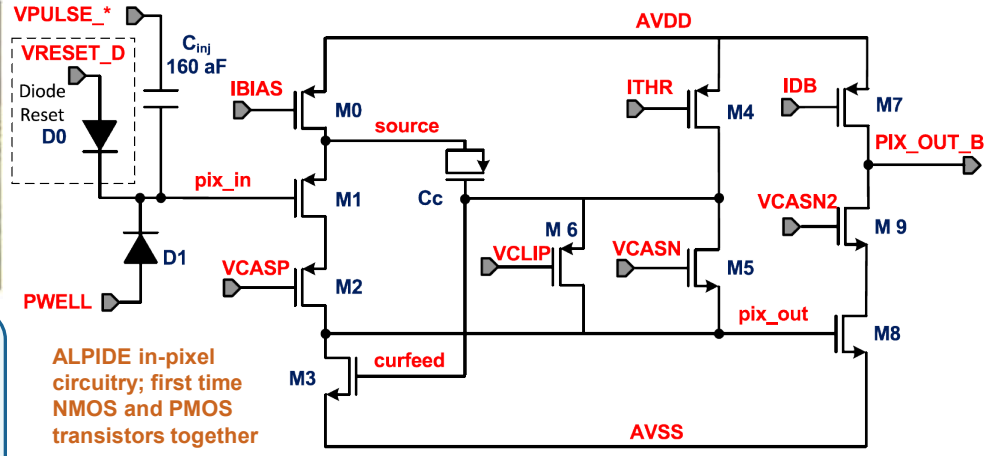
What ALPIDE demo'ed

- MAPS → mainstream collider VXD technology
- NMOS/CMOS inside every pixel without n-well charge loss
- Continuous, sparse data-driven readout at low power
- LHC-compatible efficiency, fake-rate + radiation tolerance



7-layer ITS2 layout





ALPIDE in-pixel circuitry; first time NMOS and PMOS transistors together

Why ALICE needed ALPIDE

- 50 kHz Pb–Pb continuous readout for Run 3/4 heavy-ion physics
- Improve impact-parameter resolution by ×3–5 and extend tracking to very low pT
- Reduce material budget and enable a 10 m², all-pixel silicon tracker

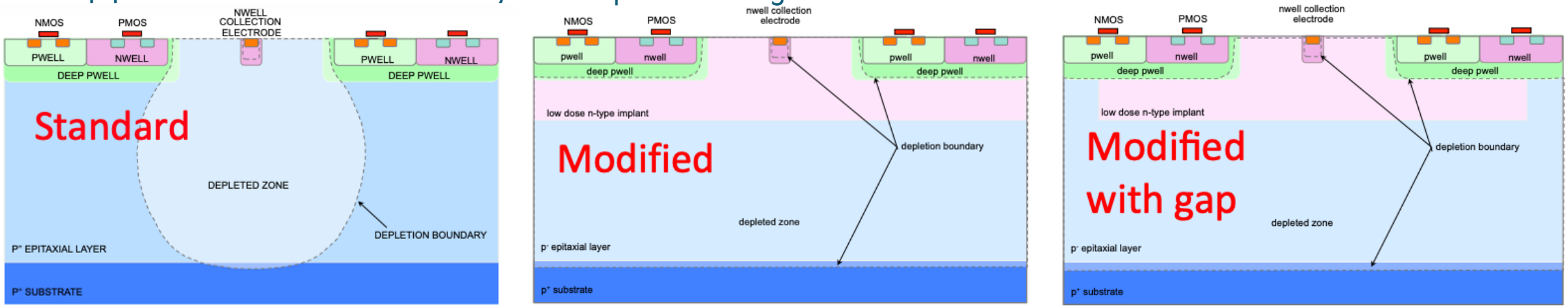
Brookhaven National Laboratory

ALICE ITS Upgrade TDR CERN-LHCC-2013-024; ALICE ITS pages and EP News "Pixels for quarks" (2019); Mager, NIM A 824 (2016) 434; Aglieri Rinella, NIM A 845 (2017) 583; Deptuch et al., NIM A 511 (2003) 240.

Next Gen MAPS: Collection by Drift

Key idea:

- Reverse-biased, high-resistivity p-type epitaxial layer forms sensitive volume.
- Low-dose deep n-type implant extends depletion beneath pixel circuitry and guides electrons to small n-well collection electrode;
- Deep p-well enables full CMOS circuitry without parasitic charge collection



ALPIDE standard process: partially depleted, mixed: diffusion and drift

180 nm → 65 nm

modified Tower process: substantially or fully depleted, predominantly drift-assisted collection

TPSCo 65 nm ISC CMOS (effectively 110 nm),

- ~10 µm epi layer, 7 metals, 300 mm wafers
- provides reticles stitching
- difficult design due to low $^{g_m}/_{g_{ds}}$

Comparison of radiation hardness

diffusion MAPS	Tower 180 nm MAPS	Tower 65 nm MAPS
TID ≈ 150 krad	TID ≈ 2.7 Mrad	TID > 10Mrad
NIEL ≈ 10^{13} neq/cm²	NIEL ≈ 1.7×10^{13} neq/cm²	NIEL ≈ 10^{14}–10^{15} neq/cm²

Brookhaven National Laboratory

Snoeys et al., NIM A 871 (2017) 90; G. Aglieri Rinella et al. NIM A 1056 (2023) 168589

MAPS: Drift-Assisted Charge Collection

Strengths:

- **Monolithic integration:** sensor, analog front end, discriminator and digital logic share the same silicon substrate, no bump bonding or separate sensor wafer → low material budget
- **Fine pitch and low material:** typically $10–30\ \mu\mathrm{m}$, retains principal mechanical and spatial-resolution benefits of early MAPS.
- **Low input capacitance:** depleted collection diode → capacitance of only a few femtofarads provides high charge-to-voltage gain, low noise and low analog power.
- **High-resistivity epitaxial layer:** reverse substrate bias enlarges depleted sensitive volume.
- **Drift-assisted charge collection:** vertical and lateral electric fields reduce collection time and suppress long diffusion tails.
- **Deep p-well isolation:** PMOS n-wells are shielded from sensitive epitaxial layer, permitting full CMOS circuitry inside each pixel.
- **In-pixel amplification and discrimination:** enables data-driven sparse readout rather than frame-by-frame raster scanning.
- **Process compatibility:** depletion-enhancing implant can be added with little or no change to pixel circuitry and layout.

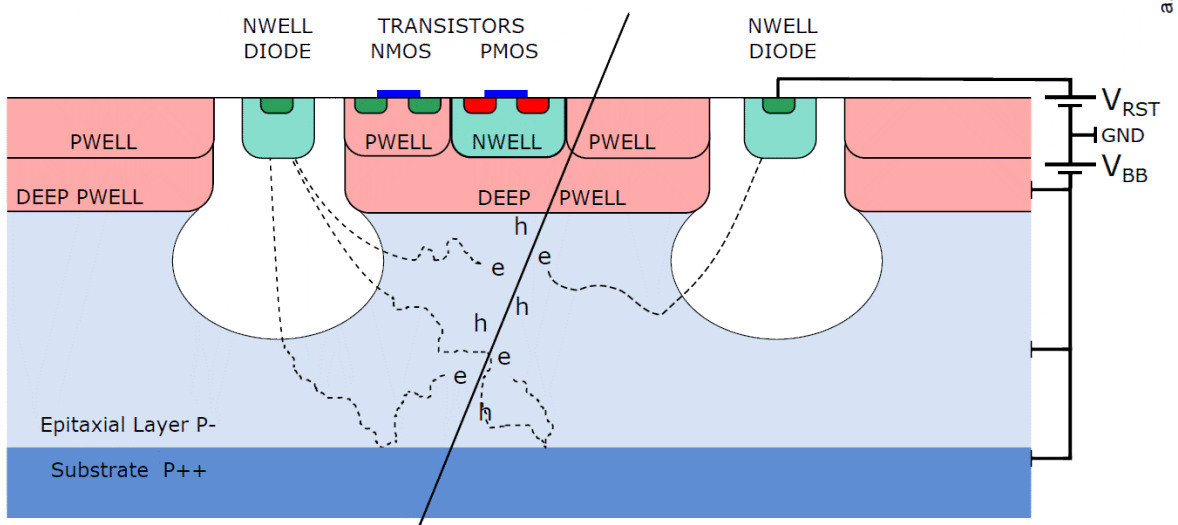
Main issues:

- **Weak lateral field at pixel boundaries:** minimum of electric field near pixel corners → uneven charge collection.
- **Charge sharing versus timing:** existing trade off between having lateral fields (n-implant gaps) and reducing charge sharing
- **Small signal charge:** thin epitaxial layers generate only a few thousand electrons for a minimum-ionizing particle.
- **Low-voltage operation:** limited voltage headroom complicates low-noise analog front-end design.
- **Sensor–electronics coupling:** digital switching activity must be isolated.
- **Bias and implant optimization:** collection speed, breakdown voltage, capacitance and charge sharing depend strongly on electrode size, well spacing, backside bias and implant geometry.
- **Residual diffusion:** without additional depletion implant, carriers generated far from collection diode still rely on diffusion.
- **Geometry dependent radiation response:** trapping near low-field pixel corners..

Brookhaven National Laboratory

MAPS: Drift-Assisted Charge Collection

Drift-Domination reduces collection time to 20-30 ns



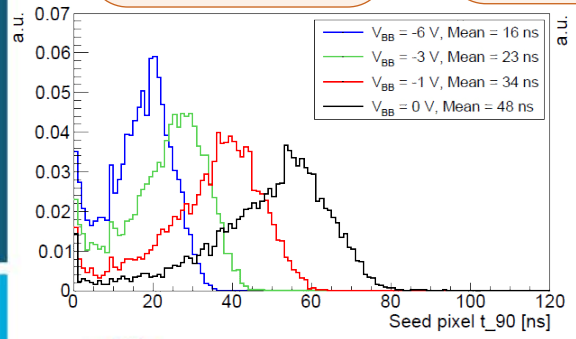
TCAD
doping, field, depletion, lifetime

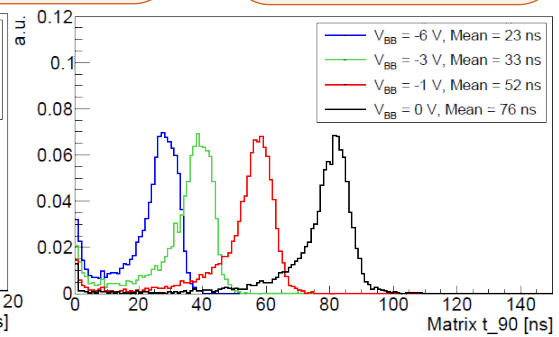
→

Transport MC
Garfield++ / Allpix² / custom MC

→

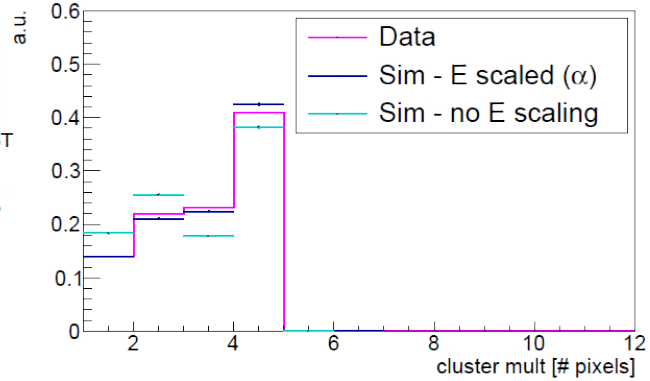
Response
charge maps, ^{55}Fe spectra, cluster size

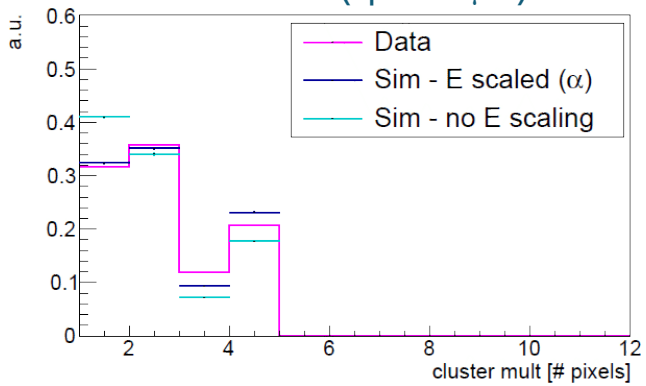




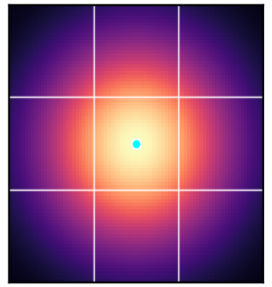
^{55}Fe event simulated for varied VBB (epi=18 μm)

Cluster sized for simulated ^{55}Fe events VBB =0V and -6 V (epi=18 μm)

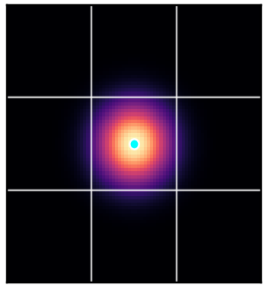




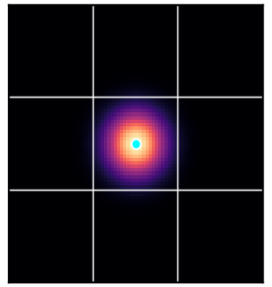
Diffusion MAPS
broad cluster

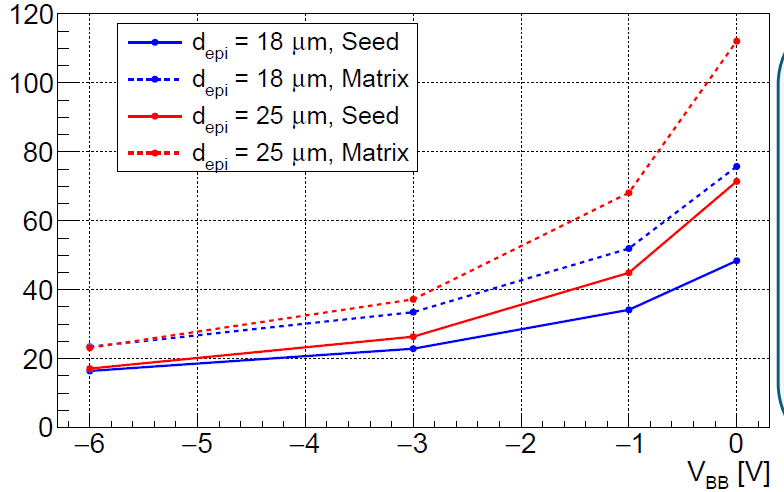


Tower 180 nm
compact drift focus



TPSCo 65 nm
sharing tuned by implants





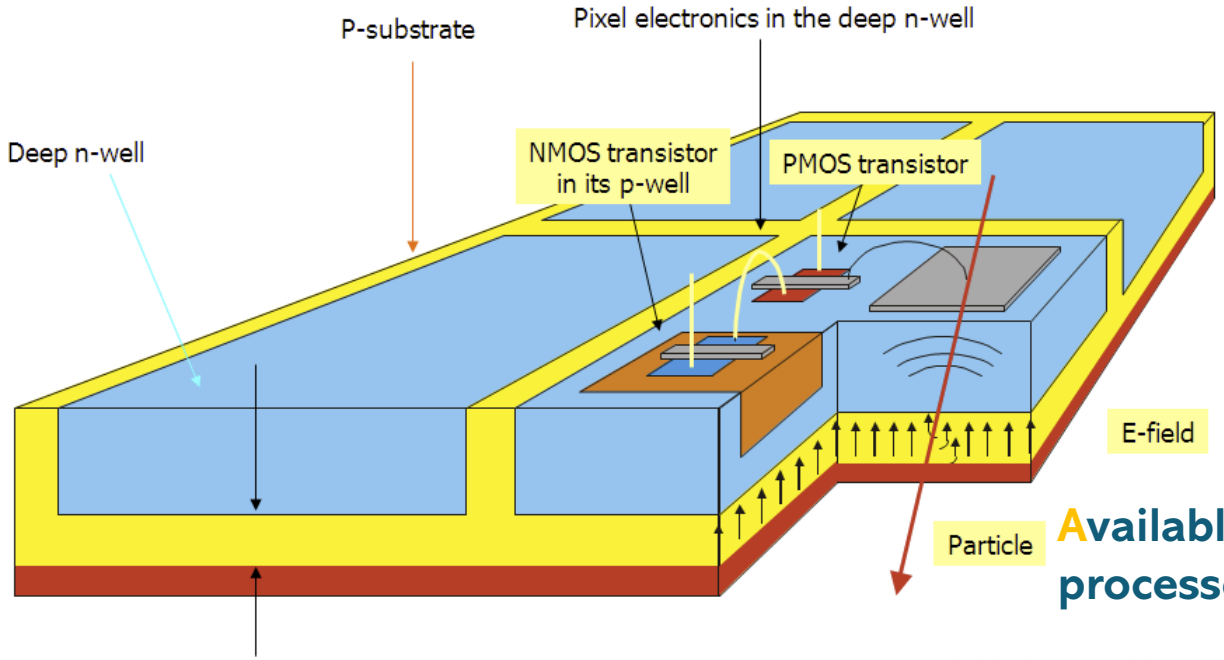
Main visual contrast

- Diffusion MAPS: broad cluster + long collection tail (>100 ns scale).
- Field shaping in Tower/TPSCo: collection drift-assisted, faster and more compact.

Brookhaven National Laboratory

Snoeys et al., NIM A 871 (2017) 90-96; Šuljić, CERN-THESIS-2017-304; Šuljić et al., NIM A 950 (2020) 162882; Sanna, CERN-THESIS-2024-359; Sanna et al., JINST 20 (2025) C06032

Depleted MAPS (DMAPS) called HV MAPS 1

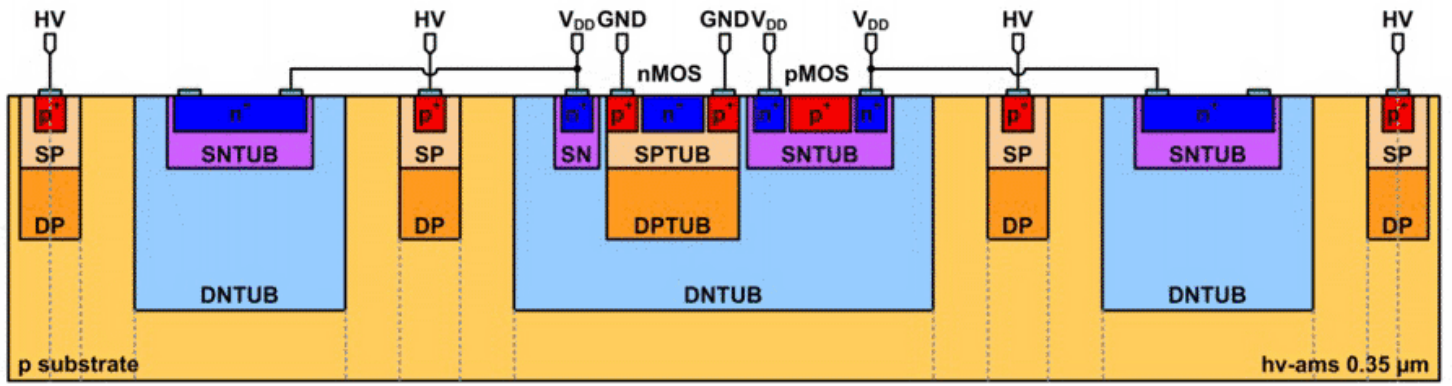


Needed Ingredients:

- "High" Voltage add-ons (present in automotive, BCD process options) to be able to to apply 50 – 200 V bias.
- "High" Resistivity substrate wafers (>100 Ωcm – kΩ cm)
- Combination of multiple deep and shallower nested wells (for shielding and relaxing electric fields) and full CMOS
- Backside Processing: thinning addition of back bias contact

Available processes:

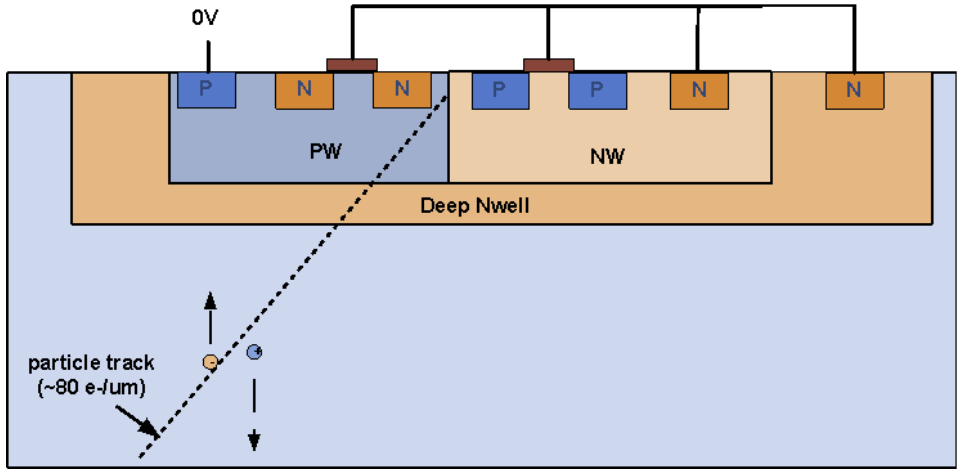
- L_{min} typically >110nm
- Typically smaller and carrying "specialized" processes foundries: AMS, LFoundry, XFAB



Brookhaven National Laboratory

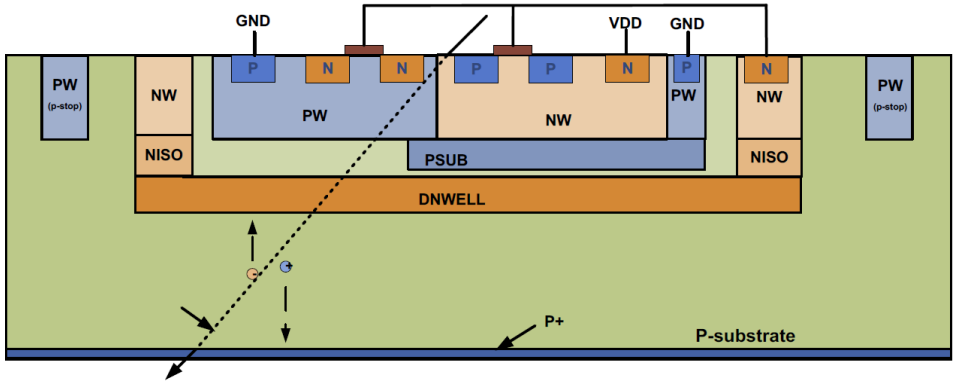
I. Peric, NIM A582 (2007) 876-885, I. Mandic et al., JINST 12 (2017) no. 02 P02021,

Depleted MAPS (DMAPS) called HV MAPS 2



AMS (HV350/180)

- Substrate: up to 2k Ohm-cm
- Bias: > 60 – 100 V
- Gate Length: 350 nm / 180 nm
- Metal Stack: 3-6 metal layers
- No PMOS isolation



Lfoundry (LFA150)

- Substrate: > 2 kΩ·cm
- Bias: Voltages up to 280 V
- Gate Length: 150 n,
- Metal Stack: Up to 7 metal layers
- Quadruple well (deep n-well and deep p-well), PMOS isolation
- Backside processing

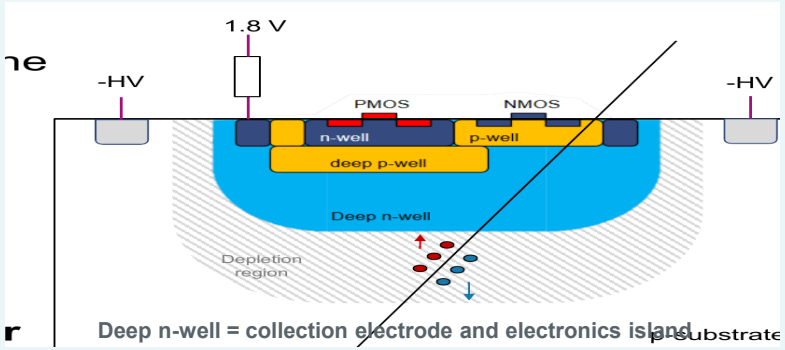
Brookhaven National Laboratory

I. Peric et al. Nucl. Instrum. Meth. A582 (2007) 876-885, I. Peric et al. Nucl. Instrum. Meth. A765 (2014) 172-176,

HV-MAPS/Large-Electrode DMAPS: Landscape

Large deep-n-well collection electrodes embed CMOS electronics in sensing node: fast drift collection, HV operation and scalable

Large-electrode HV-CMOS principle



- HR p substrate + reverse HV bias create depleted sensitive volume.
- Electrons drift to the deep n-well; shallow wells inside DNW host NMOS/PMOS circuitry.
- Best for fast timing, radiation hardness and large-area systems; pays in capacitance / power / crosstalk.

large Cdet, higher front-end power, digital-to-sensor coupling

Applications: particle tracking, calorimetry, beam monitors and telescope systems
Common: HR substrate • 60–400 V bias • nested wells • guard rings / field plates • full in-pixel analog + digital hit logic

Example of foundry path

AMS HV350 / HV180

HV-MAPS concept; MuPix / ATLASPix roots; robust HV options.

TSI 180 nm HV-CMOS

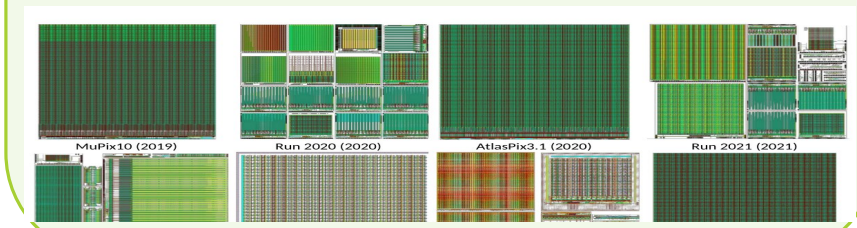
AstroPix v1–v4 / ATLASPix-derived designs; HV DNW; large-pixel spectroscopy.

2025–2026 migration

TSI/Bosch support ceased → AstroPix and MightyPix paths consider AMS and LFoundry options.

Representative implementations

MuPix / Mu3e	AstroPix	MightyPix
50 µm thin sensors ≈1.1 m² system production accomplished	TSI 180 nm 500×500 µm² pixels space/EIC BIC, 500 µm depletion goal	LHCb Mighty Tracker 30 MHz/cm² 99% in 25 ns 6×10^{14} n_eq/cm^2



Capability envelope

What improves full depletion, ns-scale drift, high rate, rad-hardness

What costs large C_D, higher front-end power, digital-to-sensor coupling

Where used Mu3e, LHCb Mighty Tracker, AMEGO-X / EIC BIC, beam monitors

Large-electrode counterpart to small-electrode depleted MAPS such as ARCADIA.

Updated status message

- Platform spanning ultra-thin tracking, large-area calorimetry and high-rate monitors.
- Real Foundry risk: TSI enabled several prototypes, but future production needed migration to available HV-CMOS processes.
- Main design question today: how much electrode capacitance/power is acceptable for required timing, radiation and system area?

HV-MAPS/large-electrode DMAPS deliberately trade capacitance and power for fast drift collection, radiation tolerance and scalable monolithic detector systems.

Brookhaven National Laboratory

Perić, NIM A 582 (2007) 876; Perić et al., NIM A 765 (2014) 172; Bespin et al., NIM A 978 (2020) 164460; Striebig et al., JINST 19 (2024) C04010; Steinhebel et al., NIM A 1083 (2026) 171021;

ARCADIA: Fully Depleted Small-Electrode MAPS in LF 110

Process-centered view: backside depletion and low-voltage CMOS are combined in commercial imaging process.

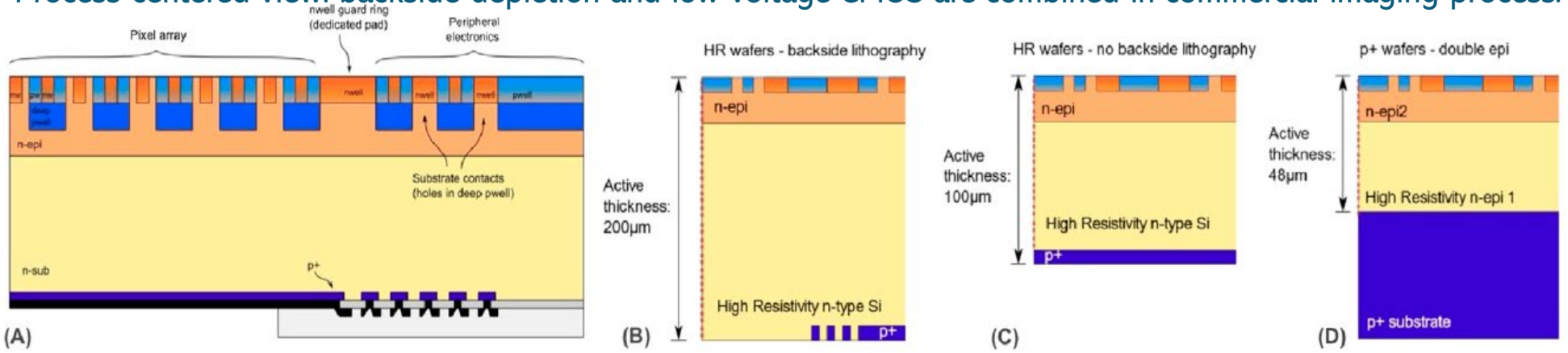


FIGURE 1
Detailed cross-section of the ARCADIA fully depleted CMOS sensor technology, depicting the arrangement of the pixel array and guard-ring terminations on the back-side **(A)**. Embodiments of the technology for thicker sensors with backside lithography **(B)**, for thinner sensors with maskless backside using a p^+ implantation **(C)**, and a maskless option **(C)** using a p^+ starting substrate as a passive carrier **(D)**.

LF11IS / LF 110 nm CIS
LFoundry 110 nm CMOS imaging.
Six metal layers;
1.2 V core CMOS.
Deep p-well isolates NMOS/PMOS.
Back thinning + B implant + laser anneal.
Final active thickness demonstrated/planned from ≈100 to 500 µm.

ARCADIA process cross-section: CMOS on top, backside junction and substrate bias underneath

Key process idea:
- n-type high-resistivity substrate is sensitive volume; fully depleted active volume.
- p+ backside implant, backside contact + guard rings → high negative backside bias.
- Full depletion grows from the backside toward the front-side CMOS.
- Collection electrode remains at low voltage → safe for standard thin-oxide CMOS.

Different from large-electrode HV-CMOS
Electronics are not placed inside a large collecting deep n-well.
Capacitance target is small-electrode-like, not O(100 fF).

Different from ALPIDE
Sensitive volume is designed to be fully depleted.
Charge transport is intended to be drift-dominated through thick silicon.

ARCADIA occupies small-electrode fully depleted corner of the MAPS landscape: low capacitance and low power are pursued together with thick depleted silicon and fast drift collection

Brookhaven National Laboratory

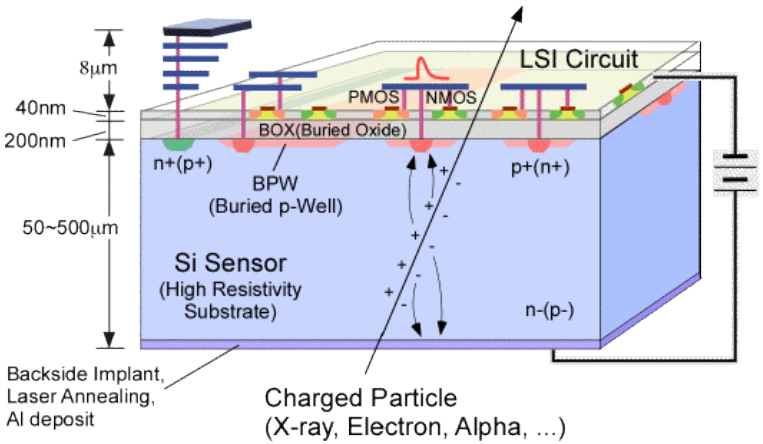
Da Rocha Rolo et al., Front. Sens. 6 (2025) 1603755; Pancheri et al., IEEE TED 67 (2020) 2393; ARCADIA process / MD demonstrator papers

Special Branch: MAPS in SOI Processes

Distinct branch of MAPS: CMOS electronics are fabricated in SOI device layer above buried oxide (BOX), while high-resistivity handle wafer forms depleted radiation sensor.

1) FD-SOI MAPS / SOIPIX

KEK SOIPIX • LAPIS 0.20 µm low-leakage FD-SOI pixel process



Key idea thin 40 nm FD transistor layer is electrically isolated from thick, fully depleted sensor wafer

Strengths low collection capacitance • large S/N • complex in-pixel CMOS • backside processing and thinning

Main issues back-gate effect, BOX trapped charge/TID, circuit–sensor cross-talk

Mitigations Buried BPW/BNW, nested wells, Double-SOI shield, optimized backside treatment, FZ high-ρ wafers …

Brookhaven National Laboratory

Sources: Y. Arai, SOIPIX Status & Perspectives, CEPC 2018; M. Okihara et al., Lapis SOI Pixel Process, SOIPIX2015/arXiv:1511.05224;

Common SOI detector principle

CMOS readout tier
thin SOI device layer
BOX
depleted high-ρ sensor / handle wafer

vias + implanted collection nodes connect sensor to pixels

First MAPS were proposed in SOI processes

Historical Timeline:

- 1980 – SOI CMOS technology matures (IBM, Honeywell, MIT-LL, etc.)
- 1990 – First discussions on monolithic SOI radiation detectors as an alternative to hybrid pixels
- 1990 – demonstration
- 2003-2005 – SOIPIX Collaboration OKI 0.20 µm FD-SOI and first practical SOI monolithic pixel detector

FD-SOI:
optimized detector wafer + thin FD logic

PD-SOI/HV-SOI:
thicker active layer + isolation wells

Conceptually attractive for radiation hardness and HV operation, but largely superseded by the broader adoption of bulk CMOS MAPS.

2) PD-SOI / thick-film HV-SOI

CMOS + HV devices
thick active Si: wells / isolation islands
BOX
handle wafer as depleted sensor

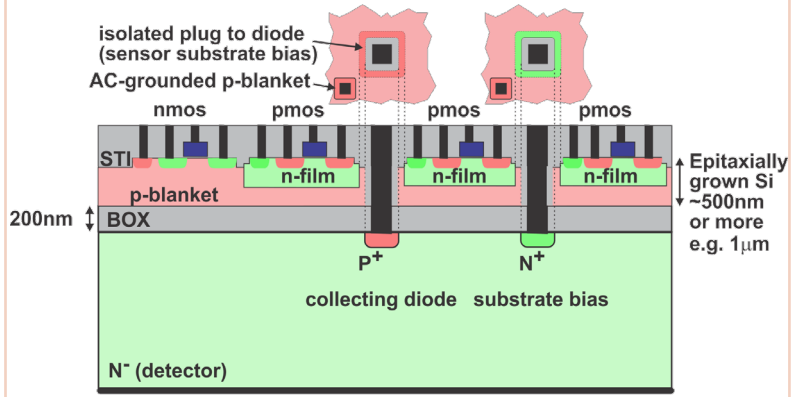
biased wells shield CMOS from BOX/sensor potential

Key idea use of partially depleted / thick active silicon and deep wells to isolate electronics from BOX charge and sensor bias

Strengths no back-gate sensitivity • thick active silicon • fast drift collection • high-voltage operation

Main issues scarce detector-suitable PD/HV-SOI processes + difficult customization of BOX contacts and deep buried wells, especially deep n-type implants.

Mitigations dedicated funding + collaboration with foundry for detector-process customization.



Deptuch, Patents US 9,437,771 B1 and US 9,923,017 B2

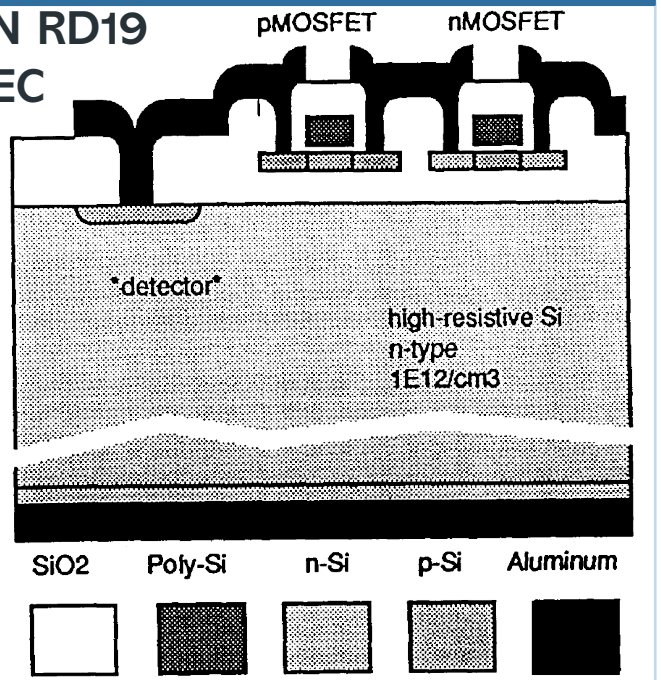
Evolution of MAPS in SOI Processes

From first CERN RD19 concept to modern FD-SOI with implanted multi-layer shieldings and HV-/PD-SOI implementations.

1) OLD TIMES

CERN RD19 / IMEC

1991–1993



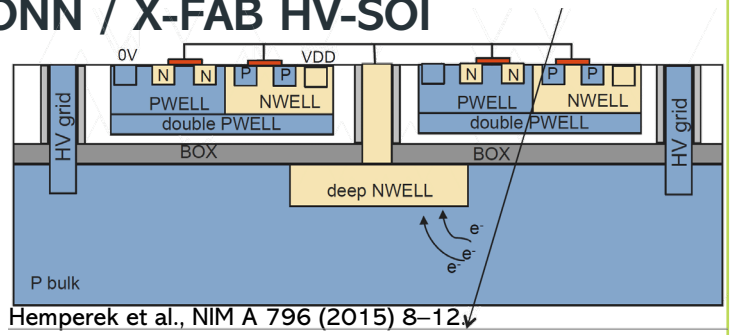
Architecture: HR handle wafer = depleted PIN sensor.
Processes: SIMOX and laser/strip-heater ZMR; IMEC SOI CMOS on HR n-type silicon.
Demonstrated: working CMOS circuits, sensor diodes + detector/amplifier arrays; $I_{LEAK} \approx 5–20$ nA/cm² @ 100 V.
Motivation: Monolithic detector–electronics integration, full CMOS, 100% FF, low parasitics and fine pixel pitch.
Main issues: back-gate + circuit–sensor cross-talk, SOI-MOSFET kink, process-induced sensor degradation.
Significance: first demo of monolithic SOI integration of CMOS electronics with depleted HR sensor.

Dierickx et al., CERN RD19, IEEE TNS 40 (1993) 753.

2) MIDDLE AGES

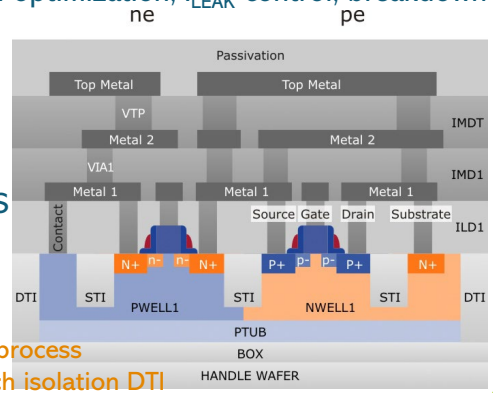
BONN / X-FAB HV-SOI

2013-2016



Hemperek et al., NIM A 796 (2015) 8–12

Architecture: 180 nm thick-film HV-SOI with multi-well shielding between the BOX and CMOS electronics; XTB01/02: 25/50/100 µm pixels; small deep-n-well collection electrode; 3T analog readout.
Processes: XFAB XT180 modified.
Demonstrated: >200 V bias, ≈40–50 µm depleted depth, $C_D \approx 15$ fF, ≈30 e⁻ ENC; charge collection retained after irradiation up to 5×10^{14} n_eq/cm^2; after p-stop/p-field structures added I_{LEAK} reduced by ≈10× and $V_{BD} > 300$ V.
Motivation: full CMOS, 100% fill factor, no hybridization, low parasitics and narrow pixel pitch.
Main issues: HV field optimization, I_{LEAK} control, breakdown margin and radiation -induced charge collection.
Significance: commercial HV-SOI revived the SOI-MAPS concept for fast, radiation-tolerant depleted sensors.

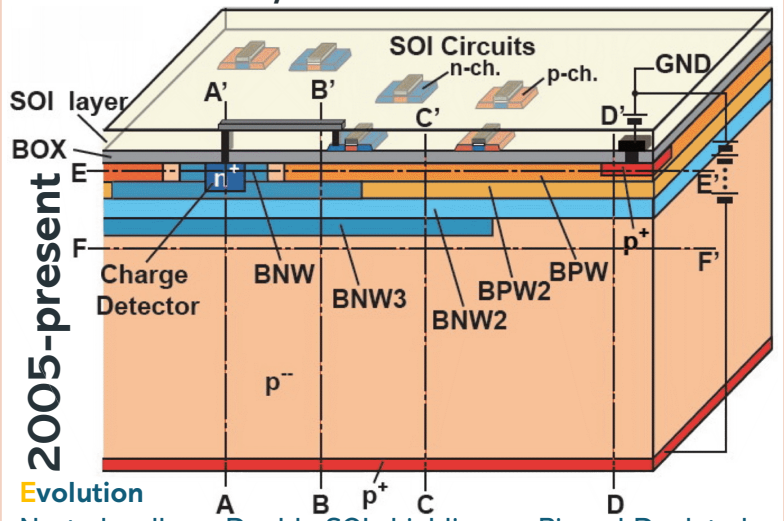


x-section of XT018 process featuring deep trench isolation DTI

3) MODERN TIMES

KEK SOIPIX / LAPIS

2005-present

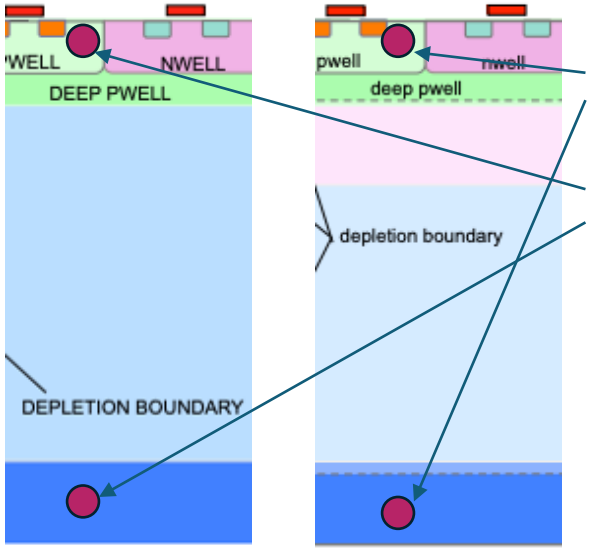


Evolution Nested wells → Double-SOI shielding → Pinned Depleted Diode (PDD) → Multiple buried wells (3×BNW + 2×BPW) BPW1 - interface pinning; BPW2 - field shaping; BNW1 - buried channel; BNW2 - lateral drift; BNW3 - electrostatic shielding; n^+ - low-capacitance sensing node
Architecture: FD-SOI CMOS above fully depleted sensor with 3 BNWs, 2 BPWs and small n^+ sensing node..
Processes: Lapis 1P5M, 40 nm Si, 200 nm BOX, HR wafer.
Demonstrated: ✓ fully depleted thick sensor, ✓ engineered 3-D potential, ✓ charge from entire sensor volume, ✓ very small $C_D \approx 3.2$ fF, ✓ reduced crosstalk and I_{LEAK}=56 pA/cm² @-35°C, ✓ ENC ≈11 e⁻ rms, ✓ 200 eV FWHM @ 5.9 keV.
Motivation: low-noise spectroscopy with strong CMOS shielding and efficient drift collection.
Main issues: precise optimization of wells profiles and bias.
Significance: buried implants become a primary tool for 3-D sensor electrostatic design.

Kamehama et al., Sensors 18, 27 (2018); Arai, KEK SOI Meeting 2026

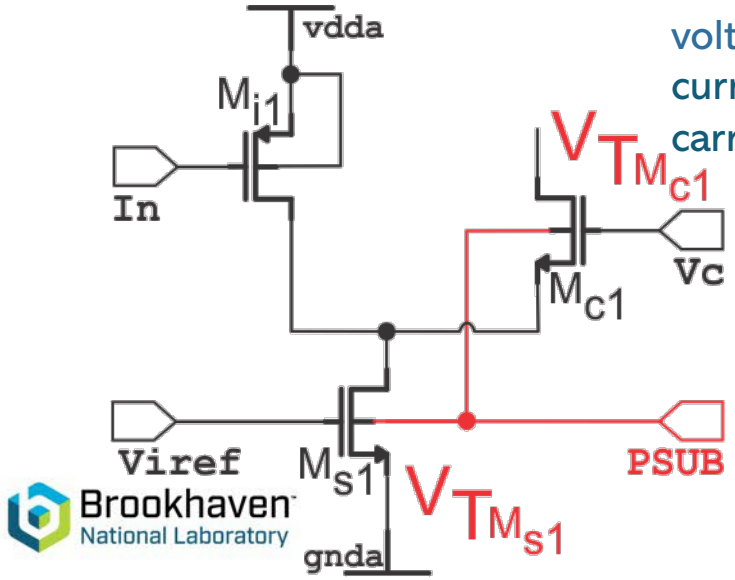
Bulk MAPS v.s. SOI MAPS

Bulk MAPS



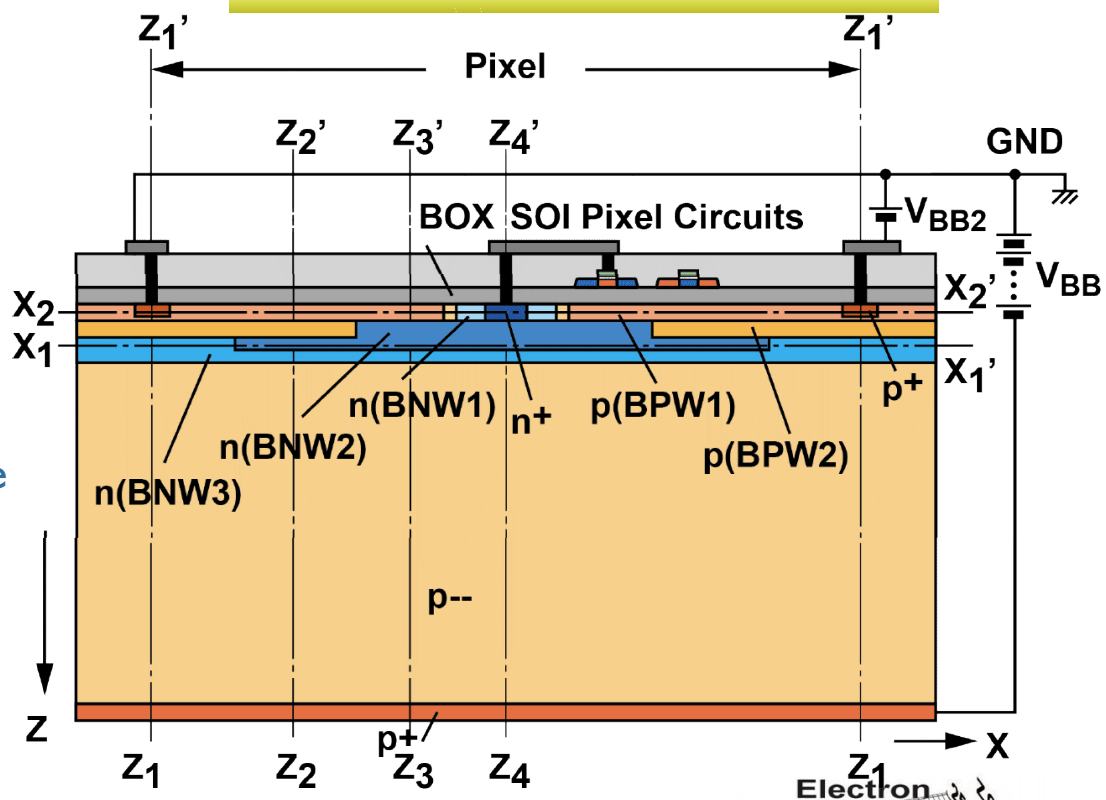
Trade-off of biasing

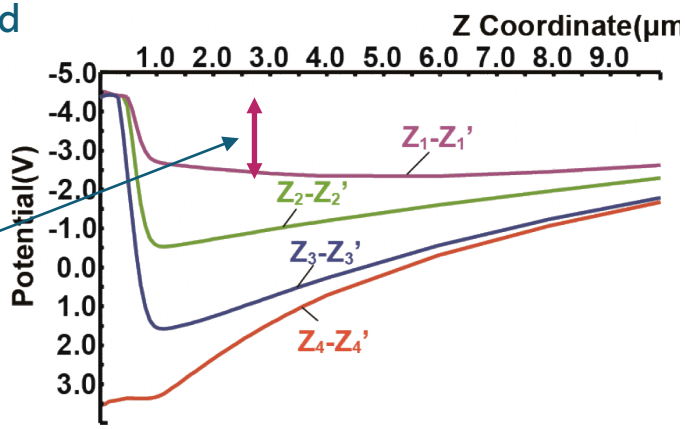
- P-well - back-side need to be biased "negatively" in cases A or B, (independent of presence or not of blanket n_implants).
- P-well and back-side both large negative → significant threshold shift of NMOS transistors, but low substrate current of majority carriers
- Too small p-well negative voltage → increased substarte current of majority injected carriers

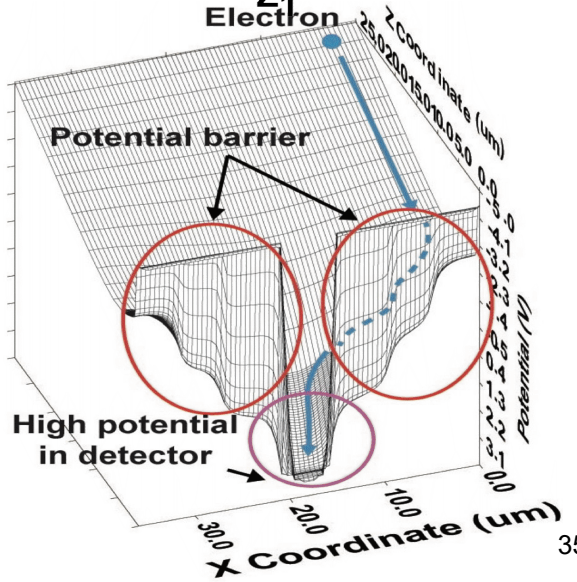


High barrier created and thick BOX reduces VTH shifts

PDD SOI MAPS







Advancement in Simulation and MAPS in EIC

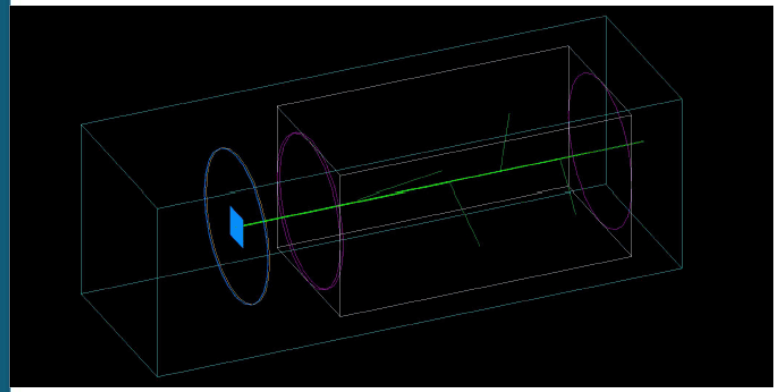
Brookhaven National Laboratory

Comprehensive Simulations

Particles interaction with silicon

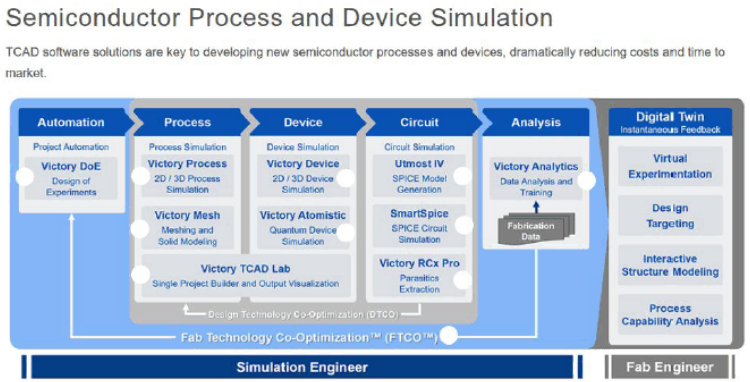
GEANT4 A SIMULATION TOOLKIT

40 um inactive + 10 um active Si with 20x20 um^2 pixels



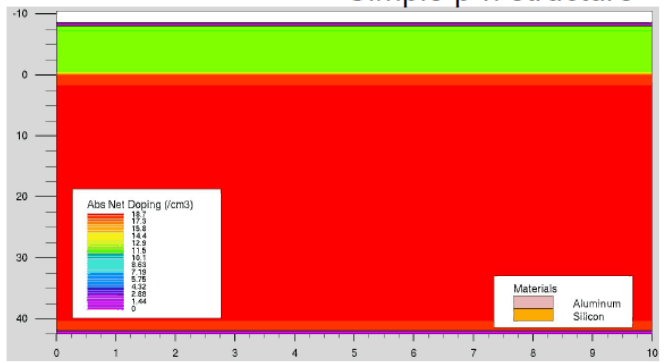
10 E_γ @ 80 keV

Sensor Doping profile and E-field



comprehensive suite of **Technology Computer-Aided Design (TCAD)** software tools to model semiconductor fabrication processes and device behaviors

Simple p-n structure



Transport model + Detector Response

ap^2 allpix squared

Geometry Definition
Layout, materials

GEANT4 Wrapper
position + E_{dep}

Charge Transport
Drift, diffuse…

Signal Formation
Charge→electrical signal

Digitization
Thr. Noise, Elec response

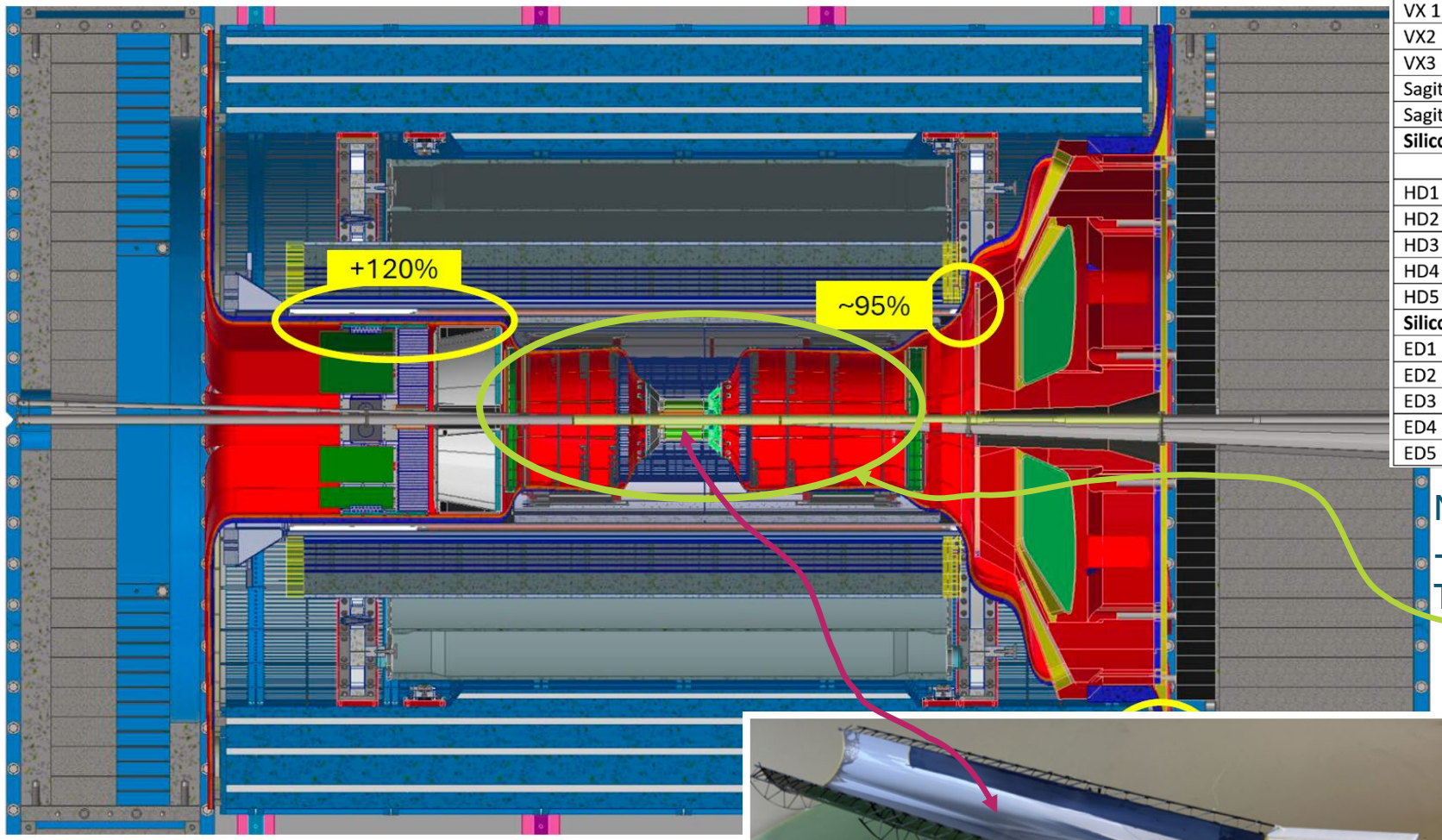
Output
w. ROOT

Generic simulation framework for semiconductor tracker and vertex detector which combines particle transport and detailed detector response simulation

Brookhaven National Laboratory

MAPS in EIC

Routing for data handling + services is problematic in highly granular detector system

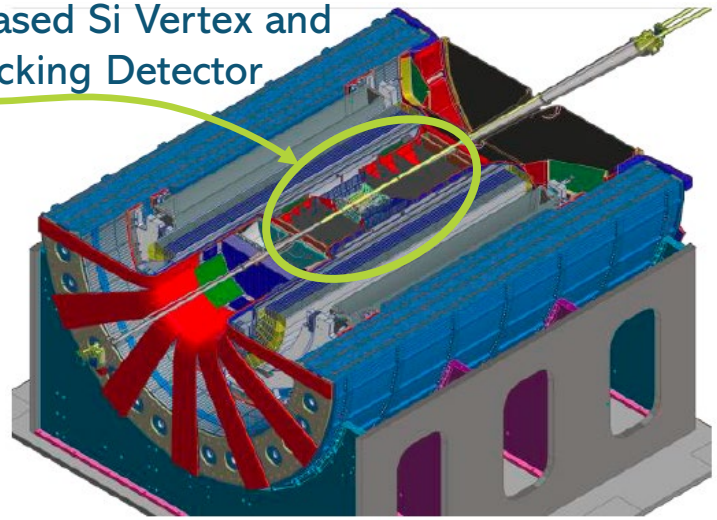


Electron-Ion collider ePIC Detector

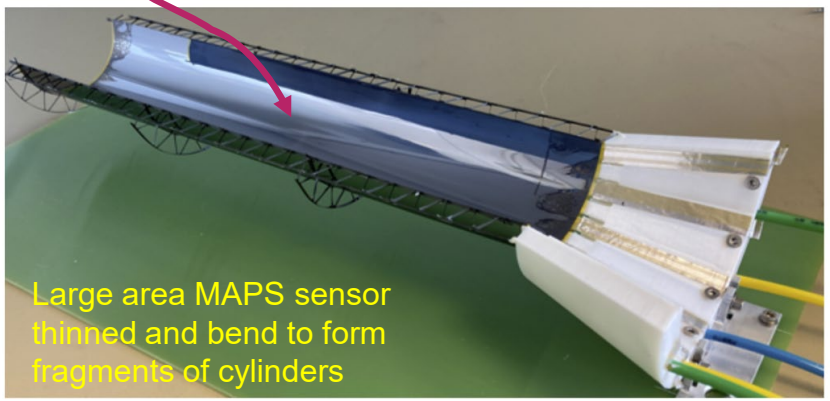
ePIC SVT detector layout configuration
(in total > 20B pixels, on ~ 10 m^2 of Si)

Silicon Barrel Layers			
	Radius [mm] (min, max)	Length [mm]	X/X0 [%]
VX 1 (L0)	36	270	0.05
VX2 (L1) IB	48	270	0.05
VX3 (L2)	120	270	0.05
Sagitta1 (L3)	270	540	0.25
Sagitta2 (L4) OB	420	840	0.55
Silicon Hadron Endcap (wheels)			
	Distance [cm]	Radius [mm] (min, max)	X/X0 [%]
HD1	25	(36.76, 230)	0.24
HD2 H-End	45	(36.76, 430)	0.24
HD3 Cap	70	(38.42, 430)	0.24
HD4 Disks	100	(54.43, 430)	0.24
HD5	135	(70.14, 430)	0.24
Silicon Electron Endcap (wheels)			
ED1	-25	(36.76, 230)	0.24
ED2 E-End	-45	(36.76, 430)	0.24
ED3 Cap	-65	(36.76, 430)	0.24
ED4 Disks	-90	(40.0614, 430)	0.24
ED5	-115	(46.3529, 430)	0.24

Monolithic Active Pixel Sensors (MAPS) - based Si Vertex and Tracking Detector



courtesy of Roland Wimmer



Brookhaven National Laboratory

G. Feofilov et al.,
ITS3 WP4 10 October 2023.

Conclusions: Design Space, Not Single Detector

The historical trend is from passive charge diffusion to engineered electrostatics, sparse readout, and system-level optimization.

main idea - evolution

Diffusion MAPS
MIMOSA → STAR

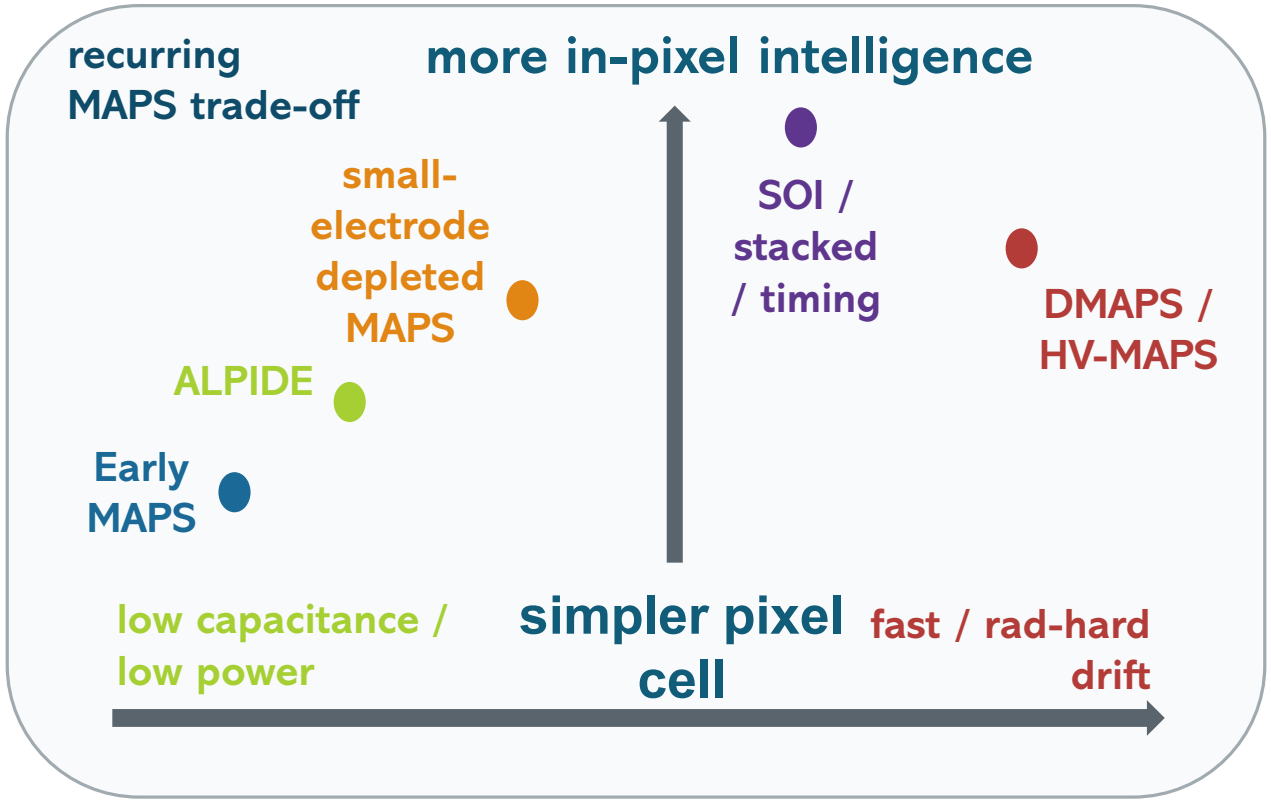
→ **ALPIDE / ITS2**
full CMOS + sparse RO

→ **Tower/TPSCo small electrode**
depletion + field shaping

→ **DMAPS / HV-MAPS**
large electrode, full drift

→ **SOI / PDD / 3D fields**
shielding + buried wells

→ **Future**
stacked + timing + intelligence



1 Physics first
Electric field transports charge; weighting field defines signal.
Drift, diffusion, trapping and capacitance decide usable pulse.

2 Electrostatics is the technology
Implants, wells, bias and geometry sculpt the potential landscape.
Modern MAPS are designed as 3-D electrostatic structures.

3 No universal best pixel
Small electrode: low C, low noise, low power.
Large electrode: fastest drift and strongest radiation tolerance.

4 The system chooses
Vertexing, timing, X-rays and trackers optimize different figures of merit.
Bandwidth, cooling, material and services are as important as pixels.

Brookhaven National Laboratory

Take-home message: MAPS progress comes from co-optimizing sensor volume, collection electrode, in-pixel electronics, readout architecture, mechanics, cooling and data movement.