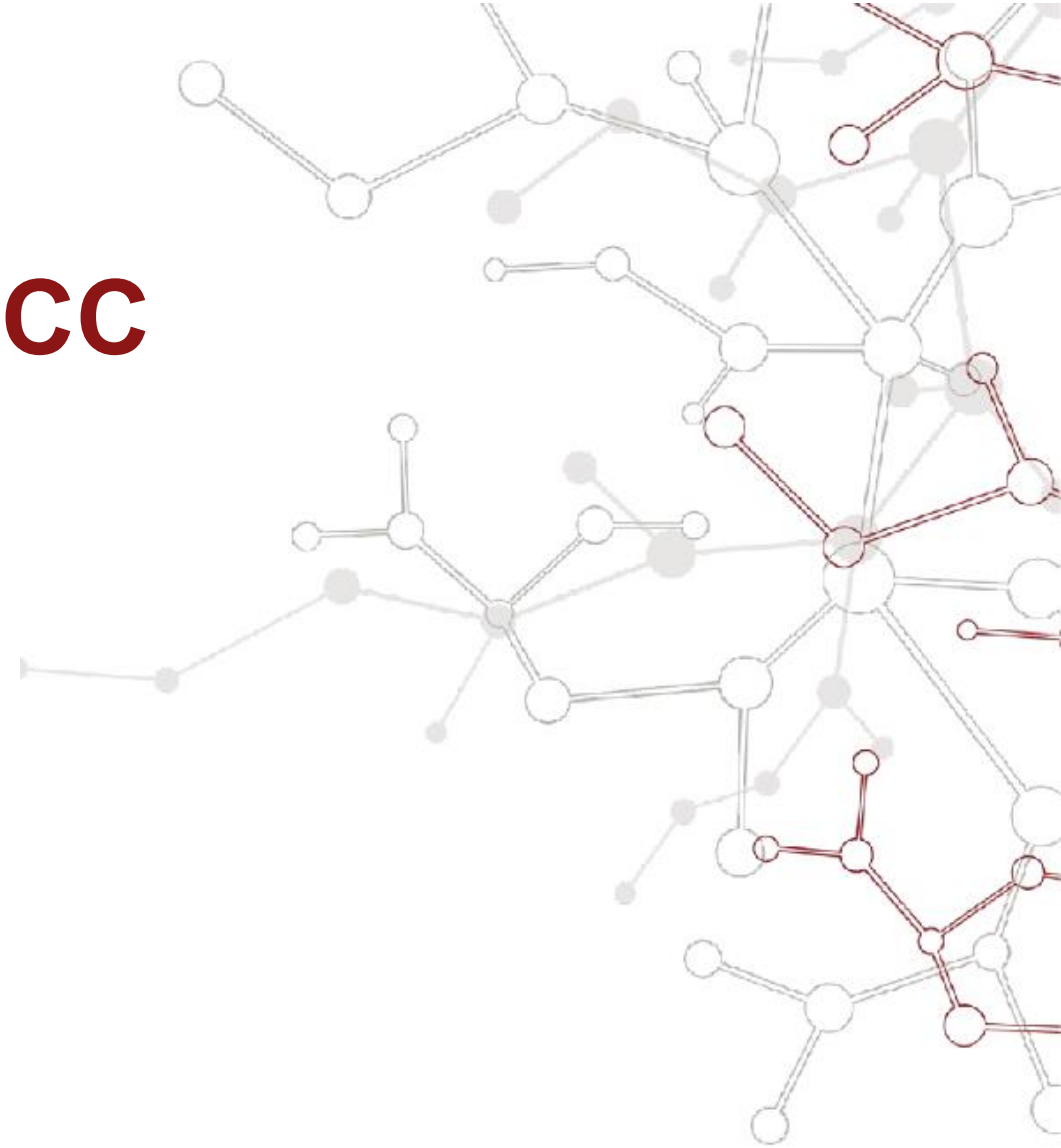
SLAC support for the US FCC effort



Caterina Vernieri for FPD/SLAC

09/10/2026

Physics of the Universe priority

FCC-ee is at the top of SLAC's list for the next major collider program

Near-term position

- Contribute to US HFCC, DRDs and the FCC study
- Focus R&D where SLAC already has distinctive capability

Technical focus

- Higgs physics and detector optimization
- Readout, AI/ML and ASIC design
- Vertex, calorimetry and fast timing

One FCC strategy, supported through several lab investments

Sizeable and sustained support from LDRD and other sources

2022–25

MAPS and NAPA

Timing-pixel and monolithic sensor capability for future vertex systems

FY26-27

eFPGA

Radiation-tolerant reconfigurable logic and on-detector ML

FY27–28 / ongoing

MDI + 5D + 4D

LDRD: vertex/MDI integration and SPAD readout

KA-29 + DOE Accelerate: LGAD timing layer

FY26-28

FACET & US-Japan

- Laser collimation for FCC-ee (FACET-II E344)
- FCC-ee injector emittance preservation (FACET-II E341)
- FCC-ee injector photocathode studies (E341, confirm)
- QD0 cryostat design with BNL
- SuperKEKB XRM for bunch-by-bunch beam sizes and nanobeam optimization

Together these investments connect detector R&D, MDI engineering and accelerator development

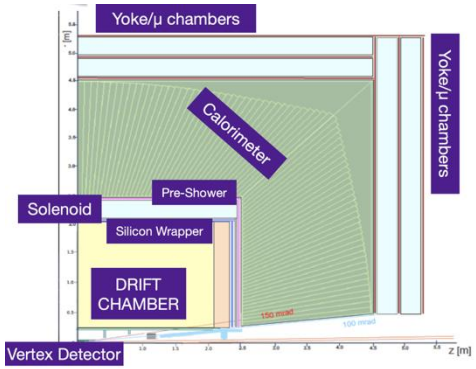
SLAC fast-timing expertise for FCC-ee

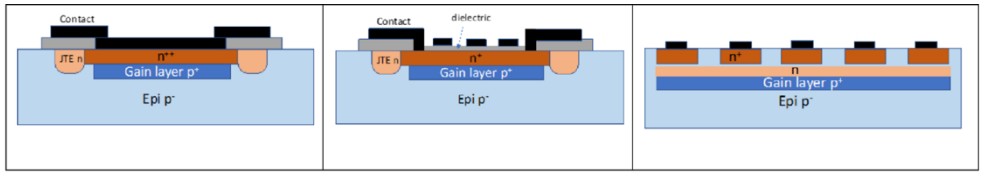
KA-29 and DOE Accelerate support an LGAD timing layer with 28 nm readout

Silicon-wrapper concepts

ALLEGRO

IDEA





DC, AC and deep-junction LGAD options

Physics role

- Improve momentum resolution with 10 μm hit precision
- Time-of-flight particle identification and long-lived-particle searches
- Provide the time reference for 5D calorimetry

Technology program

- 3D-integrated LGAD ASIC in 28 nm targeting 10 μm position and 10 ps timing
- Joint SLAC, Fermilab and LLNL effort
- Builds on ATLAS HGTD ALTIROC 20 ps TDC expertise

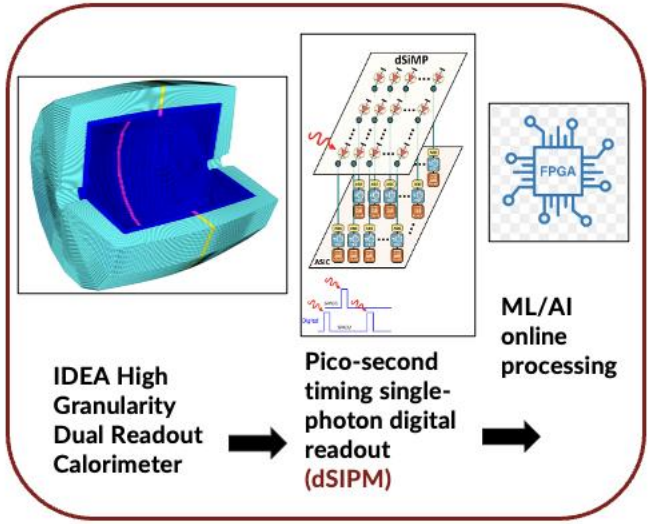
This layer links MAPS inner tracking to the 5D-calorimeter time reference

FLASH: Digital Photon Readout for 5D Calorimetry

Lead PI: Schwartzman

Main application: IDEA Fiber HCAL, in collaboration with Texas Tech University

- FLASH realizes 5D calorimetry through direct time-resolved Cherenkov detection: individual photons are detected and time stamped at the sensor front-end, replacing analog waveforms with sparse, time-tagged photon hits
- This architecture eliminates waveform digitization while enabling:
  - fine spatial granularity at the O(10 μm) scale
  - timing precision at the O(50 ps) level
  - reduced data volume and power consumption
  - scalable low-power implementation for future calorimeters
  - opens the path toward edge-level real-time processing and pattern recognition at the level of individual photons

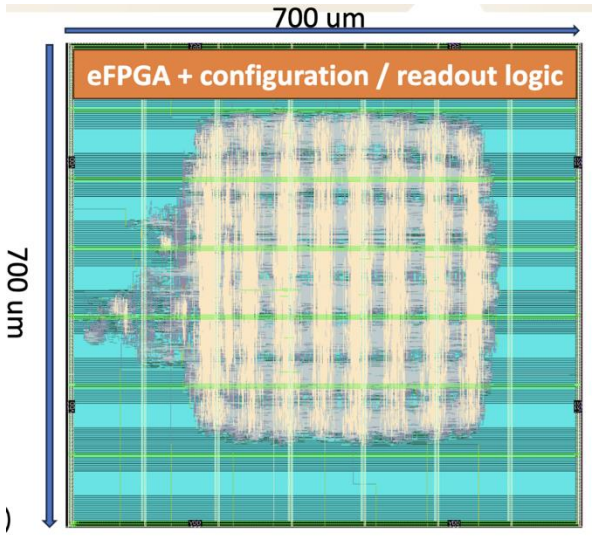


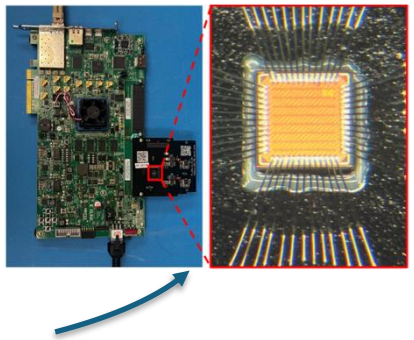
- **LDRD 2027-2028 to design and fabricate 3D-stacked SPAD - TDC and readout electronics**
- **Integration to HG-DREAM and beam tests**

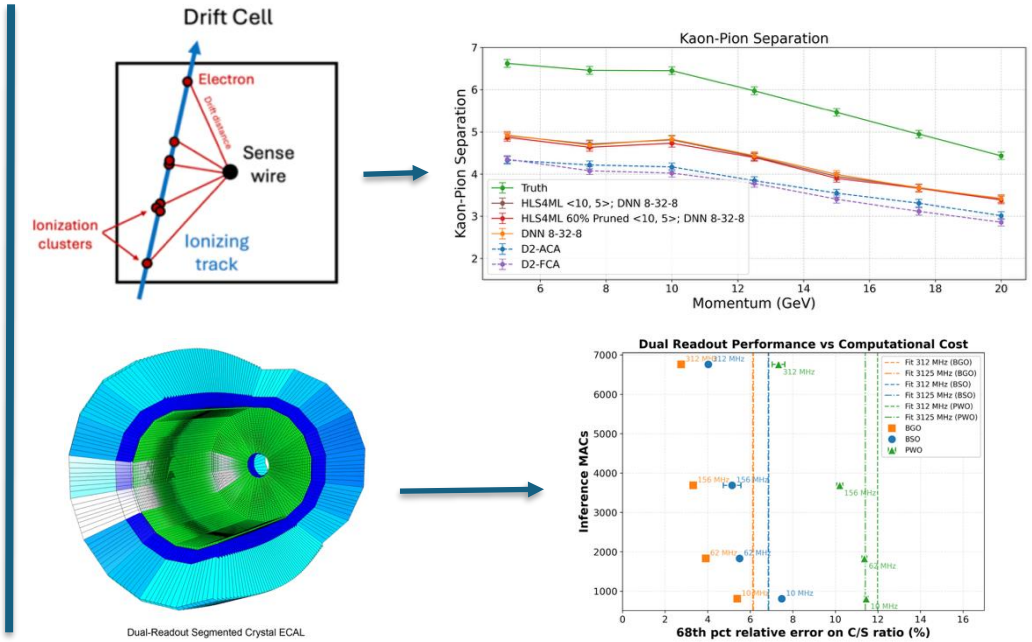
eFPGA-based Machine Learning for on-detector data processing

Lead PI: Ruckman/Gonski

- "Embedded" FPGAs: reconfigurable logic in ASIC design for configurability ease of FPGA with low power/footprint/rad-hardenability of chip
- 2024: SLAC designed prototype eFPGAs with FABulous and taped out in 130nm & 28nm CMOS on TSMC MPW: proof-of-concept for open-source design tools for eFPGAs [JINST.19.P08023]
- FY26 LDRD: incorporate CERN TMR-G for radiation-tolerant design and tape out new higher logical capacity chip
  - Co-design with front-end ML feature extraction for FCCee: drift chamber, dual readout calorimeter





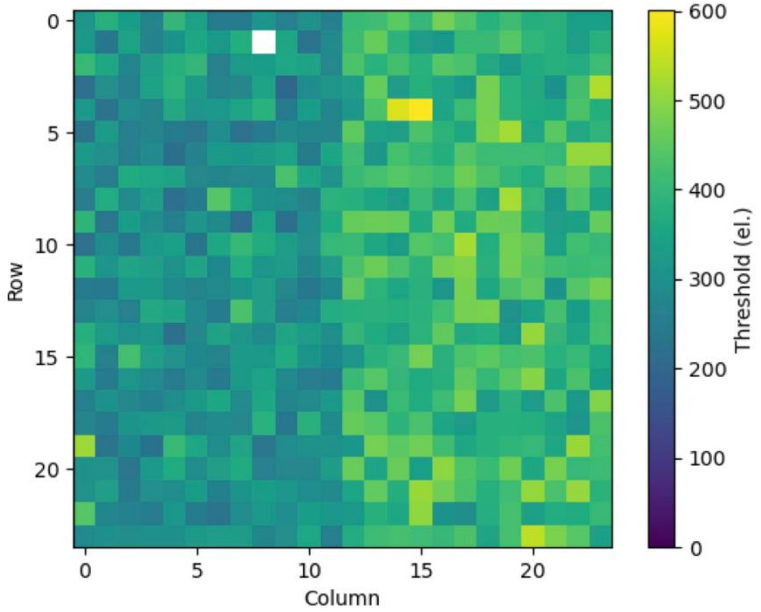


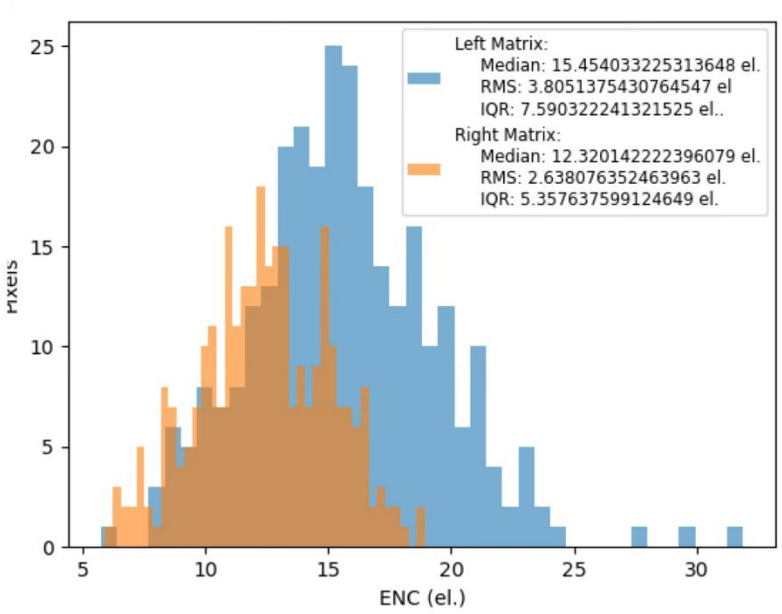
MAPS: NAPA prototypes timing capabilities

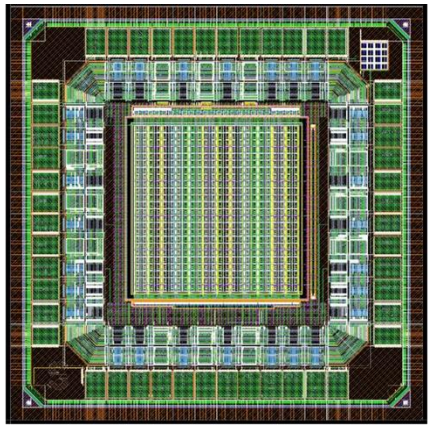
Lead PI: Vernieri/Rota

LDRD investment from 2022–25, readout and fast-timing capability

- Monolithic pixel R&D supports low material and high granularity tracking/calorimeter detectirs
- NAPA explored the power–timing tradeoff
- Napa-p1 fabrication, test stand, design of p2 supported by this LDRD, p2 fabrication and testing covered by US HFCC







Layout of SLAC prototype for WP1.2 2022 shared submission on TowerSemi 65nm

Left Matrix: Nominal Pixel Variant

Right Matrix: Pixel Variant with DC leakage current compensation

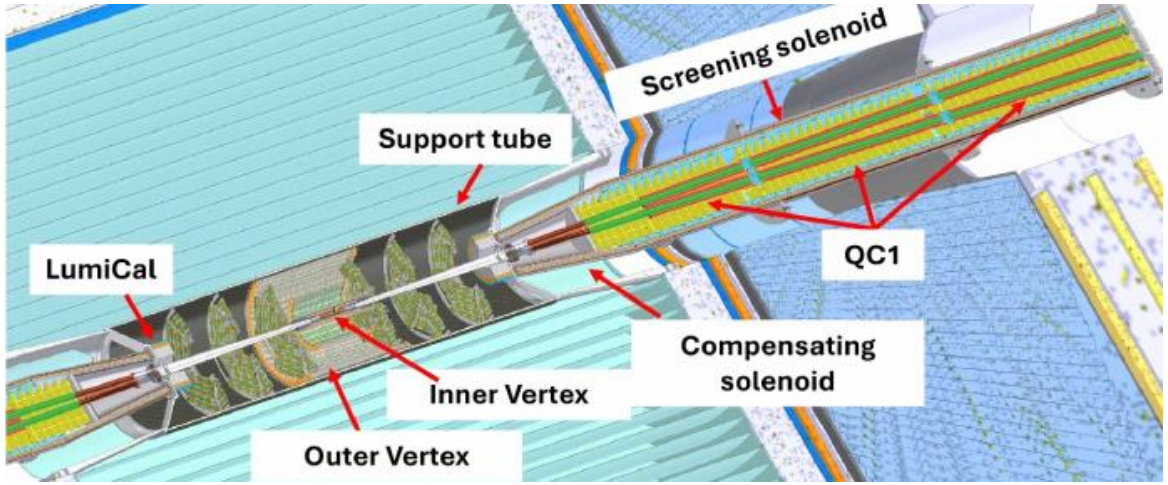
DC leakage current variant has less noise

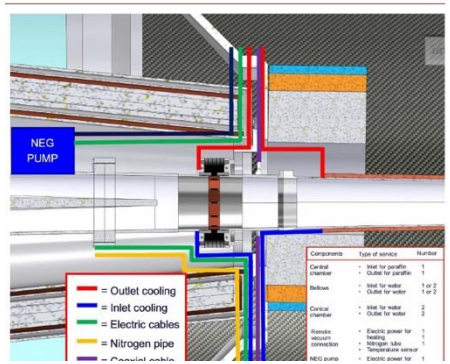
Collaboration with Brown / Stony Brook / Oregon

MDI developments

Lead PI: Vernieri/Gessner

Detector and interaction-region integration





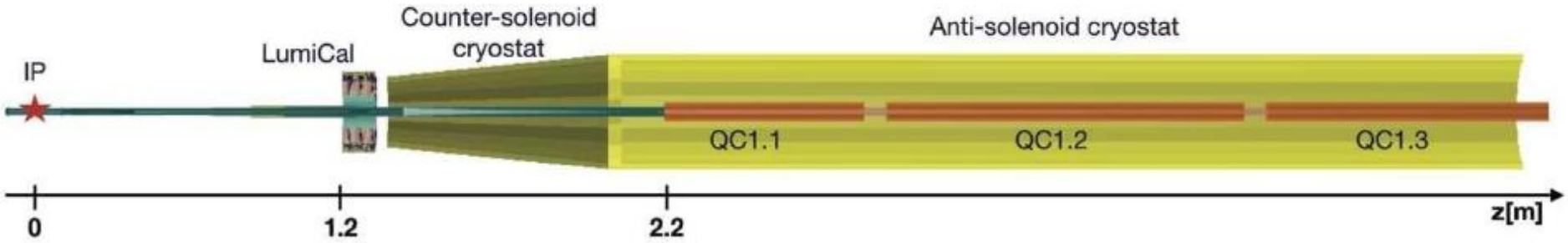
Two-year LDRD investment FY27-28

Core deliverables

- WarpX beam-induced-background simulations
- Vertex and LumiCal services routing
- QC1 integration and mechanical mockup

Collaboration with INFN Pisa/Frascati

Direct synergy: accelerator and detector work meet at QC1



Beam physics

Spencer Gessner and collaborators adapt WarpX for FCC-ee beam–beam and detector-background studies

Cryostat and mockup

J. Seeman's accelerator effort develops the QC1 cryostat test area that the detector mockup will interface with

Shared program

FACET and related accelerator activity strengthen the people and infrastructure behind the FCC strategy

Coordination point: align MDI services, QC1 engineering and accelerator support proposals

SLAC support to FCC activities

SLAC core capabilities

MAPS, LGAD and SPAD fast timing, eFPGA/ASIC design, beam–beam modeling, reconstruction, flavor tagging and accelerator expertise

Integrated FCC program

Vertexing, 4D tracking and high-granularity 5D calorimetry
AI/ML reconstruction and intelligent ASIC/eFPGA readout
Beam-background modeling, MDI and QC1 integration

- PoU prioritization places FCC as SLAC's next major collider project after completion of the HL-LHC ATLAS ITk upgrade

Near-term priorities supporting the long-term ambition

- Use LDRD to advance vertexing, calorimetry, reconstruction and intelligent readout
- Connect detector requirements to accelerator R&D through beam-background, MDI and QC1 work
- Coordinate support across LDRD, KA-29 + DOE Accelerate (fast-timing), FACET, US HFCC and potential US–Japan opportunities