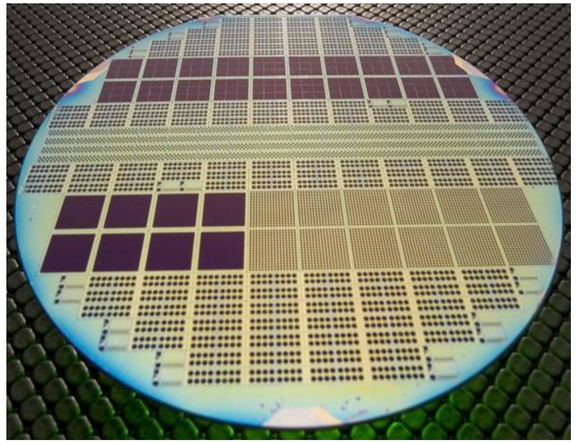
Review of MAPS progress in the US

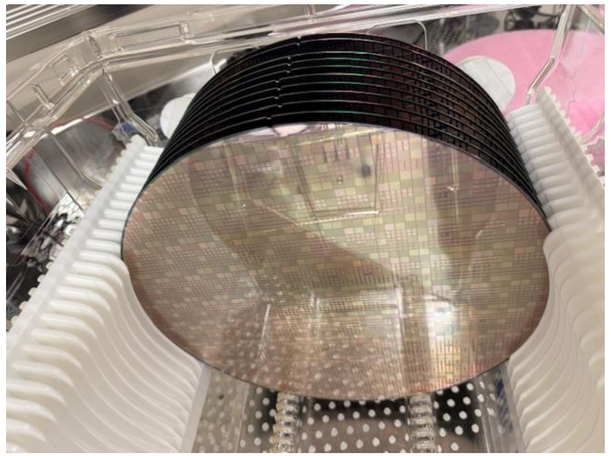
Caterina Vernieri and Artur Apreysan
4th US FCC Meeting
September 8-11 2026

FNAL

Introduction

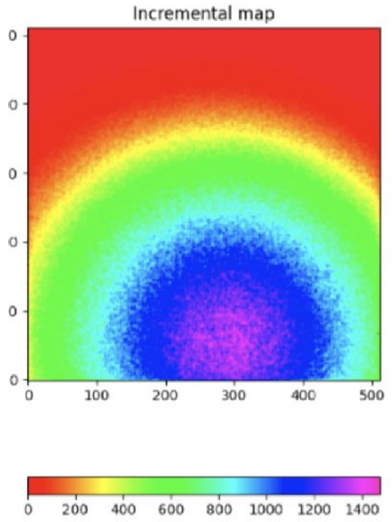
- Build on technologies developed at the for Tevatron, LHC, HL-LHC, EIC, and others
  - Unique resources of strong instrumentation groups
  - Expertise in physics simulations and tracking reconstruction
- Actively engaged in R&D on tracking detectors for FCC-ee
  - Sensor design, simulation studies, collaborations with vendors
  - Collaborative efforts with US and international universities

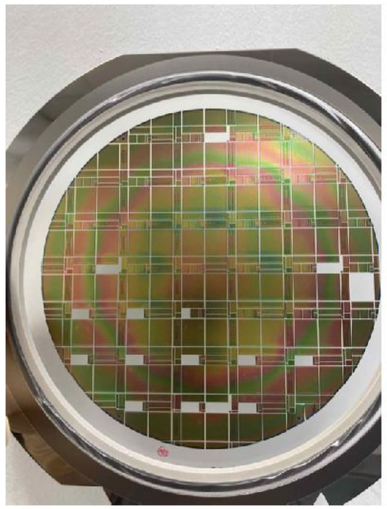


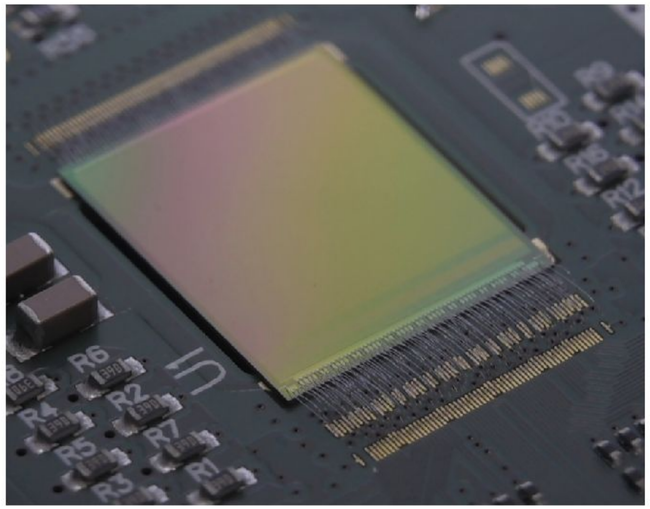


ARCADIA MAPS with LF110

- Sensor design and fabrication platform on LF11is technology
  - Developed for Future Lepton Colliders and Space Instruments
- Technology demonstrators
  - Main demonstrator (512 x 512 pixels) 25x25 μm2 pixels
  - Several other demonstrators produced: pixel and strip test structures down to 10 μm pitch, small-scale demonstrator for fast timing, etc





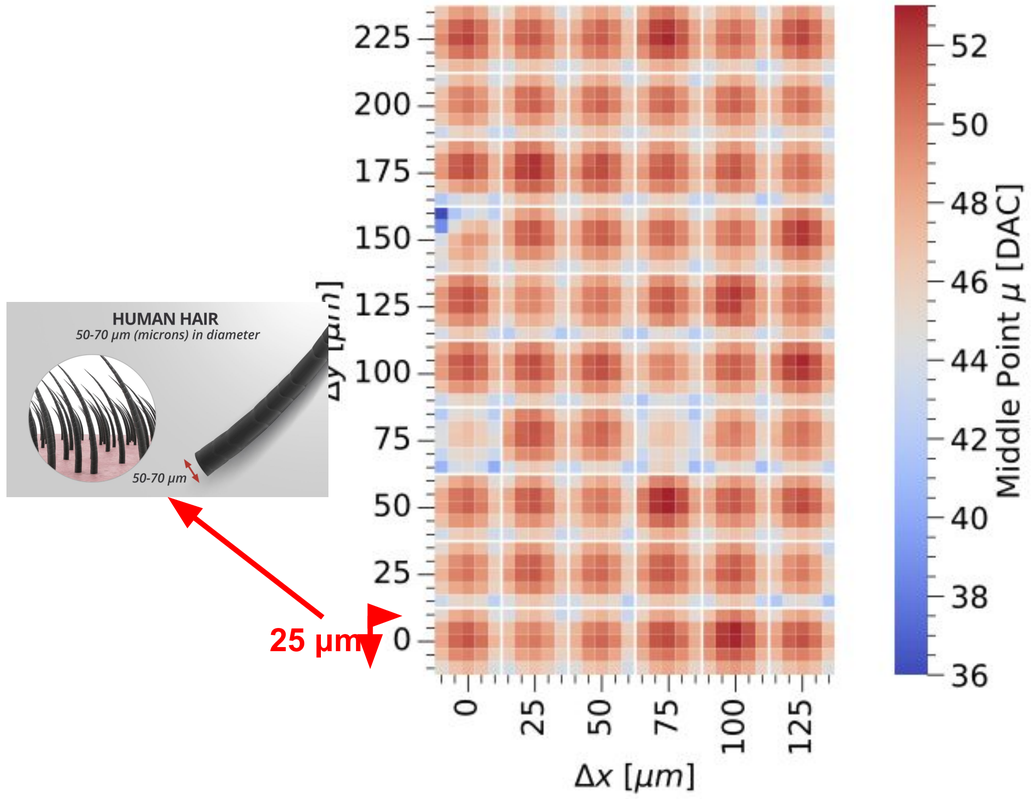


Measurements in the lab in HEERC

- Testing done in the new Precision Instrumentation and Timing (PIT) Lab at the Helen Edwards Engineering Center at Fermilab

Measurements in the lab

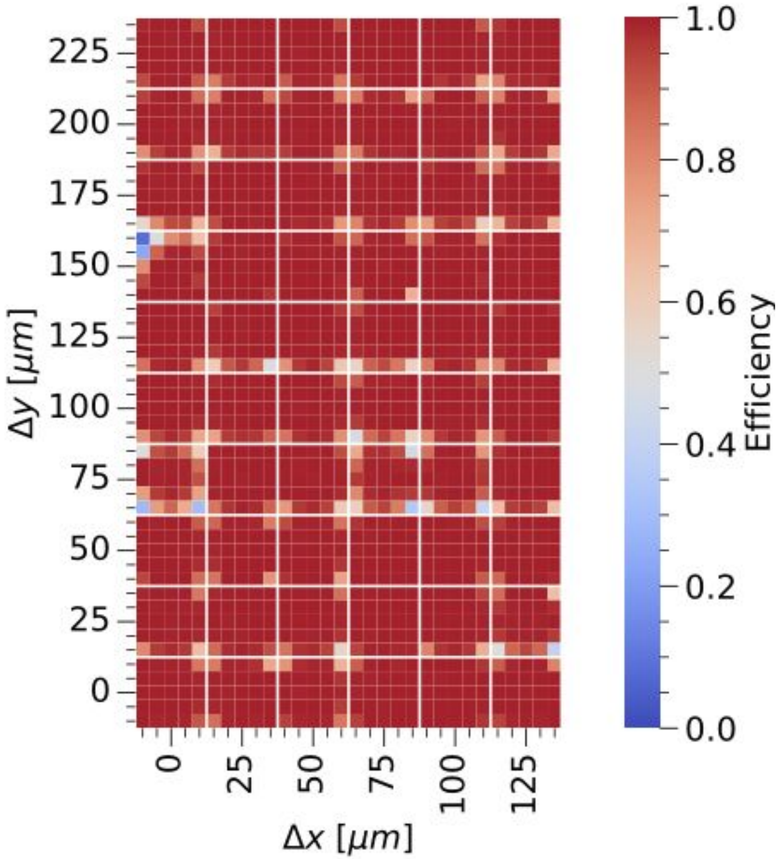
- An area of 6×10 pixels used to characterize cluster efficiency
  - Step size of 5μm is used across the scanning area
  - Total 25 scans per pixel.
  - Vary VCASN from 1 to 11, with steps of 2 to measure the efficiency.

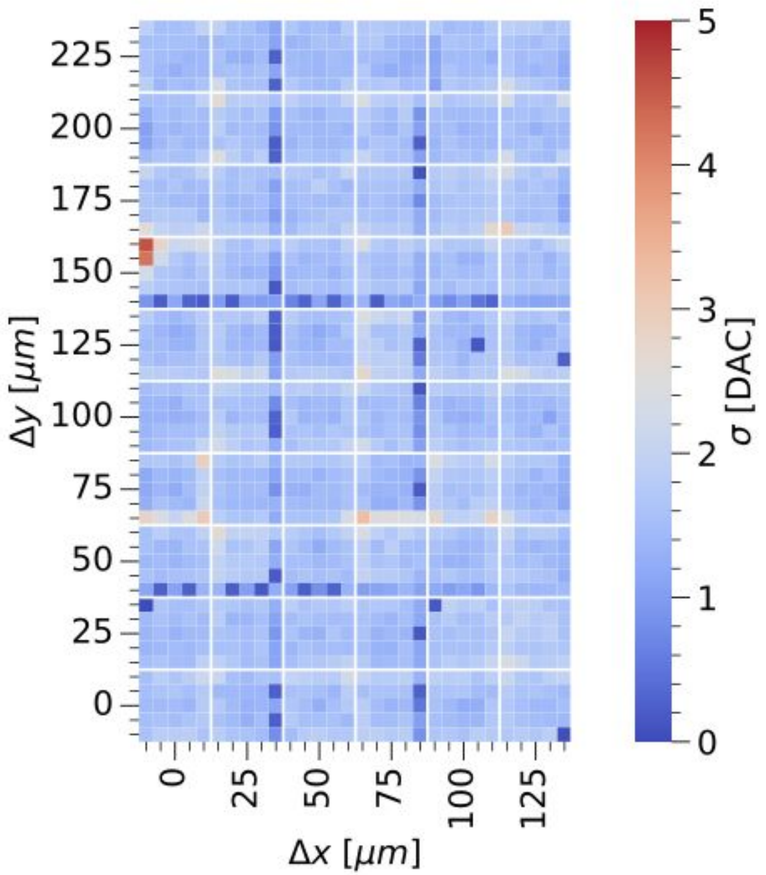


- Due to charge sharing, the value of μ is lower at pixel edges and higher at the center

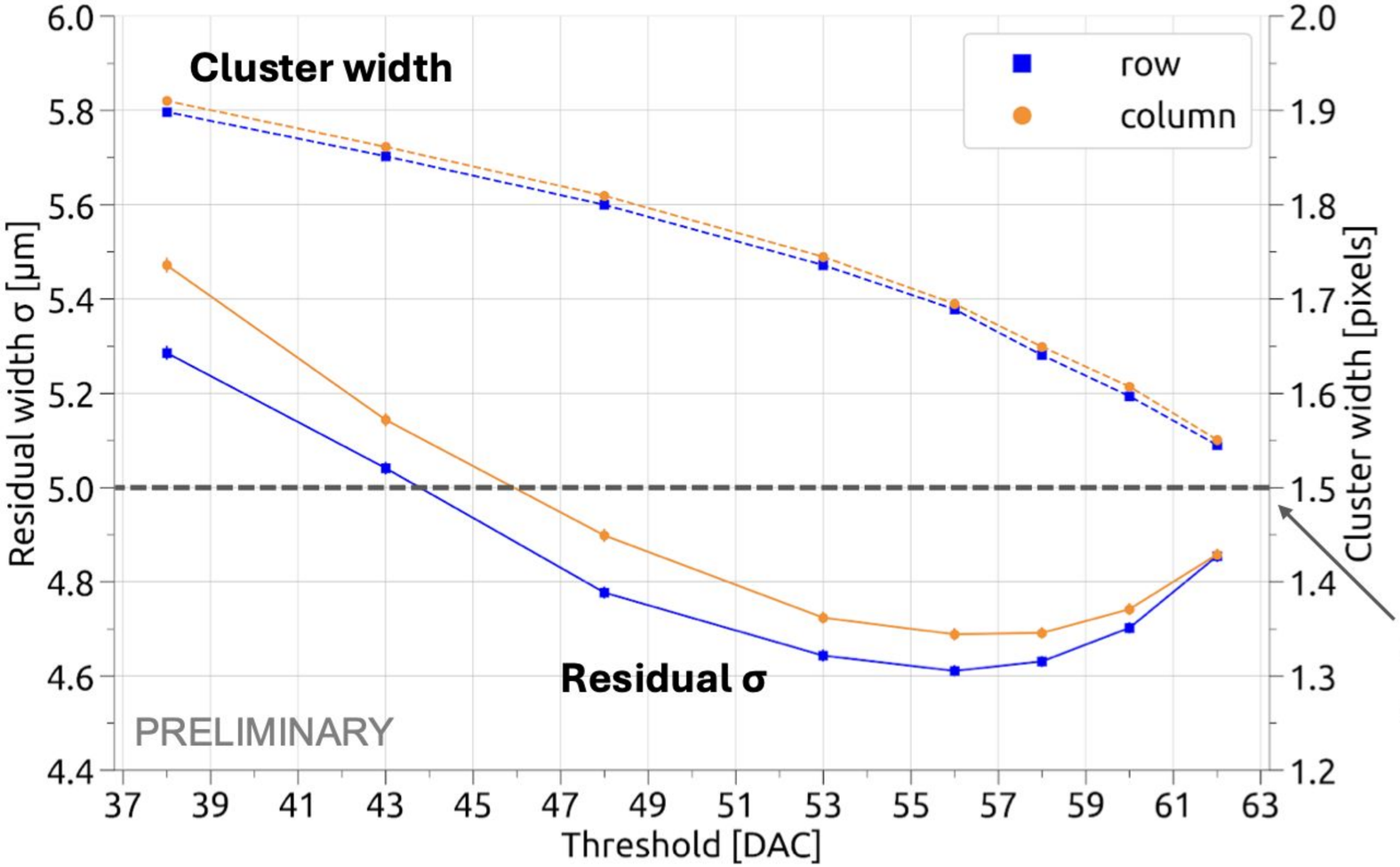
Measurements in the lab

- Excellent uniformity of detection efficiency across the pixel area
- Noise is mostly uniform across detector surface





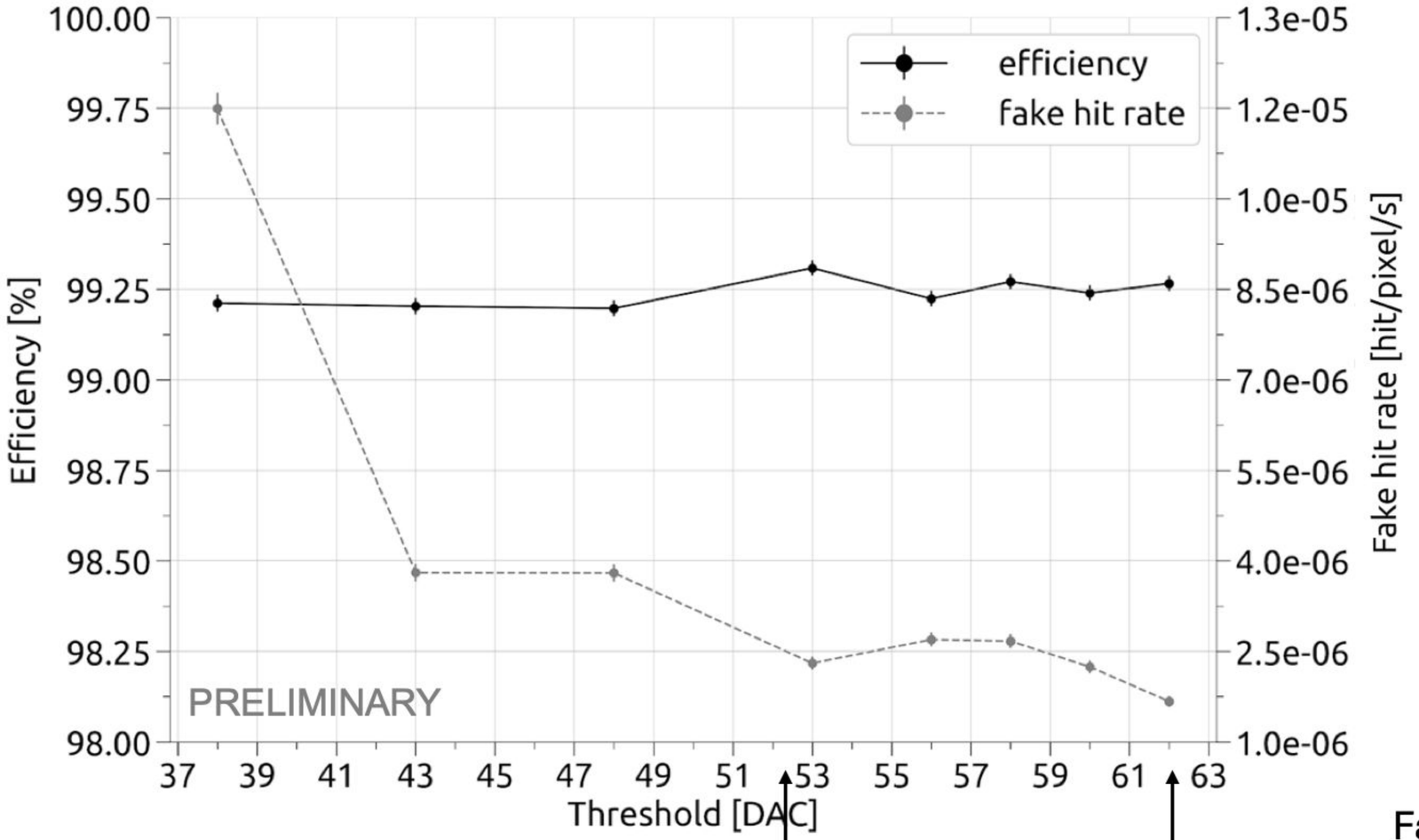
Measurements in beams



Cluster width always greater than 1.5 pixels

- Residual width always below the binary resolution (7.2 µm)

Measurements in beams



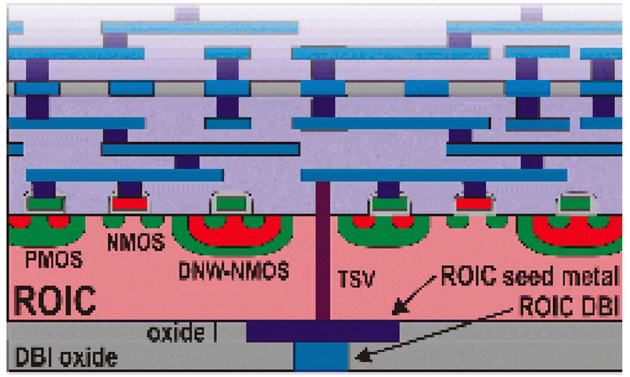
Fake hit rate measured during no-beam time
12 masked pixels on the DUT

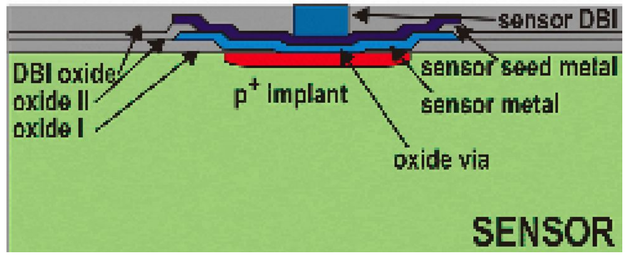
Measurements summarized in two papers

- **JINST 21 C04040 (2026)**
- **JINST 21 P04003 (2026)**

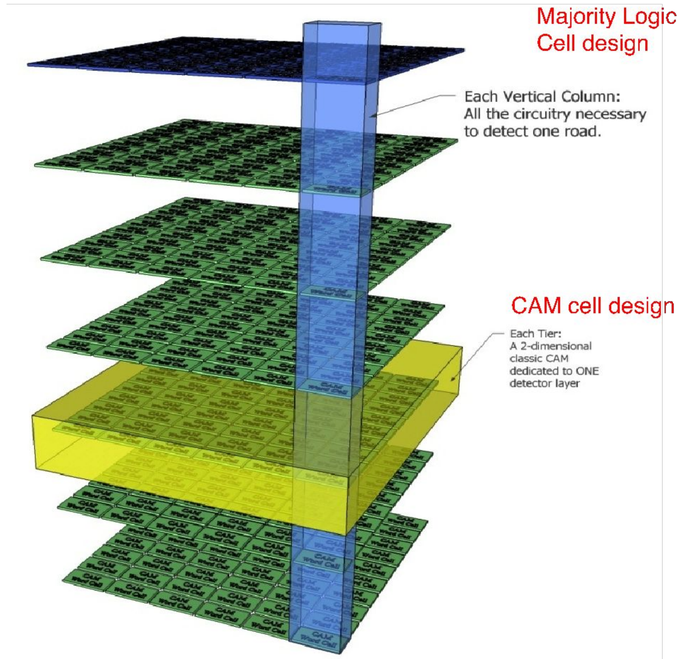
Advanced nodes, new technology

- Low-power, highly granular detectors in (***x***, *t*)
  - Implement in **TSMC 28-nm** technology node
  - Adopt **3D-integration** for HEP detectors
- Supported by DOE “Accelerated Innovation in Emerging Technologies”
  - Joint development effort of SLAC, FNAL and LLNL
  - Partner with industry leaders to implement new technologies
- 3D-integrated sensors could be candidate for vertex detectors**: high granularity, low mass and high configurability**



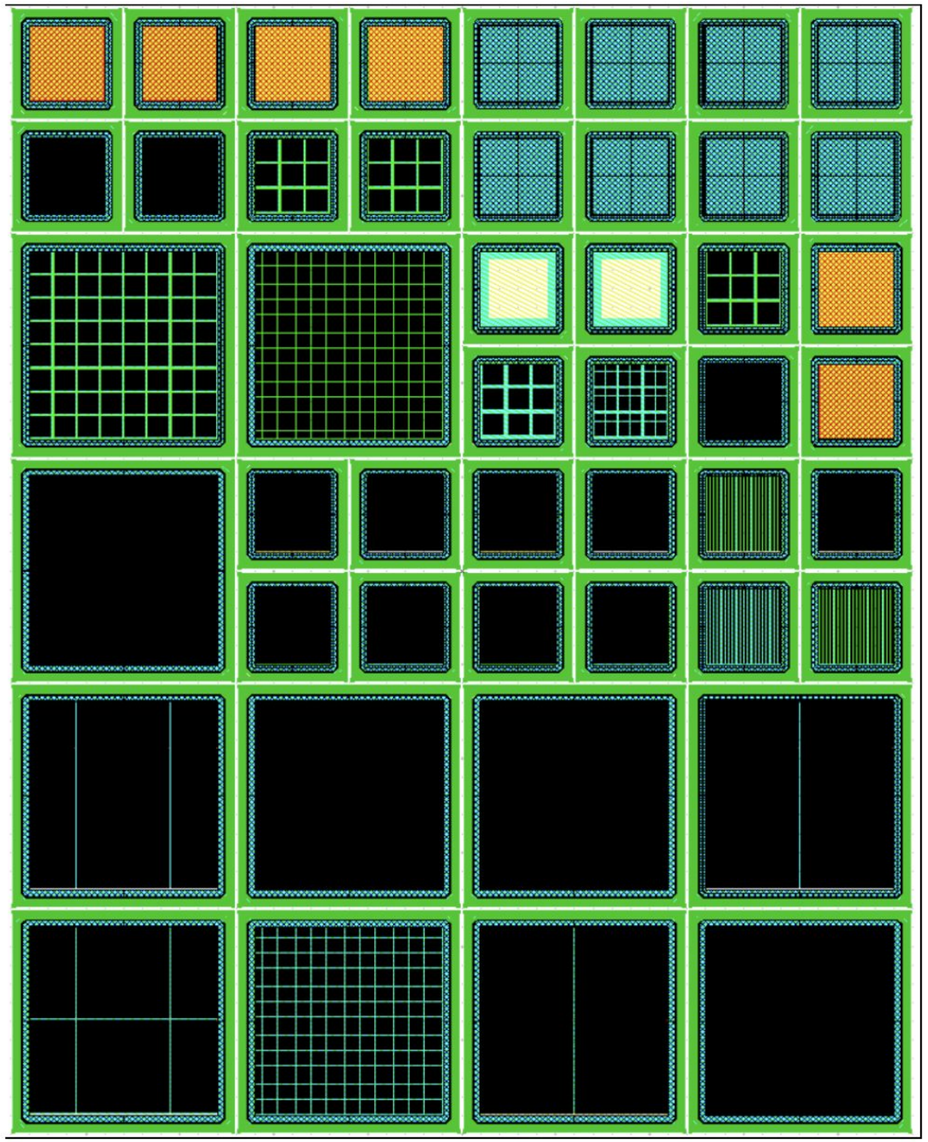


Control/interface



3D project : sensor development

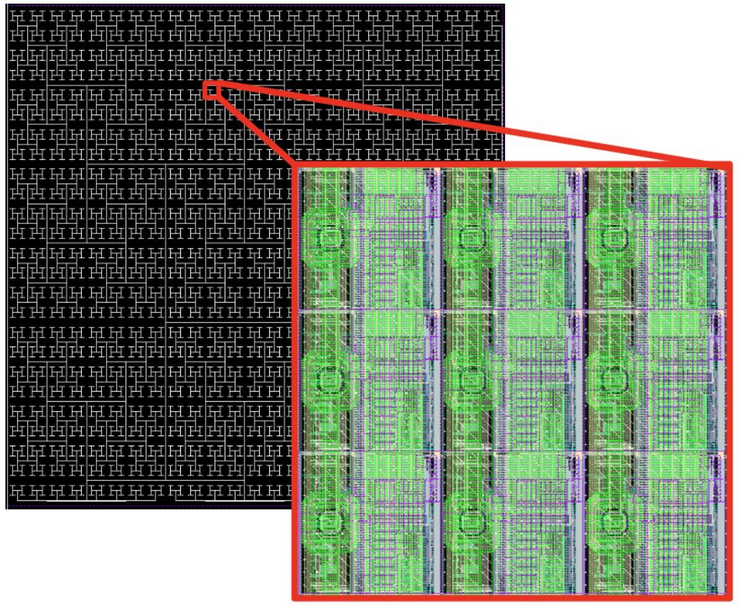
- Development in partnership with Tower Semiconductor
  - Wafer run: 12” in 65nm process
  - **First LGAD process on 12” wafers**
- Optimize doses, energies, edge termination strategies
  - Standard CMOS process forces constraints on detector design
  - Define active regions to exclude STI, metal density and spacing, angles restricted to 45° and 90°, etc…



3D project: readout ASIC 2nd prototype

- 2nd prototype in 28nm submitted in September 2025
  - THRIGLAV: THRee-d InteGrated LgAd driVer
- A 100x100 pixel array of 50μm pitch pixels
  - Optimization of pixel blocks
  - Digital control and readout logic design, fast IO driver.
  - First demonstration of 28nm readout chip bump-bonded to the prototype LGAD array with high-precision timing performance.
- For the next project phase, we would proceed to wafer-to-wafer bonding of 12” LGAD and 12” 28nm ASIC wafers.

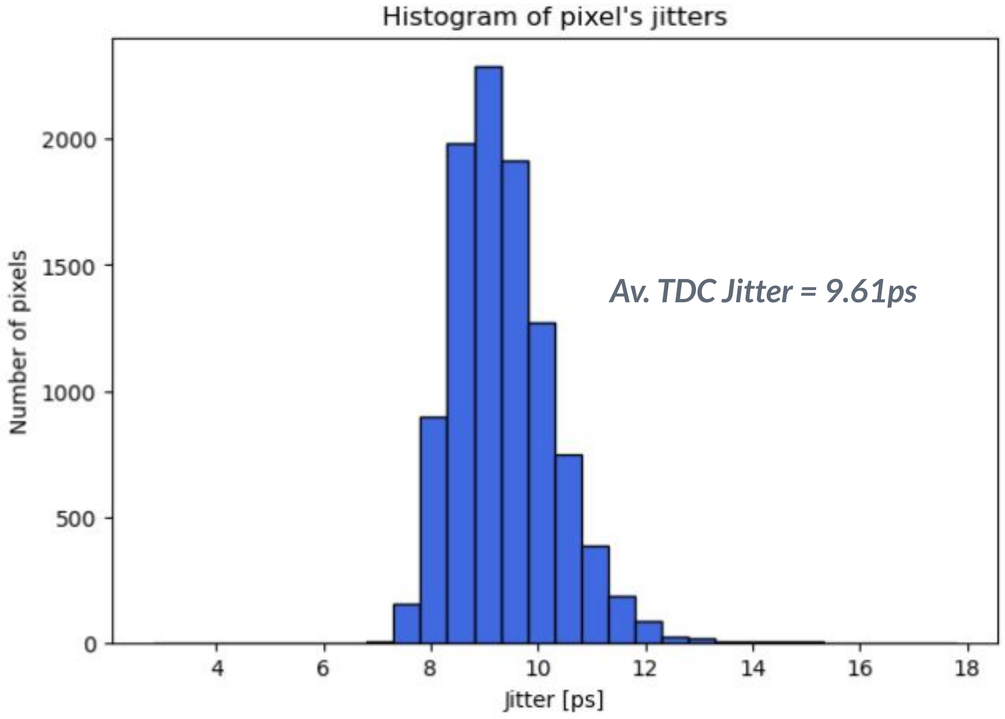
THRIGLAV v1

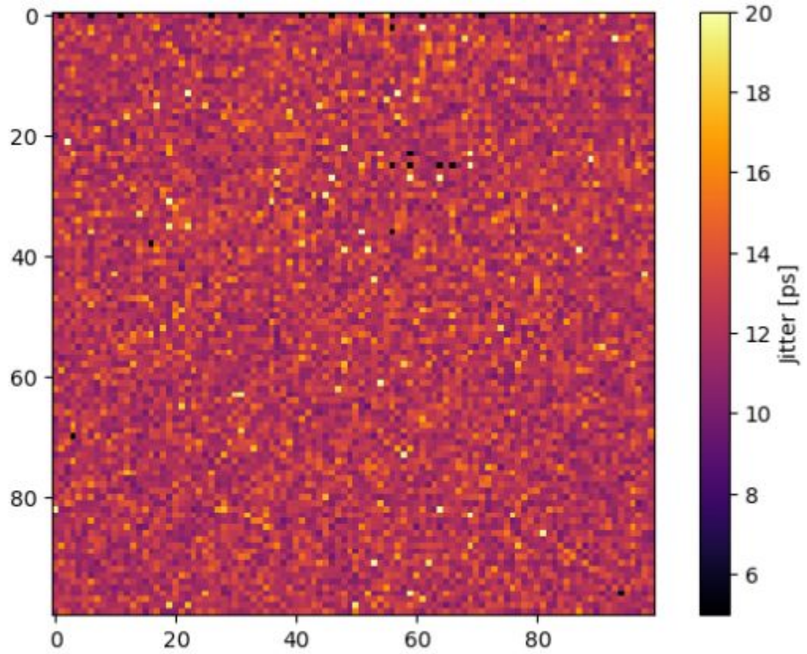


Layout of the pixel matrix highlighting the clock distribution three with zoom on 3x3 pixel region

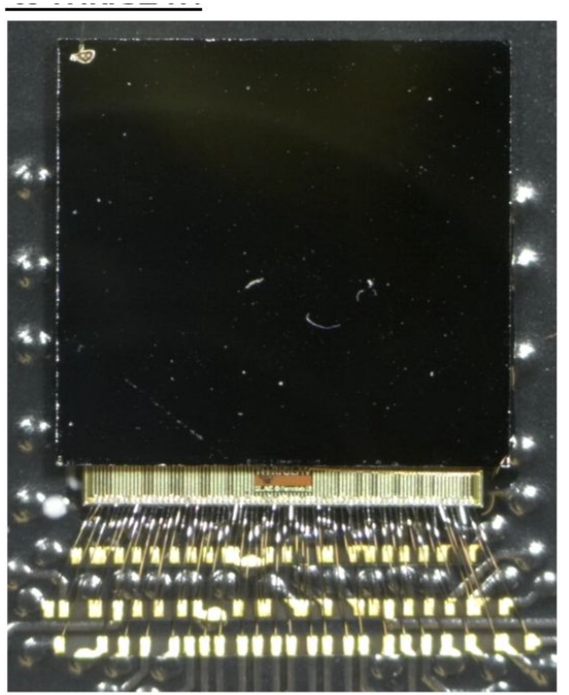
Characterization campaign

- TRIGLAV chips bump-bonded to AC-LGAD sensors
  - Measurements of the FE+TDC : **around 12 ps jitter**
- Extensive testing characterization of the full system is ongoing now





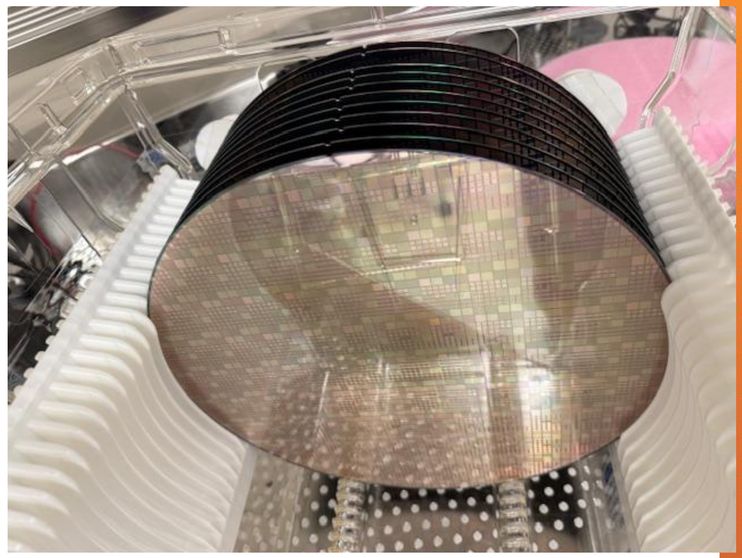
Average FE+TDC Jitter = 12.54ps



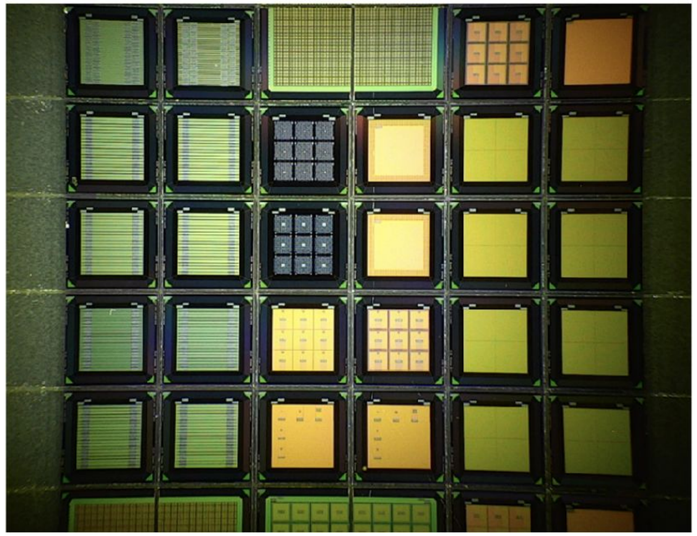
AC-LGAD bump-bonded to TRIGLAV chip

Characterization campaign

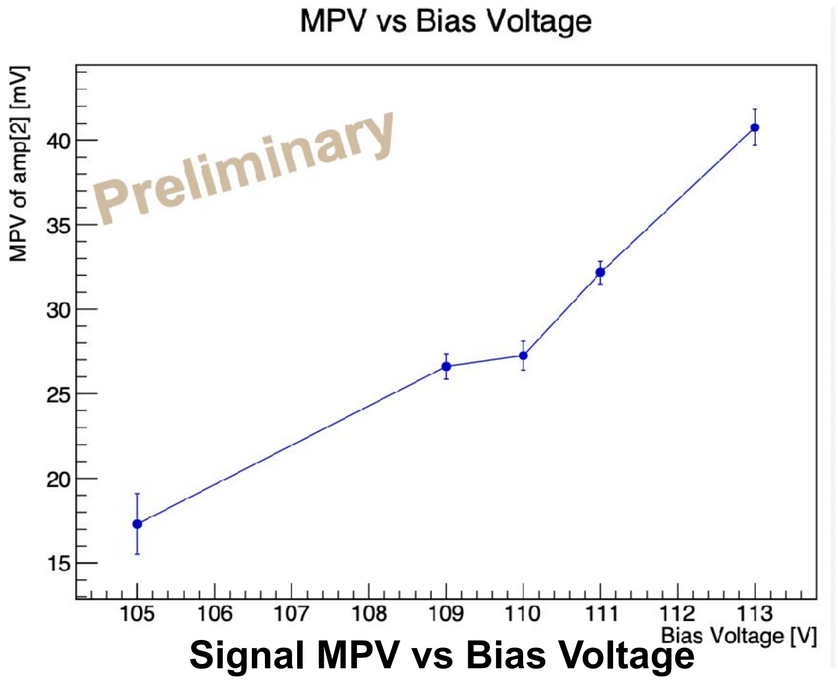
- Extensive characterization campaign
  - Testing with beta-source, IR-laser, test beams at CERN
- LGAD sensors on 12’’ wafers behave well demonstrating gain of 10
- **Time resolution of ~ 25 ps** demonstrated in beams, detection efficiency **~100%** across sensor surface



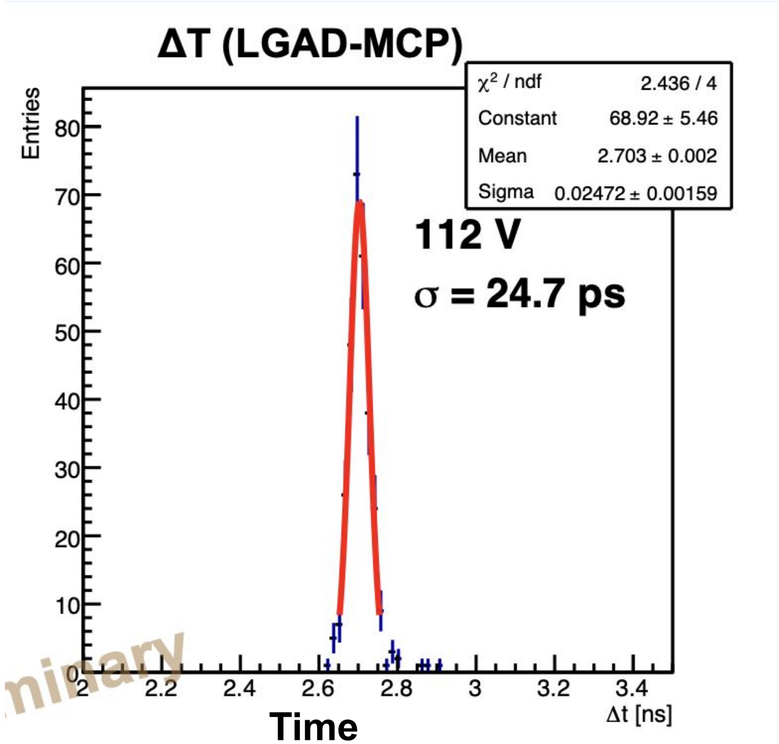
LGAD wafers



A section from Tower sensors



Signal MPV vs Bias Voltage



Time resolution

Summary

- Steady progress on multiple fronts in the development of tracking sensors for FCCee
- Actively engaged in the international and US collaborations on detector R&D: DRD and RDC
- Unique facilities and expertise enable the community to perform cutting edge detector R&D
  - New laboratory for sensor design, integration and characterization in HEERC
  - Many opportunities to make an impact on this R&D

MAPS@SLAC

Caterina Vernieri on behalf of

Christos Bakalis, James E. Brau (Oregon U), Rainer Bartoldus, Martin Breidenbach, Valerio Dao (SBU), Angelo Dragone, Loukas Gouskos (Brown U), Bojan Markovic, Giacinto Piquadio (SBU), Lorenzo Rota, Mirella Vassilev, Charles Young, Zhi Zheng, A. Duncanson, M. Zeng (Stanford - HEPIC)

SLAC NATIONAL ACCELERATOR LABORATORY

Stanford University | U.S. DEPARTMENT OF ENERGY

MAPS SLAC effort

Co-design approach: close interaction between physics studies and technology R&D

- The effort started in 2021 within CERN WP1.2 Collaboration based on TowerJazz-Panasonic (TPSCO) 65 nm CMOS imaging process with modified implants
  - Builds on sensor optimization done for the TJ180 process[1-2], excellent charge collection efficiency and low capacitance [3]
    - Increased density for circuits: Higher spatial resolution, better timing performance at same power consumption.
  - Supports stitching: enable wafer-scale MAPS → **potential to greatly reduce costs of future experiments**
- ALICE ITS3 upgrade was the main driver of CERN WP1.2 efforts
  - SLAC has been involved in Engineering Runs fabrication since 2021
  - Within this effort we have been interested in exploring the trade-offs of Nanosecond timing with power compatible with large-area, low-mass detectors

[1] M. van Rijnbach *et al.*, *Radiation hardness and timing performance in MALTA monolithic pixel sensors in TowerJazz 180 nm*, 2022 *JINST* C04034
[2] M. Munker *et al.*, *Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance*, 2019 *JINST* 14C05013
[3] S. Bugiel *et al.*, *Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology, NIMA Volume 1040, 1 October 2022, 167213*
[4] J. E. Brau et al., *The SiD Digital ECal based on Monolithic Active Pixel Sensors*, https://agenda.linearcollider.org/event/9211/sessions/5248, 2021.

FCC-ee timing motivation

Z-pole operation defines the immediate detector timing scale

20 ns

bunch spacing
at the Z pole

O(200 MHz cm^{-2})

incoherent-pair hit rate
in the vertex detector

≤ 1 μs

integration target to limit
multiple-Z overlap

~1ns time-stamp for bunch-crossing association.
The physics benefit of finer timing remains to be quantified.

NAPA target: explore nanosecond timing and measure its power and area cost below the FCC-ee bunch-association scale.

A. Ilg, A. Macchiolo and F. Palla, JINST 20 (2025) C06069, arXiv:2502.04071

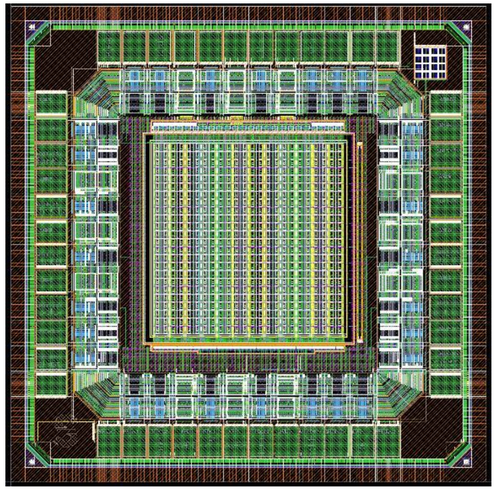
NAPA program: from architecture to characterization

Program goal

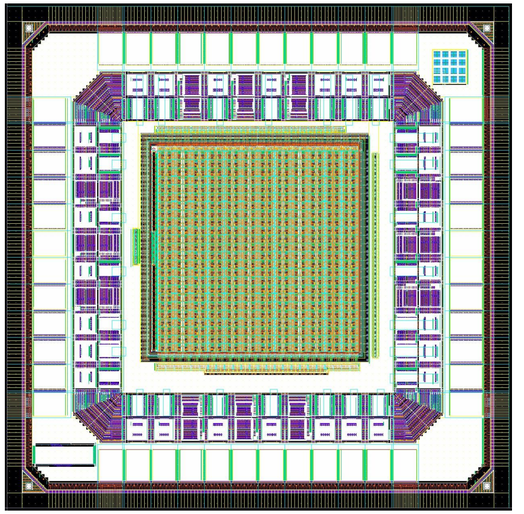
- Nanosecond timing with power compatible with large-area, low-mass detectors
- Circuit strategies that can scale toward wafer-scale MAPS

Progress - NAPA-pX : 24 × 24 matrix, 25 µm pitch, 65 nm TPSCo CMOS

- NAPA-p1 established the pixel architecture and initial design targets
- NAPA-p2 moves to systematic electrical and optical characterization
  - Single-stage charge-sensitive amplifier with pulsed reset
  - Periodically auto-zeroed leading-edge discriminator to reduce threshold dispersion
  - **New!** Programmable CSA and discriminator bias settings expose the timing versus power trade-off
  - **New!** On-chip charge-injection circuit for calibration and testing i.e. supports threshold, noise, time-walk and jitter measurements
- Current measurements isolate the front-end timing and power trade-off



NAPA-p1 layout (first 65 nm prototype)



NAPA-p2 layout

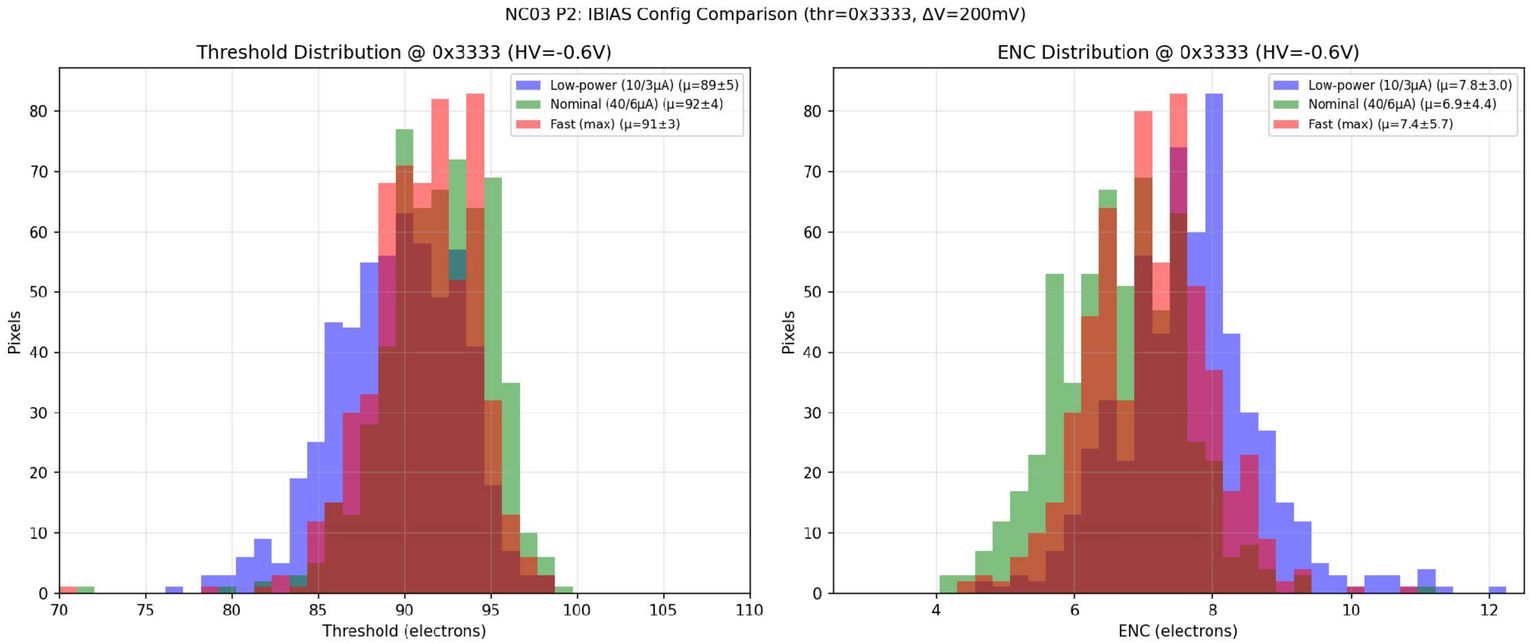
NAPA-p2 post-layout simulation targets

Design quantity	NAPA-p2 target
Nominal bias currents	CSA 520 nA, comparator 100 nA
Capacitances	Cfb = Cinj = 0.36 fF, Ccds = 9.60 fF, Cthr = 0.96 fF
Equivalent noise charge	7 e^-
Threshold at ΔVThr = 200 mV	115 e^-
Time walk for Qin > 150 e^-	27 ns
Analog power	0.70 µW/pixel (continuous analog)
Simulation status	Post-layout, nominal settings

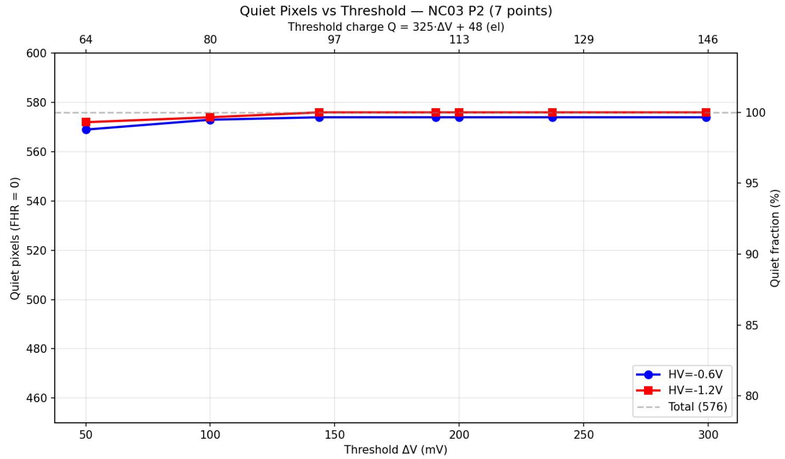
What the targets test

- The nominal point targets 7 e^- ENC and 27 ns time walk at 0.70 µW/pixel
- Measured threshold and ENC provide a direct test of the post-layout model
- The front-end bias scan measures how much timing improves with additional current

Threshold, ENC and noise occupancy



Noise occupancy



576 pixels
5000 readout opportunities per pixel
Single-count sensitivity: 2×10^{-4}/readout

At ΔVThr = 200 mV and Vsub = −0.6 V, the three power settings give mean thresholds of 89–92 e^- with 3–5 e^- RMS dispersion and mean ENC values of 6.9–7.8 e^-.

Nominal point: ENC is 6.9 ± 4.4 e^- measured versus 7 e^- simulated; threshold is 92 ± 4 e^- versus 115 e^- simulated.

Auto-zeroing gives 3–5 e^- RMS threshold dispersion; more than 98% of pixels remain quiet at ≈64 e^-.

NAPA-p2 laser setup

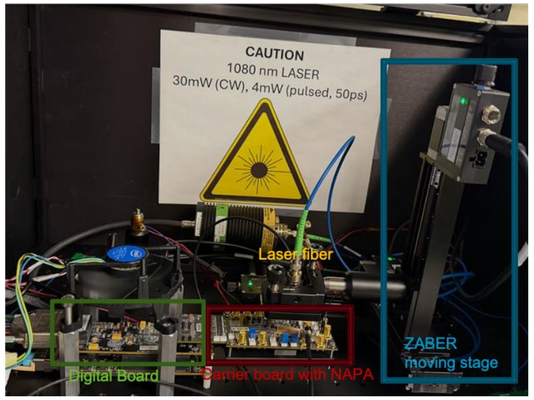
External timing reference to selected-pixel digital output

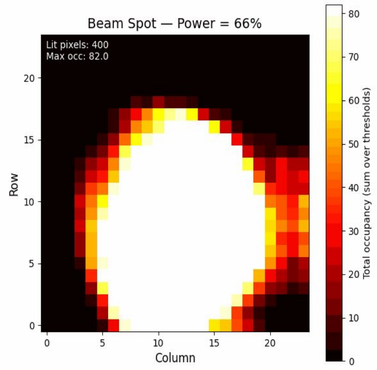
- Set up a 1080 nm picosecond pulsed laser system for NAPA-p2 testing
  - PicoQuant LDH-P-C-1080, driven by a Sepia PDL 810 laser driver
  - Backside illumination
- Collimation and micro-focus optics reach a **target spot size of ~6 µm**
- The chip is mounted on a **motorized Zaber stage** for position and focus scans.
  - Step size 0.048 um per axis

Timing Chain: The FPGA defines the NAPA readout window and provides the timing reference for internal injection and laser measurements.

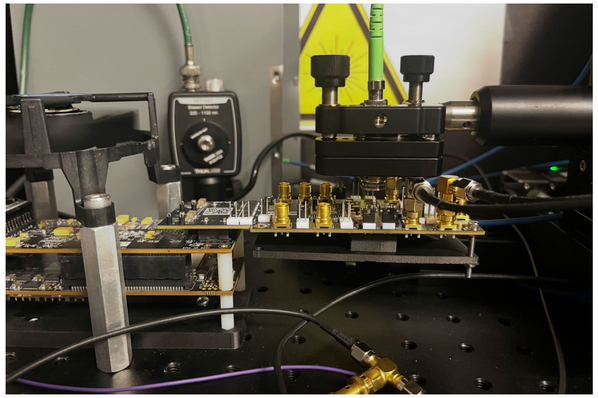
- For laser measurements, the FPGA generates a programmable delayed trigger sent to the Sepia laser driver
  - FPGA trigger is passed to PicoScope 6424E, which generates the reference pulse sent to the laser driver
- ***Timing is measured as the delay between the reference signal and the pixel discriminator output***

The custom carrier board supplies sensor and front-end biases and routes FPGA control and binary readout. NAPA-p2 has no in-matrix TDC, so the setup measures the uncorrected leading-edge response with an external reference.





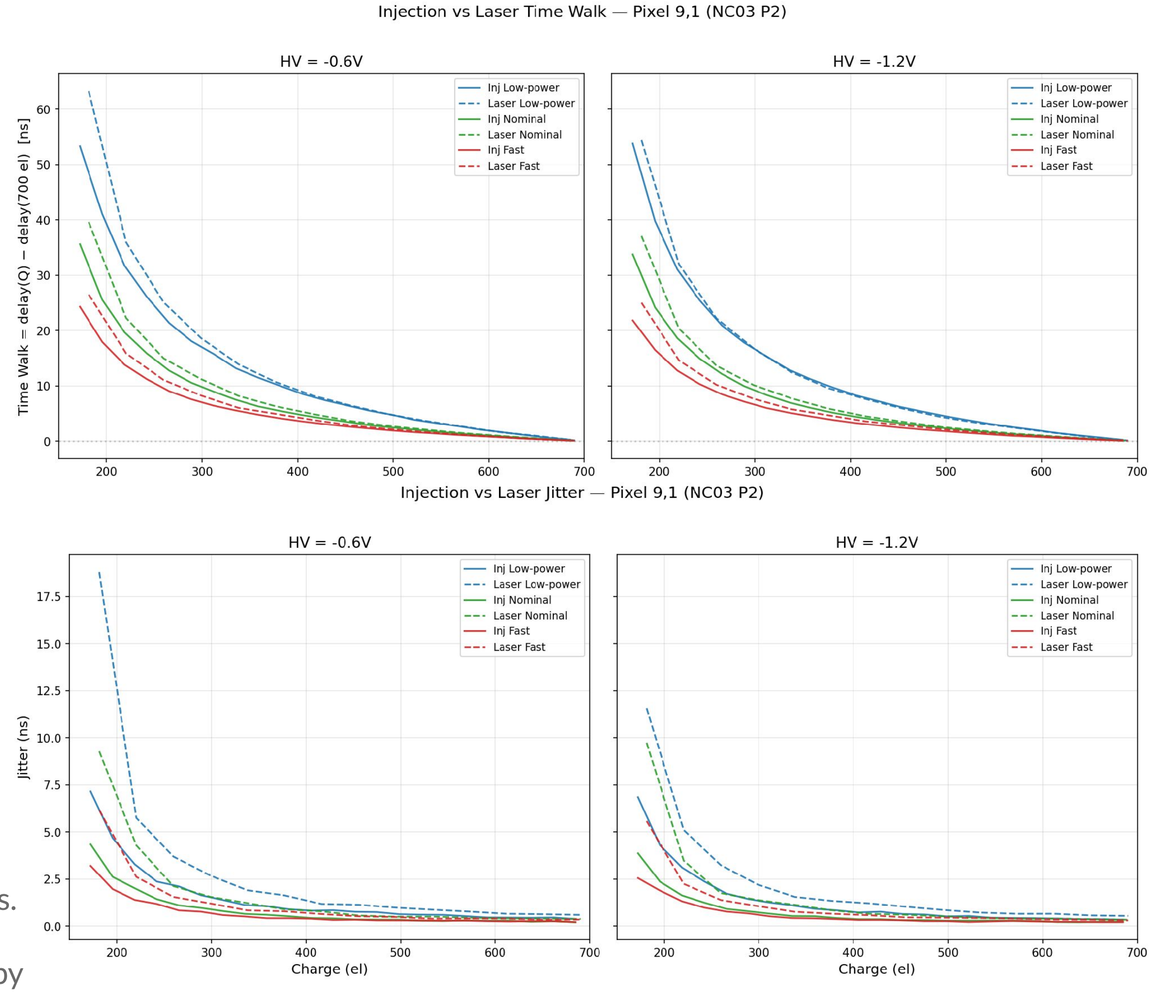
Spatial response motivates pixel-by-pixel charge calibration



NAPA-p2 laboratory characterization

First measurements with internal charge injection and 1080 nm laser excitation

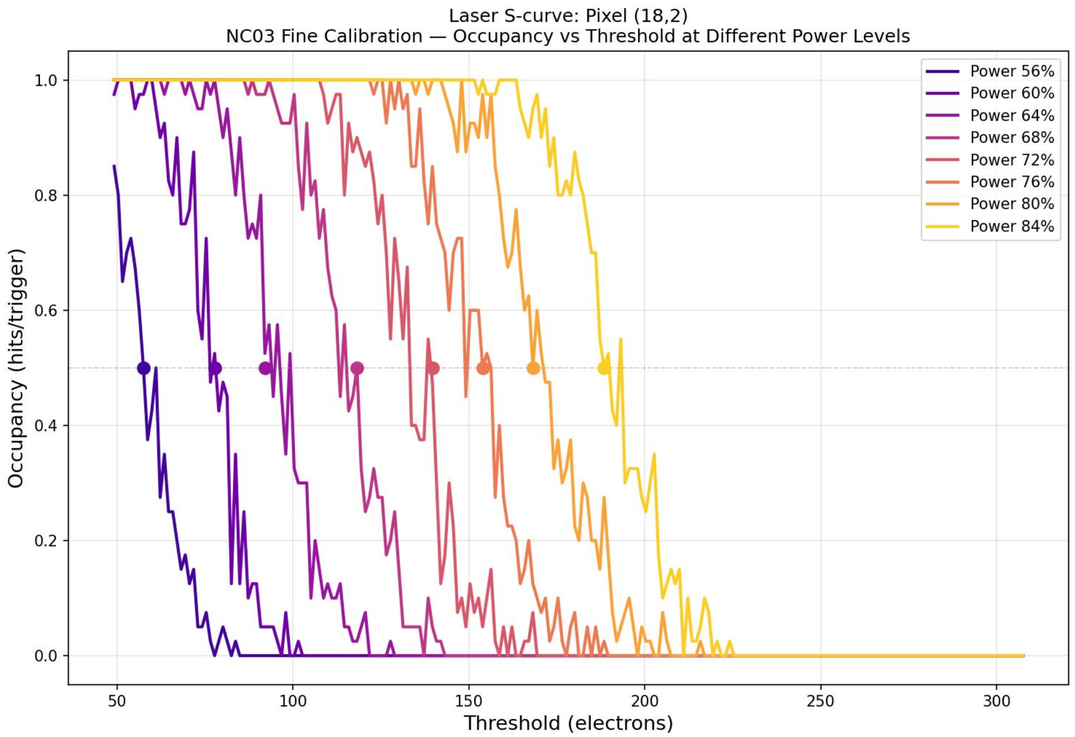
Metric	Measured NAPA-p2
Pixel matrix	24 × 24 pixels, 25 µm pitch
Mean threshold	≈90 e^- with 3–5 e^- RMS dispersion
Mean ENC	6.9–7.8 e^- across the three power points
Quiet pixels	>98% at ≈64 e^-; sensitivity 2 × 10^{-4}/readout
Jitter at 550 e^-	0.30 ns injection, 0.49 ns laser
Time walk	9.7 ns injection, 10.8 ns laser (300–700 e^-)
Analog power	0.70 µW/pixel nominal; 0.20–1.40 µW/pixel studied



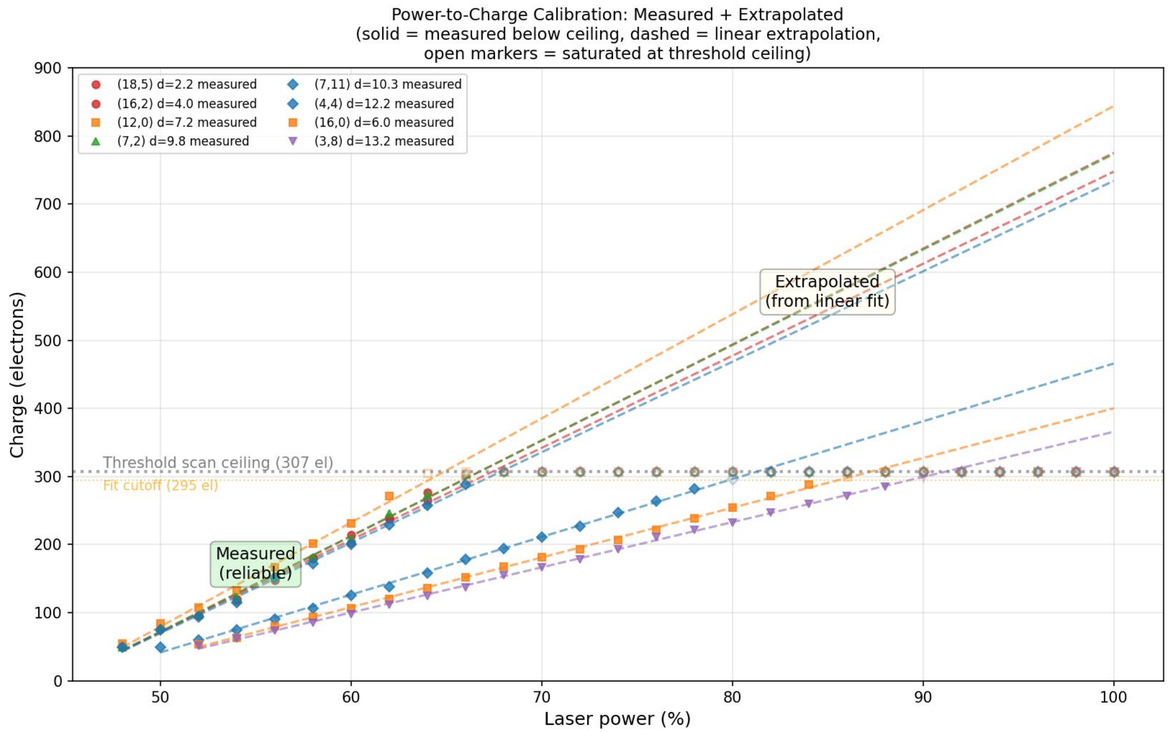
Timing values: Vsub = −0.6 V, nominal front-end power. Instrumental timing contribution: 0.24 ns.
Measured laser timing-chain contribution: 0.071 ns.
Effective front-end rise time: a few ns, comparable to sensor charge-collection time and limited by discriminator slew rate.

Laser charge calibration

Optical S-curves



Pixel-specific power-to-charge scale



At fixed laser power, scan threshold: the 50% hit-efficiency crossing defines the effective collected charge. Repeat pixel by pixel to account for non-uniform illumination.

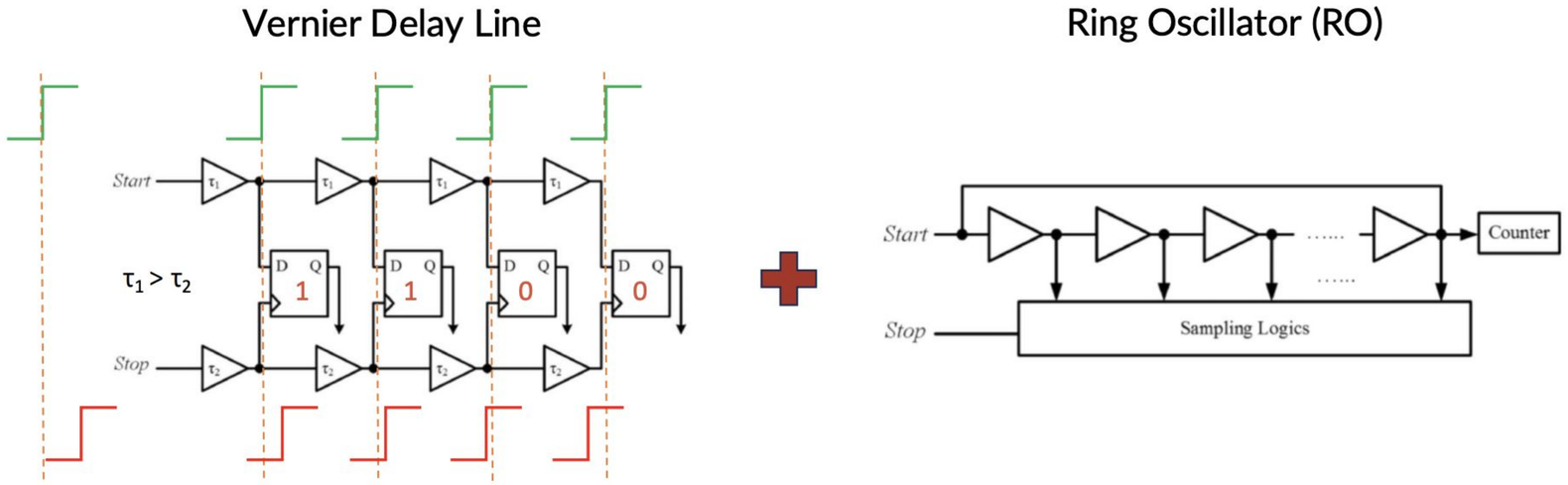
Only points below 295 e^- enter the linear fit. The dashed high-charge extrapolation carries an additional scale uncertainty.

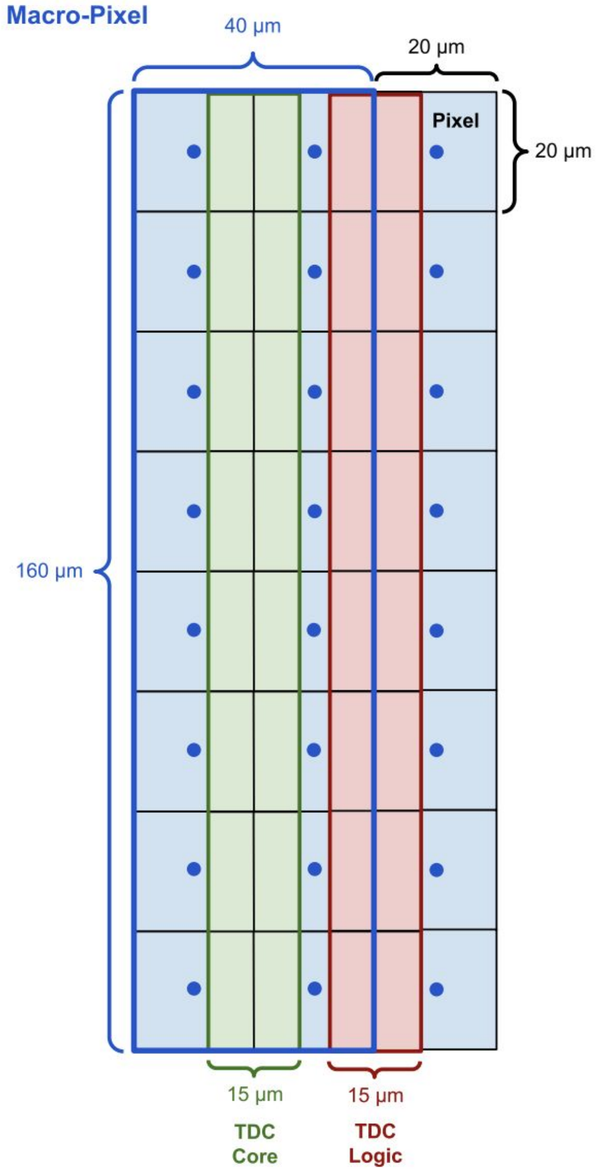
Full TDC Architecture

A. Duncanson, B. Markovic DRD7.6a meeting

Assuming a 256x256 matrix of 50 µm pixels

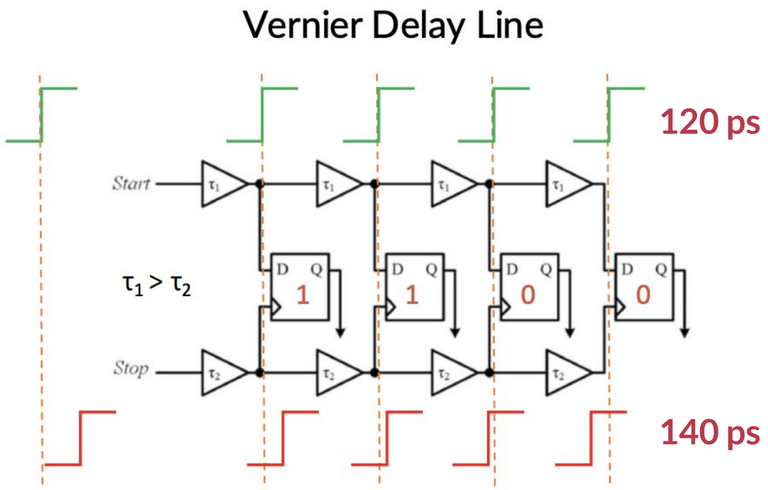
- **Preliminary integration concept: one TDC shared by approximately 4 × 8 pixels**
- HIT information from pixel combined in digital domain
  → START signal
- Clock → STOP signal
- Time-to-Digital Converter (TDC) architecture :
  - Vernier Delay line: high resolution (τ1 - τ2)
  - Ring Oscillator: large dynamic range due to counter

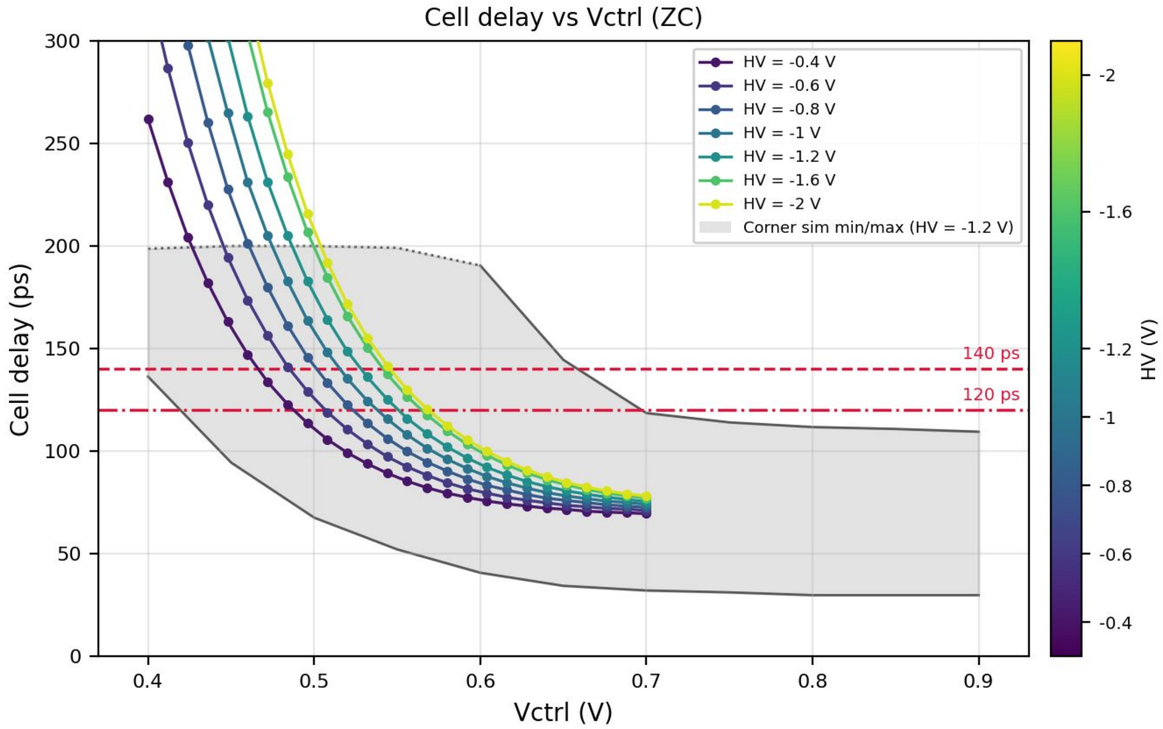




TDC Vernier: preliminary measurements

- Test structures for TDC Vernier delay cell included in the recent ER2 submission
- Measurements in good agreement with simulations for targeted 20 ps
- Complete TDC will be submitted in dedicated chiplet in shared run in Oct 2027





A. Duncanson, B. Markovic DRD7.6a meeting

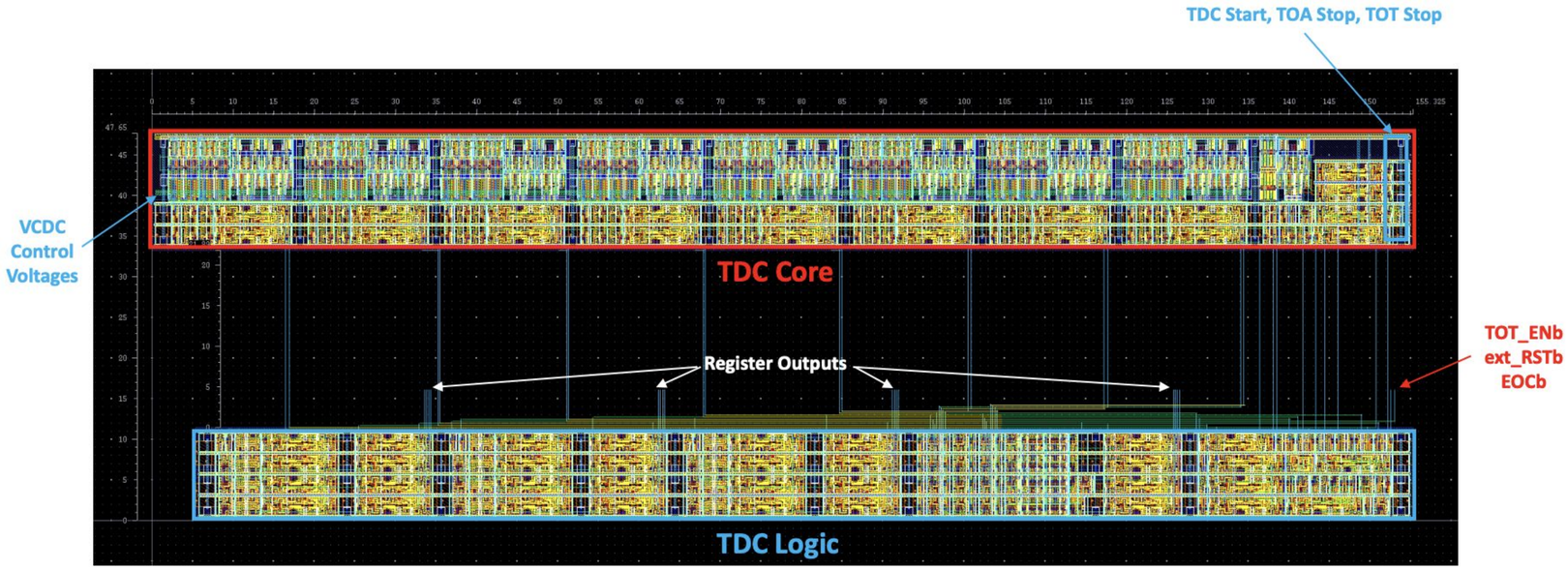
Full TDC Layout

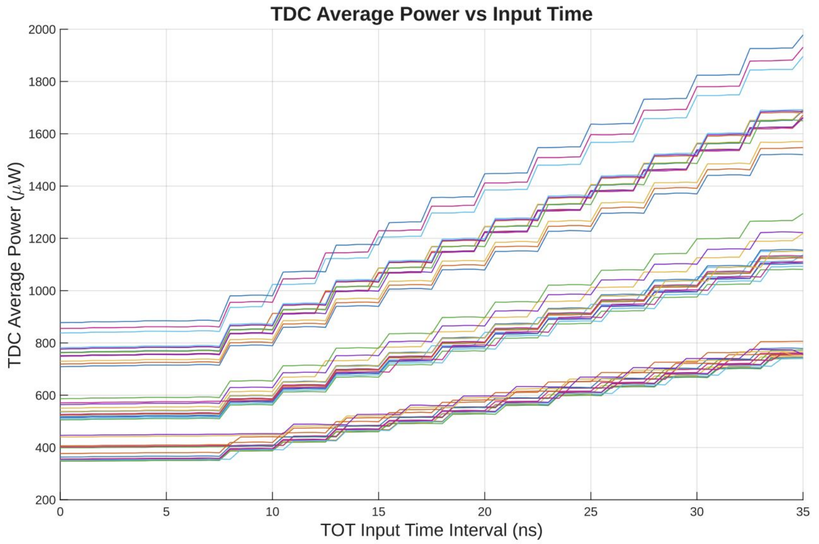
A. Duncanson, B. Markovic DRD7.6a meeting

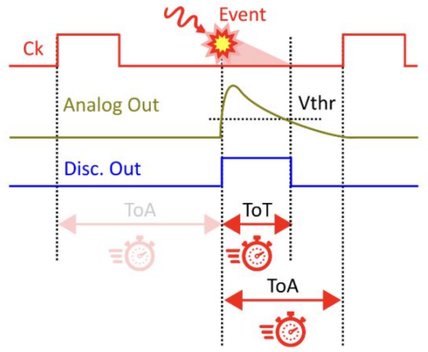
Full TDC area: TDC Core + TDC Logic = 4,250 μm^2

TOA resolution: 20 ps
TOT resolution: 2.5 ns
Power consumption:

- If no HIT: only static power consumption due to leakage
- If HIT: 60 μW assuming continuous conversion every 1 μs
  → scaled by macro-pixel occupancy



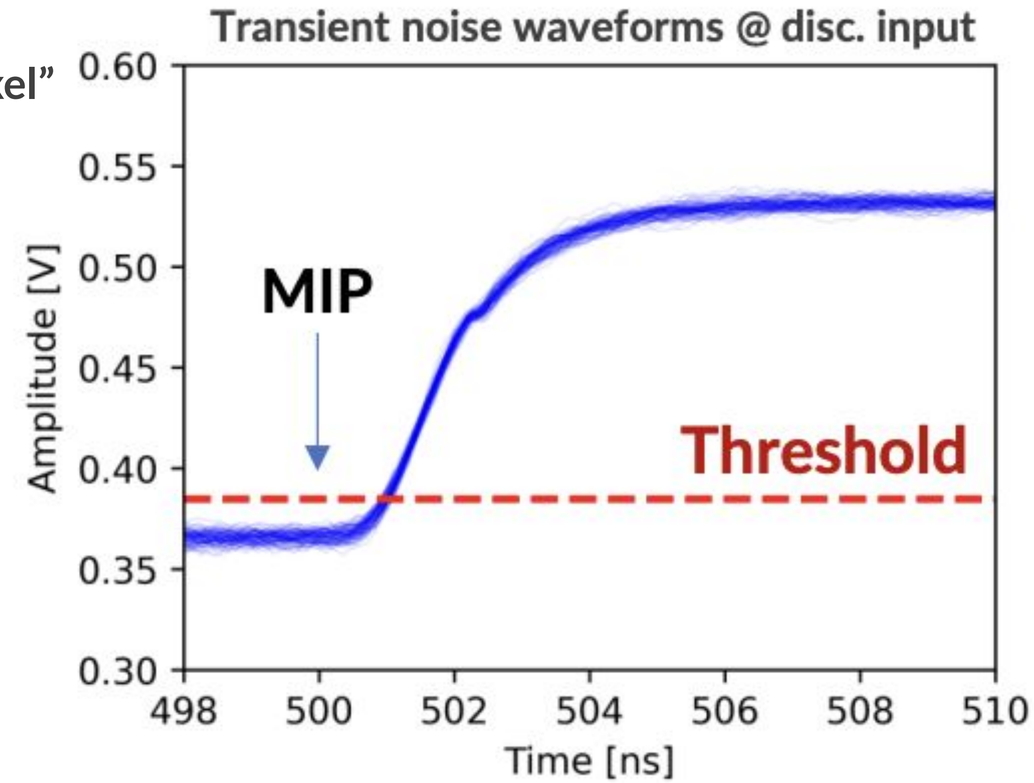




Future Pixel Front-End optimization

Pushing the timing resolution and better understanding of the power consumption

- Developed a more complete numerical simulation, including:
  - ENC from noise, bandwidth and noise shaping
- **Digital signal from multiple front-ends sent to one TDC → "macro-pixel"**
- Preliminary simulation results of pixel front-end:
  - ENC: 16 e-
  - Jitter: 36.8 ps
  - Front-end current: 2.6 µA/pixel
  - Timewalk: 3 ns → "gating" accuracy of 15±3 ns
- Note that:
  - TOT not yet included,
  - It assumes 1 ns rise time for typical signal
- Analog front-end power: 3 µW/pixel
  - Timing resolution: ~40 ps
  - Equivalent active-area density: 0.48 W/cm² at 25 µm pitch



For nsec timing resolution, power budget is within our target

Looking ahead - next steps

- In FY26 we fabricated as part of ER2 a new prototype Napa-p2 and TDC chiplet
- For FY27, key deliverables include :
  - characterization of *Napa-p2 prototype* this will enable thorough trade-off studies addressing power, timing resolution and calibration
  - submission as part of ER3 of a high-performance low-power TDC chiplet enabling targeting 20ps timing resolution
    - this features 8 channels for characterization, targeting an aggressive 20ps timing resolution.
    - This design is of interest to multiple experiments within the DRD3.1 and DRD7 collaborations, reflecting the broad applicability of the technology.

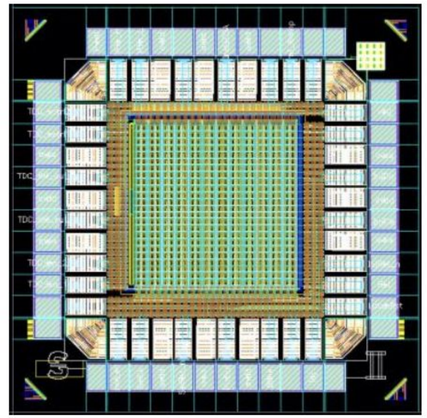
Depending on resources/funding availability, we plan to:

- implementing the TDC in the pixel matrix
- Exploring the synergies with EIC upgrades and LAS developments in 65nm
  - contribute to testing of wafer-scale MAPS devices at CERN
  - Gaining expertise with designing solutions for power distribution compatible with stitching - and potentially enabling O(ns) timing precision
- Innovative research into wafer stacking and scaled CMOS processes (below 65 nm) to achieve breakthrough improvements in vertex detector granularity.

Conclusions

Measured NAPA-p2 performance

- Threshold 89–92 e^- and ENC 6.9–7.8 e^- across the three tested power settings
- More than 98% of the matrix remains quiet at the lowest studied threshold of about 64 e^-



NAPA-p2

Timing at nominal front-end power

- At 550 e^-, jitter is 0.30 ns with injection and 0.49 ns with the laser. The instrumental contribution is 0.24 ns
- Time walk over 300–700 e^- is 9.7 ns with injection and 10.8 ns with the laser

Power trade-off and next steps

- The 0.20–1.40 µW/pixel scan confirms better timing with increasing front-end current while ENC remains nearly constant
- Complete calibration and systematic studies, then characterize the standalone Vernier TDC

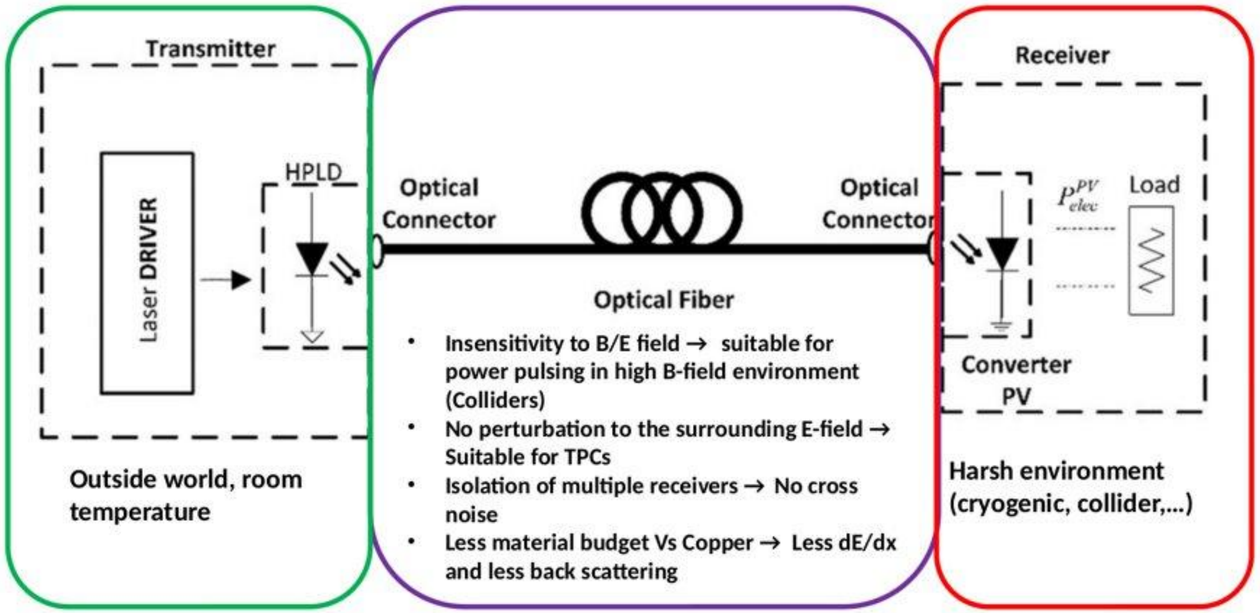
Acknowledgements
CERN-ME & ALICE group for providing access & support to TPSCo 65nm technology
Walter Snoeys for the useful discussions which guided the TDC specifications

Thank you!

Power over fiber

New effort at SLAC targeting various experimental applications

- Power over Fiber (PoF) offers an innovative solution by delivering power through optical fibers, which are immune to electric and magnetic fields, and boast 1000X lower thermal conductivity compared to coax.
- We are developing radiation-hardened photonic links that can be used in future e+e- collider environments, where radiation levels can exceed 100 krad.
- This approach will investigate advanced photovoltaic materials like perovskites and their potential to surpass current GaAs-based photodiodes in power-to-weight ratio and radiation tolerance.



Powering MAPS

System scaling from one pixel to a 2 × 5-reticle module

- Per-pixel budget includes the analog front end, digital logic and the shared TDC contribution
- Reticle power scales with the pixel count and includes conversion and distribution losses
- A 2 × 5-reticle module requires ten times the power of one reticle
- The distribution network must control cable material, voltage drop and local heat load
- Compare conventional conductors, serial powering and power over fiber at the system level
- Power over fiber remains attractive if efficiency, radiation tolerance and fiber count satisfy the module budget

0.70 µW/pixel × [pixels per reticle] = [W per reticle]
10 × [W per reticle] = [W for a 2 × 5-reticle module]

Sensors technology requirements for Vertex Detector

Services cables + cooling + support make up most of the detector mass

CERN-LHCC-2019-018

Need new generation of ultra low mass vertex detectors with dedicated sensor designs

Physics driven requirements

σ *< 3 μm*

Material budget *0.1%X0/layer*

r of the Inner most layer *12-14 mm*

Running constraints

Cooling

Beam-background

Radiation damage

Sensor specifications

Small Pixel

Thinning t

Low Powe

Fast Readou

Radiation Tolerance

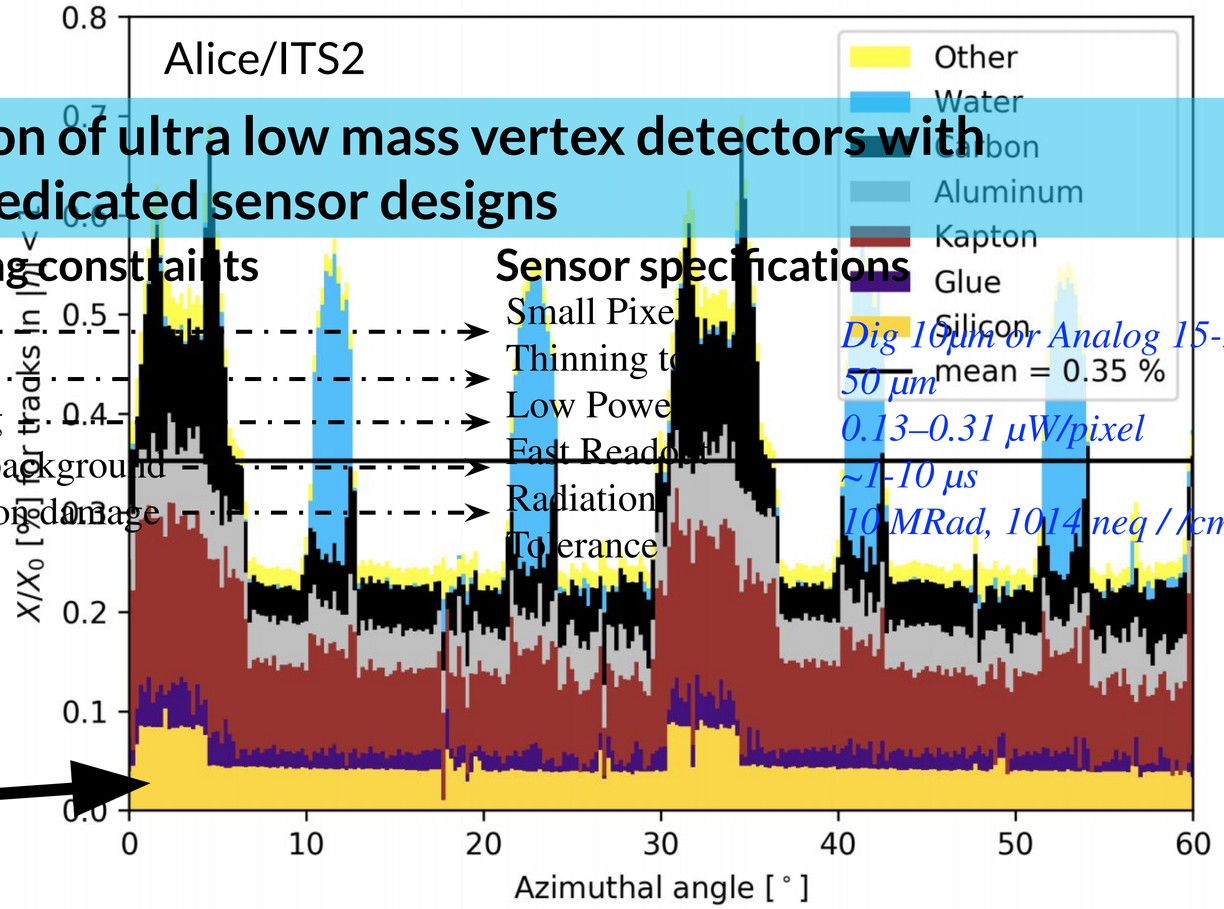
Dig 10μm or Analog 15-20μm

50 μm

0.13–0.31 μW/pixel

~1-10 μs

10 MRad, 1014 neq / /cm2



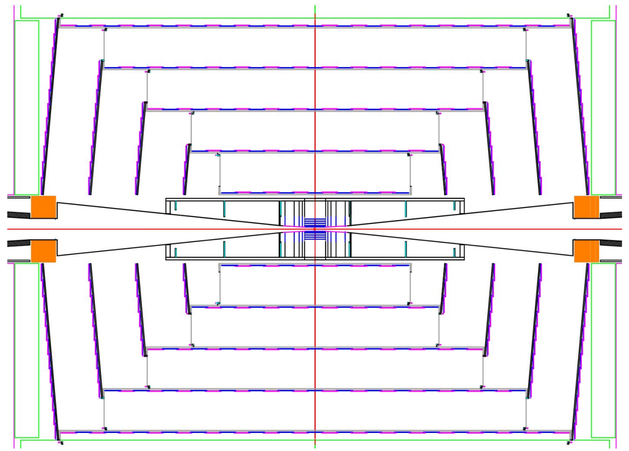
Sensor contribution: 15–30% of total

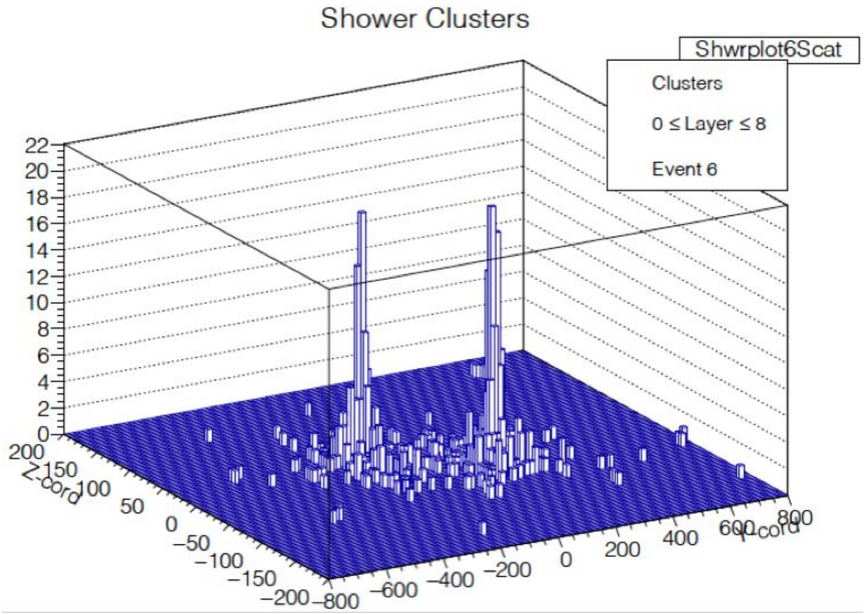
SLD VXD3: 0.40% X_0/layer

arXiv:1306.6329

Tracking & Calorimeter detectors

Instruments 2022, 6(4), 51





GEANT4 simulations of Transverse distribution of two 10 GeV showers separated by one cm

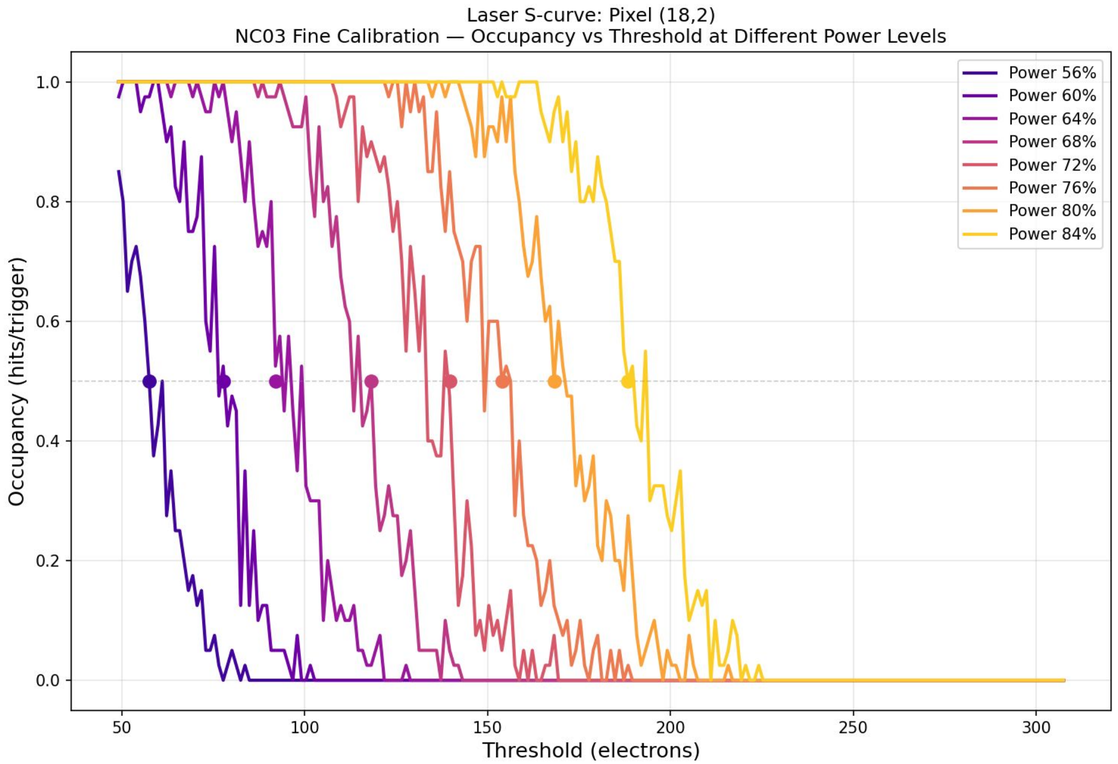
Full **silicon detectors** (SiD, CLD, CLIC-Det) aiming at 0.1-0.15% X0 in the central region

For the **ECAL detector**

- Fine granularity allows for identification of two showers down to the mm scale of separation
- The design of the digital MAPS applied to the ECal exceeds the physics performance as specified in the ILC TDR

Laser charge calibration: absolute cross-check

Measured optical S-curves



Proposed photon-statistics cross-check

- Extract the 50% crossing M and S-curve width σ(total) at each laser intensity
- Subtract the front-end noise variance σ^2(noise) measured without light
- Fit the variance difference versus M to obtain the conversion G in e^-/DAC

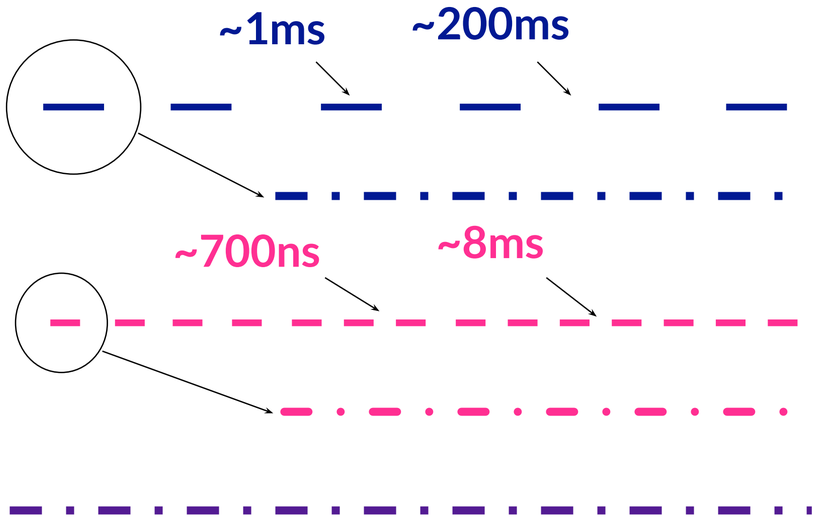
$$\sigma^2(\text{total}) - \sigma^2(\text{noise}) = M/G$$
$$G = M / [\sigma^2(\text{total}) - \sigma^2(\text{noise})]$$

This provides an independent check of the internal-injection electron scale and nominal injection capacitance.

Measured S-curves define the effective charge scale. The photon-statistics extraction remains a planned absolute cross-check.

Beam Format and Detector Design Requirements

arXiv:2003.0111
FCC Mid Term Report



ILC Trains at 5Hz, 1 train 1312 bunches
Bunches are 369 ns apart

C3 Trains at 120Hz, 1 train 133 bunches
Bunches are 5 ns apart

FCC@ZH Bunches 1 μs apart

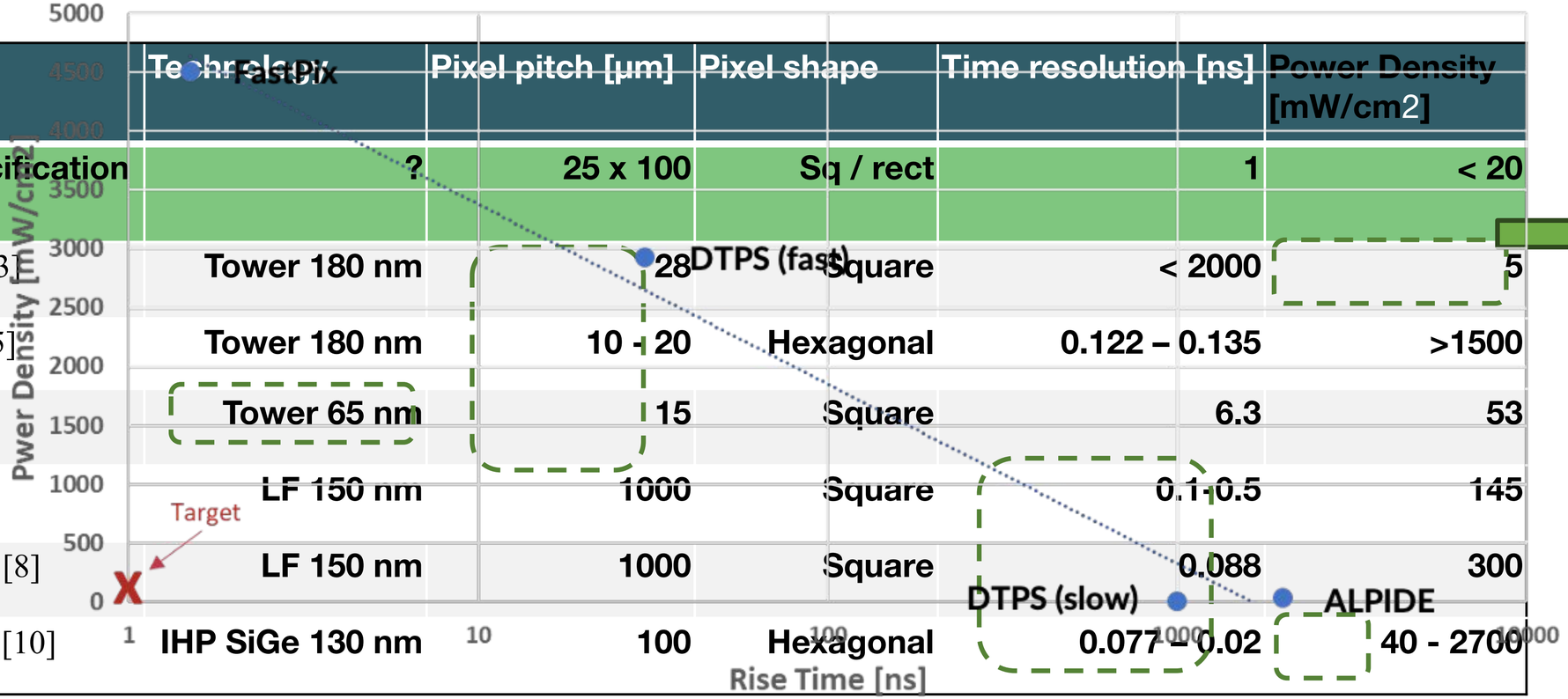
FCC@Z Bunches 20 ns apart

- Very low duty cycle at LC (0.5% ILC, 0.03% C3) allows for trigger-less readout and power pulsing
  - Factor of 100 power saving for front-end analog power
  - **O(1-100) ns bunch identification capabilities**
- Impact of beam-induced background to be mitigated through MDI and detector design
  - O(1-10) ns for beam background rejection and/or trigger decision before reading out the detector

Target Specs vs. State of the Art

JINST 19 (2024) 04, C04033

Chip name	Technology	Pixel pitch [µm]	Pixel shape	Time resolution [ns]	Power Density [mW/cm2]
Target Specification	?	25 x 100	Sq / rect	1	< 20
ALPIDE [2][3]	Tower 180 nm	28	Square	< 2000	5
FastPix [4][5]	Tower 180 nm	10 - 20	Hexagonal	0.122 – 0.135	>1500
DPTS[6]	Tower 65 nm	15	Square	6.3	53
Cactus [7]	LF 150 nm	1000	Square	0.1-0.5	145
MiniCactus [8]	LF 150 nm	1000	Square	0.088	300
Monolith [9][10]	IHP SiGe 130 nm	100	Hexagonal	0.077 – 0.02	40 - 2700



No design fulfills all target specification → The need to develop a custom design

We decided to go with the Tower 65nm technology, which has been optimized by CERN WP1.2 to have low sensor capacitance allowing very good performance with low power consumption.
+ it has the possibility of a wafer-scale stitched sensor
+ it has been proven to be radiation tolerant

Beam induced backgrounds at future HF

D. Ntounis (2023)
G. Marchiori (2023)
TDAQ@Annecy2024

Same tools and methodology between ILC & FCC within Key4HEP

- ILC physics studies are based on full simulation data and some have been recently repeated for C3
  - Time distribution of hits per unit time and area on 1st layer ~ 4.4 · 10−3 hits/(ns · mm2) ≈ 0.03 hits/mm2 /BX
- CLD detailed studies @FCC show an overall occupancy of 2-3% in the vertex detector at the Z pole

$$occupancy = hits/mm^2/BX \cdot size_{sensor} \cdot size_{cluster} \cdot safety$$

$$size_{sensor} = \frac{25\mu m \times 25\mu m\ (pixel)}{1mm \times 0.05mm\ (strip)} \qquad size_{cluster} = \frac{5\ (pixel)}{2.5\ (strip)} \qquad safety = 3$$

	Z	WW	ZH	Top
Bunch spacing [ns]	30	345	1225	7598
Max VXD occ. 1us	2.33e-3	0.81e-3	0.047e-3	0.18e-3
Max VXD occ.10us	23.3e-3	8.12e-3	3.34e-3	1.51e-3
Max TRK occ. 1us	3.66e-3	0.43e-3	0.12e-3	0.13e-3
Max TRK occ.10us	36.6e-3	4.35e-3	1.88e-3	0.38e-6

Occupancy in readout window (10μs)