

DRD3: silicon trackers *for FCCee*

- Quick tour of requirements
- Overview of DRD3 & technologies
- RSD-LGAD
- CMOS-strip
- MAPS

■ Vertexing

- Combining position res. $\lesssim 3 \mu\text{m}$ with hit rate 100 MHz/cm^2
 - Time resolution debatable: few 100 ns probably OK, few ns might be useful
 - Radiation tolerance not
- Constraints:
 - pixel size, inner layer radius,
 - material budget $\sim 0.2\% X_0$ /layer (incl. cooling) $\Rightarrow$ average power $20 - 50 \text{ mW/cm}^2$
 - Beam pipe $\sim 0.3\% X_0$

■ Tracking

- Prominent: material budget per layer $1-2\% X_0$
 - Power $< 100 \text{ mW/cm}^2$ (the lower the better)
 - Debate about sensor size: large (stitching) or small (reticule)
- Hit rate: $\sim \text{MHz/cm}^2$ or lower
- Position res $5-10 \mu\text{m}$ ($r\phi$)
- Large area coverage

■ Questions

- Triggerless?
- Time resolution similar for vertex and tracker?
- Hit rate for vertex (safety factor / simulation)

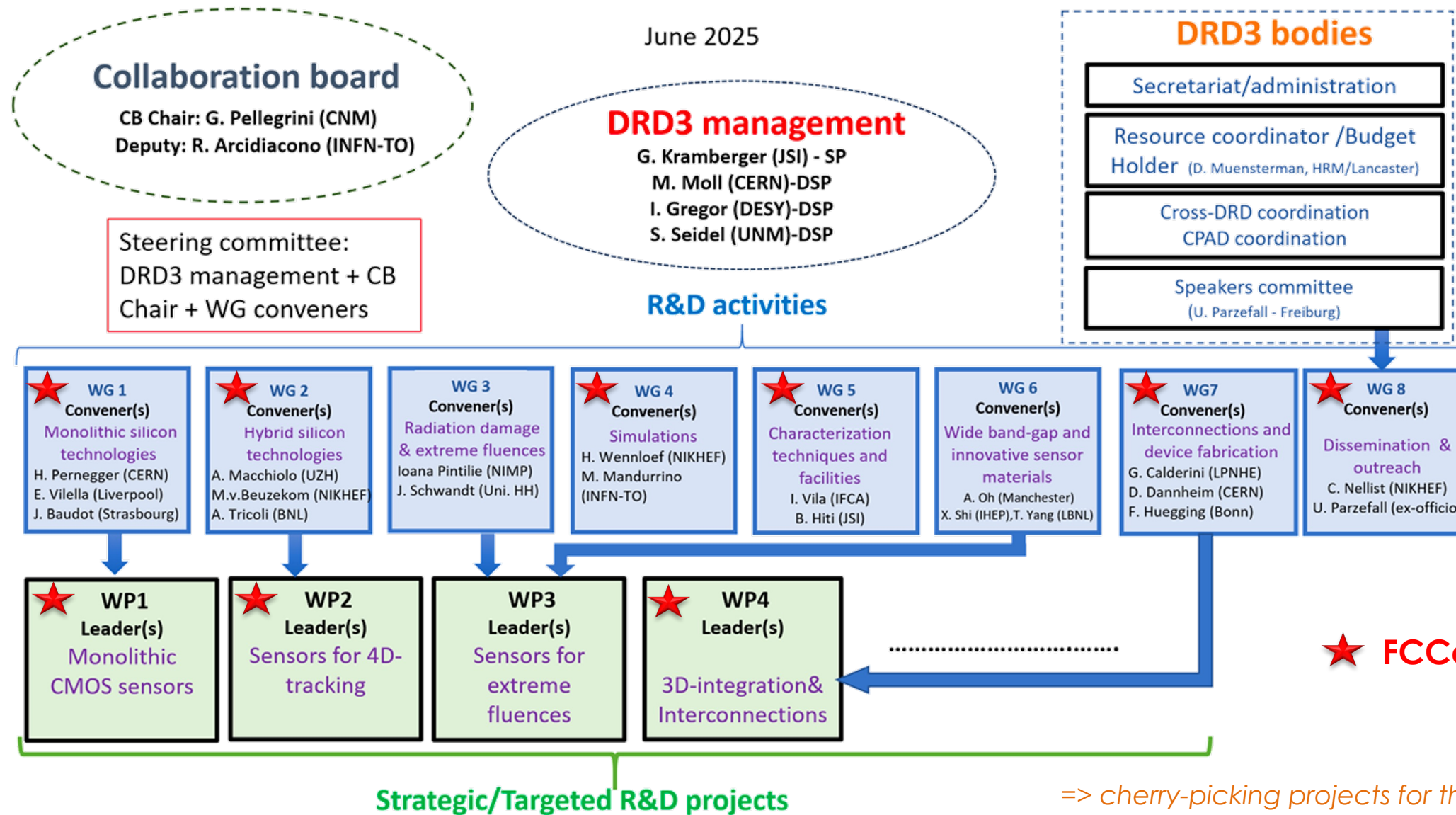
■ PID

- Main: 30-100 ps depending on radius, power budget
 - Similar issue for integration: 1-2% / layer
 - Position res. $\sim 10 \mu\text{m}$
- Secondary
 - Hit rate $< 15 \text{ MHz/cm}^2$

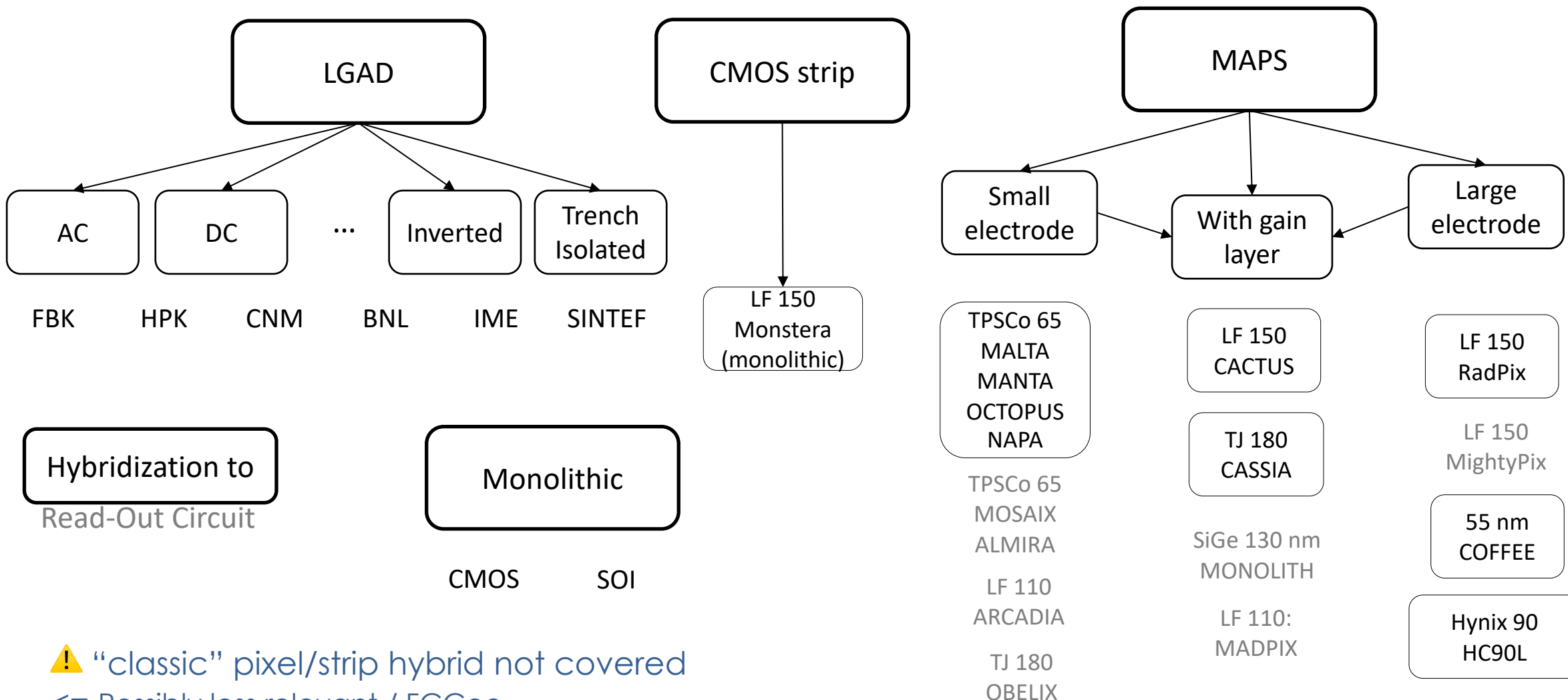
■ Electromagnetic Calorimetry

- SiW digital ECAL
 - MAPS based past/existing projects: FoCaL & EPICAL
- Essential: small pixel to count particles: 25-50 μm pitch
- Timing res. $\lesssim \text{ns}$
- Hit rate: unclear to me (locally not small)
 - Possibly dynamic range $> 1 \text{ hit} \Rightarrow$ multi-bits pixel read-out
- Power ? $< 100 \text{ mW/cm}^2$
- Large area coverage

DRD3 organisation (120 institutions, 700+ scientists)



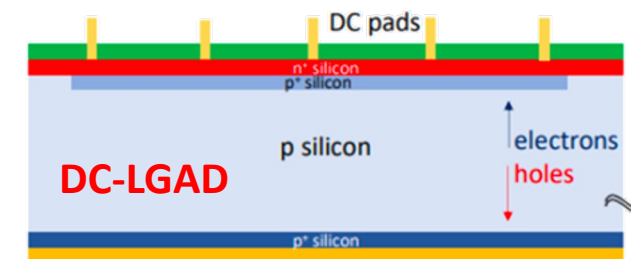
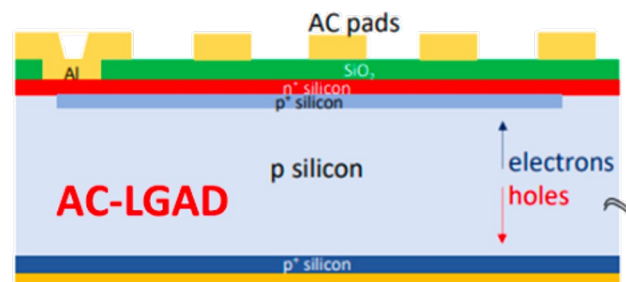
Sensor technology map



LGAD for position resolution & timing

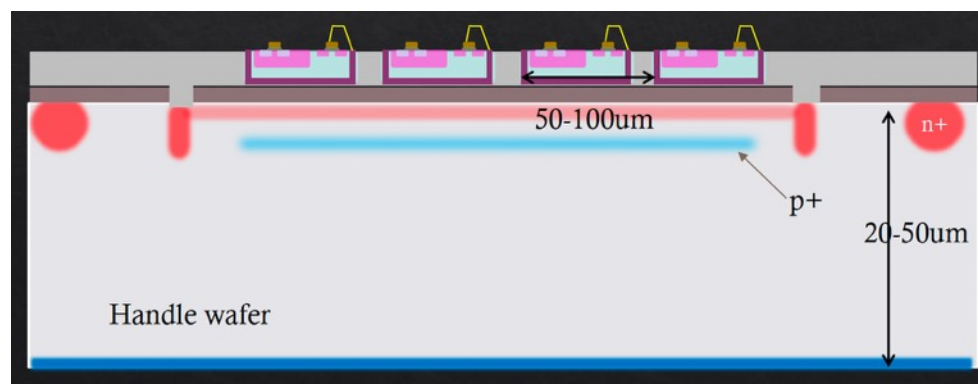
■ Resistive Silicon Det. (RSD)

- Excellent fill factor
- Multiple readout electrodes on single pad/strip
- Position/Time resolution by interpolation
=> current reach: 5% of pitch / ~40 ps
- **Need:** establish high-yield production process
explore alternative route (ex: AC-DC-RSD)

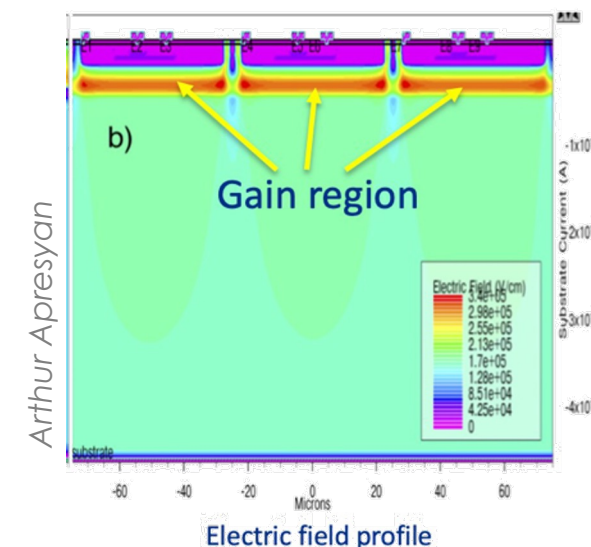


■ Monolithic (AC-RSD)

- BNL, FNAL, KEK, Osaka-U, UC-Santa-Cruz, U-Tsukuba, Zürich-U
- Potential foundries
 - CMOS: SkyWater 130nm
 - SOI: LAPIS 200 nm, XFAB 180 nm
- **Need:** proof of concept



Koji Nakamura



Common DRD3 LGAD production @ BNL

- Full development cycle: Design, Simulation, Fabrication, Tests
- Currently collecting players & specifications
BNL, Zürich, Bern, NCSR Demokritos, Uni. New Mexico, Syracuse Uni., Texas Tech Uni., Santa Cruz, Brown, Uni. Hawaii

LGAD Type	Strip/Pixel	Electrode Pitch/Length	Matrix	Size	Notes
AC-LGAD	Pixel	500x500 um2	32x32	1.6x1.6 cm2	
AC-LGAD	Pixel	100x100 um2, 55x55 um2	32x32	3.2x3.2 mm2, etc.	
AC-LGAD	Pixel	100x100 um2, 55x55 um2	32x33	3.2x3.2 mm2, etc.	
LGAD	Pad	1.3x1.3 mm2			p-in-n for optical applications
lgads/ac- lgads	pad	3x3 mm2	2x2		continuation of the current study of LGAD performance at coarser granularity
AC-LGADs					
Thick LGADs/AC- LGADs	strips	500x1-2cm		1x1, 2x2cm	500um Thick LGADs
AC-LGADs	pixels	100x100 um2, 200x200, 500x500,55x55 um2 -- diamonds, squares	32x32, 16x16, 8x8	1x1	

Gabriele Giacomini

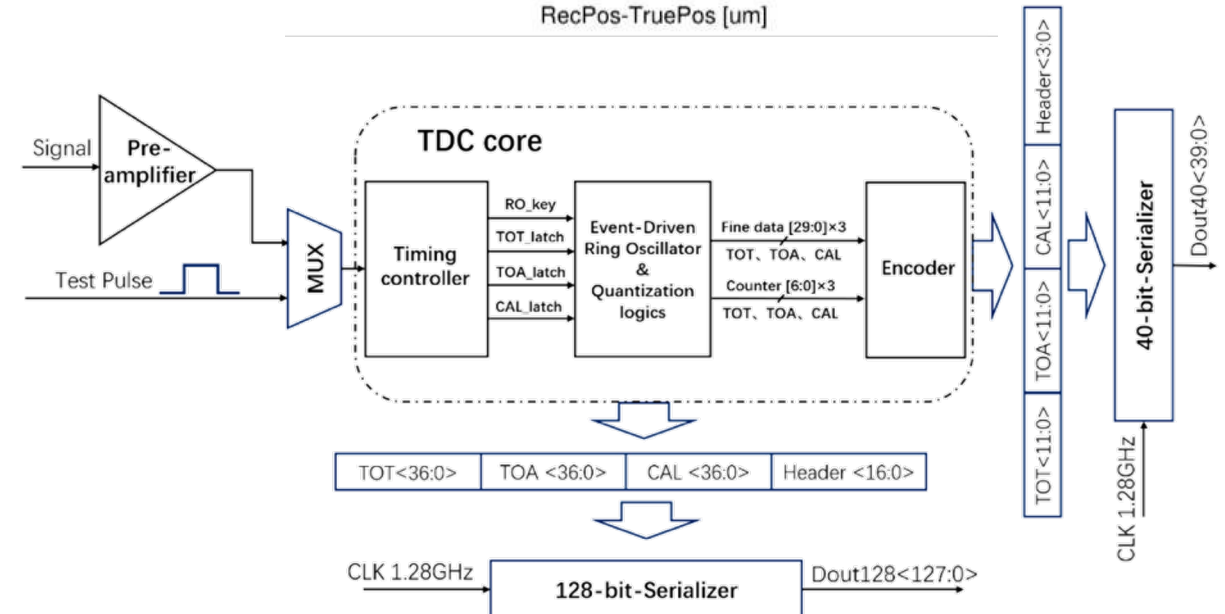
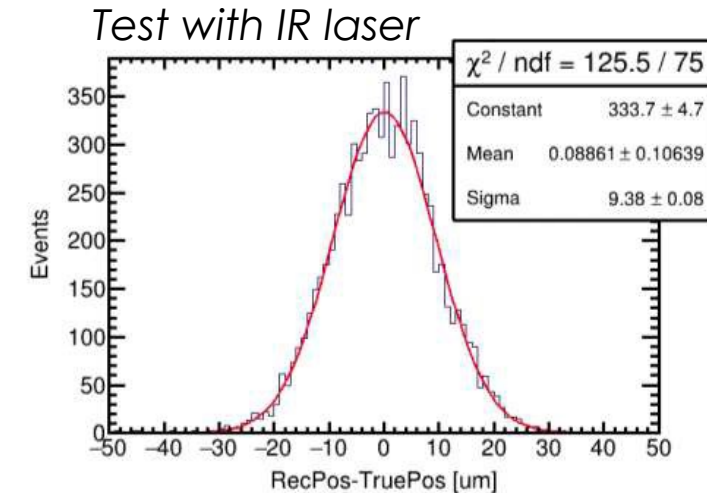
- Development plan 2025-2030

■ Sensor

- Breakdown voltage ~280 V for optimised N+ dose
- Capacitance vs pad size: 25-75x100 $\mu\text{m}^2 \Rightarrow 160 - 480$ pF
- Position resolution: 2cm strip & pad 50-100 $\mu\text{m} \Rightarrow 9.4$ μm
- **Plan for increasing area $\rightarrow$ 2029**

■ RoC ASIC

- 55 nm process
- **LATRIC**: v0+v1 2025, v2 $\rightarrow$ v4 2027 $\rightarrow$ 2030
- Increasing #channels/chip (v4: 128 channels)
- Channel pitch 100 μm
- TDC Power: 1.2V x 0.1-0.5 mA @ 0.5-2x10⁶ triggers/s
- Sensor+LATRIC1: time resolution with β : ~83 ps



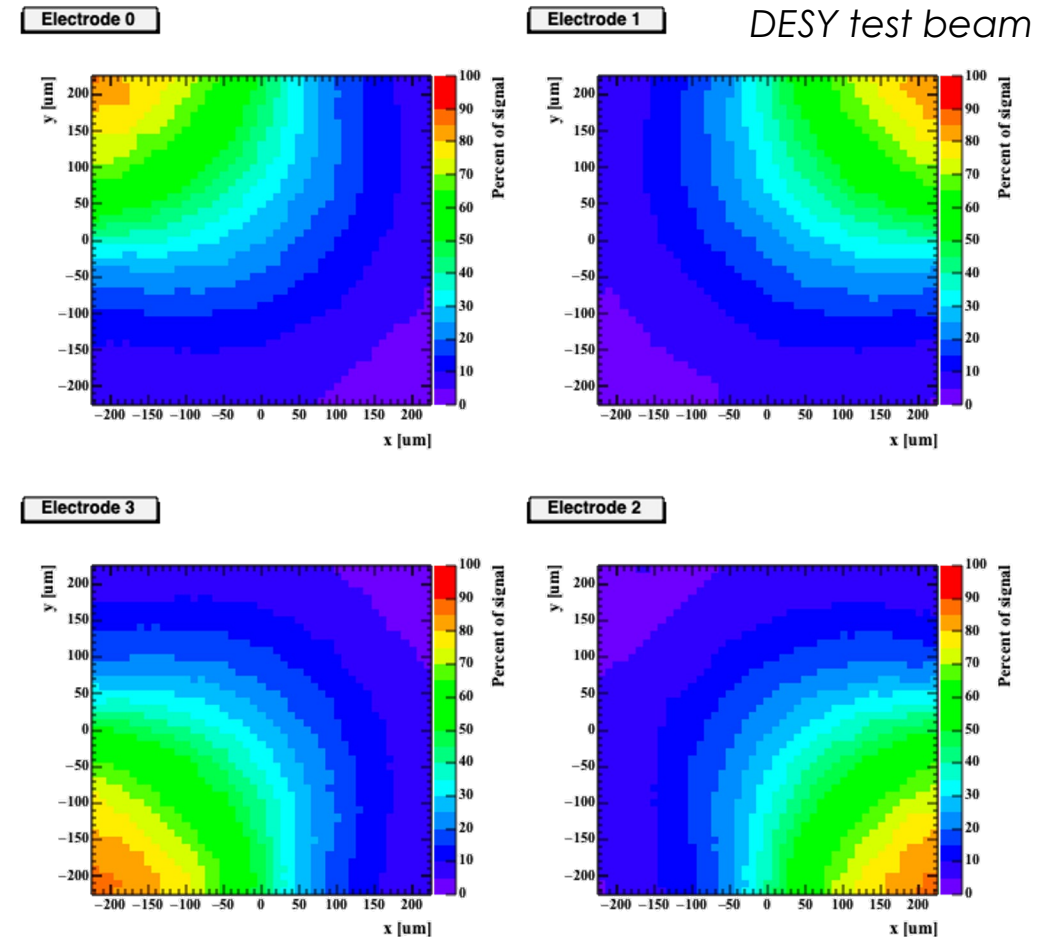
Courtesy: Mei Zhao & Jiajian Teoh

■ Sensor

- Proof of concept with 2024 FBK prod, with charge containment done with **isolating trench**
 - Thickness 55 μm , various shape, doses,
 - Coupled to FAST3 ASIC board
- **Position defined by (3)4 pixels and LUT**
- Resolution varies on the pixel area: 10-50 μm
- ToA interpolated with 4 pixels: 50 ps
 - Independent of hit position

■ ROC ASIC

- ROCSTaRS: Space-Time Tracker with Resistive LGAD Sensors
 - Pixel size 500 μm
- target: 15-20 μm , 35 ps
 - Radiation tol. Up to $2.5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$
- Power expected: 0.5 - 1 W/cm²



Courtesy: R. Arcidiacono

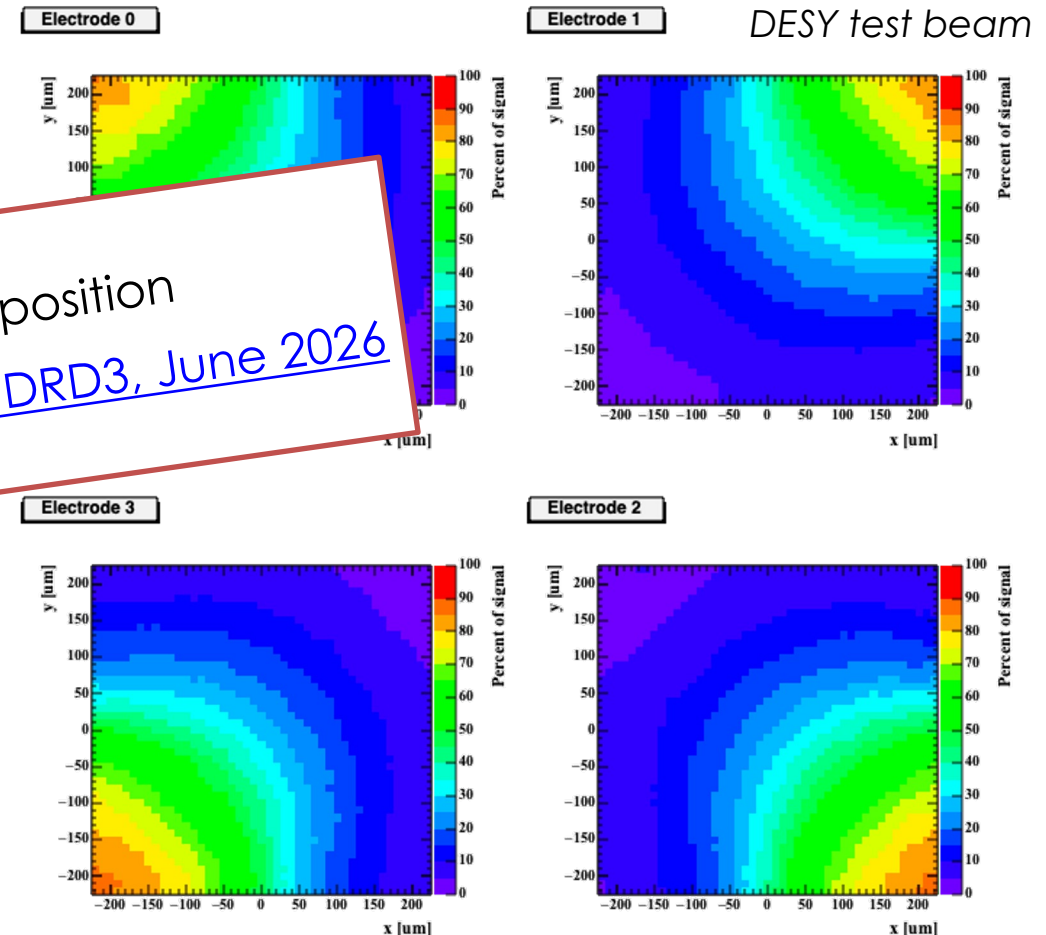
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Other **ML methods** to interpolate hit position
 ⇒ See [G.Barone, L.Diehl, L.Wang @ DRD3, June 2026](#)



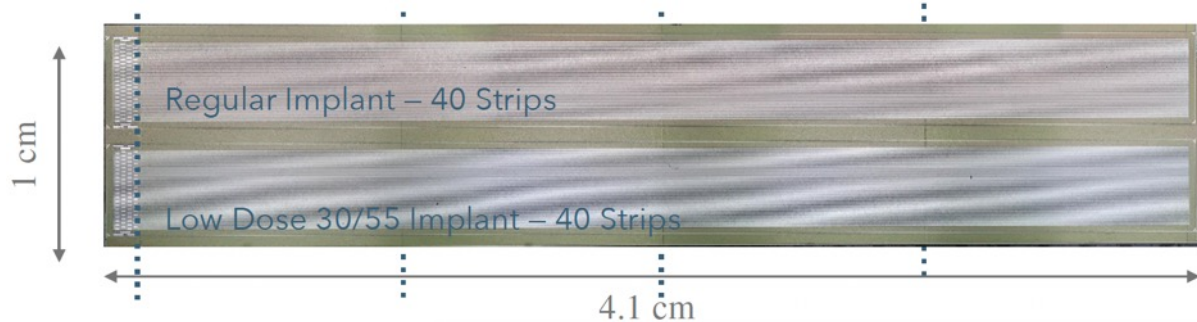
Courtesy: R. Arcidiacono

CMOS strip: concept

- Use CMOS process with STITCHING => MONOLITHIC ACTIVE STRIPS

■ 1st step: passive strip on CMOS (2022)

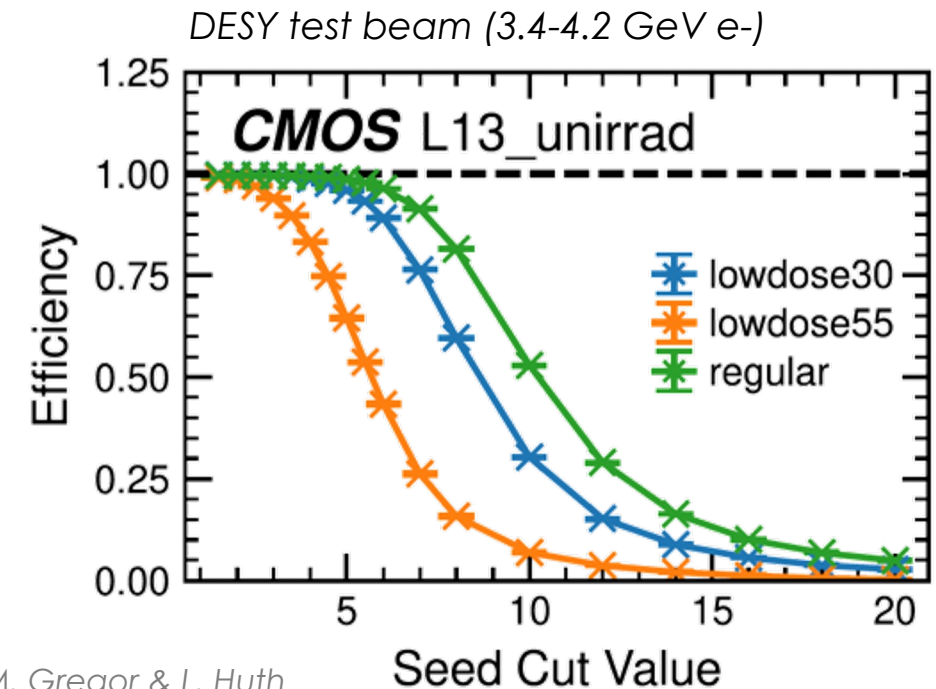
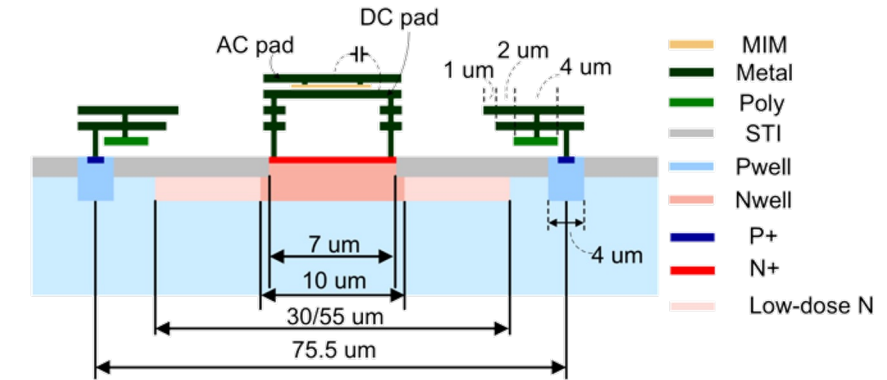
- LFoundry 150 nm, n-in-p
- Float-Zone Si 3-5 kΩ.cm, 150±10 μm thick



- **No impact on charge collection & detection efficiency**

=> <https://doi.org/10.1016/j.nima.2022.167031>

– Also tested after irradiation (not showed here)



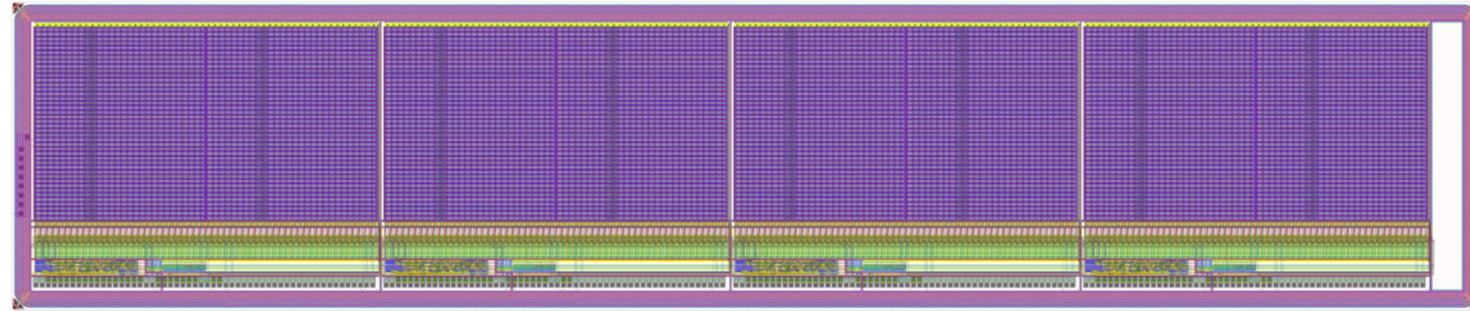
Courtesy: I.M. Gregor & L. Huth

■ 2nd step: embedding the electronics

- LFoundry 150 nm, DRD3 submission from Summer-2026
- No-stitching (already understood in 1st step)

■ MONSTERA-1

- Strips: 2.8 mm x 75 μ m
- 42x2 strips per segment
- front-end included in strip,
 - Reproduce Telepix2 <https://doi.org/10.1016/j.nima.2022.167947>
 - Targets: threshold ~ 1 ke, noise 100-300 e
- Digital logic outside
 - Reproduce Mightypix <https://doi.org/10.1016/j.nima.2026.171834>



■ Expectations

- Input charge 6 ke / Noise ~ 180 e
- Current in amplifier 50-100 μ A + 100 mW for readout
=> Power 50-90 mW/cm² (90% in FEE)
- Time jitter (thres 9x noise): 70 ps

Courtesy: I.M. Gregor & L. Huth

■ Vertexing



- Position res. $\lesssim 3 \mu\text{m}$
- Time res $\sim 5 \text{ ns}$
- Hit rate $O(100) \text{ MHz/cm}^2$
- Power budget $\lesssim 50 \text{ mW/cm}^2$
- Fluence tol. $10^{14} n_{\text{eq}}/\text{cm}^2$
- Sensor thickness $\sim 50 \mu\text{m}$

=> staged approach
(power/timing adjustment)

- Intermediate goal ~ 2028
high resolution beam telescope sensor

■ Tracking (&PID)



- Position res. $5 - 10 \mu\text{m}$
- Time res. $30 \text{ ps} - \text{few ns}$
- Hit rate $1 - 100 \text{ MHz/cm}^2$
- Power budget $20 - 200 \text{ mW/cm}^2$
- Fluence tol. $0 - 3 \times 10^{15} n_{\text{eq}}/\text{cm}^2$

=> Versality needed

- Possible intermediate goal
LHCb UP for LS4
- Sepcs compatible with Calo.

MALTA

- Porting design from $180 \rightarrow 65 \text{ nm}$
<https://doi.org/10.48550/arXiv.2301.03912>
+ improvements / in-pixel trimming
- Large hit rates & Radiation tol.

■ Calorimetry

NAPA

- $25 \mu\text{m}$ pixel pitch
- $\sim \text{ns}$ resolution
- **=> reach in low in power?**
- See [Caterina's talk](#)

■ Timeline

- Chiplets in ALICE-ER3
=> sub. $\sim \text{end } 2026$
- cm^2 proto in DRD3-MPR2
=> sub. Q3-Q4 2027

Share front-end & matrix architecture for MPR2

OCTOPUS: optimising charge sharing



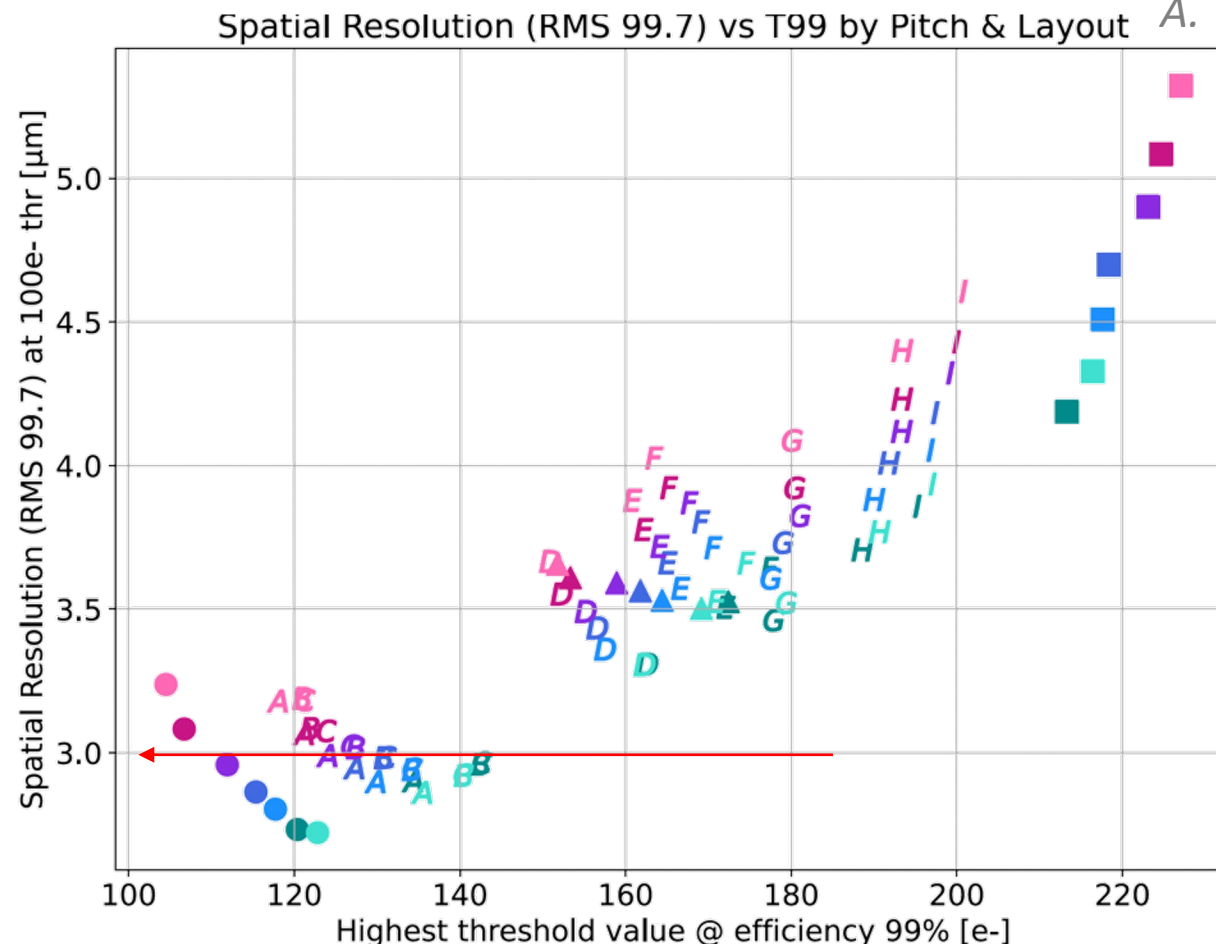
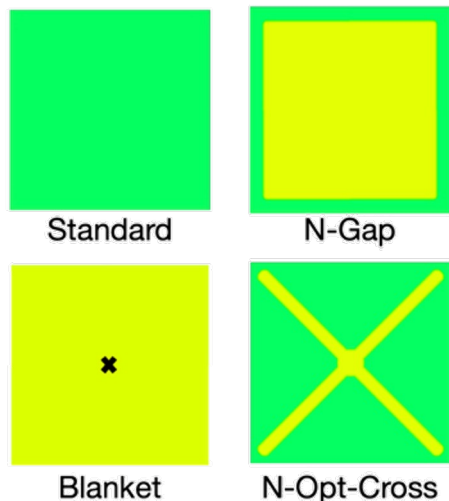
■ Simulation work:

SYNOPSYS[®]
Silicon to Software[®]



■ New process modification

- Impossibility to fit within 15 μm
=> charge sharing for pos. res.



Pitch	
●	15um
●	16um
●	17um
●	18um
●	19um
●	20um
●	21um

Layouts	
●	Standard layout
■	N-Gap layout
▲	Blanket layout

NCross	
A	A=0.5, B=high
B	A=1.0, B=high
C	A=1.5, B=high
D	A=0.5, B=medium
E	A=1.0, B=medium
F	A=1.5, B=medium
G	A=0.5, B=1.0
H	A=1.0, B=1.0
I	A=1.5, B=1.0

■ To be tested in ALICE-ER3 (end 2026)

- Chiplet APTS

=> Pixel shrink if intrinsic amplification available?

Performance of Grouped Pixels



Front-End (FE)

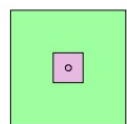
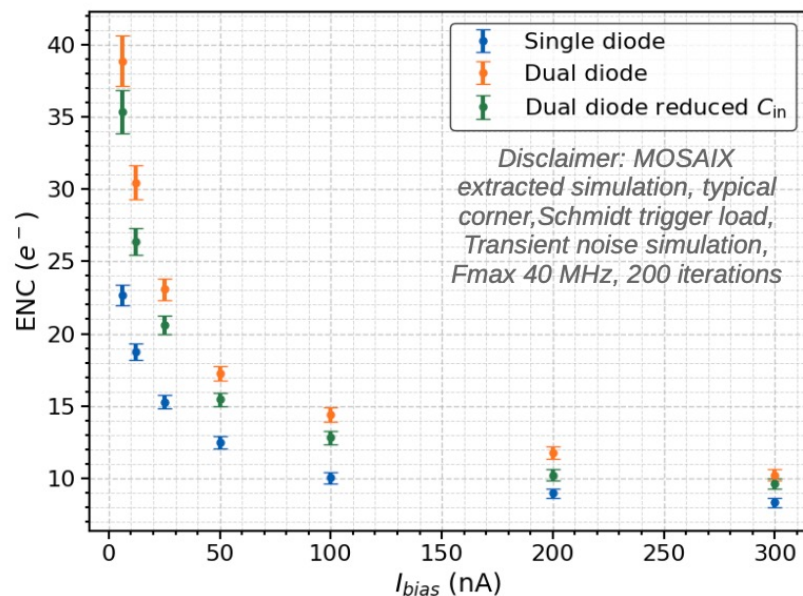
Comparison: Passive vs. Digital

Digital: 2x diodes with each $I_{bias} = 25\text{nA} \rightarrow \text{ENC} \sim 15\text{ e}^-$

Passive: 2x diodes with once $I_{bias} = 50\text{nA} \rightarrow \text{ENC} > 15\text{ e}^-$

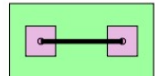
Digital grouping has better performance for same power!

*Remark: Digital grouping adds minimal power for summing
Passive grouping needs shielding $\rightarrow$ Increase C_{in}*



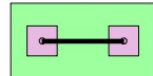
Single diode
Split 4

Passive

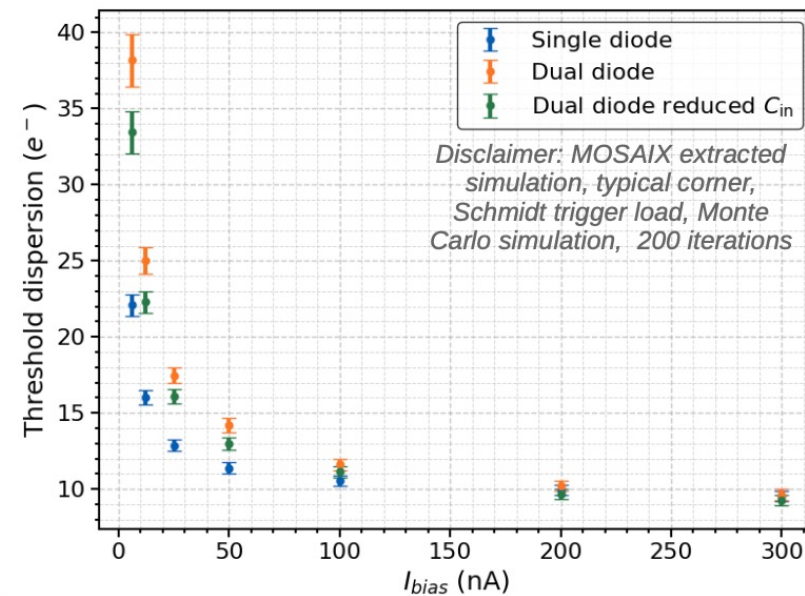


Two diodes
Split 4

Passive



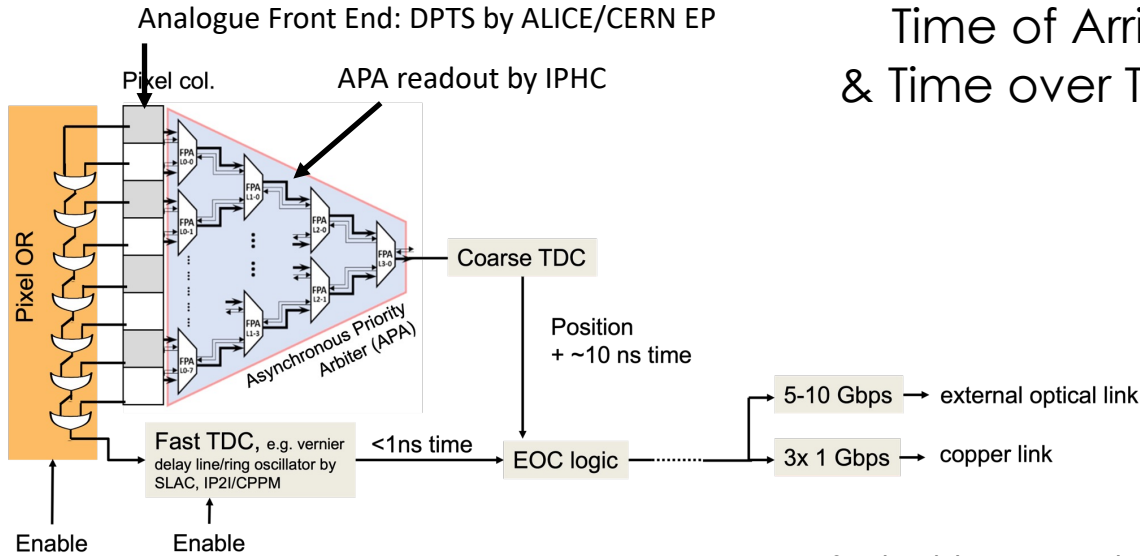
Two diodes
Split 5



■ Asynchronous Priority Arbiters (APA)

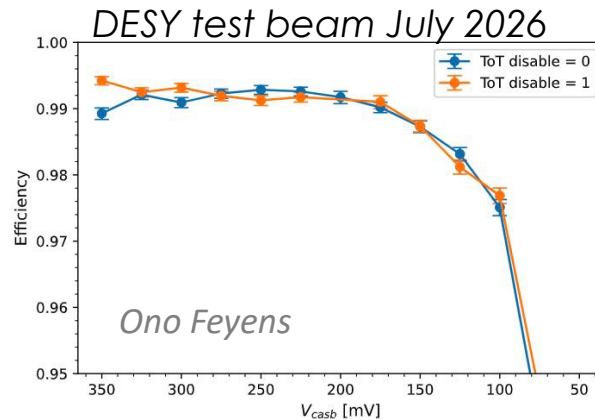
- <https://doi.org/10.1016/j.nima.2024.169663>

=> allows both
Time of Arrival
& Time over Threshold

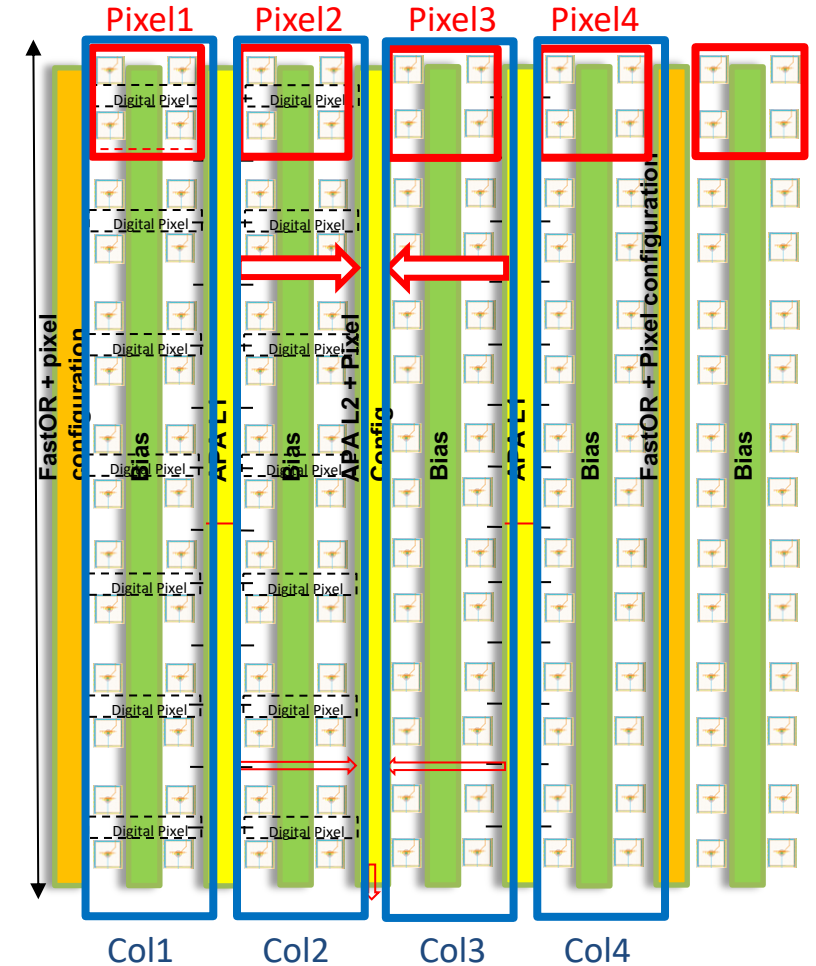


■ SPARC

- Chiplet (IPHC-IRFU) in ALICE-ER2
- First implementation of APA
- Test on-going & positive so far



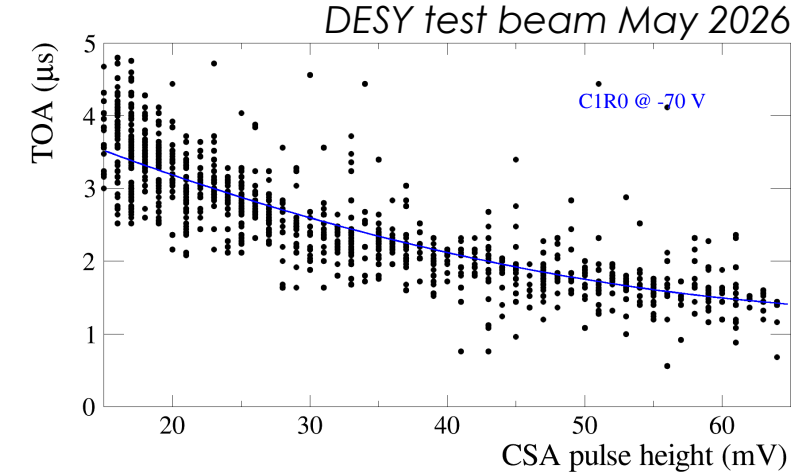
Layout including FastOR for MANTA



MAPS: deeper submicron technologies

■ COFFEE: 55 nm CMOS

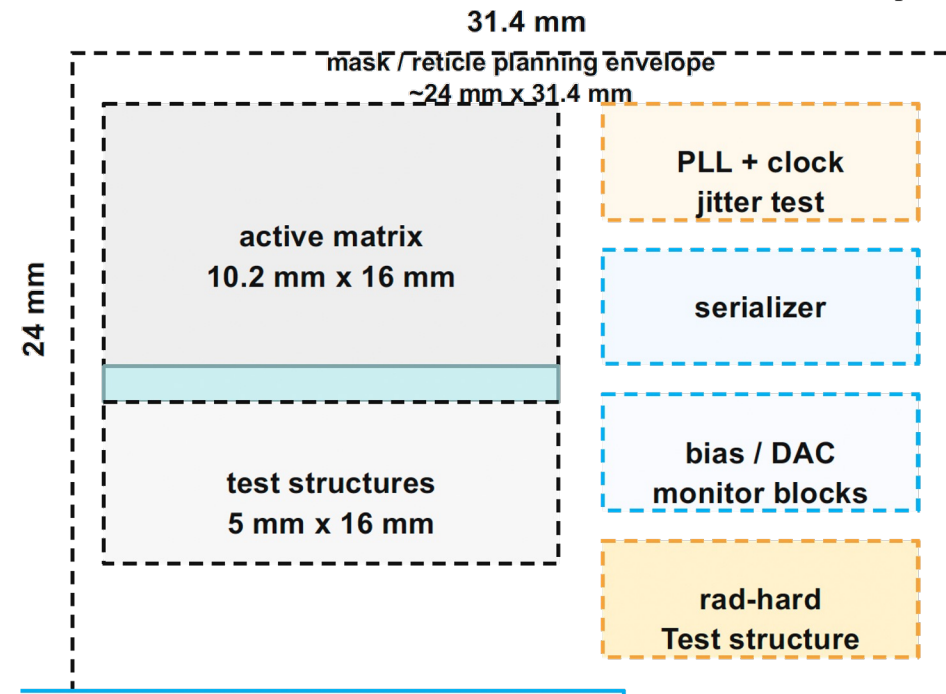
- HVCMOS concept
 - IHEP, Central South U., Dalian U., Hunan U., KIT, Nanjing U., Northwestern Polytechnical U., Shandong U., Zhejiang U.
- Started in 2022, now COFFEE 3
 - $36 \times 130 \mu\text{m}^2$
 - 2 matrix: TDC in pixel “CMOS matrix” / 3-well process “NMOS matrix”
- High resistivity: 1st MPW in 2026, next expected in 2027
 - Pixel: $38 \times 175 \mu\text{m}^2$
 - 1 to 4 k Ω .cm



Yiming LI

■ SK Hynix 90 nm CIS

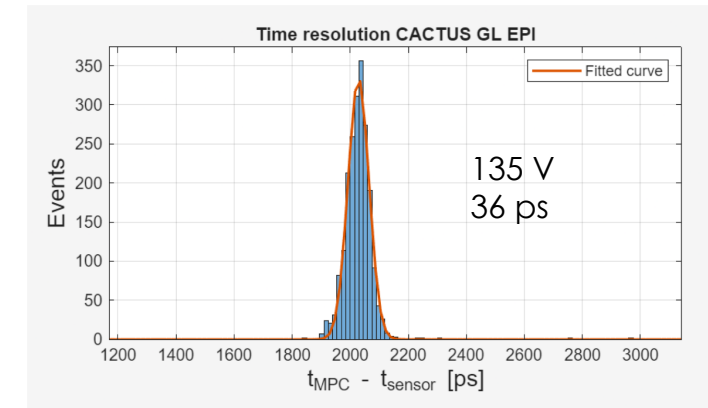
- Target vertexing with **best position resolution**
- Process investigation
 - 2 ER planned 2026-2029
 - Thin sensitive layer (up to $8.5 \mu\text{m}$), low res. for now
- IHEP, Shandong U., CCNU, Nanchang U., Northwestern Polytechnical U., Nanjing U., Nankai U.
=> Open for more collaborators



MAPS: intrinsic amplification

■ CACTUS

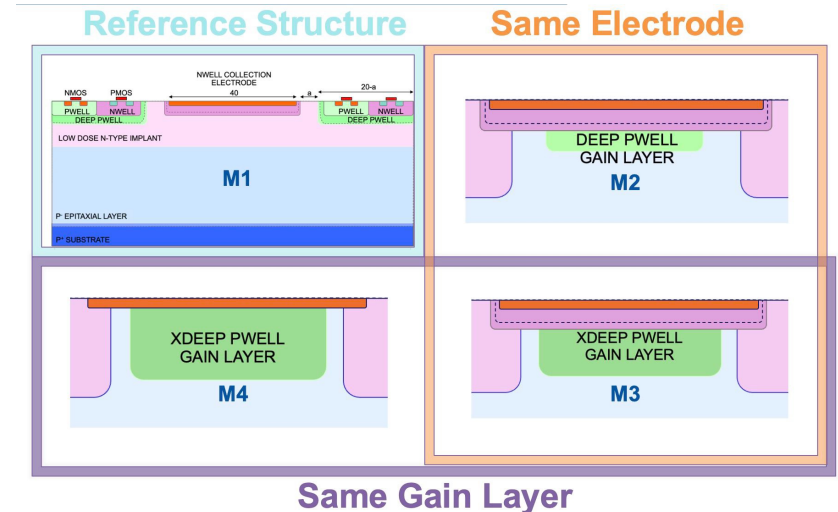
- Target time resolution ~30 ps
 - U.Liverpool, U.Bonn, CSIC, IFAE, IRFU
- R&D since 2017 without amplification in LF 150 nm: ~45 ps reached
 - Pixel 0.5x0.5 mm² over 175 μ m thickness
- Introduction of amplification (miniCACTUS-GL) since 2024, next 2026
 - Various thickness (30-200 μ m) and implant doses
 - Promising resolution 35 ps with 30 μ m epi thickness



S. Terzo

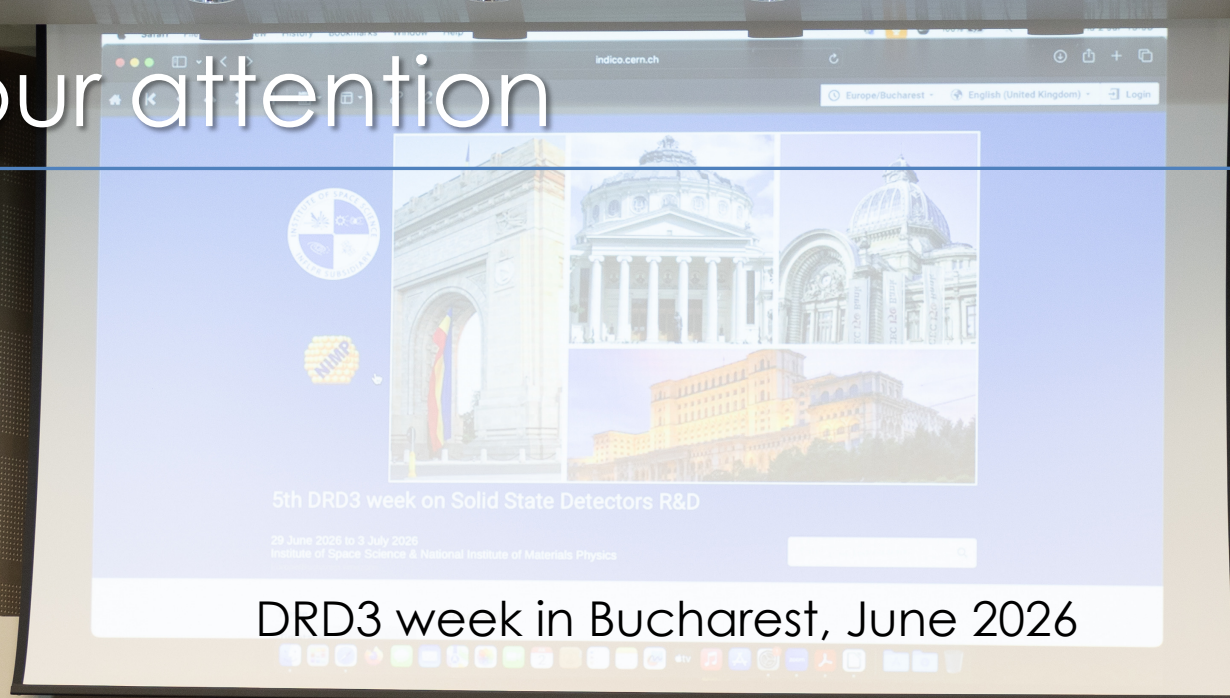
■ CASSIA

- Target either time resolution or small pixel power-friendly
- CERN, TU. Athens, U. Bern, U.Bonn, CPPM, U.Glasgow, GSI, IPHC, IIT Madras, KEK, U. Kyushu, U. Zagreb, U.Tsukuba, U. Zürich
- Tower 180 nm modified process, both LGAD or SPAD modes
 - Various pixel size, thickness
- Current results: gain up to x80, time res. ~100 ps



- Trend for all types of technologies
 - monolithicity & hybridization co-exist
 - Intrinsic amplification in Si plays a critical role
- This was a biased & non-exhaustive presentation (interest of FCChh ignored)
Hybridization (ACF, ...) , Simulation tools (Allpix², Garfield++), Serial powering,
Testing tools (CARIBOU), Outreach (MAPSacademy, TCT school, ...)
- Many developments on-going within DR3
- Key aspect for coming years: connecting with other R&D needed for a detector

Thank you for your attention



- Available material from General meetings

- [2024 June, CERN](#)
- [2024 December, CERN](#)
- [2025 June, Amsterdam](#)
- [2025 November, CERN](#)
- [2026 June, Bucarest](#)
- 2026 December, CERN
- 2027 Spring,
- Main site: <https://drd3.web.cern.ch/>

Tower 180 nm: OBELIX (Beam Telescope for DRD3)

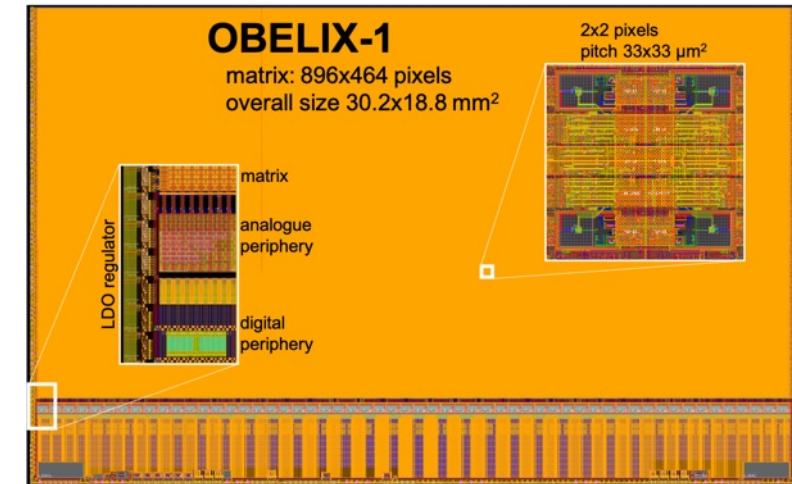
	OBELIX
Pitch	33 μm
Signal ToT	7 bits
Integration time	50 To 100 ns
Time stamping	~ 5 ns for hit rate < 10 MHz/cm ²
Hit rate max for 100% eff.	120 MHz/cm ²
Trigger handling	30 KHz with 10 μs delay
Trigger output	~ 30 ns resolution with low granularity
Power (with hit rate)	120 to 200 mW/cm ² (1 to 120 MHz/cm ²)
Bandwidth	1 output 320 MHz

■ From TJ-Monopix2

- TJ 180 nm CIS process
- Bonn, CERN, CPPM, CEA-IRFU
[DOI: 10.1016/j.nima.2020.164403](https://doi.org/10.1016/j.nima.2020.164403)
- Modified process for depletion
=> radiation tolerance
- Column-drain read-out
inherited from ATLAS FE-I3

■ To Optimised Belle pIXel sensor

- Extension of pixel matrix
- New peripheral digital logic
 - Triggered read-out
 - Fast time stamping for hit-rate < 10 MHz/cm²
 - Coarse granularity (8 stripsels) for track-trigger
- Add LDO regulator
- **From OBELIX v1 to v2**
 - **corrections & option choice driven by tests**
 - **Addition of SEU protection**



Contributors:

- Matrix block:
Bonn, IFIC, IPHC, CPPM,
Bergamo/Pavia, KEK
- Regulator: Dortmund, KEK
- Digital periphery:
CPPM, HEPHY, IPHC
- Integration
IPHC

=> V1 Expected from TOWER
In October 2026

■ Common submission Summer 2026

- Organised by E.Vilella (U.Liverpool)
- **RadPix1**
 - Inherit RD50-MPW developments (HVCMOS)
 - Target high rate & radiation tolerance
 - LHCb trackers upgrade for LS4

